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A Methodology for Characterizing and Introducing MOSFET Imperfections in Analog Top-Down Synthesis and Bottom-Up Validation

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en vue de l'obtention du grade de
Docteur en Sciences Appliquées

August 2005

Acknowledgments

First of all, I would like to thank Prof. Denis Flandre, my advisor, for the oppportunity he offered me to carry on this research and for the acuteness of his technical advices. I am also grateful to the members of the jury: Prof. Paul Jespers for his guidance throughout this work, Prof. Bernabe Linares-Barranco for welcoming me in Seville and for the interesting discussions on mismatch, Piet Wambacq for the careful reading of the manuscript, Yannick Hervé for the introduction to the fascinating research field of design languages and for the many discussions during conferences, and Jean-Didier Legat for chairing the examination board.

The present Ph.D. thesis was done in the context of the IST-1999-12342 "SPRING" European project and I want to thank the European Commission for its financial support to this project. It was a pleasure working with the different partners involved in the project and I would like to thank all of them for their technical insights as well as for the nice dinners we had. Lionel Beneteau deserves a special mention for the incredible energy he devoted to promote this research project despite of all the juridical and administrative issues.

I would also like to thank all the people from the IMSE in Seville for welcoming me so friendly. Extra thanks go to everyone from *el despacho de los amigos de la Manzanilla*; I spent a wonderful time with them.

In Louvain-la-Neuve, my gratitude goes to every person I worked with and to all the people of the a.195 office for the good ambiance; in particular Stéphane Adriaensen, Aryan Afzalian, Maryline Bawedin, David Levacq, Amaury Nève de Mévergnies, Rémi Pampin and Bertrand Rue. Special thanks go to Valeria Kilchytska and to all the members of Cissoid s.a.: Pierre Delatte, Laurent Demeûs, Vincent Dessard and Gonzalo Picun, for sharing their experience with me. Particular thanks also go to Bertrand Parvais for all the joyful discussions ranging from non-linearity in MOS transistors to songs of *Les Snuls*. I also thank Brigitte Dupont, Pascal Maes and all the people in charge of the computer park for their great job as well as the administrative staff: Anne Adant, Marie-Hélène Dewael and Annette Kreuwels.

At last, I want to sincerely thank friends and family for their support during these Ph.D. years and especially Gaëlle, for her patience, particularly in the last full-time months of this Ph.D.

Preface

In the introduction of the present thesis, we will motivate our work by referring to the rapidly evolving electronic market. In fact, during this Ph.D. I experienced this fact personally. At the beginning, my research topic was the assessment of silicon-on-insulator (SOI) technologies for low-voltage, low-power analog circuits, as part of a European research project. The continuous-time MOSFET-C filters were a judicious test vehicle and the related transistor-level issues were identified: MOSFET mismatch causing the offset voltage and linearity of MOSFETs in triode, key building blocks of these filters. After a year of research activities, the project experienced a one year time-out due to contract issues with the European commission and internal reorganization of the industrial partner. The third year, our work was reoriented towards operation at high temperature and analog-to-digital conversion, for which the $\Delta\Sigma$ modulator is the most appropriate test vehicle. Time was nonetheless running and we had to re-use most the work done before. It further stressed the importance of the improvement of the analog design flow, to which we contribute in this thesis. On the other hand, the benefit of working in a EU consortium was to expose me to the capabilities of VHDL-AMS, a mixed-signal hardware description language. It was particularly appropriate in this context since it constitutes a link between the device physics and the design issues of the $\Delta\Sigma$ modulator. In the present thesis, the reader will find an investigation of device physics for analog IC design, methodologies to introduce the device physics in practical designs and VHDL-AMS models for the design of a $\Delta\Sigma$ modulator incorporating device physics point-of-view.

Abstract

Electronic systems include ever more features. Their increased potential mainly comes from the huge improvements of device fabrication technologies and from the combination of analog and digital signal processing on the same chip. State-of-the-art applications possibly gather electronical, mechanical, optical and thermal subsystems. At the same time, cost and development time are reduced; stressing the need for an efficient design flow for fast and reliable design of multi-domain mixed-signal systems. The present thesis focuses on the analog design flow in the context of multi-domain, mixed-signal systems.

In a hierarchical view, the electronic systems are divided into subsystems, which can in turn be further subdivided, down to basic cells and transistor level. The ideal design flow results of a top-down synthesis, from the system specifications to the physical realizations of the basic cells, and of a bottom-up validation, from the test of the basic cells up to the test of the system. An efficient design flow should enable the exchange of relevant information between the different levels of abstraction; the specifications must be propagated from the system to its subsystems and the performance of the different subsystems determines the performance of the system. In this case, the subsystems can be efficiently designed according to the system specifications. In this thesis, we contribute to the improvement of this design flow at three levels. We focus on analog parameters which require better modeling to link the physical realizations with the description of the analog cells; we provide a common frame to the description of the different abstraction levels using mixed-signal hardware description languages; and the system level is studied through a test vehicle, a $\Delta\Sigma$ modulator, the mixed-signal part of a $\Delta\Sigma$ analog-to-digital converter.

In deep-submicron technologies, second-order effects which could be neglected at previous technology nodes must now be taken into account. Actual SPICE models however do not accurately model these effects and due to the short time-to-market, designers cannot wait for exhaustive models. We develop a measurement-based analog ID card which aims to optimize the power consumption and the reliability at high temperature by enabling the choice of optimal process (bulk vs. partially-depleted silicon-on-insulator vs. fully-depleted silicon-on-insulator), optimal devices (different threshold voltages in a multi-threshold process) and optimal bias (weak inversion vs. moderate inversion vs. strong inversion). In this thesis, we deal with the following analog parameters: gain, gain-bandwidth product, MOSFET mismatch in weak inversion and harmonic distortion of MOSFETs in triode regime. Typical figures-of-merit provided by the process engineers to describe the device performance cannot be used directly by the circuit designer and they don't provide an intuitive insight in the device performance. For each of the analog parameters, we develop design-oriented characterization methodologies, which are applica-

ble to any device on any technology. Based on measurements of state-of-the-art CMOS processes, we show that silicon-on-insulator transistors from an optimized process are still advantageous over bulk in deep-submicron technologies and that silicon-on-insulator transistors with short channels of $0.15\ \mu m$ can safely be used for mixed-signal applications up to $250°C$. Wide temperature range measurements performed on very different CMOS technologies enable us to point out that to better model the MOSFET mismatch in weak and moderate inversion, an additional term based on the gate voltage dependence of the mismatch on the linearized body effect factor (n) should be included in existing models. We also introduce mismatch measurement data in a top-down design methodology of a current mirror revealing non-obvious design rules as well as typical misconceptions. The interaction of body-related and mobility-related effects to determine the harmonic distortion of MOSFETs in triode is experimentally confirmed for deep-submicron devices and at high temperature. An original harmonic distortion comparison methodology is used to select the device type, bias and resistive structure to design MOSFET-C filters with optimal linearity.

The analog ID card can be included in a top-down design flow supported by mixed-signal hardware description languages. Using such languages, we present behavioral models for the basic analog cells. The implementation of $\Delta\Sigma$ modulators with continuous-time integrators possibly consumes less power than discrete-time implementations. The design issues related to the continuous-time $\Delta\Sigma$ modulator are assessed using the behavioral models. Based on this analysis, a design optimization method is presented for active RC integrators with passive resistors, key building blocks of the $\Delta\Sigma$ modulator. We also point out the potential of the continuous-time implementation for analog-to-digital conversion at high temperature.

Scientific Publications

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Awards

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Glossary

List of Symbols

Ain	input signal amplitude $[V]$
A_{int}	integrator gain $[Hz]$
Av	gain $[V]$
β	current factor $[A/V^2]$
$C_{\mathrm{CH-GND}}$	channel to ground capacitance per unit area $[F/m^2]$
C_g	gate capacitance $[F]$
C_{db}	drain-to-substrate capacitance $[F]$
C_{gso}	gate-to-source overlap capacitance $[F]$
C_{ox}	front-gate capacitance per unit area $[F/m^2]$
C_L	load capacitance $[F]$
$\frac{\Delta I_D}{I_D}$	drain current mismatch $[-]$
δ_τ	pulse width jitter $[s]$
δ_{t_d}	pulse delay jitter $[s]$
$\Delta Ileak$	leakage current impairment between N and P MOSFETs $[A]$
ΔR, ΔC	chip-to-chip variation of the resistance and capacitance $[\Omega,\ F]$
ΔVth	threshold voltage mismatch $[V]$
$\frac{\Delta\beta}{\beta}$	mismatch on the current factor $[-]$
ε_{Si}	silicon permittivity $[F/m]$
f_b	signal bandwidth $[Hz]$
$Fsamp$	$\Delta\Sigma$ modulator sampling frequency $[Hz]$
γ	body effect coefficient $[V^{1/2}]$
GBW	gain-bandwidth product $[Hz]$
gd	output conductance $[A/V]$
gm	gate transconductance $[A/V]$
$\frac{gm}{I_D}$	transconductance over drain current ratio $[1/V]$
HD3	third-order harmonic distortion $[dB]$
I_{bias}	bias current $[A]$
ic	inversion coefficent $[-]$
I_D	drain current $[A]$
$I_{D,sat}$	drain current in saturation $[A]$
$Inorm$	normalized current $(\frac{I_D}{W/L})$ $[A]$
$Ileak$	physical junction leakage current $[A]$
$Ion/Ioff$	on-to-off current ratio $[-]$

k	Boltzmann constant $[C.V/K]$
k_i	loop filter coefficient $[-]$
L	MOSFET length $[m]$
L_{nom}	technology nominal gate length $[m]$
μ	carriers mobility $[m^2/V/s]$
μ_0	low-field carriers mobility $[m^2/V/s]$
n	linearized body-effect factor $[-]$
ni	intrinsic carrier concentration $[cm^{-3}]$
N_A	MOSFET channel doping $[cm^{-3}]$
OSR	oversampling ratio $[-]$
ϕ_b	surface potential in strong inversion $[V]$
Φ_F	Fermi potential $[V]$
$P_{noise,int}$	total input-referred in-band noise power $[W]$
q	electronic charge magnitude $[C]$
Q_{depl}	depletion charge $[C]$
Ron	MOSFET-C resistive structure resistance $[\Omega]$
$\rho(\Delta P_i, \Delta P_j)$	correlation between the mismatches in parameters P_i and P_j $[-]$
ρ	correlation between $\frac{\Delta I_D}{gm}$ at $V_G = Vth$ and at other V_G $[-]$
$\sigma_{(\Delta I_D/I_D)}$	standard deviation of the drain current mismatch $[-]$
S	subthreshold slope $[V/dec]$
SR	amplifier slew-rate $[V/s]$
θ	mobility reduction due to vertical field $[1/V]$
τ	RTZ pulse duty cycle $[s]$
t_d	RTZ pulse delay $[s]$
t_{rise}	pulse rise time $[s]$
t_{fall}	pulse fall time $[s]$
T	temperature $[K]$ or $[^\circ C]$
T_j	semiconductor junction temperature $[K]$ or $[^\circ C]$
t_{ox}	front oxide thickness $[m]$
t_{si}	silicon film thickness $[m]$
U_T	thermal voltage $[V]$
Va	signal amplitude applied to the MOSFET-C resistive structures $[V]$
Vb	body potential $[V]$
$Vback$	back-gate voltage $[V]$
Vch	voltage-to-substrate applied to the MOSFET channel $[V]$
$V_{CM,in}$	amplifier common-mode input signal $[V]$
$Vdac$	DAC output voltage $[V]$
V_D	drain voltage $[V]$
V_{EA}	Early voltage $[V]$
V_{fb}	flat-band voltage $[V]$
V_G	gate voltage $[V]$
$V_{G,fixed}$	fixed gate voltage in 4-MOS resistive structures $[V]$
Vo	DC bias of the signal applied to the MOSFET-C resistive structures $[V]$
V_P	pinch-off voltage $[V]$
V_S	source voltage $[V]$
Vth	threshold voltage $[V]$
W	MOSFET width $[m]$

List of Abreviations

2-MOS	MOSFET-C resistive structure with two MOSFETs
4-MOS	Czarnul-Song MOSFET-C resistive structure
ADC	analog-to-digital converter
AC	alternative current
ASP	analog solution point
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CS	common-source
CT	continuous-time
DAC	digital-to-analog converter
DAE	differential algebraic equation
DC	direct current
DIBL	drain-induced barrier lowering
DR	dynamic range
DSP	digital signal processing
DT	discrete-time
FD	fully-depleted
FFT	fast-Fourier transform
FOM	figure-of-merit
FSM	finite state machine
GVO	gate voltage overdrive
HD	harmonic distortion
HDL	hardware description language
HW	hardware
IC	integrated circuit
IF	intermediate frequency
IFM	integral function method
IP	intellectual property
ISI	inter-symbol interference
LPLV	low-power/low-voltage
MCM	multi-chip module
MEMS	micro-electromechanical system
mi	moderate inversion
MOSFET	metal-oxide-semiconductor field-effect transistor
NRTZ	non-return-to-zero
NTF	noise transfer function
OpAMP	operational amplifier
OTA	operational transconductance amplifier
PCB	printed circuit board
PDA	personal digital assistant
PD	partially-depleted
PDF	probability density function
PLL	phase-locked loop
PSD	power spectral density
PSRR	power supply rejection ratio

RTZ	return-to-zero
SC	switched-capacitor
SCE	short-channel effects
si	strong inversion
SiP	system-in-a-package
SNR	signal-to-noise ratio
SNDR	signal-to-noise-and-distortion ratio
SoC	system-on-chip
SOI	silicon-on-insulator
SOS	silicon-on-sapphire
SRAM	static random access memory
STF	signal transfer function
SW	software
Verilog	verify logic (hardware description language)
Verilog-AMS	mixed-signal extension to Verilog
VHDL	very high speed integrated circuit hardware description language
VHDL-AMS	analog and mixed systems extension to VHDL
wi	weak inversion
ZTC	zero-temperature coefficient point

Contents

Chapter 1

Introduction

1.1 Context

Electronics is almost everywhere in our life. Starting from the alarm clock that wake us up and is possibly getting its internal clock right through a satellite, to the cell phone in our pockets, we are in constant interaction with a huge amount of electronic systems. This number will keep increasing. We are not even aware of the presence of a large number of such systems like the controllers in washing machines or in different parts of our car.

These electronic systems are composed of electronic circuits themselves but also sensors and actuators. Electronic circuits consist of discrete components and integrated circuits (IC): digital (sampled or discrete-time and discrete quantities) and analog (continuous-time and continuous quantities). Digital IC's are for example digital signal processing (DSP) units, memories and micro-controllers, potentially with embedded software. In a mixed-signal integrated circuit (i.e. containing both digital and analog blocks), most of the area ($\approx$ 80%) is occupied by the digital circuits while most of the design time is required for the analog part. The design flows are indeed far from similar. Well-established design documentations - the VHDL or Verilog description of the circuit - and design methodologies - relying on VHDL-based synthesis tools - are indeed available for digital IC's. On the contrary, the design of analog circuits rely more on the designer's expertise as the number of design parameters and design trade-offs are far more important. These two types of circuits must however work together as the analog signal coming from the outside world through an antenna or from a sensor must be first processed and converted to a digital word before processing by the digital unit, for example. Depending on the application, the analog and digital IC's may be present on the same chip forming a system-on-a-chip (SoC) or on different chips. These chips are then connected together on a printed circuit board (PCB) or are assembled in a multi-chip module (MCM) placed into a single package forming a system-in-a-package (SiP). On the other hand, the sensors and actuators are usually separated from the electronic circuits [1] but can also be co-integrated [2] [3] on the same chip. This is more and more so as micro-electro-mechanical-systems (MEMS) technology matures. The nowadays electronic systems are thus highly multi-disciplinary, gathering parts from different physical domains and operating in both discrete- and continuous-time on both discrete and continuous quantities.

Most of the IC market concerns memories and micro-processors or micro-controllers

in CMOS technologies. Due to the huge technology improvements and the downscaling of the MOSFET characteristic dimensions, the on-chip transistor density has grown from $1k$ transistor/chip in the early 70's to $1G$ in today's memories and micro-processors. This device dimensions downscaling also increased the density and allowed to gather more and more functions on the same chip. It corresponds to (or maybe generates) the user requirements of processing images from their digital video camera on a common personal computer or the need to dispose of a cell phone which can be used as personal digital assistant (PDA), video game player, e-mail sender, photo camera and even, as a phone. This increased number of applications, associated to the trend towards portable applications impose stringent restrictions on the power consumption as the available energy is limited.

This downscaling of the device dimensions also profoundly affects the MOSFET physical behavior and hence the models used to describe these devices in a circuit simulator. Physical effects which were negligible at previous technology nodes are now rather important like charge sharing, drain-induced barrier lowering (DIBL), non-negligible gate current, ... In order to correctly describe these phenomena, the MOSFET models complexity has increased. For example, the widely used BSIM[4] model counts now over tens of parameters. Even, if other, more physical, models like the EKV[5] succeed to keep the number of parameters low, their complexity however increase. The simulation time for large circuits is then notably increased.

The technology roadmap being driven by digital applications, i.e. the IC market major player, the analog designer must cope with these technology evolutions. For baseband applications, it implies supplementary design constraints like the reduction of the available dynamic range, making designs even tougher. On another hand, the speed of analog circuits increase thanks to the shorter device dimensions. The device downscaling and related supply voltage reduction also forces the analog designer to bias the devices in the moderate and weak inversion regimes of operation, where the device efficiency is increased (higher $\frac{gm}{I_D}$ ratio[5]), allowing power savings, but other figures of merit such as matching or linearity can be degraded.

1.1.1 Harsh environments

In this electronic systems context, the present thesis is more particularly focused on IC's which have to operate in harsh environments by assessing some of the issues related to this type of applications. Harsh environments can be met in oil and gas, aerospace and automotive applications. Compared to the computer industry, it is a niche market but of growing importance, mainly due to the increased amount and added value of electronic in cars and aircrafts of the (near) future (Fig. 1.1). The world market for automotive semiconductor weighted $12.9B\$$ in 2003 and is indeed expected to grow up to about $18.6B\$$ in 2007 [1].

Harsh environments are characterized by temperature ranges up to $150-200°C$ for most of the applications (Tab. 1.1) and up to $300°C$ for e.g. geothermal wells [6]. In addition, other environmental factors include high pressure, vibration stresses up to 100 times the gravitational acceleration (g) in cars [1], mechanical shocks up to $100[g/ms]$ in a drilling bit [6] and these applications are in contact with highly dirty and corrosive materials.

More specifically, the temperature range at which the system will be exposed depends on the location of the electronics. The electronics, which controls the car engine actuators

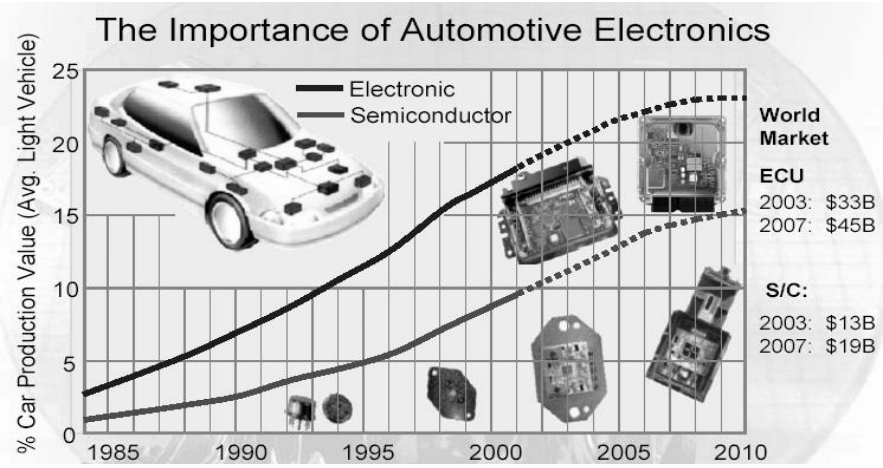

Figure 1.1: Percentage of the production value of an average light vehicle due to the semiconductors (lower curve) and due to the whole electronic systems (upper curve) vs. years (source: Bosch [1]).

Table 1.1: Applications areas and operating parameters for electronics operating at high temperature [7]

Application	**Temperature** $[^\circ C]$	**Minimal practical duration**	Duty
Well-logging oil and gas	150 – 300	from hours up to years	cyclic or continuous
Well-logging geothermal	150 – 400	from hours up to $\approx$ 100 hours	cyclic
Aircraft systems engines, transducers	300 – 500	100 s	cyclic
Automobiles	150 – 250	8000 hours operating $\approx$ 10 years car life	cyclic
Sun or planetary probes	150 – 300 500 and more	100 – 1000 hours operating years probe life	long dormant period followed by short high-temperature operation

for example, is nowadays separated from the actuators, where the so-called semiconductor junction temperature (T_j) is kept below $150^\circ C$. In the next few years, the electronics will be more and more located adjacent to the actuators ($T_j \geq 175^\circ C$). The suppliers of automotive electronics system even hope to move the electronics inside the actuators such as injection heads or gas pipe by the year 2010 [1].

The cost of testing is the main reason to move the electronics inside the actuators. The electronics and actuators then form a single mechatronics system tested in one time, while if not merged these two systems have first to be tested separately and again together. In oil and gas applications, deeper wells have to be exploited rising the temperature of operation up to $200^\circ C$ [6].

Such severe constraints must be sustained by all the different system components: from packaging and solder wires down to the semiconductor devices. Focusing on the semiconductor devices and circuits, harsh environments applications also require high reliability in addition to high temperature robustness. It should indeed not be allowed that

a car would die on the freeway for no reason and print out a message at the dashboard such as "This application has performed an illegal operation and needs to close, we are sorry for the inconvenience. Please restart your car". More seriously, in the case of automotive, given a warranty target of $160000km$ over 10 years, the reliability constraints on the different electronic subsystems are given in Tab. 1.2.

Table 1.2: Reliability demands on automotive electronics for a warranty target of $160000km$ over 10 years compared with the reliability demands for mobile phones (source: Bosch [1]). An ASIC is an application specific IC.

Item description	Failure rate [ppm]
Electronic Control Units (Field)	< 50
Electronic Control Units ($0km$)	< 15
Module and Sensors	< 10
ASIC	< 3
Standard IC	$<< 1$
Discrete components	< 0.5
Mobile phone	≈ 5000

Moreover, in automotive and depending on the application, the reliability targets will be particularly tough to meet as IC will experience temperature cycles (Tab. 1.1) each time the car is turned on and off. The same, or even more severe, constraints are met in oil and gas and aerospace applications. The electronics may indeed not fail once in space on board of a satellite, due to the launching costs or during a passenger flight for evident safety reasons. The cost to stop a drilling or oil-well analysis operation when the drilling bit is already downhole is huge and imposes such reliability constraints. In this particular oil and gas case, the reliability demand includes robustness to temperature but the temperature of operation is stable (Tab. 1.1). The IC is then supposed to work a large number of hours at a given temperature. With such severe reliability constraints, the test is very important and can weight as much as 50% [8] of the total manufacturing cost. It is thus really important to dispose of tools and methods ensuring zero-defects multi-domain designs by simulation.

1.1.2 Silicon-On-Insulator Technology

In the particular context of harsh environments, the use of silicon-on-insulator (SOI) technology presents major advantages for operation at high temperature and/or with a reduced power consumption. The basic difference between Bulk and SOI MOSFET's lies in the starting wafer. Bulk MOSFET's are fabricated directly at the surface of a thick monocrystalline silicon wafer, acting both as the semiconductor material and as the mechanical substrate (Fig. 1.2 (a)). On another hand, the active silicon layer of SOI devices is separated from the substrate by an insulating layer (Fig. 1.2 (b)). Depending on the thickness of the active silicon layer and on its doping level, the device depletion region may or may not extend across the whole film thickness, leading to respectively fully-depleted (FD) and partially-depleted (PD) SOI MOSFETs.

Beside the suppression of latch-up issues, the reduction of short-channel effects and the improved resistance to substrate noise [10], SOI technology is interesting for

1) low-power operation since [11]

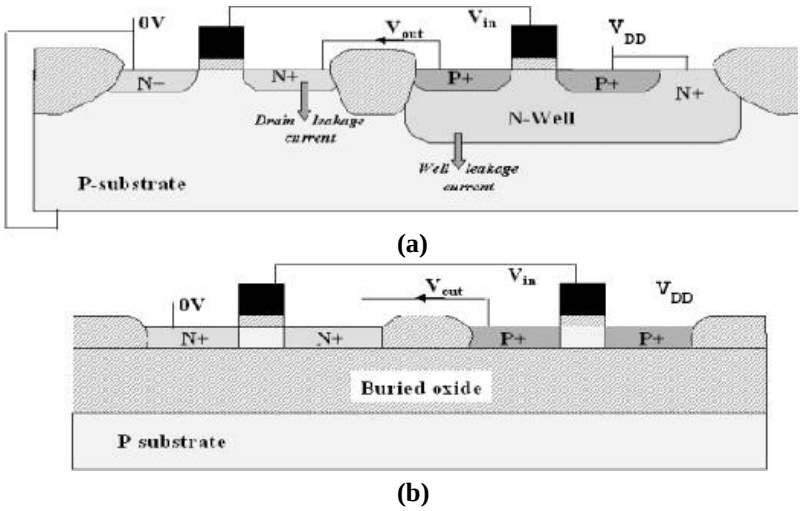

Figure 1.2: Cross-section of a CMOS inverter in a bulk (a) and in a silicon-on-insulator (b) technology [9].

- the device *parasitic capacitances are reduced*, allowing to reach the same frequency of operation with less drive current or alternatively, to operate at higher frequency with the same power consumption.
- in addition, in FD SOI, the *body-effect factor (n) is close to unity*. The drain current in saturation ($I_{D,sat}$) then increases as $I_{D,sat} \propto \frac{1}{n}$, improving the on-state current. The sub-threshold slope (S) is also improved thanks to the near-ideal body effect as $S = nU_T \ln 10$, U_T being the thermal voltage, which yields a lower off-state current for the same threshold voltage (Vth) or a lower Vth for the same off-state current. These effects combine in a *higher on-to-off current ratio*. For the same signal headroom, the supply voltage can also be decreased and power can be saved.

  2) high-temperature applications as [12]

- the *physical leakage current* of junctions ($Ileak$) is smaller in SOI thanks to the reduced junction area (Fig. 1.2). Moreover, in FD SOI, $Ileak$ increases less with temperature than in Bulk and PD SOI as it keeps proportional to the intrinsic carrier concentration, ni, while above around $150°C$, the bulk and PD SOI $Ileak$ is proportional to ni^2.
- the decrease of the threshold voltage (Vth) with temperature is steeper in Bulk and PD SOI, as Vth depends on the depletion width, than in FD SOI in which the depletion width is constant. The off-current, defined as the drain current at zero gate voltage, then increases more rapidly with temperature in Bulk, degrading the performance of digital cells.

These advantages are well known in theory and have been demonstrated experimentally for long-channel MOSFETs. Nevertheless, in this thesis, we will come back on their discussion and point out other benefits of SOI technology. The resistance of these advantages to deep-submicron scaling will also be assessed.

1.2 Motivation of the work

Actual and future state-of-the-art electronic systems, possibly operating in harsh environments thus require to take reliability, test and power consumption into account. When designed in submicron technologies, the potential of IC's increases but new issues arise and the device performance must be assessed. Multi-domain and multi-signal approach are a must due to the integration of subsystems from different physical domains. A typical hierarchical view of an electronic system is depicted in Fig. 1.3. The highest system description level must ensure that the hardware and software parts correctly operate together. Refining the description for the hardware part, the system is divided into mixed-signal circuits and further subdivided into analog and digital cells. At the lowest level, all the cells are built using devices described by technological and physical parameters which are gathered in device model used at the cell level to emulate the circuit behavior. In a wider mixed-signal circuit, the device model are too complex and the behavioral description is preferred. At the system level, the software is described jointly with the behavioral description of the hardware.

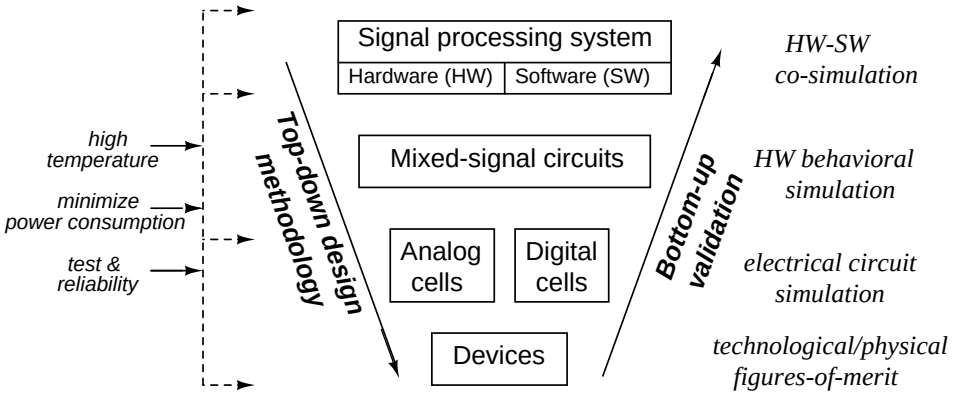

Figure 1.3: A signal processing system is divided into its subsystems: mixed-signal circuits, which are further divided into digital and analog circuits, both relying on devices. The different subsystems use different types of description and simulation protocols which must be linked in a hierarchical structure supporting top-down design and bottom-up validation.

For increased efficiency, the device challenges must be tackled at all these levels of abstraction. Great power savings can indeed be achieved by concurrent optimization of the hardware and software at the system level. This is however only possible if the power-specifications trade-offs are known from lower levels of description, implying the accurate modeling of the related imperfections. The designer hence needs e.g. information on the power consumption of the underlying analog and digital blocks and can then fix their specifications according to the constraints of the system at a higher level. At the digital and analog cells levels, power can also be saved by appropriately biasing the devices which requires intimate knowledge of the device i.e. accurate characterization and models at the physical or technological level. Moreover, the rapidly moving electronic market

imposes shorter and shorter time-to-market, reducing the design time and pushing forward the re-usability of designs and the creation of intellectual property (IP) units. IP's must be integrated and simulated as well in the IC or electronic system and therefore need a common description language. Efficient design thus results of the combination of a bottom-up validation and transmission of the power-specifications trade-offs and of a top-down synthesis methodology to best determine the specifications and design time for the different subsystems. For harsh environments, the subsystem behavior evolution with temperature must be included in the trade-offs.

The hierarchical description of the electronic systems in subsystems corresponds to models with different levels of abstraction, from the most abstract down to physical models. For digital applications, these abstraction levels are well defined. For the analog part, links and methodologies are missing. Among the different possibilities to improve the analog design flow (i.e. to improve the exchange of relevant information between the different levels of abstraction), we focus on three research fields in the present thesis.

- The efficiency of the device characterization for analog applications must be improved. (i) The figures-of-merit used by the process engineers to describe the device performance cannot be used directly by the analog circuit designer to predict the performance of the circuits. The technological parameters provided by the process engineers must be first included in a device model and simulated before the analog circuit designer knows how well the device corresponds to its needs. (ii) Moreover, some imperfections are not accurately modeled in weak and moderate inversion, preventing the designer to benefit of the increased efficiency of the device in these regions of inversion.
- A description common to behavioral and physical models as well as its efficient integration in mixed-signal circuits behavioral simulators is not yet widely available.
- For non-critical cells, automated synthesis would be useful and is still in the early phases of development for analog circuits [13]. More generally, tools which guide the designer to the optimal design choices or design-optimization methods would save time in the design of mixed-signal circuits.

1.3 Outline of the thesis

A refined illustration of the typical analog design flow is presented in Fig. 1.4. This design flow results of a top-down synthesis, from the specifications to the physical realizations, and of a bottom-up validation, from the test of the basic cells up to the test of the system.

In this thesis we contribute to improve the analog design flow at different levels. We deal with particular issues of the research fields identified in section 1.2. In part I, we deal with the characterization of MOSFETs in deep-submicron CMOS processes. Building an analog ID card, we improve the efficient transmission of specifications and analog performance, from the basic cell level to the actual implementation and vice-versa (Fig. 1.4). In part II, we develop models of basic analog cells in VHDL-AMS [14], a mixed-signal hardware description language. The basic cells can be further assembled in subsystems and electronic systems. This language provides a common description for different levels of abstraction and can support the entire design flow (Fig. 1.4). In part III, we assemble the basic cells VHDL-AMS models in a mixed-signal system, a third-order $\Delta\Sigma$ modula-

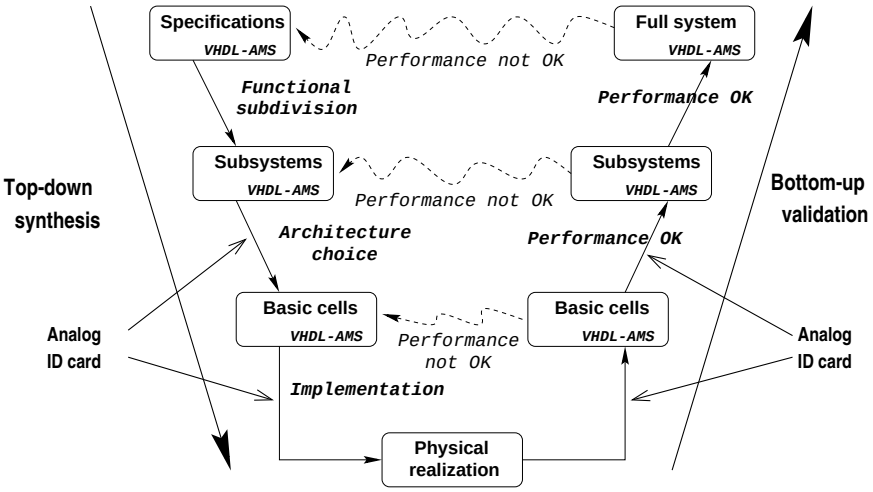

Figure 1.4: Top-down design and bottom-up validation design flows of analog circuits. VHDL-AMS provides a common description of the different abstraction levels and the analog ID card enables the transmission of relevant information: specifications and analog performance, from the basic cell level to the actual implementation and vice-versa.

tor using continuous-time integrators. We present an optimization methodology for the design of these integrators that can form the basis of a semi-automated design method for this type of circuit.

Integrated in a top-down design flow, our **analog ID card** (part I) aims to optimize power consumption and reliability of analog circuits at high temperature by enabling the choice of optimal process (bulk vs. partially-depleted silicon-on-insulator vs. fully-depleted silicon-on-insulator), optimal devices (different threshold voltages in a multi-threshold process) and optimal bias (weak inversion vs. moderate inversion vs. strong inversion). The design-oriented analog ID card is based on measurements only, as accurate models for high temperature or for devices biased in weak inversion are not always available. The lack of accurate models is particularly problematic in deep-submicron technologies as second-order effects which could be neglected at previous technology nodes must now be taken into account. Apart from the gain and gain-bandwidth product, the main analog parameters, we identify two analog bottlenecks on which we focus: the MOSFET mismatch in weak inversion and the harmonic distortion of MOSFETs in triode operation.

The **gain and gain-bandwidth product** (chap. 2) are assessed using the transconductance over drain current ratio ($\frac{gm}{I_D}$) vs. normalized drain current characteristic as it is the basis of a well-known design methodology [15] [16] [17]. Used in conjunction with this design methodology, we show how the $\frac{gm}{I_D}$ characteristic can be used to efficiently compare devices from different technologies. We apply the method to two practical cases. The first one (section 2.2.1) compares bulk, partially-depleted silicon-on-insulator and fully-depleted silicon-on-insulator in deep-submicron technologies as well as the impact of the HALO dopings for these technologies. The second one (section 2.2.2) investigates

the use of 0.15 μm long transistors for mixed-signal applications up to 250$^{\circ}C$. Using our comparison methodology for various bias ranges, we are able to show that

- using fully-depleted silicon-on-insulator instead of bulk can improve the power consumption even in deep-submicron technologies;
- the HALO dopings are detrimental to analog performance and should be avoided in analog MOSFETs, except for short-channel devices targeting high-gain and low-frequency applications;
- transistors from a well-optimized silicon-on-insulator process can reliably be used up to 250$^{\circ}C$ for mixed-signal applications.

Concerning the gain and gain-bandwidth product, the analog ID card can as requested optimize the power consumption and reliability at high temperature and is still applicable in deep-submicron technologies. Concerning the reliability at high temperature, aging phenomena and failure modes are not assessed in this work. They can however be integrated in the VHDL-AMS models.

To benefit from the technology downscaling, ever more signal processing is done in the digital domain. Continuous-time signal processing however still remains unavoidable or very advantageous for some applications. MOSFET-C continuous-time filters are for example good candidates for low-power filtering of signals with bandwidths lower than 1 MHz [18]. The bottleneck of these filters is their linearity, mainly determined by MOSFETs in triode emulating the resistances. If we want to use these filters to benefit from their low-power consumption, we have to evaluate if their linearity complies with the application under consideration. Focusing on fully-differential structures, we use the third-order harmonic distortion (HD3) as figure-of-merit. The **third-order harmonic distortion of MOSFETs in triode** (chap. 3) is however rarely predicted accurately by actual SPICE models. Two different resistive structures using two and four MOSFETs in triode, respectively, were proposed to emulate the resistances [19] [20] [21] for MOSFET-C filters; we assess both of them. We develop an original HD3 measurement-based comparison methodology under practical design considerations and wide temperature range (section 3.5). The methodology relies on a design-oriented investigation of the physical phenomena causing the third-order harmonic distortion, which gives insight on the best gate bias and device type for optimal linearity. Based on measurements of different device types in a deep-submicron silicon-on-insulator CMOS process and in a wide temperature range, we show

- that HD3 of the resistive structures employing two MOSFETs is determined by the mutual interaction of body-related effects and of effects linked to mobility reduction with vertical field (section 3.3).
- that, under practical design considerations including tuning to compensate on-chip for variations of process in a wide temperature range, the structure composed of four MOSFETs should be preferred. In this particular process and for the design specifications under consideration, we can target applications for which 0.1% linearity is sufficient (section 3.5).

The HD3 comparison methodology fits in the analog ID card as it predicts the linearity we can achieve for a particular application with MOSFET-C filters and hence evaluate their

use compared to other types of continuous-time filters. The structure composed of four MOSFETs still require better understanding and modeling (section 3.4). Our analysis of the structure with two MOSFETs is only qualitative, which is however coherent with our design-oriented approach.

In deep-submicron processes, the supply voltages are reduced, forcing to bias the transistors in weak or moderate inversion. In the very common case of an input stage of an amplifier, constituted of a differential pair loaded by a current mirror, the output dynamic range can be indeed improved by biasing the transistors of the current mirror in weak inversion. This is however known to be detrimental to the drain current mismatch between the transistors of the current mirror and hence to the offset of the input stage [22] [23]. In chapter 4, we focus on the **MOSFET drain current mismatch in weak inversion**. On one hand, we question the validity of the classical models in weak inversion and on the other hand, we evaluate the impact of the bias of the transistors of the current mirror on the current mirror mismatch. Based on measurements of the drain current mismatch on very different technologies and at different temperatures,

- we show that, contrarily to the classical assumption, the mismatch on the drain current in weak inversion is not only determined by the mismatch on the threshold voltage. The gate voltage dependence of the linearized body effect factor (n) must also be taken into account and we propose a semi-empirical term to improve the mismatch models in weak and moderate inversion (section 4.4).
- we predict that, if the mismatch is evaluated along with the other analog parameters (i.e. in practical design situation), biasing the transistors of the current mirror in weak inversion can even improve the current mirror mismatch (section 4.5).

As the mismatch data can be integrated in an efficient top-down design methodology, it improves the efficient transmission of specifications and analog performance, from the basic cell level to the actual implementation and vice-versa. We did not include the additional term we propose in a complete mismatch model as it dependence on the MOSFET size has not been investigated yet and as it would require the development of a complete drain current mismatch model, which is beyond the scope of our analysis.

To improve the efficiency of the design flow, we also need a language common to all the abstraction levels, which allows to mix the description levels in a single simulation. The effect of the performance of the different subsystems on the system, as well as the comparison between different topologies or implementations of the subsystems can be evaluated more easily. **VHDL-AMS**, a mixed-signal hardware description language fits these specifications as it is a language with multi-domain and multi-level of abstraction capabilities. In part II, we develop VHDL-AMS models for basic analog cells, which can be further assembled in subsystems. They provide the language through which the specifications and analog performance are exchanged, from the basic cell level to the actual implementation and vice-versa. The design-oriented models are written to support top-down design methodologies.

The VHDL-AMS models are assembled in a mixed-signal system in part III. The mixed-signal test vehicle is **the modulator, the analog part of a $\Delta\Sigma$ analog-to-digital converter** (Fig. 1.5) and its specifications are a resolution of $14\ldots16$ *bits* and a signal bandwidth of ≈ 10 *kHz* corresponding to metering applications.

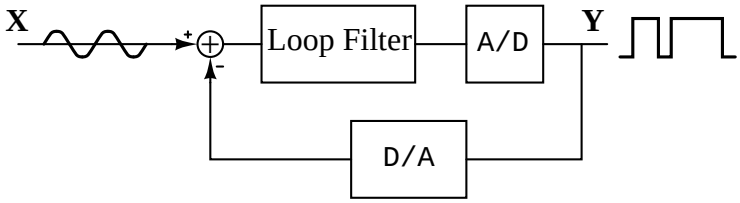

Figure 1.5: A modulator of a $\Delta\Sigma$ analog-to-digital converter is composed of an analog loop filter, an internal analog-to-digital converter and a feedback digital-to-analog converter.

The loop filter of the modulator consists of integrators which can be implemented using discrete-time or continuous-time techniques. $\Delta\Sigma$ modulators implemented using continuous-time techniques are potentially interesting for lowering the power consumption (section 6.2). In chapter 6, the potential and design challenges of such $\Delta\Sigma$ modulators are reviewed. We also show their potential for operation at high temperature (section 6.3). Continuous-time integrators can be implemented by different filter topologies: $gm-C$, MOSFET-C or active RC techniques with integrated resistors. We show that the linearity of the first integrator of the loop filter is a determining factor of the converter resolution; its linearity must match the target resolution. The $gm-C$ filters are known to exhibit poor linearity [24], active RC integrators with passive resistors attain high linearity and are then a possible choice. MOSFET-C are a good candidate to lower the power consumption and provide on-chip tuning but, based on the analog ID card of part I, we predict that their linearity would be insufficient for the specifications under considerations (section 6.4.6). Focusing on active RC integrators with passive resistors, we develop a design optimization methodology that can be used in a semi-automated analog design flow (section 6.4.7.4). The entire analysis is based on simulations using behavioral models and no silicon implementation is presented as it would have required too much time.

Finally, in chapter 7 we present in more detail the current analog design flow and show how the use of the analog ID card combined with mixed-signal hardware description languages can **improve this design flow**. We also put our work in perspective in this new design flow.

1.4 Major Contributions

In the different domains we investigated, we here below quickly identify the key contributions of the present thesis.

- The analog ID card combined with mixed-signal hardware description languages can improve the efficiency of the current analog design flow (chap. 7).
- Fully-depleted silicon-on-insulator is still advantageous over bulk for analog applications in deep-submicron technologies and HALO dopings are unfavorable to analog applications for various processes, except for short-channel devices targeting high-gain and low-frequency operation. Surprisingly, 0.15 μm long devices can reliably be used at high temperature for mixed-signal applications (chap. 2).

- The third-order harmonic distortion (HD3) in MOSFET-C resistive structures with two MOSFETs are determined by body- and mobility reduction related effects. Based on an original HD3 comparison methodology, we recommend the use of the resistive structures based four MOSFETs over the ones based on two MOSFETs (chap. 3).

- The gate voltage dependence of the mismatch on the linearized body effect factor (n) plays a role in the mismatch in weak inversion, in addition to the mismatch on the threshold voltage. Optimizing the mismatch of the current mirror of an input stage of an amplifier along with other analog performance parameters, we show that, under the design targets considered in chapter 4, the mismatch decreases if we bias the transistors of the current mirror in weak inversion (chap. 4).

- We provide a VHDL-AMS model to emulate the thermal noise in a time-domain simulation (chap. 5).

- The potential of continuous-time implementations of $\Delta\Sigma$ modulators for operation at high temperature is pointed out. The use of MOSFET-C integrators to implement the loop filter of the $\Delta\Sigma$ modulator is assessed. Active RC integrators with passive resistors are the best implementation for the design specifications considered. For such integrators, a design optimization methodology is presented to be included in a semi-automated analog design flow (chap. 6).

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Part I

From device performance to analog cells performance : the device analog ID card

Introduction

The semiconductor market is driven by the digital applications, decreasing ever further the devices dimensions. Effects which could be neglected at previous technology nodes must now be taken into account. While the performance of a technology for digital applications is generally assessed, the tools and methodologies are still lacking for analog, and hence mixed-mode, applications. The figures-of-merit defined by process engineers to describe the device performance cannot indeed be directly used by the circuit designer to predict the performance of the circuits. The technological parameters must be first included in a device model and simulated before the analog circuit designer knows how well the device corresponds to its needs. Moreover due to the short time-to-market it is not possible to wait for optimal device models including all MOSFETs imperfections.

The measurement-based analog ID card developed below aims to make the link between the technology and the analog cells. In the context of guided top-down design and bottom-up validation flows, the analog ID card characterizes the devices for analog cells. In conjunction with the design flow, it **optimizes** the **power consumption** of analog cells and their **reliability at high temperature** by **choosing the optimal process** (e.g. bulk vs. silicon-on-insulator), **device** (e.g. in a multi-threshold voltages process) and **bias**. We limit our analysis of the underlying physical phenomena to what is of interest for the design of high-performance analog circuits.

Each class of analog cells requires the definition of its proper subset of the analog ID card. In this work, we focus on the main analog parameters (gain *Av* and gain-bandwidth product *GBW*) and on two important MOSFET imperfections (the MOSFET mismatch in weak inversion and the distortion of MOSFETs in the triode regime). For these two imperfections, there is indeed a lack of accurate models and it is difficult to take them into account in practical design situations, i.e. together with other design constraints.

We start in chapter 2 with the major analog parameters: **Av** and **GBW**. Focusing on the major analog cell, the **amplifier** and based on measurements, we investigate if, in deep-submicron CMOS technologies,

- the fully-depleted silicon-on-insulator technology is still advantageous over bulk;
- the HALO dopings are favorable to analog design as they are for digital;
- the short-channel devices can safely be used up to $250°C$ in mixed-mode circuts.

The figures-of-merit defined for this purpose can moreover be used for any device on any technology and can be combined with powerful top-down design methodologies.
In chapter 3, we focus on the **MOSFET-C analog filters**, in which resistors are implemented by transistors in triode regime and investigate the **third-order harmonic distor-**

tion of such MOSFET. In this context,

- we extend previous analyses to deep-submicron technologies and to operation at high temperature and identify the underlying physical phenomena;
- we gather the knowledge gained by the physical analysis in an original design-oriented comparison methodology;
- using this comparison methodology, we can predict, based on measurements, the linearity of a MOSFET-C integrator and optimally choose the resistance implementation, the device type and bias.

The comparison methodology can also be applied to any process and provides efficient information on the resistive structures in MOSFET-C filters.

The **mismatch in weak inversion** is studied in chapter 4 as current models do not provide an adequate characterization. The downscaling of the technologies indeed moves the transistor bias point to weak inversion. Current mirrors biased in weak inversion are usually assumed to be detrimental to the **offset voltage**. Based on measurements on very different technologies, we

- show the drain current mismatch evolution with temperature in the case of a silicon-on-insulator process;
- identify the physical phenomena not included in current models, which plays a role in the drain current mismatch in weak inversion and propose a new semi-empirical term;
- integrate the mismatch information in a top-down design methodology to determine the best bias of the current mirror of an amplifier input stage for minimum offset voltage.

Chapter 2

Major analog figures-of-merit

In order to present our methodology we start from a simple analog cell: the common-source amplifier stage (Fig. 2.1 a), in which a MOSFET transistor is biased by a DC current source (I_{BIAS}) and loaded by a capacitance (C_L). The results may nevertheless be extended to more complex analog cells.

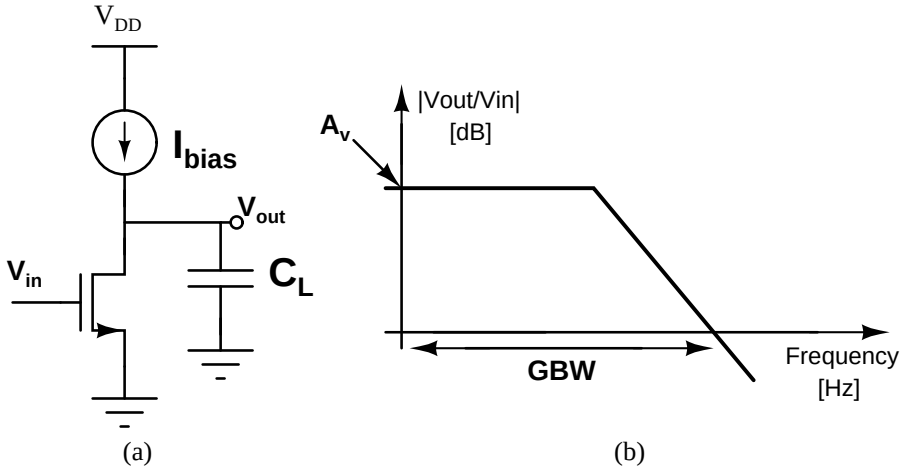


Figure 2.1: (a) Common-source amplifier stage: MOSFET transistor biased by a DC current source (*Ibias*) and loaded by a capacitance (C_L). (b) Major analog characteristics of an amplifier: low-frequency gain (*Av*) and gain-bandwidth product (*GBW*).

The major analog performance of this common-source amplifier, i.e. the low-frequency gain (*Av*) and gain-bandwidth product (*GBW*) (Fig. 2.1,b), are given by

$$Av = \frac{gm}{gd} = \frac{gm}{I_D} V_{EA} \tag{2.1}$$

$$GBW = \frac{gm}{2\pi C_L} = \frac{gm}{I_D}\frac{Ibias}{2\pi C_L} \tag{2.2}$$

where *gm* is the device transconductance, *gd* its output conductance and V_{EA} the Early voltage defined as $V_{EA} = \frac{I_D}{gd}$, I_D being the drain current and *Ibias* in this particular case.

The transconductance over drain current ratio ($\frac{gm}{I_D}$) and V_{EA} in saturation are chosen as analog figures of merit for the amplifier as they indicate the device efficiency to convert DC power into gain (2.1) and AC frequency (2.2). The $\frac{gm}{I_D}$ ratio is moreover an insightful design parameter as shown in (2.1) and (2.2) and V_{EA} is preferred over gd as it avoids the gd dependence on the drain current (I_D). We define $\frac{I_D}{W/L}$ as the normalized current ($Inorm$), W and L being the device width and length, respectively. We use the curve of $\frac{gm}{I_D}$ ratio vs. $Inorm$ (Fig. 2.2) as key in our design-oriented characterization methodology. It is a powerful device comparison tool as will be demonstrated here below.

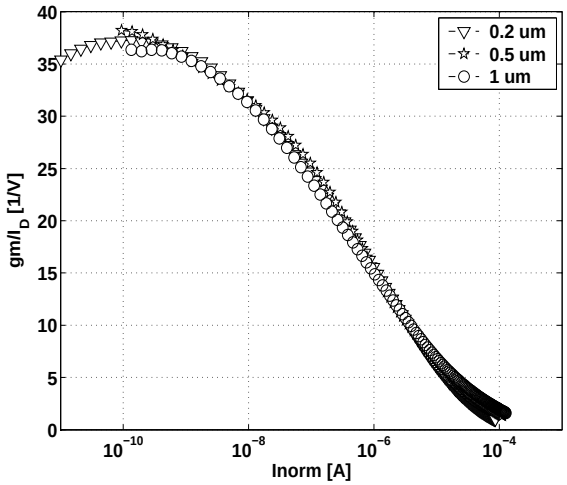


Figure 2.2: Measured $\frac{gm}{I_D}$ ratio vs. $Inorm$ for n-type MOSFETs of a fully-depleted silicon-on-insulator 0.15 μm technology with $L = 0.2\ \mu m$ (∇), $L = 0.5\ \mu m$ ($\star$), $L = 1\ \mu m$ ($\circ$). $W = 10\ \mu m$ for all devices, $V_D = 0.75\ V$, $V_S = 0\ V$.

The two figures-of-merit are chosen for they are the basis of a well-known design methodology proved to be efficient in state-of-the-art designs [1] [2] [3]. Associated to this powerful top-down design methodology, the figures-of-merit can be turned into a design-oriented assessment methodology. Here below, we first remind the basis of the $\frac{gm}{I_D}$ design methodology in section 2.1 and in section 2.2 we apply it to new and interesting cases of study: 1) the influence of HALO doping on the analog performance in different CMOS technologies; and 2) the assessment of deep-submicron SOI CMOS transistors for high-temperature applications.

2.1 The gm/I_D vs. $Inorm$ curve: a comparison tool

The $\frac{gm}{I_D}$ vs. $Inorm$ curve, obtained from an I_D vs. V_G DC curve in saturation by $\frac{gm}{I_D} = \frac{\partial \ln I_D}{\partial V_G}$, is fairly independent on the device sizes and threshold voltage (Vth), making it a characteristic common to all nMOSFET or pMOSFET transistors of the same type of a technology and hence a powerful comparison tool (Fig. 2.2). Using the EKV model [4],

the $\frac{gm}{I_D}$ ratio is indeed described as

$$\frac{gm}{I_D} = \frac{1}{nU_T}\frac{1-e^{-\sqrt{ic}}}{\sqrt{ic}} \tag{2.3}$$

where U_T is the thermal voltage, *ic* is the inversion coefficient and *n* is the slope factor, defined by

$$n = \left(1 - \frac{\gamma}{2\sqrt{V_G - Vth + \left(\frac{\gamma}{2} + \sqrt{\psi_0}\right)^2}}\right)^{-1} \tag{2.4}$$

where γ is the body effect factor, Vth is the threshold voltage and $\psi_0 + Vch$ is the surface potential in strong inversion, Vch being the voltage-to-substrate applied to the MOSFET channel. *ic* is an indicator of the inversion regime as it is lower (higher) than 1 in weak (strong) inversion. *ic* is given by [4]

$$ic = \frac{I_D}{2n\mu C_{ox}\frac{W}{L}U_T^2} \tag{2.5}$$

where C_{ox} stands for the front gate capacitance per unit area and μ is the channel mobility. (2.3) and (2.5) indicate that the $\frac{gm}{I_D}$ vs *Inorm* characteristic is on the first order independent on the device size and Vth. The influence of the size will show up through second-order effects like mobility reduction, for example. In practical design cases, the $\frac{gm}{I_D}$ vs *Inorm* can be considered as common for devices of the same type of the same technology (Fig. 2.2).

The $\frac{gm}{I_D}$ vs. *Inorm* characteristic is also continuous from the weak inversion (wi) to the strong inversion (si) regime. It can be asymptotically divided in three zones (Fig. 2.3): 1) at low *Inorm*, where the $\frac{gm}{I_D}$ is constant vs. *Inorm* corresponding to weak inversion as in this region, $\frac{gm}{I_D} = \frac{1}{nU_T}$; 2) at high *Inorm*, $\frac{gm}{I_D} \propto \sqrt{\frac{1}{Inorm}}$, corresponding to strong inversion and 3) in the central part of the characteristic, a transition region corresponds to moderate inversion.

To better understand the key role of the $\frac{gm}{I_D}$ factor on the analog performance (2.1) (2.2) we describe the top-down design of a common-source amplifier (Fig. 2.1 a) using the $\frac{gm}{I_D}$ methodology [1] [5] [6] [2] [3]. The design specifications are the low-frequency open loop gain (*Av*), the gain-bandwidth product (*GBW*) and the load capacitance (C_L) while the transistor performance is described by the $\frac{gm}{I_D}$ vs. *Inorm* characteristic and Early voltage (V_{EA}). The bias current (*Ibias*), the transistor width (W) and length (L) are determined for each transistor bias point, i.e. each value of the $\frac{gm}{I_D}$ ratio, as follows (Fig. 2.4):

- *gm* is computed from the specifications as $gm = 2\pi GBWC_L$;
- *Ibias* can be derived from *gm* as $Ibias = \frac{gm}{\frac{gm}{I_D}}$;
- *Inorm* is obtained, for a given $\frac{gm}{I_D}$ value, through the $\frac{gm}{I_D}$ vs. *Inorm* characteristic;
- $\frac{W}{L} = \frac{Ibias}{Inorm}$ by definition, which yields $\frac{W}{L}$;
- defining $V_{EA,L}$ as $V_{EA,L} \equiv \frac{V_{EA}}{L}$ and using (2.1), $Av = \frac{gm}{I_D}V_{EA,L}L$, it yields the transistor length as $L = \frac{10^{\frac{Av[dB]}{20}}}{\frac{gm}{I_D}V_{EA,L}}$;
- and finally, $W = \frac{W}{L}L$.

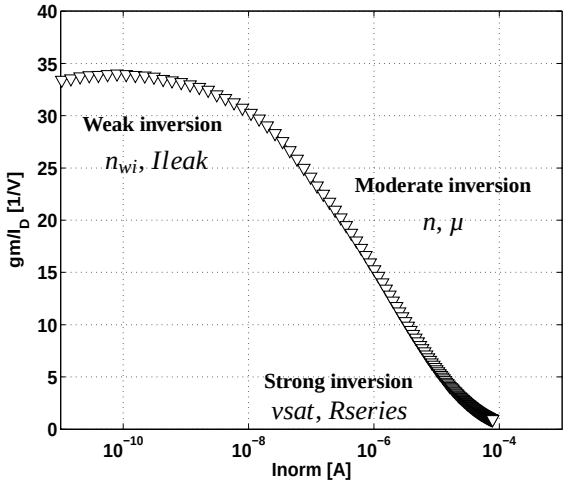


Figure 2.3: Typical $\frac{gm}{I_D}$ ratio vs. $Inorm$ showing the different regions of inversion and the main physical parameters playing a role in weak (n_{wi}, the inverse of the subthreshold slope and $Ileak$, the leakage current), in moderate (n, the linearized body effect factor and μ the mobility) and strong inversion ($vsat$, the velocity saturation and $Rseries$, the series resistance).

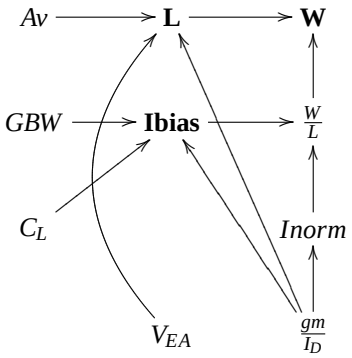


Figure 2.4: Top-down $\frac{gm}{I_D}$ design methodology of a common-source amplifier. The design specifications are Av, GBW and C_L while the transistor performance is described by the $\frac{gm}{I_D}$ vs. $Inorm$ characteristic and V_{EA}. The results are W, L and $Ibias$.

When represented vs. $Inorm$, the $\frac{gm}{I_D}$ characteristic allows to quickly distinguish the performance in the different regions of operation, corresponding to different applications (Fig. 2.5).

Concerning **baseband applications**, where the focus lies on the gain and the precision, the designer will look for high $\frac{gm}{I_D}$ ratios following (2.1). It corresponds to the weak inversion region (Fig. 2.5 a). The small drive current available in this region is in this case not a problem as the frequency requirements are low. To compare the device performance, we will then focus on the maximum value of the $\frac{gm}{I_D}$ as it corresponds to the highest achievable gain.

In this region of inversion, the characteristic will be mainly influenced by the leakage

current (*Ileak*) and by the n_{wi} factor, defined as the inverse of the subthreshold slope. The $\frac{gm}{I_D}$ characteristic is shifted 1) up for lower n_{wi} (i.e. more ideal transistor) and 2) to higher *Inorm* for higher *Ileak* (Fig. 2.3). The $\frac{gm}{I_D}$ vs. *Inorm* characteristic can also be used to determine the causes of the differences in the performance of different devices.

The higher the $\frac{gm}{I_D}$ ratio in weak inversion the more efficient the device for high-precision applications as it corresponds to higher gain for the same power consumption and lower bias current for the same *GBW* (2.1).

Concerning **high-frequency application**, where a higher drive current is needed to rapidly charge/discharge the load capacitance (Fig. 2.1), the region of operation will shift toward higher *Inorm*, i.e. toward the moderate and strong inversion regions. For this kind of applications, the best device will be the one yielding the highest *Inorm* for a given bias (i.e. a given $\frac{gm}{I_D}$). This device indeed achieves higher frequency of operation for the same power consumption or alternatively, same frequency of operation with a lower power consumption (2.2). We will then compare the *Inorm* corresponding at different devices for a fixed $\frac{gm}{I_D}$ (Fig. 2.5 b).

In the region of the $\frac{gm}{I_D}$ characteristic under concern, the most influencing parameters are the linearized body factor (*n*) and the mobility; the characteristic is shifted to lower *Inorm* 1) for higher *n* and 2) for lower mobility (Fig. 2.5).

The best device for high-frequency applications will be the one yielding the highest *Inorm* for the same $\frac{gm}{I_D}$ as it corresponds to higher *GBW* for the same power consumption or reduced power consumption for the same *GBW* (2.1).

The use of $\frac{gm}{I_D}$ vs. *Inorm* characteristic as pivot of a characterization methodology allows to rapidly investigate the device performance in the wanted region of operation by inspecting the right zone of the characteristic.

The $\frac{gm}{I_D}$ ratio is as shown moreover the basis of practical design methodologies [1] [6] [7] [3] [8] that have already been successfully adapted to practical and high performance design cases. These design methodologies are particularly interesting as they provide *hand calculations* for analog design valid in all region of operation, contrarily to methodologies [9][10] relying on the MOSFET square-law model, which fail for advanced submicron devices and devices biased in the moderate inversion regime. As already highlighted, this is an advantage as the technology evolutions force the designer to bias the transistors in this moderate inversion regime.

As a conclusion, we choose the $\frac{gm}{I_D}$ as figure-of-merit and the $\frac{gm}{I_D}$ vs. *Inorm* characteristic as pivot of our characterizing methodology as

- *Av* and *GBW* directly depend on it, so it provides design-oriented information.
- It is the basis of practical design methodologies.
- The characteristic is continuous across all regions of operation allowing to assess the device performance in all regions of operation without any model.
- The $\frac{gm}{I_D}$ vs. *Inorm* characteristic can be used as a comparison tool as it can be considered as common for all devices of the same type of the same technology.
- It is valid for deep submicron MOSFETs.
- It offers a quick insight into the device performance for a given application.

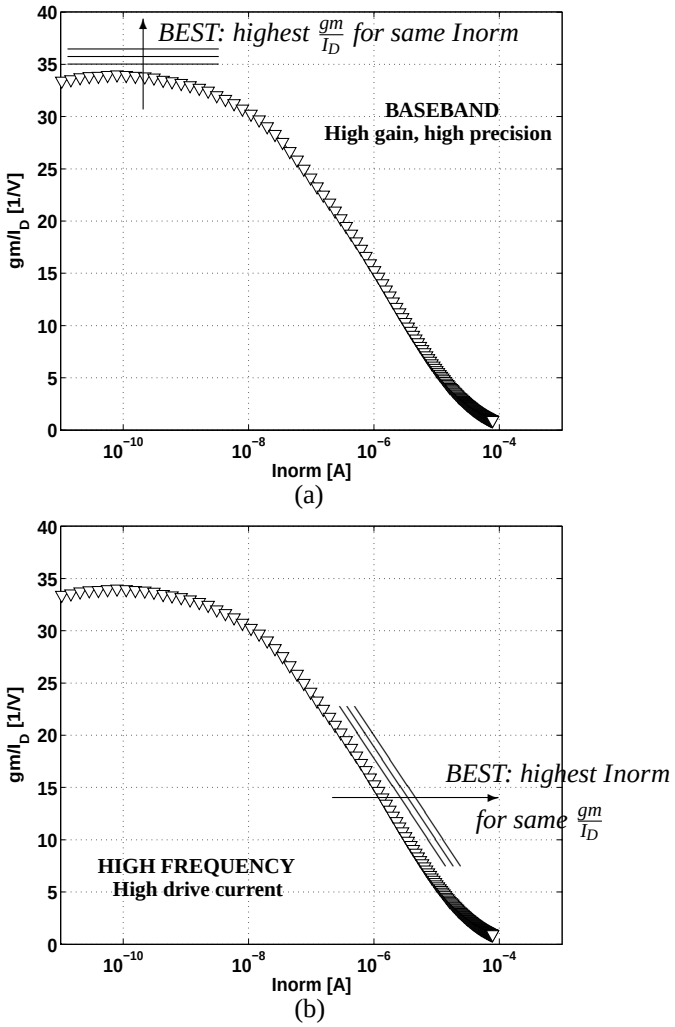


Figure 2.5: Measured $\frac{gm}{I_D}$ ratio vs. *Inorm* showing the different region of inversion corresponding to different types of application

The choice of the V_{EA} as second figure-of-merit for the evaluation of *Av* and *GBW* is then straightforward.

2.2 Application to practical cases

In the two following sections, we use our figures-of-merit to assess the analog performance of very advanced devices, i.e. we don't look for deep physical understanding (which is addressed in appendix A and [11] [12]). In the first application of the methodology, we assess the pertinence from designer perspectives, for devices targeting mixed-signal operation, of a channel engineering process step: the HALO implants. We compare

different device types (conventional bulk, partially-depleted (PD) and fully-depleted (FD) silicon-on-insulator (SOI) transistors) with and without HALO implants. Our methodology is used to assess the impact of HALO on the analog performance, for the first time systematically and on different technologies. The second application questions also for the first time the possibility of using deep-submicron silicon-on-insulator CMOS technologies for mixed-signal applications up to 225°*C*.

2.2.1 Mixed-mode devices: with or without HALO implants ?

The HALO (or pocket) implants are additional implants near the source and the drain of the transistor, targeting better control of the short channel effects [13] (Fig. 2.6). For very small devices the two HALO dopings merge and the channel doping level is then increased. HALO dopings in this way prevent the drop of the threshold voltage for very short channels. Maintaining Vth for short-channel transistors, the HALO implants reduce the off-state leakage current while maximizing transistor linear and saturated drive currents in digital applications. The influence of HALO implants on Vth and off-currents has been investigated in [14][15] but their influence on analog performance must be assessed when considering mixed-signal applications.

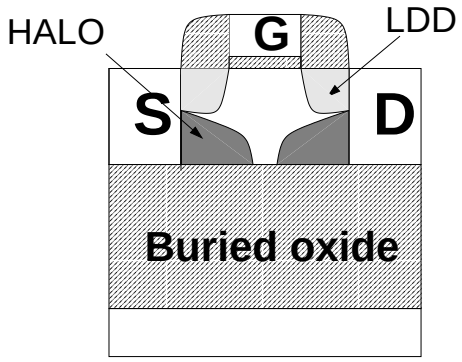


Figure 2.6: Cross-section of a silicon-on-insulator transistor showing the LDD regions and HALO doping.

The nominal gate length (L_{nom}) of the three technologies we investigated is 0.12 μm. We measured devices with gate lengths varying from 10 μm down to 0.08 μm. The oxide thickness (t_{ox}) of the measured FD and PD devices is 2.5 nm, the final Si film thickness (t_{si}) is 30 nm for the FD and 100 nm for the PD while the buried oxide thickness are, respectively 400 nm and 200 nm [16]. As the measured PD devices suffer from the kink effect [17] for a drain voltage (V_D) above 1 V, we performed all comparisons for $V_D < 1\,V$ to fairly compare the devices. We will in turn investigate the devices targeting baseband and high-frequency applications.

A) Focusing on **baseband applications**, we focus on the maximum gain, i.e. maximum of $\frac{gm}{I_D}\left(\left(\frac{gm}{I_D}\right)_{\max}\right)$ and V_{EA} (2.1) (Fig. 2.5 a). The HALO implantation clearly helps

to keep a good device performance when scaling down the length (Fig. 2.7) for they better control the short-channel effects (SCE) due to the higher doping level for short transistors.

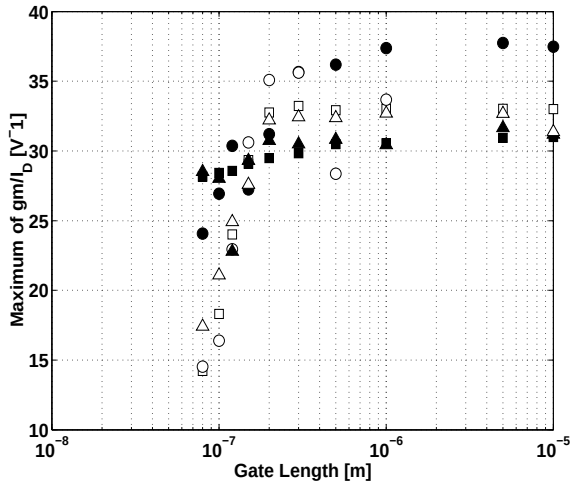


Figure 2.7: Maximum of measured $\frac{gm}{I_D}$ ratio vs. gate length for n-type MOSFETs of Bulk (□), FD SOI (○) and PD SOI (△) transistors. Each device type with (full symbols) and without HALO implantation (void symbols). $W = 10\ \mu m$ for all devices, $L_{nom} = 0.12\ \mu m$, $V_D = 0.75\ V$ and $V_S = 0\ V$.

As expected from known theory [17], FD devices down to the nominal channel length of $0.12\ \mu m$ indeed maintain a higher maximum $\frac{gm}{I_D}$ (when compared to PD and bulk) resulting in a higher gain for the same power consumption (2.1). For channel lengths smaller than $0.12\ \mu m$, HALO implantation still needs further optimization, which is however less relevant than longer lengths when focusing on baseband applications. Bad influence of HALO implants on V_{EA} for long channel devices was reported [18] and is here confirmed (Fig. 2.8 and 2.9). The V_{EA} is extracted for all devices for $V_D = 0.5\ V$ as I_D vs. V_D characteristic of the PD devices with HALO implants exhibit an enhanced kink effect, starting at V_D as low as $0.5\ V$.

The value of V_{EA} for nominal length transistor $L = 0.12\ \mu m$ is about $1\ V$; it amazingly confirms the proportionality to the usual design rule of thumb of V_{EA} on the order of $10\ V$ per μm of channel length. The positive influence of the HALO implants on short channel transistor performance is also demonstrated from a V_{EA} point-of-view as the higher HALO doping prevents drain field penetration [19]. However, at longer channel lengths (i.e. for $L > 2 * L_{\mathrm{HALO}}$, where L_{HALO} is the length of the HALO), the HALO implants clearly deteriorate the V_{EA} characteristic and suppress proportionality to L (Fig. 2.8). For devices with HALO doping and $L > 2 * L_{\mathrm{HALO}}$, V_{EA} is indeed not determined anymore by classical channel-length modulation. The HALO doping causes the apparition of two sharp potential barriers near source and drain. Due to the high doping level in a small region, the sensitivity of the drain barrier height to variation of the V_D potential is high [20], which has a detrimental effect on V_{EA}. The Early voltage in the case of long-channel devices ($L > 2 * L_{\mathrm{HALO}}$) with HALO doping is then dominated by the modulation of the barrier of potential created near the drain [21] and is indeed quasi constant with device length (Fig. 2.8 and 2.9) while it takes off for devices without HALO. Using devices with

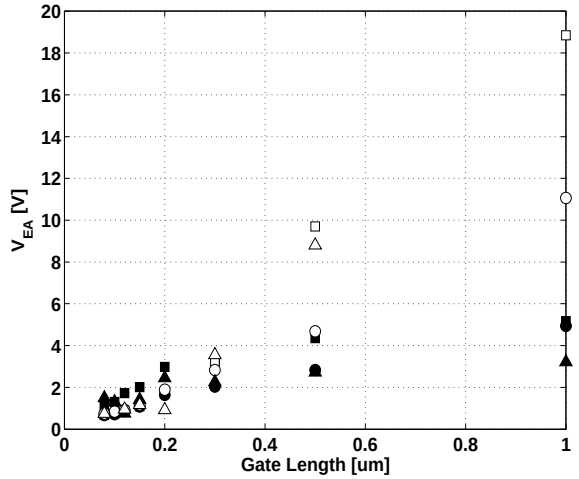


Figure 2.8: Measured V_{EA} at $Inorm = 4\ \mu A$ vs. gate length for n-type MOSFETs of Bulk (□), FD SOI (○) and PD SOI (△) transistors. Each device type with (full symbols) and without HALO implantation (void symbols). $W = 10\ \mu m$ for all devices, $L_{nom} = 0.12\ \mu m$, $V_D = 0.50\ V$ and $V_S = 0\ V$.

HALO, high gain values can not be reached by increasing, as usually, the device length, rendering the achievable gain much smaller for such devices (2.1). For 1 μm long devices, the loss in the achievable gain due to V_{EA} is already of $\approx 55\%$ and $\approx 74\%$ for FD and Bulk (Fig. 2.8) devices, respectively.

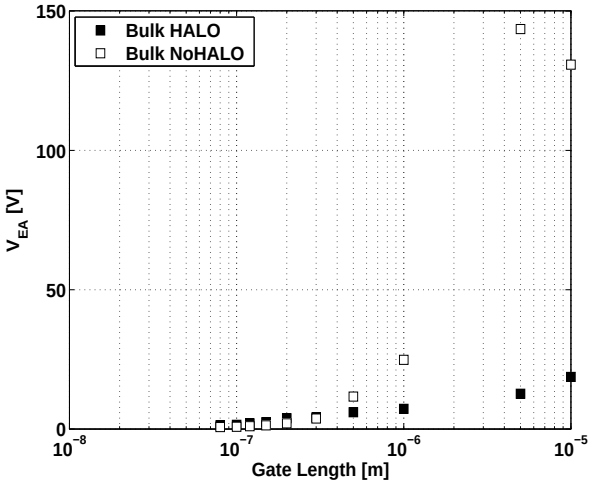


Figure 2.9: Measured V_{EA} at $Inorm = 4\ \mu A$ vs. gate length for n-type Bulk MOSFETs, with (full symbols) and without HALO implantation (void symbols). $W = 10\ \mu m$, $L_{nom} = 0.12\ \mu m$, $V_D = 0.75\ V$ and $V_S = 0\ V$.

B) High-frequency applications, on the other hand, require high drive currents and shorter channel lengths in order to reach high frequencies while consuming as low power

as possible (2.2). We compare the devices for a fixed $\frac{gm}{I_D}$ ratio equal to 10 V^{-1}, corresponding to the widely used gate voltage overdrive (GVO, $V_{GS} - Vth$) value of 200 mV [9]. Due to the lower quality of the wafers (old and damaged gate oxide), the measured FD devices without HALO implants are irrelevant for this bias. The FD devices with HALO implants perform better than the other devices types also with HALO implants (Fig. 2.10).

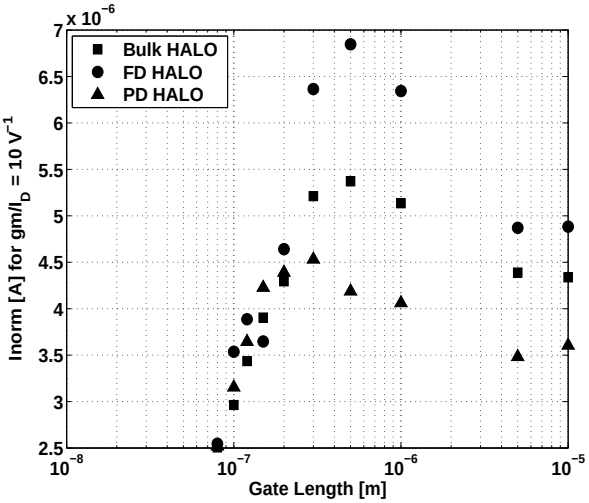


Figure 2.10: Measured $Inorm$ **corresponding to** $\frac{gm}{I_D} = 10\ [V^{-1}]$ **vs. gate length for n-type MOSFETs: Bulk (□), FD SOI (○) and PD SOI (△) with HALO implantation.** $W = 10\ \mu m$ **for all devices,** $L_{nom} = 0.12\ \mu m$**,** $V_D = 0.75\ V$ **and** $V_S = 0\ V$**.**

The HALO implants degrade the drive current achievable for all device lengths due to the higher or non-uniform doping, which lowers the mobility (Fig. 2.11). The HALO influence is not quantitatively the same for different device types and lengths, probably due to different technological optimization choices for each device type.

C) A first **conclusion** can be drawn: our study demonstrates for the first time that well-processed and optimized **FD SOI MOSFETs are clearly interesting for analog applications** as, when fairly compared to other device types in design situations, they allow the designer to reach higher gain and higher GBW for the same power consumption or, alternatively, to reduce the power consumption for the same GBW (2.2) and (2.1). The application of our methodology moreover allowed to efficiently assess the HALO implants for analog and hence, mixed-signal applications, for the **first time in SOI and systematically on different technologies**. Our conclusions are that the HALO implants are

- favorable to short-channel devices biased in moderate or weak inversion (i.e. targeting high gain or high precision) as a better maximum $\frac{gm}{I_D}$ (Fig. 2.7) and a comparable V_{EA} (Fig. 2.8) are obtained, and then, a higher gain for the same power consumption (2.1). On the contrary to [21], we demonstrated that HALO implants may be favorable to analog applications in this case.

- unfavorable to long-channel devices biased in moderate or weak inversion (i.e. target-

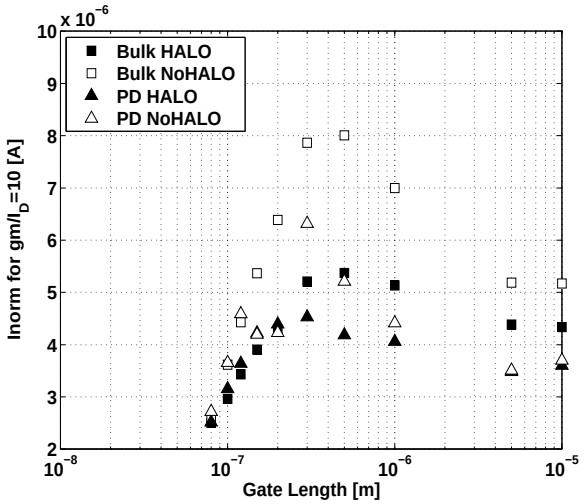


Figure 2.11: Measured $Inorm$ **corresponding to** $\frac{gm}{I_D} = 10\ [V^{-1}]$ **vs. gate length for n-type MOSFETs: Bulk (□) and PD SOI (△) with (full symbols) and without HALO implantation (void symbols).** $W = 10\ \mu m$ **for all devices,** $L_{nom} = 0.12\ \mu m$**,** $V_D = 0.75\ V$ **and** $V_S = 0\ V$**.**

ing high gain or high precision) as the obtained gain is reduced (2.1) due to the much smaller V_{EA} (Fig. 2.8).

- unfavorable to devices biased in strong inversion (i.e. targeting high drive current) as the drive current of devices with HALO implants is smaller (Fig. 2.11), requiring a higher power consumption to reach the targeted transition frequency (2.2).

Our assessment methodology has been shown to efficiently benchmark very different technologies in practical design situations. According to the targeted application (i.e. high gain or high frequency, ...), the designer is then able to easily select, based on our figures-of-merit: $\frac{gm}{I_D}$ and V_{EA}, the device type and, if available in the technology, devices with or without HALO implants. The designer can for example win $\approx 20\%$ of power consumption for the same transition frequency by using 1 μm long FD SOI transistors in place of other device types with the same length (Fig. 2.10). Furthermore, the methodology can evidently be used to assess other technologies or process options.

For increased performance, analog designers should

(1) use FD SOI MOSFETs

(2) avoid if possible transistors with HALO implants in all cases except for short-channel devices biased in weak or moderate inversion.

2.2.2 $0.15\ \mu m$ CMOS at $250^{\circ}C$: unthinkable ?

The present section illustrates the application of the methodology to the design of analog cells at high temperature. Based on measurements of a $0.15\ \mu m$ nominal gate length fully-depleted (FD) silicon-on-insulator (SOI) process in a wide temperature range ($25^{\circ}C - 250^{\circ}C$), we have assessed for the first time the use of deep-submicron CMOS processes

for mixed-mode designs at high temperature. The measured devices are nMOSFETs divided in three types corresponding to three different channel dopings: naturally doped (or undoped), high speed (low threshold voltage (Vth), with channel doping $\approx 1x10^{18}\ cm^{-3}$) and low leakage (high threshold voltage with channel doping of $\approx 2x10^{18}\ cm^{-3}$). Note that even if the process is FD, the low leakage nMOSFETs are partially-depleted (appendix A) due to their high doping level. At room temperature, the corresponding values for the short-channel threshold voltage extracted at V_D of 50 mV are about 0.05 V, 0.42 V and 0.64 V; the gate length is 0.15 μm for the high speed and low leakage and 0.16 μm for the undoped devices. For all device types the silicon film is 30 nm thick and tox is 3 nm. The transistor gate lengths range from 10 μm down to 0.14 μm, while the nominal gate length of the technology is 0.15 μm.

The assessment of the devices for digital applications may be found in Annex A, where the leakage current, on-to-off drain current ratio and Vth shift are considered as well as their evolution with temperature. More detailed explanation on the device physics can be found in [12].

We will here again consider successively high frequency and baseband applications, focusing on the different parts of the $\frac{gm}{I_D}$ vs. $Inorm$ characteristic (Fig. 2.5) and using, on one hand, the drive current and on the other hand, $\frac{gm}{I_D}$ ratio and V_{EA} as figures-of-merit (2.1)(2.2). When considering high temperature operation, the evolution of the $\frac{gm}{I_D}$ ratio with the temperature must also be considered. The $\frac{gm}{I_D}$ vs. $Inorm$ characteristic at different temperatures is presented in Fig. 2.12 for the high speed devices as an example. As temperature increases, the mobility lowers while n and the junction leakage current ($Ileak$) increase. The maximum of the $\frac{gm}{I_D}$ ratio is then decreasing at first order as [4]

$$\left(\frac{gm}{I_D}\right)_{\max} = \frac{1}{n(T) * U_T(T)} \tag{2.6}$$

The $\frac{gm}{I_D}$ plateau moreover moves towards higher $Inorm$ due to the increase of $Ileak$ and hence shrinks the range of $Inorm$ available for the design. At still higher $Inorm$, the $\frac{gm}{I_D}$ curve is shifting to the left as result of both the lowering of the mobility and the increase of n with temperature.

A) For **high frequency applications**, we then compare the drive current for the reference bias point corresponding to $\frac{gm}{I_D} = 10\ V^{-1}$ as this value can be reached for all devices in the temperature range of interest (Fig. 2.13). The drive current for a fixed $\frac{gm}{I_D}$ ratio decreases with temperature as a result of the shift to the left of the $\frac{gm}{I_D}$ vs. $Inorm$ characteristic. This shift is as already said due to the decrease of mobility and to the increase of n with temperature. The undoped devices outperform the other device types with a higher drive current for the same $\frac{gm}{I_D}$ ratio. The first-order drive current temperature dependence is 0.011, 0.008 and 0.019 $\mu A/^{\circ}C$ for, respectively, the high speed, low leakage and undoped device types.

The higher drive current of the high speed devices compared to the low leakage is due to their higher mobility because of their lower doping level and smaller n factor as they are FD and the low leakage are PD. A higher drive current is indeed related to a $\frac{gm}{I_D}$ characteristic shifted to the right, i.e. a same $\frac{gm}{I_D}$ corresponds to higher $Inorm$ (section 2.1) and for inversion regions corresponding to $\frac{gm}{I_D} = 10\ [V^{-1}]$, the characteristic is dominated by the influence of the mobility and the n factor. The first-order drive current temperature dependence of the undoped devices differs from the low leakage and high

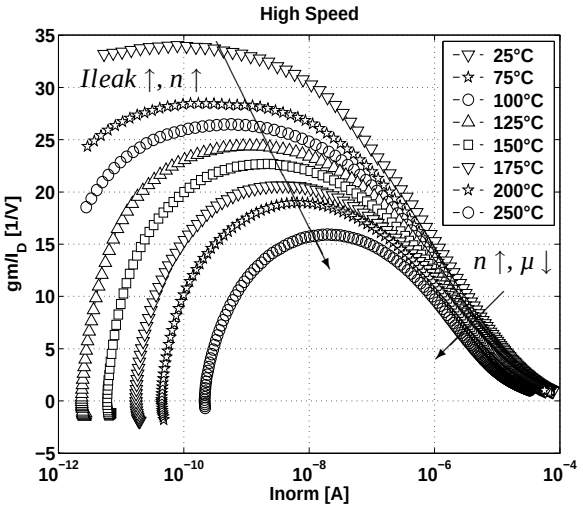


Figure 2.12: Measured $\frac{gm}{I_D}$ $[V^{-1}]$ vs. $Inorm$ $[A]$ characteristic for a n-type high speed (low Vth) MOSFET as a function of the temperature from room temperature up to $250°C$. $W = 10$ μm, $L = L_{nom} = 0.15$ μm, $V_D = 1\,V$ and $V_S = 0\,V$.

speed devices. We suspect that it is due to edge effects [17]. It is however more related to this particular technology as undoped devices should be less sensitive to edge effects due to their low doping level [17] and could be solved in further layout masks definition [22]. An additional hint for edge effects in the undoped devices is their low $\frac{gm}{I_D}$ value in weak inversion (Fig. 2.14).

Using high speed devices, the analog designer can then reach the same *GBW* with less power or a higher *GBW* consuming the same power as these devices present a higher *Inorm* for the same $\frac{gm}{I_D}$.

B) Concerning **baseband applications**, the maximum of $\frac{gm}{I_D}$ is here irrelevant. If we bias the devices with a normalized current corresponding to the $\left(\frac{gm}{I_D}\right)_{\max}$ at room temperature, we will indeed end up with an impossible bias point at high temperature due to Vth and n evolutions with temperature. The zero-temperature coefficient point (ZTC) is a particular bias voltage at which the transistor I_D does not change with temperature [23]. Whereas this point can be observed in conventional bulk technologies only up to $200°C$ [23], the observation of the ZTC point in SOI technologies has been reported up to $300°C$ [6]. In our particular case, we observe a ZTC point when measuring this deep-submicron 0.15 μm FD technology up to $250°C$, the highest temperature in our measurement set-up. Choosing this bias point generally leads to non-optimal, although secure, designs. The figures-of-merit for this bias point can be found in [24]. A better design strategy is to determine first the maximum temperature of operation ($T_{max} = 250°C$, in our case) and extract, at this temperature, the maximum $\frac{gm}{I_D}$ and the corresponding normalized current ($Inorm_{Tmax}$). This last value of $\frac{gm}{I_D}$ leads to the maximum achievable gain in the whole temperature range of interest. The gain at the other temperatures is found by extracting the different $\frac{gm}{I_D}$ and V_{EA} corresponding to $Inorm_{Tmax}$ (Fig. 2.14). In our particular case,

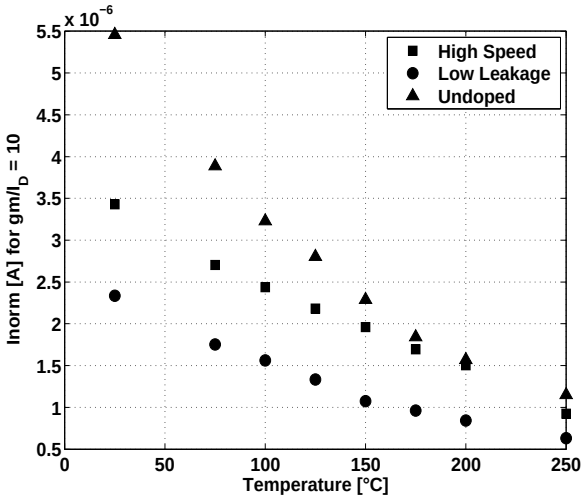
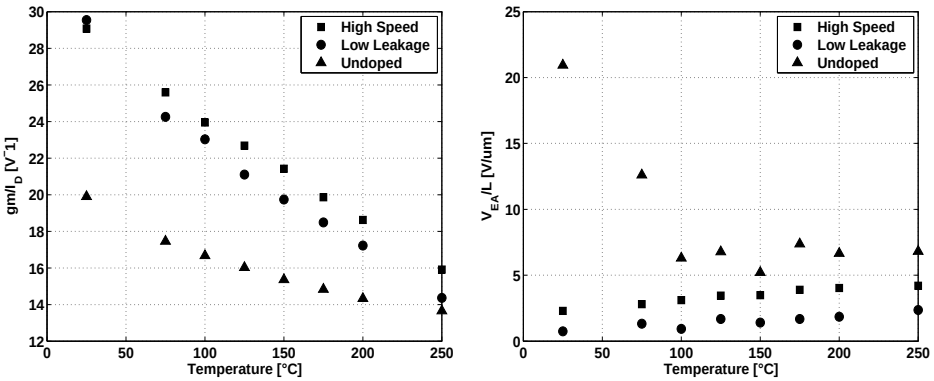


Figure 2.13: Measured $Inorm\ [A]$ corresponding to a $\frac{gm}{I_D} = 10\ [V^{-1}]$ vs. temperature for n-type high speed (■), low leakage (●) and undoped (▲) MOSFETs. $W = 10\ \mu m$ and $L = L_{nom} = 0.15\ \mu m$ for high speed and low leakage devices. $W = 5\ \mu m$ and $L = 0.16\ \mu m$ for undoped MOSFETs. $V_D = 1\ V$ and $V_S = 0\ V$ for all.

due to different channel lengths for the different devices, we use $\frac{V_{EA}}{L}$ to better compare the devices.



(A) **(B)**

Figure 2.14: Measured $\frac{gm}{I_D}$ (A) and $\frac{V_{EA}}{L}$ (B) vs. temperature for n-type high speed (■), low leakage (●) and undoped (▲) MOSFETs. $\frac{gm}{I_D}$ and V_{EA} are extracted for a normalized drain current $Inorm$ corresponding to the $\frac{gm}{I_D}, max$ at $250°C$. $W = 10\ \mu m$ and $L = L_{nom} = 0.15\ \mu m$ for high speed and low leakage devices. $W = 5\ \mu m$ and $L = 0.16\ \mu m$ for undoped MOSFETs. $V_D = 1\ V$ and $V_S = 0\ V$ for all.

For a same *Inorm*, the high speed devices reach a higher $\frac{gm}{I_D}$ than the low leakage. Their $\frac{gm}{I_D}$ vs. *Inorm* characteristic at a given temperature is thus on top and on the right of the characteristic corresponding to the low leakage devices. In the zone of inversion under consideration, it means that the higher $\frac{gm}{I_D}$ is due to smaller *n* factor and higher mobility as they are FD and less doped (section 2.1). The low performance of the undoped devices

is as already said suspected to be caused by edge effects.

As V_{EA} increases for higher doping levels, we would expect a higher V_{EA} for the low leakage devices contrarily to the extracted data (Fig. 2.14). It is probably due to the kink effect which has a negative influence on V_{EA} and is more pronounced for highly doped transistors [17]. The slight increase of V_{EA}/L with temperature for high speed and low leakage devices (Fig. 2.14) can additionally be explained by the reduction of both the kink and short-channel effects as temperature increase. A kink can indeed be observed in the device measurements [24] and could influence the device performance for V_D at which the extraction is performed. $V_D = 1\,V$ was chosen for the extraction of V_{EA} in order to be coherent with the extraction of $\frac{gm}{I_D}$. The better performance of undoped devices is then partially explained by the absence of kink effect in these devices. The gain is then obtained by applying (2.1) (Fig. 2.15).

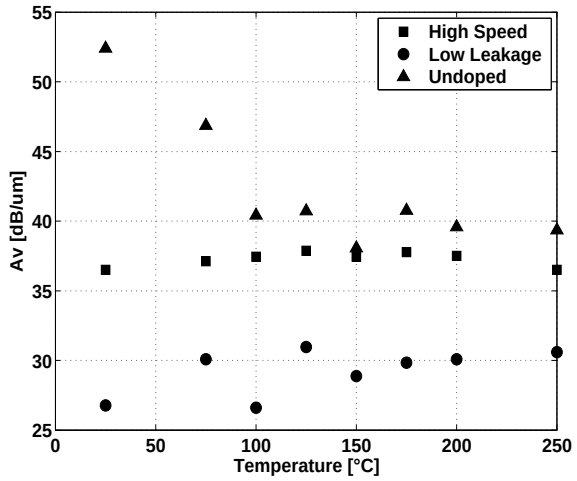


Figure 2.15: Measured $Av/L\ [dB/\mu m]$ **vs. temperature for n-type high speed (■), low leakage (•) and undoped (▲) MOSFETs.** Av/L **is extracted for a normalized drain current** $Inorm$ **corresponding to the** $\frac{gm}{I_D}, max$ **at** $250°C$**.** $W = 10\ \mu m$ **and** $L = L_{nom} = 0.15\ \mu m$ **for high speed and low leakage devices.** $W = 5\ \mu m$ **and** $L = 0.16\ \mu m$ **for undoped MOSFETs.** $V_D = 1\,V$ **and** $V_S = 0\,V$ **for all.**

The undoped devices clearly show outstanding performance as the gain stays rather stable over temperature for all devices with values above 35 $[dB/\mu m]$ in the whole temperature range. Using this type of transistors, the analog designer can improve the gain for the same power consumption or, alternatively, keep the same gain performance and reduce the power consumption.

C) In **conclusion**, our measurement-based methodology was here again successfully applied to assess very quickly the device performance in a wide temperature range, here, using design parameters in practical design situations. The designer can then better estimate the behavior of the circuit at high temperature and, moreover, he is able to select the best device for the targeted application.

The analog designer who have access to **well-processed and optimized deep-submicron SOI MOSFETS**

(1) **can surprisingly use SOI transistors for analog operation up to** $250°C$ as the decrease of the drive current is quite limited (Fig. 2.13) and the gain stays rather stable with high performance values (Fig. 2.15).

(2) **better use undoped devices** for they are very promising for analog applications as (i) exhibit higher $Inorm$ for a same $\frac{gm}{I_D}$ (Fig. 2.13) and (ii) higher intrinsic gain (Fig. 2.15).

(3) **can** moreover **safely build mixed-signal applications up to** $250°C$ on the same process with high Vth devices as they are suitable for digital operation up to $250°C$ (Annex A).

2.3 Conclusion

In this chapter, we started the definition of the elements of the analog ID card by focusing on two main analog parameters: the gain (Av) and the gain-bandwidth product (GBW). The goal of the analog ID card is to characterize the transistor for analog applications (chapter 1). We want design-oriented figures-of-merit so they can be used in an efficient design flow of analog applications on which we will come back in chapter 7. We defined the transconductance over drain current ratio ($\frac{gm}{I_D}$) and the Early voltage (V_{EA}) as figures-of-merit and first elements of the device analog ID card for Av and GBW for they are the basis of a well-known and efficient design methodology.

As an example, technologies with nominal gate lengths of $0.12\ \mu m$ and $0.15\ \mu m$ have been assessed and in each case, different devices were compared in various bias conditions corresponding to practical design situations, including the moderate inversion regime. We compared different technologies (fully-depleted SOI vs. partially-depleted SOI vs. bulk) as well as devices from the same technology but with different doping levels and hence Vth. The methodology was also shown to be useful to evaluate the device performance at high temperature. $\frac{gm}{I_D}$ and V_{EA} are then analog figures-of-merit adapted to characterize deep-submicron technologies, capable of comparing devices in different bias conditions and operating temperature. Moreover, they have been shown to be designer-oriented as they offer a quick insight in the device specification-power trade-offs continuously across the different regions of inversion corresponding to different types of application. These figures-of-merit are thus adapted to provide information on the device performance to the analog cell designer (Fig. 1.4).

The application of the methodology also revealed important and non-obvious conclusions. The benefits of SOI technology for low-power operation are confirmed for very short channel transistors. The negative influence of HALO doping (or pocket implants) has been experimentally confirmed for the first time on different technologies for long-channel transistors targeting high-gain and for devices targeting high-frequency operation and biased in strong inversion. However, HALO proved favorable for short-channel transistors biased in weak or moderate inversion. Additionally, deep-submicron SOI MOSFETs have surprisingly and for the first time been shown to be suitable for mixed-signal operation up to $250°C$.

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Chapter 3

Harmonic distortion in triode regime

The aim of our analog ID card is to accurately characterize analog circuits for top-down design and bottom-up validation methodologies. In the previous chapter, the figures-of-merit for the gain and gain-bandwidth product of amplifiers were identified. The MOSFET-C continuous-time filters are still very advantageous for specific functions in state-of-the-art mixed-signal systems. A key parameter is the distortion they introduce; and it is mainly caused by a transistor in the triode regime emulating a resistance. SPICE models generally fail to simulate adequately the harmonic distortion of order greater than two, which is of interest here. The MM11 model [1] is capable of that but, up to now, it is not widely delivered by the semiconductor foundries and obtaining the full set of parameters is costly. Moreover, this model does not describe silicon-on-insulator devices, which are under consideration here. Predicting the distortion performance of the MOSFET-C filters based on measured characteristics is thus the only way.

Although the MM11 model [1] is the only model to our best knowledge to adequately describe the distortion of a MOSFET biased in triode, its description of the drain current (I_D) is too complex for hand calculations. We use the much simpler expression of I_D in triode regime using the classical source-referred model to get a qualitative insight in the device behavior:

$$I_D = C_{ox}\frac{\mu_0}{1+\theta\,(V_{GS}-Vth)}\frac{W}{L}\left[(V_{GS}-Vth)V_{DS}-\frac{1}{2}V_{DS}^2\right] \tag{3.1}$$

where C_{ox} is the front gate oxide capacitance, μ_0 is the zero-field mobility, θ accounts for the mobility reduction with the vertical field, Vth is the threshold voltage and V_{GS}, V_{DS} are the gate-to-source and drain-to-source voltages, respectively. The third-order harmonic distortion is the quantity of interest as will be justified below and is determined to first order [2] by the mutual influence of the effects related to θ and the body effect factor γ, through Vth.

In this chapter, we review the two possible implementations of the resistance using MOSFETs in triode regime. For these two implementations, we question the validity of the analysis of the underlying physical phenomena carried in [2], in the case of deep-

submicron CMOS technologies and we moreover extend it to operation at high temperature (up to 225°C) (sections 3.3 and 3.4). Knowing which physical phenomenon is dominant for a particular case is important to the MOSFET-C filter design as it allows to choose the bias and the device type more optimally. We also develop an original design-oriented characterization methodology to predict the MOSFET-C filter third-order harmonic distortion (section 3.5). The methodology can moreover be used to efficiently elect the best implementation, device type and bias under practical design constraints.

3.1 Context

The decrease of the oxide thickness (t_{ox}) and increase of the channel doping level (N_A) in modern advanced deep-submicron technologies, driven by the tremendous evolution and potential of digital processing, have a deep impact on MOSFET analog current-voltage ($I-V$) characteristics [3]. However, purely analog circuits are still unavoidable, just for example as anti-alias continuous-time filter prior to any analog-to-digital conversion, or very advantageous as intermediate frequency (IF) band filter in transceivers. For frequency bands up to 1 MHz and especially if high dynamic range and low-power operation are of concern, the MOSFET-C approach is one of the best candidates [4]. In such active RC filters, tunable resistors are implemented by MOSFETs in triode regime [5], the drain and source being the resistor terminals while the gate voltage (V_G) controls the resistance (Fig. 3.1 A). The tuning of the resistance through V_G is implemented on-chip to automatically compensate for process parameters and temperature variations. Those continuous-time filters however often appear as the bottleneck of state-of-the-art front-end or signal acquisition chains as the MOSFET non-linear $I-V$ behaviors and hence their harmonic distortion (HD) deteriorate the whole system performance. For MOSFET-C filters applications, fully-differential structures are generally preferred for increased robustness. We will then consider the third-order harmonic distortion (HD3) as the figure-of-merit, as it dominates the HD behavior in this case [6].

Accordingly, the present study is focused on the HD3 of MOSFETs operating in the triode regime which in modern advanced deep-submicron CMOS processes, drives new questions and design concerns:

- the scaling of t_{ox} and additionally the trend to low-power/low-voltage (LPLV) operation impose a reduction of V_G possibly worsening the device HD.
- taking into account the resistor value (Ron) direct proportionality on t_{ox} and length, the scaling imposes the use of particularly long transistors in order to reach a Ron which matches the frequency bandwidth with typical capacitor value (e.g. pF).
- the circuit designer can moreover choose between different devices with various threshold voltages (Vth) and hence $I-V$ characteristics.

This motivates an extensive discussion of the MOSFET HD3 characteristics vs. t_{ox}, N_A and V_{th}, which to our best knowledge, didn't take place in the literature yet in triode regime for deeply scaled CMOS technologies.

Finally, an alternative structure using four MOSFETs (4-MOS, Fig. 3.1 B) has been proposed to overcome the imperfections of the structure using two MOSFETs (2-MOS, Fig. 3.1 A) and hence possibly improving HD3 [7][8]. In the 4-MOS, one of the gate

biases is kept constant at a high level ($V_{G,fixed}$ in Fig. 3.1 B) while the other (V_G) ensures the tunability. In addition to the tuning V_G range and to the device type in multi-Vth processes, the designer must also choose the best structure (2-MOS vs. 4-MOS), for a given application. We will come back on the pros and cons of the two structures later in the text. However, available SPICE models generally fail to accurately predict HD of orders greater than two. We thus present a measurement-based and design-oriented comparison methodology allowing the designer to efficiently elect the best structure, device type and gate bias for his target application.

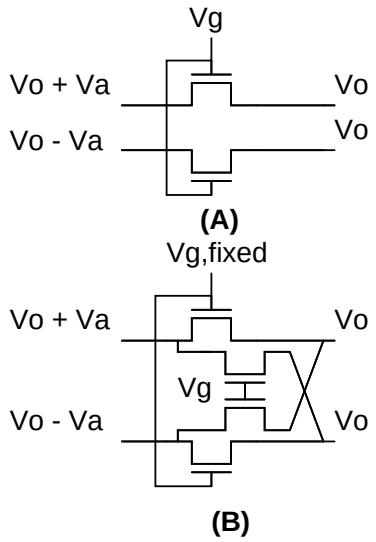

Figure 3.1: Resistive structures used in MOSFET-C filters to emulate tunable resistances: 2-MOS structure (A) [5] and 4-MOS *Czarnul-Song* structure (B) [7][8]

In this section, we base our analysis on measurements performed in a silicon-on-insulator (SOI) 0.12 μm CMOS technology with multi-Vth devices, allowing us to discuss the HD characteristics of long MOSFETs in triode operation vs. t_{ox} and N_A, all other process parameters being identical. We perform this analysis in a wide temperature range, from room temperature up to 220$^{\circ}C$, revealing the evolution of HD3 in triode regime vs. temperature. In section 3.2, we describe the measured devices and measurement procedure. Section 3.3 and section 3.4 present the HD3 characteristics of the 2-MOS and 4-MOS resistive structures, respectively. Section 3.5 is dedicated to the developed design methodology.

3.2 Devices description and HD measurement procedure

We measured four different device types from a 0.12 μm SOI CMOS process from room temperature up to 220$^{\circ}C$:

Acronym	Gate oxide thickness $[nm]$	Relative doping level *for devices with same oxide thickness*	Vth at $25°C$ [V]
GOX	≈ 5 *(thick)*	-	0.3995
gox-LoVth	≈ 2 *(thin)*	Low	0.2238
gox-HiVth	≈ 2 *(thin)*	High	0.3193
gox-NeVth	≈ 2 *(thin)*	natural	-0.04

We will come back below on the Vth extraction procedure and evolution with temperature. The GOX and gox-NeVth target analog applications, the others usually digital gates. The availability of two t_{ox} on the same process permit us to directly investigate the effect of the scaling. In order to implement resistor values (Ron) around 100 $k\Omega$ or higher, typical for baseband continuous-time filters, long transistors are needed as Ron is proportional to L/W. The measured device lengths are then 10 μm for all but gox-NeVth for which $L = 20$ μm. All transistors are partially-depleted (PD) at room temperature, except the gox-NeVth with natural doping, which depletion region extends over the entire film thickness in strong inversion making it fully-depleted (FD) in this region of inversion [9]. To avoid floating body transient effects, we measured all PD devices with a body contact, connecting the floating body to the source of the transistor. Long-channel Vth for the different devices in the temperature range of interest is presented in Tab. 3.1. For gox-LoVth, gox-HiVth and GOX devices, V_{th} was extracted using the EKV method ([10] , appendix D), while for the gox-NeVth devices, we used the maximum of the second derivative of the drain current (I_D) vs. gate voltage (V_G) characteristic as in this last case, the measured devices do not have any body contact.

Table 3.1: Threshold voltage (Vth) for the different device types in the temperature range of interest. $W = L = 10$ μm for gox-LoVth, gox-HiVth and GOX and $W = L = 20$ μm for gox-NeVth.

$Vth[V]$	$25°C$	$100°C$	$150°C$	$200°C$	$220°C$
GOX	0.3995	0.3322	0.2860	0.2330	0.2197
gox-LoVth	0.2238	0.1744	0.1383	0.1089	0.0963
gox-HiVth	0.3193	0.2842	0.2427	0.2088	0.1932
gox-NeVth	-0.04	-0.11	-0.16	-0.21	-0.225

To extract the HD3 in a fast way for different configurations and at different temperatures, we use the Integral Function Method (IFM) ([11], appendix D) directly starting from device DC characteristics. The validity of the IFM in the frequency range of interest here has been demonstrated [12]. We start from an I_D vs. drain voltage (V_D) characteristic, with V_D ranging from -0.5 V to 0.5 V in 5 mV steps and for gate voltages ranging up to maximal gate voltage in 50 mV steps. HD levels are extracted for a given signal amplitude around a DC bias point, respectively Va and Vo in Fig. 3.1. To evaluate the worst-case HD3 we use $Va = 200$ mV around $Vo = 0$ V, yielding a 400 mV signal amplitude in a fully-differential architecture, which appears as a maximum for operation under a low supply voltage of about 1.5 V.

3.3 HD3 for the 2-MOS resistive structures

HD3 has been extracted for different gate biases using the methodology described in the previous section for the four device types in a wide temperature range from room temperature up to $220^{\circ}C$ (Fig. 3.2). The gate biases are chosen so that to keep the device in the triode part of the I_D-V_D characteristic. Comparing the results of Fig. 3.2 three device groups can easily be identified: 1) gox-LoVth and gox-HiVth 2) gox-NeVth and 3) GOX.

The HD3 for a 2-MOS resistive structure composed of body grounded bulk or PD transistors (gox-HiVth, gox-LoVth and GOX devices) can to first order be described as a function of the mobility reduction coefficient (θ), of the body effect coefficient (γ) and the surface potential in strong inversion (ϕ_b) as given by [2]

$$HD3 \propto \frac{-1}{V_{GS}-Vth}\left(\frac{\theta}{2}-\frac{\gamma}{12\phi_b^{3/2}}\right) \tag{3.2}$$

HD3 is thus determined by the mutual influence of θ and γ related effects. A typical characteristic (Fig. 3.2) exhibit a ν-like shape with a local minimum, at which θ and γ compensate each other. At low gate voltage, HD3 is dominated by body related effects. Moving to higher V_G, the influence of the body and mobility related effects respectively decreases and increases, yielding the local minimum and after this, a region where HD3 is dominated by θ. In section 3.5, the exploitation of the local minimum in practical designs will be investigated.

The HD3 characteristics are thoroughly examined later in this chapter. We extract the linearized body effect factor (n) and the mobility reduction coefficient (θ) beforehand in order to link the differences in the HD3 vs. $V_G - Vth$ characteristics with the underlying physical parameters (3.2).

3.3.1 Body effect

The linearized body effect factor (n) obtained from the measurements is used as an image of the $\frac{\gamma}{12\phi_b^{3/2}}$ term in (3.2) as they reflect the same physical phenomena. The body effect coefficient is indeed given by [13]

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}} \tag{3.3}$$

where ε_{Si} is the permittivity of the silicon and q is the magnitude of the electronic charge. On another hand, the n factor is defined by [14]

$$n = 1 + \frac{C_{\text{CH-GND}}}{C_{ox}} \tag{3.4}$$

where $C_{\text{CH-GND}}$ is the capacitance formed by the depletion region between the channel and ground and C_{ox} is the gate capacitance. In strong inversion [14]

$$n = 1 + \frac{\varepsilon_{Si}\sqrt{\frac{qN_A}{2\varepsilon_{Si}}}}{C_{ox}}\frac{1}{\sqrt{\phi_b(V_G)}} \tag{3.5}$$

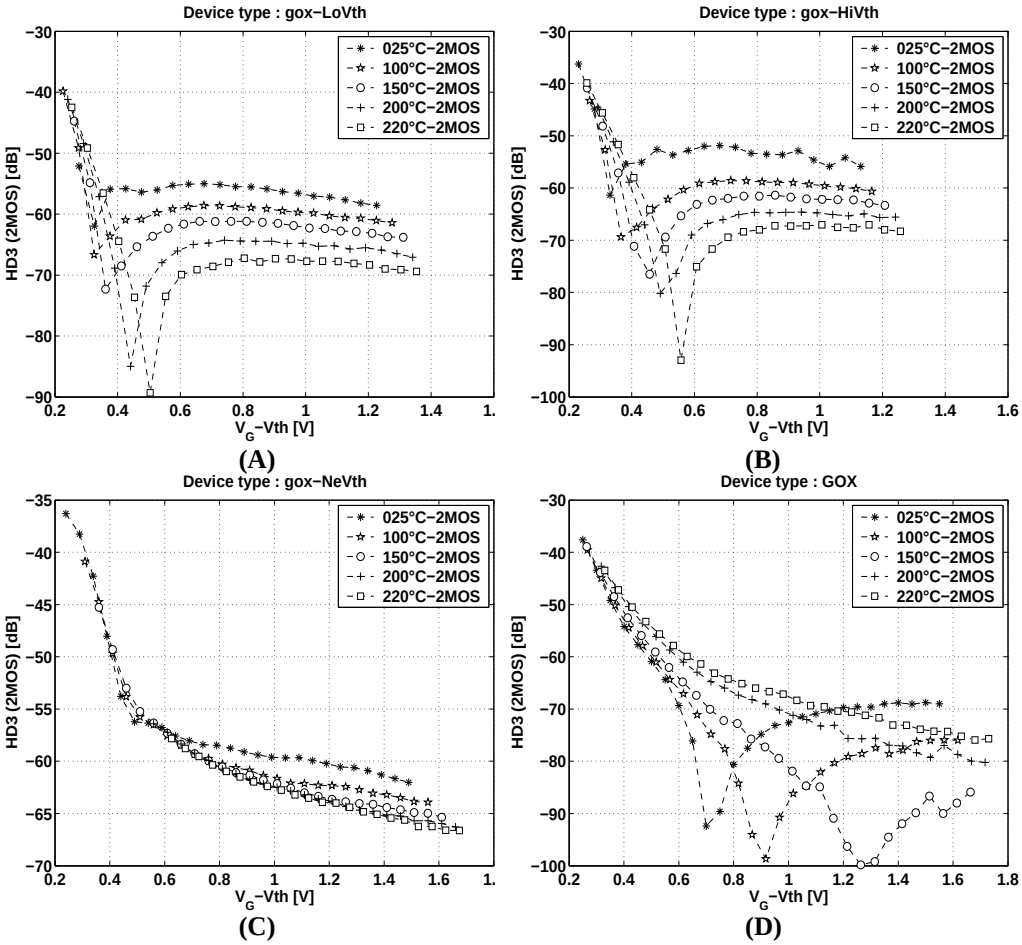

Figure 3.2: HD3 [dB] vs. $V_G - Vth$ for 2-MOS structures composed of the following devices: gox-LoVth (thin-gate oxide, low Vth)(A), gox-HiVth (thin-gate oxide, high Vth)(B), gox-NeVth (thin-gate oxide, natural doping)(C) and GOX (thick-gate oxide) (D). Cases A, B and D correspond to partially-depleted devices with body connected to the source and are $10\ \mu m$ long and $10\ \mu m$ large. gox-NeVth (case C) is fully-depleted and has $W = L = 20\ \mu m$. $Va = 200\ mV$ around $Vo = 0\ V$.

Using EKV formulation [15]

$$n = \left(\frac{\partial V_P}{\partial V_G}\right)^{-1} \tag{3.6}$$

where V_P is the pinch-off voltage, i.e. the voltage at which the inversion charge is zero when only strong inversion is considered. n was extracted using the EKV method ([10], appendix D) for gox-LoVth, gox-HiVth and GOX devices (Fig. 3.3, for gox-LoVth as an example), revealing that, for all devices, n decreases for increasing V_G and increases with increasing temperature as expected from the evolution of the depletion layer (3.4). Moreover, $n_{GOX} > n_{GO1\ LL} > n_{GO1\ HS}$ in accordance with the device relative t_{ox} and N_A (3.5).

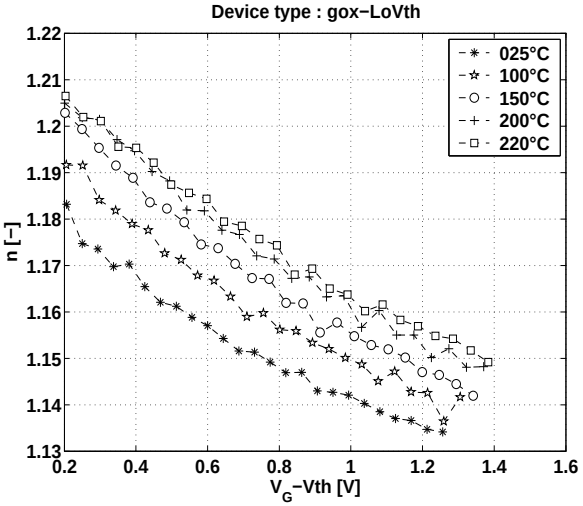

Figure 3.3: Linearized body effect factor (n) in strong inversion [-] vs. $V_G - Vth$ for gox-LoVth device at different temperatures. $W = 10\ \mu m$ and $L = 10\ \mu m$.

To compare the HD3 evolution with temperature for the four device types, we also represent n at a fixed bias $V_G - Vth$ of $0.7\ V$ at the different temperatures (Fig. 3.4) showing a steeper increase of n with temperature for thicker oxide (GOX vs. gox-HiVth and gox-LoVth) and for more heavily doped devices (gox-HiVth vs. gox-LoVth).

For V_G around Vth, the gox-NeVth MOSFETs exhibit a transition from partially to fully-depleted mode of operation. It renders the extraction of the n factor impossible using the EKV method. The slope of Vth vs. the back-gate voltage ($Vback$) is then the only way to extract n. Vth is extracted using the $\frac{I_D}{\sqrt{gm}}$ method, where gm is the gate transconductance, $V_D = 50\ mV$ and $Vback$ swept from $0\ V$ to $30\ V$ in $1\ V$ steps, ensuring the back interface is not inverted. We are here only interested on the variation of Vth vs. $Vback$ and not on the absolute values of Vth. The obtained n factor value are 1.00405 and 1.0052 at 25 and 100$^\circ C$, respectively. These values are very close to one as expected from the fully-depleted operation of these devices and slightly increase with temperature.

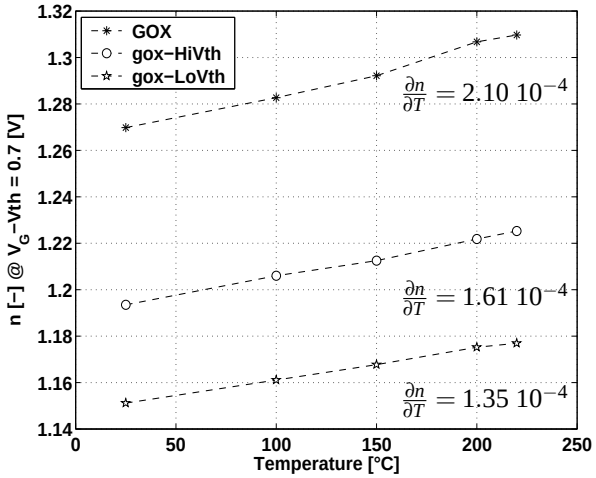

Figure 3.4: n **body effect factor [-] for** $V_G - Vth = 0.7\ V$ **vs. temperature for gox-LoVth, gox-HiVth and GOX devices. The slope of** n **vs. temperature (**$[-/^\circ C]$**) is given next to the curves.** $W = 10\ \mu m$ **and** $L = 10\ \mu m$ **for all devices.**

3.3.2 Mobility reduction

The correct extraction of the mobility reduction factor (θ) would require an array of long channel transistors as for short devices the channel behavior is masked by the HALO doping [16]. Such devices were not available on the wafers. In order to obtain a qualitative estimation of the mobility and mobility reduction with V_G, we extract the gate transconductance (gm) for all devices at the different temperatures and, to get rid of the influence of t_{ox}, we consider gm/C_{ox}. We use the maximum value of gm/C_{ox} as an indicator of the mobility (Tab. 3.2). The maximum of gm is indeed proportional to the mobility and a qualitative information is sufficient as we are interested in the comparison of different devices.

Table 3.2: $\frac{gm_{max}}{C_{ox}} at V_D = 50\ mV$ **for the different devices in the temperature range of interest.** $W = 10\ \mu m$ **and** $L = 10\ \mu m$ **for all.**

$\frac{gm_{max}}{C_{ox}}[\mu A.m^2/V/F]$	$25^\circ C$	$100^\circ C$	$150^\circ C$	$200^\circ C$	$220^\circ C$
GOX	1561.2	1059.2	841.84	686.46	637.62
$GO1HS$	1122	749.72	590.47	484.97	443.33
$GO1LL$	1032.5	705.99	558.35	458.53	420.49

On the other hand, we focus on the decrease of gm with V_G for $V_G > V_{G,gm_{max}}$ where $V_{G,gm_{max}}$ is the gate voltage corresponding to the maximum of gm/C_{ox}. The magnitude of this decrease indeed reflects the mobility reduction effects, possibly including the effect of series resistances. Here again, a qualitative information is sufficient for the comparison between different devices. The series resistance are moreover expected to have low impact for long-channel devices and were estimated to tens of Ohms, which are in any case negligible when compared to Ron. The gm/C_{ox} slope is represented as a function of

temperature for GOX, gox-HiVth and gox-LoVth devices in Fig. 3.5. From Fig. 3.5, the mobility reduction parameter decreases as temperature increases and is smaller for thicker oxide devices (GOX vs. gox-LoVth and gox-HiVth) and for higher N_A (gox-HiVth vs. gox-LoVth).

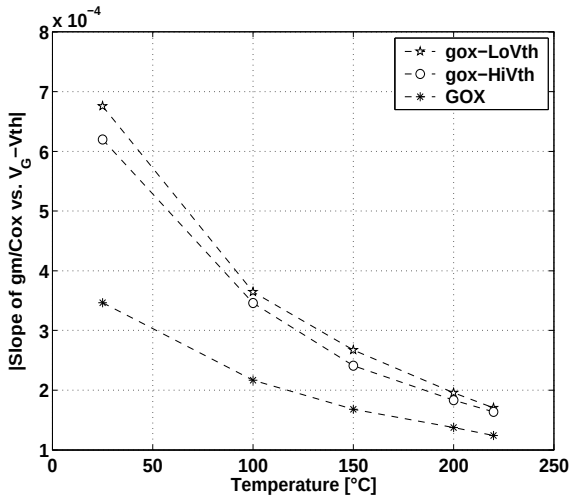

Figure 3.5: Magnitude of the decreasing slope of the gm/C_{ox} vs. $V_G - Vth$ characteristic beyond its peak, in function of the temperature for gox-LoVth, gox-HiVth and GOX devices. $W = 10\ \mu m$ and $L = 10\ \mu m$ for all devices.

These two last figures of merit are in the present case irrelevant for gox-NeVth devices because their *gm* vs. $V_G - Vth$ characteristics are mainly dominated by the transition from partially to fully-depleted mode of operation around Vth, showing up as an amplification of *gm* in the region where it is maximum (Fig. 3.6) [17].

3.3.3 Mutual interaction of body and mobility related effects in 2-MOS HD3

The mutual interaction of body and mobility related effects determine the HD3 in 2-MOS structures. Using the extracted parameters, we now examine in more detail the three device groups concerning HD3 performance (Fig. 3.2) as identified here above.

- **gox-LoVth and gox-HiVth** MOSFETs reach about the the same HD3 values. We can identify three regions in the HD3 characteristics of both devices:

  1) before the local minimum, the increase of HD3 with temperature as well as the slightly higher HD3 values in gox-HiVth can be linked to the corresponding increase of *n* observed in Fig. 3.3 and Fig. 3.4.

  2) following the compensation peak, gox-LoVth and gox-HiVth devices feature very close HD3 which decreases strongly with temperature and slightly with $V_G - Vth$ but ever weaker as temperature increases. These behaviors strongly relate to the evaluations of mobility reduction effect presented in Fig. 3.5.

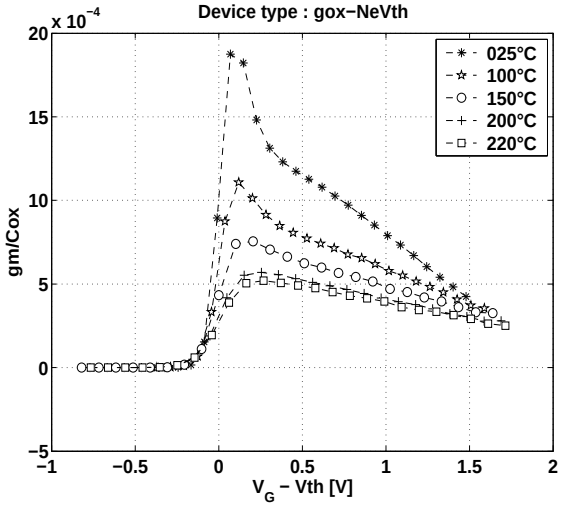

Figure 3.6: gm **[A/V] vs.** $V_G - Vth$ **for gox-NeVth (thin-gate oxide, natural doping) device,** $L = 20\ \mu m$**,** $W = 20\ \mu m$ **and** $Vd = 50\ mV$**.**

3) As temperature increases, the position of the compensation peak moves to higher V_G for both devices as n and θ are indeed respectively increasing and decreasing with temperature (Fig. 3.4 and Fig. 3.5). The peak of the gox-HiVth devices is always on the right side of the gox-LoVth peak (Fig. 3.7), as the n factor of the more heavily doped gox-HiVth devices is higher than for gox-LoVth (Fig. 3.4). θ also evolves with N_A. Fig. 3.5 indeed shows a smaller slope of gm/C_{ox} vs. $V_G - Vth$ for gox-HiVth devices. The difference in the peak position additionally increases with temperature (Fig. 3.7) as a result of the higher $\frac{\partial n}{\partial T}$ of gox-HiVth (Fig. 3.4) while the dependence of the slope of gm/C_{ox} vs. $V_G - Vth$ with temperature is about the same for gox-LoVth and gox-HiVth.

- **GOX** MOSFETs exhibit a behavior, which strongly differs from the three other device types probably due to their thick gate oxide. At relatively low temperatures (below $150°C$), we observe a compensation peak and the three regions we mentioned when describing the gox-LoVth and gox-HiVth. As temperature increases, the peak is strongly shifting to the right and then disappearing. Due to the thicker oxide, $\frac{\partial n}{\partial T}$ is indeed much bigger here than for gox devices (Fig. 3.4) occasioning the stronger peak shift. Additionally, the compensation peak occurs at higher $Vg - Vth$ here since n is larger (Fig. 3.4) again due to thicker t_{ox}. Between room temperature and $150°C$, as it was the case in gox-LoVth and gox-HiVth, we observe the θ influence to be dominant on the right side of the peak, as HD3 is improving with temperature. This trend however disappears as the temperature further increases and we no longer observe any peak, the HD3 worsens with temperature above $150°C$ and we no longer observe any peak. As with temperature, n increases (Fig. 3.3) and the slope of gm/C_{ox} vs. $V_G - Vth$ decreases (Fig. 3.5), the compensation peak is then further moved to higher V_G, out of the range of interest. The n related distortion to become dominant as HD3 now increases with temperature and decreases with V_G. It should be noted here that the absence of

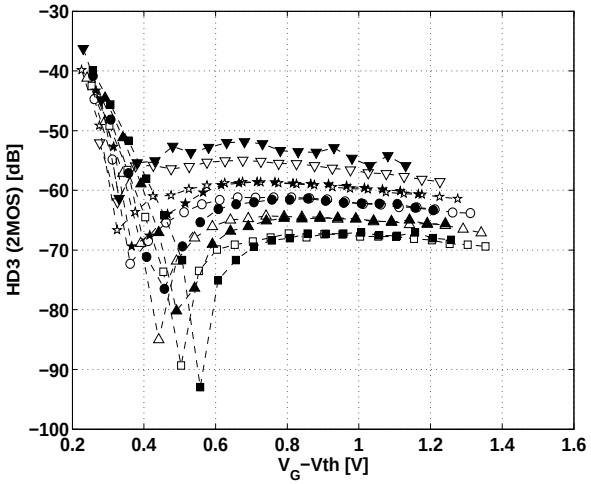

Figure 3.7: HD3[dB] vs. $V_G - Vth$ **for 2-MOS resistive structures with gox-LoVth (thin-gate oxide, low** Vth**) (void symbols) and gox-HiVth (thin-gate oxide, high** Vth**) (full symbols),** $W = L = 10\ \mu m$ **at different temperatures:** $25°C$ **(▽) ,** $100°C$ **(⋆),** $150°C$ **(○),** $200°C$ **(△) and** $220°C$ **(□)**

compensation worsens the global distortion performance as stated in [2].

- Although **gox-NeVth** MOSFETs exhibit the most stable behavior over temperature, they feature relatively high HD3 compared to the other device types as they are influenced by the already stated transition from PD to FD (Fig. 3.6). This influence however weakens as temperature increases and for high temperatures their HD3 becomes comparable to other device types. The decrease of HD3 with both temperature and V_G and the absence of compensation peak are not straightforward to explain, since for FD SOI MOSFETs, (3.2) is not applicable and no adequate formula can be easily derived (cf. appendix B) because it must include a lot of second-order effects modeled accurately [1]. At low V_G, the transition from PD to FD dominates and the interaction between the different effects can hardly be identified. At high V_G, the respective decrease and increase of HD3 and n with temperature would indicate that the HD3 of gox-NeVth devices is only determined by θ thanks to the close to one n factor of these devices. These interpretation difficulties further stress the need for improved modeling of the HD3 of such devices.

3.4 HD3 for the 4-MOS resistive structures

HD3 has also been extracted for the 4-MOS structures, for different gate biases and using the same methodology. Measurements were also performed in a wide temperature range ($25°C - 220°C$) for the different device types (Fig. 3.8).

The link with the underlying physical parameters can be hardly drawn as no accurate analytical description of HD3 in the 4-MOS structures was reported to date. Such analytical description is moreover tough to obtain as it must include a lot of accurately modeled second-order effects [1] and the compact models may no be appropriate (cf. appendix B

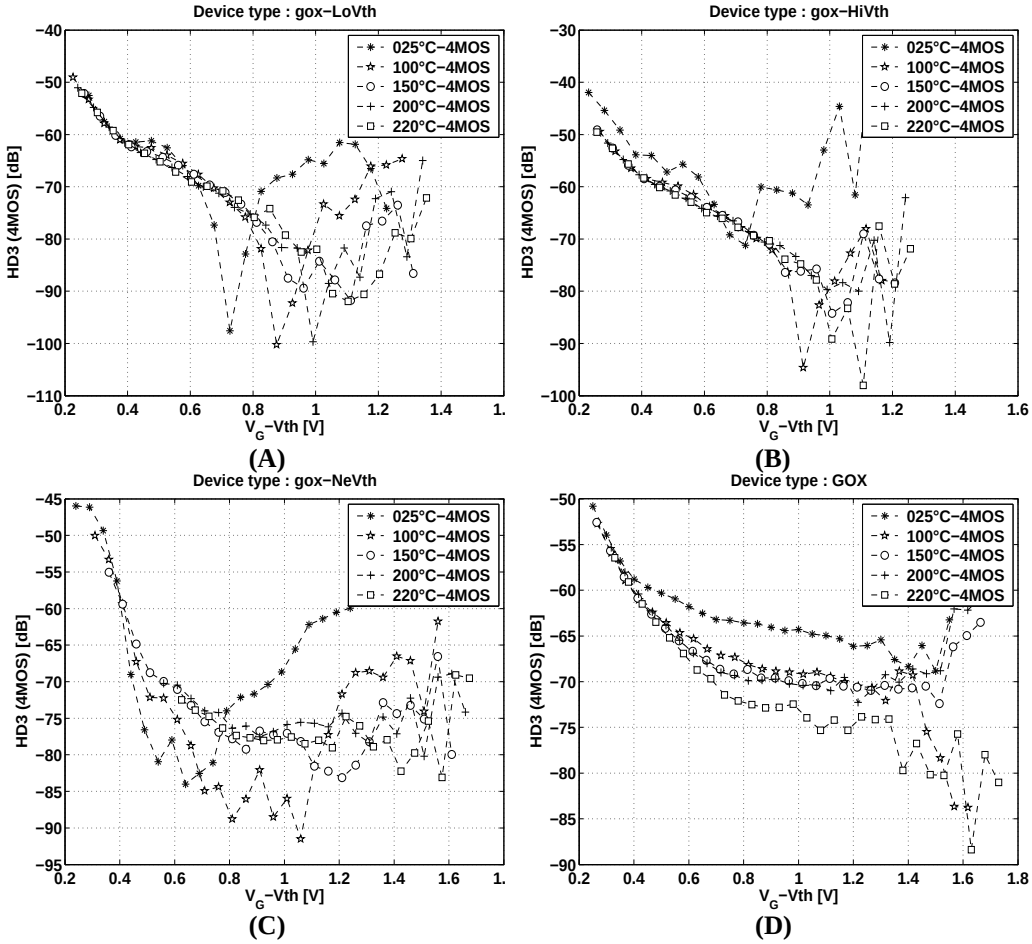

Figure 3.8: HD3 [dB] vs. $V_G - Vth$ for 4-MOS structures composed of the following devices: gox-LoVth (thin-gate oxide, low Vth)(A), gox-HiVth (thin-gate oxide, high Vth)(B), gox-NeVth (thin-gate oxide, natural doping)(C) and GOX (thick-gate oxide) (D). Cases A, B and D correspond to partially-depleted devices with body connected to the source and are $10\ \mu m$ long and $10\ \mu m$ large. gox-NeVth (case C) is fully-depleted and has $W = L = 20\ \mu m$. $Va = 200\ mV$ around $Vo = 0\ V$.

for the case of the EKV model [15]). Compared to the 2-MOS, the 4-MOS structure was reported to be less sensitive to n effects but the variation of the surface potential with V_G [18], and hence the variation of n with V_G plays a role. The θ related effects should play a similar role than in the 2-MOS structures.

The HD3 characteristics corresponding to low V_G seem to be dominated by n related effects as the HD3 values are 10 to 15 dB lower than the corresponding HD3 of the 2-MOS structure (Fig. 3.2); the 4-MOS structure is indeed predicted to be less sensitive to n effects and it is here confirmed. In that region, the HD3 is also more stable with temperature (Fig. 3.8). At low V_G, the gox-NeVth MOSFETs furthermore exhibits the lowest HD3 which could be linked to their lowest n and n variation with V_G as they are FD. Finally, GOX devices, contrarily to the other device types, present a higher HD3 in 4-MOS than in 2-MOS. For the V_G for which the n related effects are suspected to dominate (i.e. low V_G), the HD3 is lower for thin oxides (gox-LoVth, gox-HiVth and gox-NeVth vs. GOX), low doping level (gox-LoVth and gox-NeVth vs. gox-HiVth) and fully-depleted mode of operation (gox-NeVth vs. gox-LoVth and gox-HiVth) as in these cases the surface potential is better controlled.

Even if the extracted data is less clear than in the case of 2-MOS structures, a compensation peak can be observed in most of the device types and temperatures. Here again, the peak is shifted to higher V_G as temperature increases (Fig. 3.8, gox-LoVth for example) and the peak moves to lower V_G for larger θ (gox-LoVth vs. gox-HiVth) possibly as n and θ respectively increases and decreases with temperature. As in the 2-MOS case, some characteristics do not exhibit any compensation peak, e.g. GOX, at low temperatures. At high V_G, the 4-MOS HD3 values (Fig. 3.8) are comparable to the corresponding 2-MOS HD3 (Fig. 3.2), suggesting that θ becomes dominant.

The comparison between different device types is not straightforward looking at Fig. 3.8. We therefore develop a design-oriented comparison methodology presented in the next section.

3.5 Design-oriented HD3 comparison methodology

The designer of MOSFET-C filters has to select the best combination of device sizes (W, L) and bias (V_G) to implement a given value of *Ron*, ensuring the value of *Ron* can be tuned on chip by varying V_G to compensate for temperature and process variations.

Using measurement data extracted using the procedure described in the previous section, we here below compare structures and devices in practical design situation:

- we fix a value for *Ron*.
- we focus on the $25°C - 150°C$ temperature range, which covers most industrial application requirements.
- we fix a tuning range margin of $\pm 10\%$ to compensate for process variations.

Based on these design requirements, our original comparison methodology:

1) selects a target *Ron* value to perform the comparison;

2) computes, at each temperature of interest, the V_G needed to reach the *Ron* value and extracts the HD3 corresponding to this bias, ensuring the resistance can be tuned on-chip in the whole temperature range;

3) finds, at each temperature, the V_G corresponding to corner values of *Ron* determined by the chosen tuning range and extracts HD3 at these V_G, ensuring on-chip tuning can cover process variations.

As $Ron*W$ vs. V_G evolution is drastically different in 2-MOS and in 4-MOS structures (Fig. 3.9, for GOX as an example), we must select different $Ron*W$ for each structure to fairly compare them. In practice, we would reach the same *Ron* value by adjusting W. We implicitly assume that W doesn't influence the HD3 level, which is correct provided that no narrow-channel effects are present.

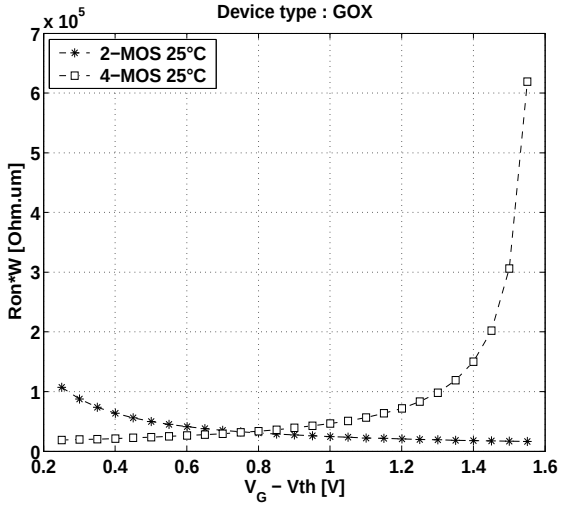

Figure 3.9: Ron*W $[\Omega.\mu m]$ **vs.** $V_G - Vth$ **for 2-MOS and 4-MOS resistive structures with GOX devices at** $25°C$**.** $V_{G,fixed} = 2\ V$ **and** $L = 10\ \mu m$**.**

For the device lengths under consideration, we target values for $Ron*W$ of $4*10^4\ \Omega.\mu m$ and $2*10^5\ \Omega.\mu m$, for 2-MOS and 4-MOS structures respectively, both yielding a *Ron* value of $0.8*10^5\ \Omega$ with $W = 0.5\ \mu m$ and $W = 2.5\ \mu m$, respectively. Such *Ron* is adapted to MOSFET-C filters targeting signal bandwidth of a few *MHz* while keeping the MOSFET dimensions sufficiently small to ensure that the parasitic pole caused by the gate capacitance ($C_g \propto C_{ox}WL$) of 2-MOS structures [19] would not be problematic. The *Ron.W* value is at first chosen identical for all device types and could then be adapted for each device type in order to really get the best of each device type, refining the comparison but is beyond the scope of our analysis.

Table 3.3 shows the results of the application of the methodology to the four device types. $V_{G,fixed}$ of the 4-MOS structure was chosen to benefit from the local minima for each device type: $2V$ for GOX, $1.2V$ for gox-LoVth and gox-HiVth and $1.1V$ for gox-NeVth. The minimum and maximum HD3 referenced in Tab. 3.3 are obtained over the tuning range **and** over temperature.

As expected from Fig. 3.2, the GOX devices outperform all other device types in the 2-MOS configuration. Due to the imposed tuning range, their performance are however less impressive than expected stressing the importance of the design-oriented comparison methodology to adequately compare the devices. Aside from their lower HD3, the tuning

Table 3.3: V_G tuning range and HD3 levels for 2-MOS and 4-MOS structures for the different devices. Target $Ron*W$ are of $4*10^4$ $\Omega.\mu m$ for 2-MOS and of $2*10^5$ $\Omega.\mu m$ for 4-MOS structures. Tuning range is $\pm 10\%$ in the temperature range $25°C-150°C$. gox-NeVth with $L=20$ μm, all other devices with $L=10$ μm. For the 4-MOS structure, $V_{G,fixed}=2\ V,\ 1.1\ V,\ 1.1\ V$ and $1.2\ V$ for respectively, the GOX, the gox-NeVth, the gox-HiVth and the gox-LoVth.

	$V_{G,min}$ [V]	$V_{G,max}$ [V]	ΔV_G [V]	HD3$_{min}$ [dB]	HD3$_{max}$ [dB]
GOX-2MOS	0.96	1.54	0.58	-99	-66
GOX-4MOS	1.70	1.86	0.16	-75	-66
gox-LoVth-2MOS	0.54	0.85	0.31	-62	-55
gox-LoVth-4MOS	1.02	1.11	0.09	-83	-67
gox-HiVth-2MOS	0.73	1.01	0.28	-63	-53
gox-HiVth-4MOS	1.02	1.08	0.06	-67	-61
gox-NeVth-2MOS	0.34	1.14	0.80	-65	-46
gox-NeVth-4MOS	0.75	0.92	0.17	-79	-66

range moreover imposes a bias mostly located at the right side of the peak (Fig. 3.2), where θ influence is dominant, advantageous for the thick oxide GOX devices. The gox-HiVth and gox-LoVth exhibit similar performance, again expected from their similar HD3 vs. V_G-Vth characteristics (Fig. 3.2). The gox-NeVth devices do not seem interesting when placed in a 2-MOS configuration and for the optimization targets considered here, since they feature a HD3 20 dB higher than the other device types (Tab. 3.3). The $Ron*W$ vs. V_G-Vth behavior of 2-MOS structures (Fig. 3.9) is indeed particularly detrimental to these devices since driving them to low V_G-Vth, where its HD3 steeply increases. In the $25°C-150°C$ range considered here, gox-NeVth are moreover badly influenced by the transition from partially to fully-depleted mode of operation (Fig. 3.2).

Surprisingly but according to the HD3 characteristics (Fig. 3.2 and Fig. 3.8), the 4-MOS structure degrades the HD3 performance of GOX devices (Tab. 3.3). For gox devices (i.e. thin-oxide), the HD3 is clearly improved by the 4-MOS. Moreover, the benefit of the 4-MOS structure is more important for the gox-LoVth than for the gox-HiVth and even more for the gox-NeVth devices as for thin t_{ox}, low N_A and fully-depleted devices, the surface potential is better controlled by V_G, improving the HD3 of 4-MOS structures. Even if, as in the GOX case, HD3 can be slightly worse, the 4-MOS structure presents advantages when compared to the 2-MOS one as discussed hereafter. Aside from the well-known advantages of the 4-MOS structure [7] [8], we would like to emphasize that 1) Ron*W is one order of magnitude higher in the case of 4-MOS, allowing the designer to use wider devices, which is an advantage for the noise performance of the circuit and the matching between different transistors which both improve for devices with a bigger area; 2) the transistors in the 4-MOS are biased at higher V_G, also decreasing the mismatch [20]; 3) the required V_G tuning range is lower in the 4-MOS case. One could argue that the smaller value of the $Ron*W$ for 2-MOS structure is in fact an advantage for the 2-MOS structure, allowing the use of longer transistors. However, the HD3 does not necessarily improve with increasing length (Fig. 3.10) and 2-MOS structures composed of long transistors are furthermore problematic due to the parasitic pole caused by the gate capacitance ($C_g \propto C_{ox}WL$) while 4-MOS structures intrinsically compensate for that [19].

For these reasons, we would recommend to use the 4-MOS structure for all our de-

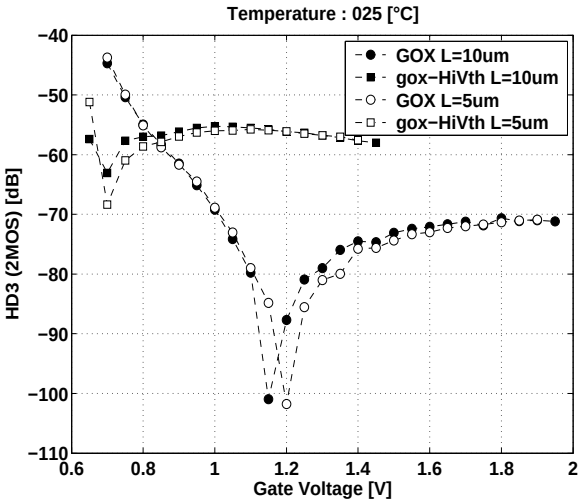

Figure 3.10: HD3[dB] vs. V_G at room temperature for 2-MOS resistive structures with gox-HiVth (thin-gate oxide, high Vth) (□) and with GOX (thick-gate oxide) (○). $L = 5\ \mu m$ (void symbols) and $L = 10\ \mu m$ (full symbols).

vices. The results of the comparison additionally show that for the optimization targets considered here: 1) we at least attain HD levels around $-60\ dB$ for $Va = 200\ mV$ in the whole tuning range, which is adequate for applications with 0.1 % linearity specifications; 2) we better select the gox-LoVth (i.e. thin-gate oxide, low V_{th}) with $Vg, fixed = 1.2\ V$ as its HD3,max is indeed the best one ensuring $HD3 \leq -67\ dB$ in the whole tuning range and its HD3,min is also among the best ones. Note that without the use of our methodology it would have been very difficult to predict the effect of a thin oxide on the HD characteristics and very difficult to anticipate the good performance of gox-LoVth devices, not usually recommended for analog parts.

3.6 Conclusion

Focusing on MOS transistors used as tunable resistors in MOSFET-C continuous-time fully-differential filters, measurements of HD3 in triode regime have been presented for the first time in a deep-submicron multi-Vth SOI process. This multi-Vth process allowed a discussion of HD3 vs. t_{ox}, N_A and hence Vth. Our experimental study thus validates and extends the theoretical analysis of [2] for deep-submicron MOSFETs and a very wide temperature range ($25°C - 220°C$), confirming the interaction of body and mobility reduction related effects in determining the device HD3 performance for the 2-MOS structure. HD3 was also extracted for the 4-MOS topologies using the same methodology, stressing the lack and the need for improved modeling of the linearity behavior of the 4-MOS structures.

An original design-oriented comparison methodology was developed to help the analog designer to select the best device type, device dimensions, gate bias and resistive structure in practical design conditions, i.e. ensuring the HD performance can be reached

in the whole tuning range, necessary to compensate on-chip for process and temperature variations. This measurement-based methodology can be applied to any device on any technology. The comparison methodology is then pertinent in the frame of the device analog ID card (Fig. 1.4) as, concerning applications where MOSFETs have to be used as tunable resistors, the methodology efficiently characterize the HD3 and provides design-oriented information for the design of analog cells.

Applied to this particular deep-submicron $0.12\mu m$ SOI process, the methodology revealed that

1) at least HD3 levels around $-60dB$ can be reached in the whole tuning range by all devices, which is adequate for applications with 0.1 % linearity specifications;

2) the 4-MOS structure should be preferred to the 2-MOS one in all cases as those structures were confirmed to be less sensitive to *n* effects and moreover offer other advantages;

3) surprisingly, that devices targeting digital applications (thin gate oxide, low Vth) emerge as the best choice for the considered optimization targets and for the technology under study. In this case, the devices are indeed biased in a region where *n* related effects are dominant and it is particularly favorable to lightly doped devices with thin oxides. It justify the interest for the design of the analysis of the underlying physical phenomena.

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Chapter 4

MOSFET mismatch

In this chapter, we study another imperfection of the MOS transistor related to high-performance analog designs: the mismatch, which characterizes the slight differences of the $I-V$ curves of two devices placed on the same chip and originally designed to be identical. The mismatch on the drain current (I_D) in a transistor pair is defined by $\frac{\Delta I_D}{I_D}$, where ΔI_D is the difference in the drain current of the two transistors. As the mismatch is a random phenomenon, $\frac{\Delta I_D}{I_D}$ for a transistor pair is in fact a particular realization of the distribution of the possible values of $\frac{\Delta I_D}{I_D}$. Assuming that the statistical distribution of the mismatch is normal, we can characterize it completely by its mean and its standard deviation $\left(\sigma_{(\Delta I_D/I_D)}\right)$, which are to be described by the mismatch models. As an example, the measured $\sigma_{(\Delta I_D/I_D)}$ of nMOSFETs from a 0.35 μm bulk CMOS technology are represented in Fig. 4.1 vs. the normalized drain current $\left(Inorm = \frac{I_D}{W/L}\right)$ for different device widths (W) and lengths (L). We will come back later on the test structure used to measure such mismatch curves and on their interpretation.

The mismatch depends both on the inversion level (corresponding to $Inorm$) and on the device size (Fig. 4.1). In our study we focus on one hand on the I_D mismatch in weak and moderate inversion and on another hand on the efficient integration of mismatch information into top-down analog design methodologies. We will first point out the importance of the MOSFET mismatch in analog design and briefly review the existing mismatch models, showing their limitations in describing the mismatch in weak inversion and in the information they provide to the analog designer. A more comprehensive review of the current mismatch models is presented in appendix C. Based on drain current mismatch measurements done on very different technologies and large operating temperature range, we then propose a new term related to the body factor dependence on the gate voltage to model more adequately the mismatch in weak and moderate inversion. The measured mismatch data is also included in a top-down design methodology, applied to the current mirror case, to predict the effect of mismatch on the analog performance, revealing nonobvious design rules as well as typical misconceptions.

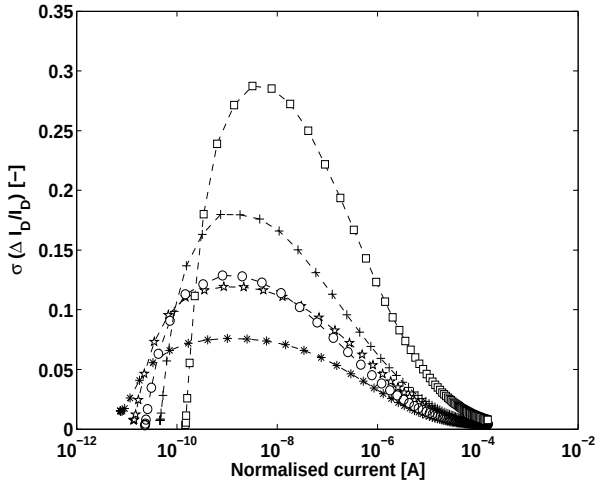

Figure 4.1: Measured $\sigma_{(\Delta I_D/I_D)}$ vs. normalized drain current ($Inorm$) for n-type MOSFETs of a $0.35\ \mu m$ bulk CMOS technology for devices with minimal length ($L = 0.35\ \mu m$) and different device widths: $W = 40\ \mu m$ ($*$), $W = 20\ \mu m$ ($\star$), $W = 10\ \mu m$ ($\circ$), $W = 5\ \mu m$ ($+$) and $W = 2\ \mu m$ ($\square$). $V_D = 1.3\ V$, $V_S = 0\ V$.

4.1 Impact of MOSFET mismatch on analog performance and existing models

The MOSFET mismatch influences key parameters of mixed-signal circuits. It is quite straightforward in the case of digital-to-analog converters (DAC), in which the analog output is determined by a binary scaled ladder of elements (resistors, MOSFETs working as current sources, ...). Any mismatch between elements of the ladder will directly degrade the DAC resolution and yield. In [1], the case of a 14-bit current-steering DAC is investigated and to obtain a yield of at least 99.7%, the drain current mismatch standard deviation must be lower than 0.1%. The static random access memory (SRAM), a major digital block of almost any mixed-signal sytem, also suffers from high sensitivity to MOSFET mismatch as it drastically reduces the noise margins [2]. The risk here is that the value read from the SRAM cell differs from the one which was written a few clock cycles before. The performance of analog cells is also degraded by MOSFET mismatch. Consider for example the case of a basic amplifier constituted by a nMOS differential pair, each one loaded by a resistor. The mismatch between the transistors of the differential pair will create a desequilibrium between the two branches, i.e. an offset voltage. The offset voltage is more and more important as the available signal range decreases with technology evolution, driving the analog blocks which follow the amplifier into nonlinear operation [3]. Fully-differential circuits are also often used in analog design for increased robustness, extended dynamic range and suppression of the even-order non-linearities thanks to the symmetry of these signals. The MOSFET mismatch degrades the symmetry such that these even-order non-linearities are not fully canceled. Finally, if we apply a variation of a common-mode signal (V_{CM}) to the inputs of this basic amplifier ($\Delta V_{CM,in}$), in presence of mismatch, a differential voltage will appear between the amplifier outputs, converting the common-mode input signal to a differential one. In this way, the MOS-

FET mismatch then worsens the common-mode rejection ratio (CMRR) [3]. The power supply rejection ratio (PSRR) is also badly influenced by mismatch [4]. In [5], P. Kinget investigates the effect of mismatch for a multi-stage design. Taking only the mismatch on the threshold voltage (ΔVth) into account and making the assumption that the devices are biased in strong inversion, the power (P) needed to reach a particular dynamic range (DR) at a given frequency (f) is estimated as [5]

$$P = 24.C_{ox}.A_{Vth}^2.f.DR^2 \tag{4.1}$$

where C_{ox} is the oxide capacitance and A_{Vth} is a technology dependent parameter such that $\sigma^2_{(\Delta Vth)} = \frac{A^2_{Vth}}{W.L}$. The same kind of analysis was done by E. Vittoz in [6] to evaluate the influence of the noise on the power consumption, estimated in this case to

$$P = 8.k.T.f.DR^2 \tag{4.2}$$

where k is the Boltzmann constant and T is the absolute temperature. The limits imposed by the mismatch is reported to be more important by two orders of magnitude [5]. Low risk and high performance design then requires both accurate modeling of mismatch and its efficient integration in design methodologies.

The mismatch on the drain current is caused by variations in process parameters like the oxide thickness (t_{ox}), the flat-band voltage (V_{fb}), the doping concentration (N_A), the zero-field mobility (μ_0) and the device width and length. These variations result in the variation of the typical SPICE parameters used to describe the MOSFET behavior in circuit simulators: Vth, the body effect factor γ, θ describing the mobility reduction with the vertical field and the current factor β equal to $\frac{W}{L}\mu C_{ox}$, where μ is the mobility. Among the existing mismatch models, two modeling options can be identified. [7][8] start from the fluctuations on the technological parameters and propagate these variations to classical SPICE parameters and hence drain current. [9][10][11][12][13] on the contrary start from the variations on the SPICE parameters and combine them through a quite simple expression of the drain current or through the BSIM3v3 drain current model [14]. In the first approach, the variances of the mismatch on the technological parameters ($\sigma^2_{\Delta p}$) are not measured directly but are calculated by [7]

$$\sigma^2_{(\Delta I_D/I_D)} = \sum_j \frac{1}{I_D}\left(\frac{\partial I_D}{\partial p_j}\right)^2 \sigma^2_{\Delta p_j} \tag{4.3}$$

where p_j is a given technological parameter (t_{ox}, N_A, ...), $\sigma_{(\Delta I_D/I_D)}$ is measured and $\frac{\partial I_D}{\partial p_j}$ is obtained by simulation of a SPICE model. The width and length dependence of $\sigma^2_{\Delta p_j}$ is in this case obtained automatically. In the second approach, except for [9], the drain current mismatch model is obtained as follows [11][13]

$$\sigma^2_{(\Delta I_D/I_D)} = \sum_i \left(\frac{1}{I_D}\frac{\partial I_D}{\partial P_i}\right)^2 \sigma^2_{\Delta P_i} + \sum_{i,j} \frac{2}{I_D^2}\frac{\partial I_D}{\partial P_i}\frac{\partial I_D}{\partial P_j}\rho\left(\Delta P_i, \Delta P_j\right)\sigma_{\Delta P_i}\sigma_{\Delta P_j} \tag{4.4}$$

where P_i and P_j are given SPICE parameters (Vth, β, ...) and $\rho\left(\Delta P_i, \Delta P_j\right)$ is the correlation between the mismatches in P_i and P_j. $\frac{1}{I_D}\frac{\partial I_D}{\partial P_i}$ and $\frac{2}{I_D^2}\frac{\partial I_D}{\partial P_i}\frac{\partial I_D}{\partial P_j}$ are obtained by analytical derivation of the used SPICE model. $\sigma_{\Delta P_i}$ and $\sigma_{\Delta P_j}$ are obtained by fitting of the

measured $\sigma_{(\Delta I_D/I_D)}$ characteristics. Note that the partial derivatives terms depend on the nominal value of Vth, β, ..., which are extracted from the I_D measurements. The width and length dependence of σ_{P_i} must then also be derived from the experimental $\sigma_{(\Delta I_D/I_D)}$. The best mismatch prediction is obtained by the model of T. Serrano [11] in [15] with an accuracy on the drain current mismatch of 5 % in strong inversion regime and of 13.5 % in weak inversion. More details on the different models using the second approach can be found in Appendix C.

Despite the importance of transistor mismatch for high-performance analog designs, efficient integration of mismatch constraints in top-down analog models is still lacking. The provided mismatch information on the SPICE parameters is indeed not adequate for design, requiring complex sensitivity analysis and/or lengthy Monte-Carlo simulations. Moreover, today IC's are driven to moderate and weak inversion regimes by the ever tougher constraints on power consumption and device downscaling. The existing mismatch models are not adequate in weak and moderate inversion regime as the mismatch parameters are fitted to the same expression of $\sigma_{(\Delta I_D/I_D)}$ (4.4) for all inversion regimes whereas the underlying MOSFET physics differ from one region to the other.

The mismatch on the drain current in weak inversion is usually said to be dominated by ΔVth and described by [16]

$$\frac{\Delta I_D}{I_D} = -\frac{gm}{I_D}\Delta Vth \tag{4.5}$$

Indeed assuming that ΔVth is the only parameter influencing $\frac{\Delta I_D}{I_D}$ in weak inversion, the model in [13] is presented as continuous from weak to strong inversion. The validity of this assumption is however also tested in [13] revealing that some other phenomena should play a role. Additional terms should then be used to better reflect the different mechanisms taking place in the weak/moderate and strong inversion regimes. Here below, we test the validity of (4.5) first using measurements of a 0.35 μm CMOS bulk technology and then measurements in a wide temperature range of a 2 μm fully-depleted (FD) silicon-on-insulator (SOI) CMOS. The generalization of the observations leads to propose a new term based on the dependence of the n body effect factor on the gate voltage (V_G) to better describe $\sigma_{(\Delta I_D/I_D)}$ in weak and moderate inversion.

4.2 0.35 μm bulk CMOS

In this section we present measurements [17] performed on a 0.35 μm bulk CMOS process and we check the validity of (4.5) in this particular case. The test structure [11] is made of a 8×8 matrix of identical cells. Each cell includes 30 NMOS and 30 PMOS transistors of different sizes: widths are $W = 40,\ 20,\ 10,\ 5,\ 2$ and 0.8 μm and lengths $L = 10,\ 5,\ 2,\ 0.8$ and 0.35 μm. The outer cells of the matrix are not considered to ensure that all measured devices have the same environment. The drain current mismatch statistics are then computed on 36 different transistors for each size. The standard deviation of the drain current mismatch is represented vs. *Inorm* as in Fig. 4.2 for MOSFETs with different sizes.

For a given size, $\sigma_{(\Delta I_D/I_D)}$ increases as we move from the strong to the weak inversion regime, ending up as a plateau at its maximum (Fig. 4.2). We can indeed, in a first approximation, model the drain current mismatch as the combined effect [9] [10] [11] [12] [13] of the mismatch on the threshold voltage (ΔVth) and of the mismatch on the

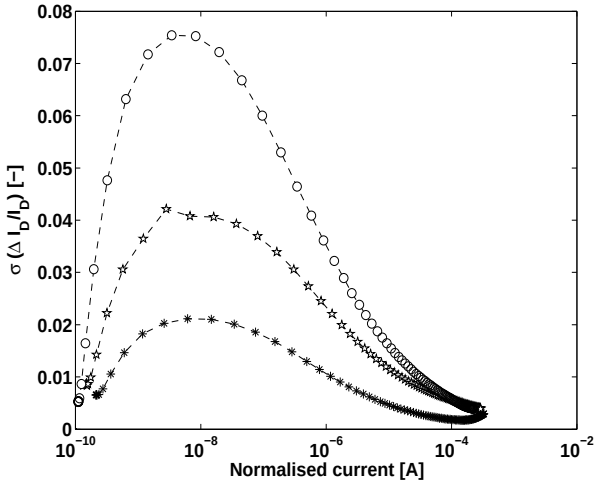

Figure 4.2: Measured $\sigma_{(\Delta I_D/I_D)}\,[-]$ vs. $Inorm\,[A]$ for n-type MOSFETs of a $0.35\ \mu m$ bulk CMOS technology for different device sizes: $W = 40\ \mu m$ and $L = 10\ \mu m$(∗); $W = 10\ \mu m$ and $L = 2\ \mu m$ (⋆); $W = 5\ \mu m$ and $L = 0.8\ \mu m$(○). $V_D = 1.3\,V$, $V_S = 0\,V$.

current factor $\left(\frac{\Delta\beta}{\beta}\right)$. If we further assume that these two mismatches are statistically independent, we can derive from (4.4) [9]

$$\frac{\Delta I_D}{I_D} = \frac{1}{I_D}\left(\frac{\partial I_D}{\partial Vth}\right)\Delta Vth + \frac{1}{I_D}\left(\frac{\partial I_D}{\partial \beta}\right)\Delta\beta \tag{4.6}$$

$$\frac{\Delta I_D}{I_D} = -\frac{gm}{I_D}\Delta Vth + \frac{\Delta\beta}{\beta} \tag{4.7}$$

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \left(\frac{gm}{I_D}\right)^2\sigma^2(\Delta Vth) + \sigma^2\left(\frac{\Delta\beta}{\beta}\right) \tag{4.8}$$

When we move to lower *Inorm* (i.e. weak inversion), the device efficiency ($\frac{gm}{I_D}$) is increased and $\sigma_{(\Delta I_D/I_D)}$ levels up as well (4.8) as $\sigma_{(\Delta Vth)}$ and $\sigma_{\left(\frac{\Delta\beta}{\beta}\right)}$ are considered constant for a given transistor size. The plateau in weak inversion is assumed to be related to the plateau of $\frac{gm}{I_D}$ and hence to the exponential dependence of the drain current in this region of inversion. The range of normalized current covered by the plateau varies with the size and with the technology (Fig. 4.2). $\sigma_{(\Delta I_D/I_D)}$ also depends on the devices sizes. We will not go into more details here, focusing only on the differences between the weak and the strong inversion. In a first approximation, we can write [9]

$$\sigma(\Delta Vth) = \frac{A_{Vth}}{\sqrt{W.L}} \tag{4.9}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{W.L}} \tag{4.10}$$

where A_{Vth} and A_β are technology dependent parameters. Short and narrow channels require more detailed expressions [11][12][13]. For a given inversion level (i.e. a given

Inorm in Fig. 4.2), $\sigma_{(\Delta I_D/I_D)}$ is then, in a first approximation anèd for long, inversely proportional to the square root of the device area which has been verified in our measurements for long and wide transistors.

In weak inversion, due to the drain current exponential dependence on Vth, the $\frac{\Delta I_D}{I_D}$ is, as already said, usually considered to depend only on the mismatch on Vth, yielding from (4.5)

$$\frac{\Delta I_D}{gm} = \Delta Vth \tag{4.11}$$

In order to verify the assumption of the dependence of $\frac{\Delta I_D}{I_D}$ on ΔVth only in weak inversion, following [13], we represent the correlation coefficient (ρ) between the value of $\frac{\Delta I_D}{gm}$ at a gate bias (V_G) corresponding to Vth and the value of $\frac{\Delta I_D}{gm}$ at other gate biases. It is indeed around $V_G = Vth$ that (4.5) was reported to be the closest to the reality [13]. $\frac{\Delta I_D}{gm}$ is computed from the measurements as $\frac{\Delta I_D}{I_D} / \frac{gm}{I_D}$. Vth was extracted using the second derivative method but its value is not critical as the Vth mismatch is not extracted here. ρ for the 0.35 μm CMOS technology under study is represented in Fig. 4.3 vs. *Inorm* and vs. V_G.

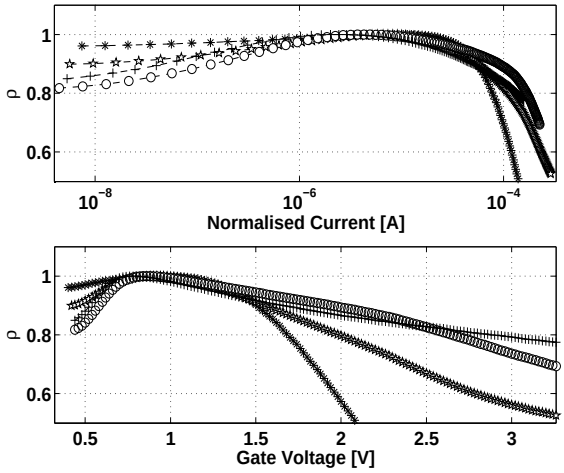

Figure 4.3: Correlation coefficient ρ $[-]$ extracted from measurements vs. $Inorm$ $[A]$ **(up) and** V_G $[V]$ **(down) for n-type MOSFETs of a** 0.35 μm **bulk CMOS technology for different device sizes:** $W = 40$ μm **and** $L = 10$ μm**(**$*$**);** $W = 10$ μm **and** $L = 2$ μm **(**$\star$**);** $W = 5$ μm **and** $L = 0.8$ μm**(**$\circ$**);** $W = 2$ μm **and** $L = 0.35$ μm**(**$+$**).** $V_D = 1.3$ V**,** $V_S = 0$ V**.**

The correlation factor is evidently equal to one for $V_G = Vth$ and decreases as expected at high gate bias as we move toward the strong inversion and the importance of the mismatch of the current factor and of other parameters increases accordingly (Fig. 4.3). More surprisingly, ρ rapidly decreases for gate biases immediately lower than Vth. Considering the value of *Inorm* at which ρ starts to decrease in terms of the $\frac{gm}{I_D}$ vs. *Inorm* characteristic corresponding to the different devices under investigation (Fig. 4.4) highlights that ρ decreases when the device is still in the moderate inversion region and far

from the weak inversion regime. The sharp decrease of the $\frac{gm}{I_D}$ characteristic at very low *Inorm* is due to the leakage current (section 2.2.2).

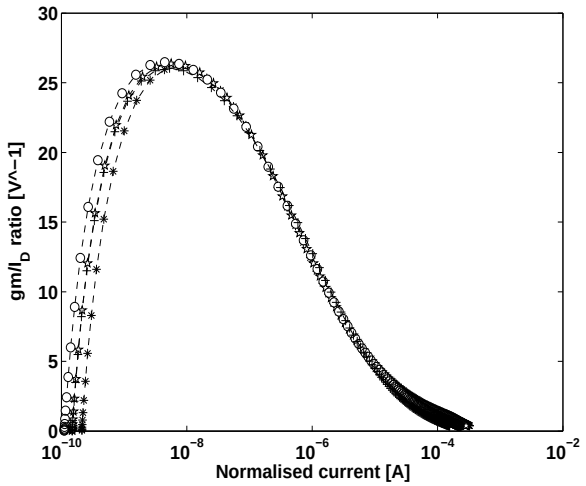

Figure 4.4: Measured $\frac{gm}{I_D}$ ratio $[V^{-1}]$ vs. $Inorm\,[A]$ for n-type MOSFETs of a $0.35\ \mu m$ bulk CMOS technology for different device sizes: $W = 40\ \mu m$ and $L = 10\ \mu m$(∗); $W = 10\ \mu m$ and $L = 2\ \mu m$ (⋆); $W = 5\ \mu m$ and $L = 0.8\ \mu m$(○); $W = 2\ \mu m$ and $L = 0.35\ \mu m$(+). $V_D = 1.3\,V$, $V_S = 0\,V$.

The assumption that $\frac{\Delta I_D}{I_D}$ is only determined by ΔVth is then only true in a very limited range in moderate inversion and needs further consideration. We first present mismatch measurements on a very different technology in the next section before generalizing the observations.

4.3 2 μm fully-depleted silicon-on-insulator CMOS

A deeper understanding of mismatch in weak inversion has been gained from experiments in a 2 μm fully-depleted (FD) silicon-on-insulator (SOI) CMOS technology [18]. In this case, the test structure consists of an array of 20 identical nMOSFETs, each 20 μm wide and 10 μm long. The drain current mismatch measurements are performed in a wide temperature range from room temperature up to $225^{\circ}C$. In order to keep the chuck temperature variations small, we force the chuck temperature to be regulated between the measurements of two transistor pairs, while the heating system is disconnected from the chuck during the quick measurement of the MOSFET pair for improved signal integrity.

The measured $\sigma_{(\Delta I_D/I_D)}$ in saturation are represented in Fig. 4.5 vs. the normalized current for different temperatures.

As temperature increases, three zones can be clearly identified. First, at high *Inorm*, i.e. in strong inversion, the standard deviation of the drain current mismatch improves with the level of inversion and with the temperature as expected from (4.8) and from the decrease of the $\frac{gm}{I_D}$ ratio with temperature (Fig. 4.6). A second zone can be defined for very low values of the normalized drain current (i.e. in very weak inversion), where $\sigma_{(\Delta I_D/I_D)}$ abruptly increases. This can be linked to subthreshold junction currents. Finally,

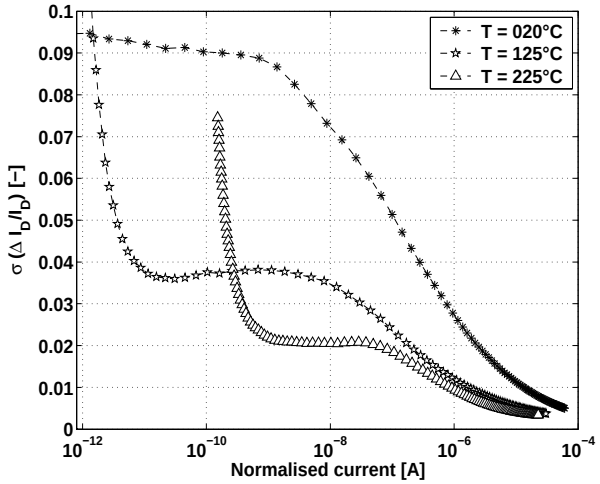

Figure 4.5: Measured $\sigma_{(\Delta I_D/I_D)}$ $[-]$ vs. $Inorm$ $[A]$ for n-type MOSFETs of a 2 μm fully-depleted SOI CMOS technology with $W = 20$ μm and $L = 10$ μm for different temperatures: $T = 25°C$ $(*)$, $T = 125°C$ $(\star)$ and $T = 225°C$ (Δ). $V_D = 1.5\,V$, $V_S = 0\,V$.

in the central zone, the mismatch exhibits a plateau value expected from the exponential dependence of the drain current as already explained. According to (4.5), the $\sigma_{(\Delta I_D/I_D)}$ plateau level decreases with temperature as consequence of the decrease of the $\frac{gm}{I_D}$ ratio as temperature increases (Fig. 4.6). From room temperature to $125°C$, the plateau level however decreases more steeply than the corresponding value of the maximum of $\frac{gm}{I_D}$ (Fig. 4.6). The difference for the $125-225°C$ transition is less pronounced but still exists. Moreover, $\sigma_{(\Delta I_D/I_D)}$ remains almost constant for *Inorm* values lower than the normalized drain current corresponding to the maximum value of the $\frac{gm}{I_D}$ ratio. This is unexpected and unpredicted by (4.5) as for those *Inorm* values, $\frac{gm}{I_D}$ significantly decreases (Fig. 4.5 and Fig. 4.6). This again further stresses that additional phenomena influence the mismatch in the moderate and weak inversion regimes.

To further stress these experimental discrepancies from the assumption that the threshold voltage mismatch is the only relevant effect in determining $\frac{\Delta I_D}{I_D}$ in weak inversion, we again compute the correlation coefficient (ρ) between the value of $\frac{\Delta I_D}{gm}$ at a gate bias corresponding to Vth and the value of $\frac{\Delta I_D}{gm}$ at other gate biases in this case of the SOI technology and at the different temperatures (Fig. 4.7). Again referring to the $\frac{gm}{I_D}$ evolution with *Inorm* (Fig. 4.6), ρ stays very close to one down to *Inorm* values corresponding to the very weak inversion at room temperature. As temperature is increased, ρ starts to drop from 1 at higher and higher *Inorm* but still corresponding to weak inversion. In the next section, we will generalize these observations with the one pointed out in the previous section for the 0.35 μm bulk technology.

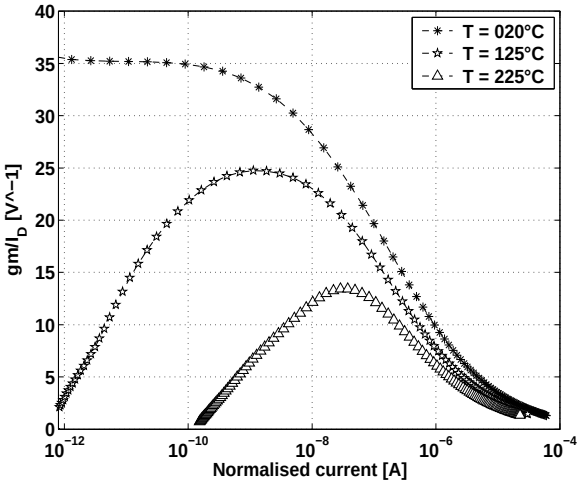

Figure 4.6: Measured $\frac{gm}{I_D}\ [V^{-1}]$ vs. $Inorm\ [A]$ for n-type MOSFETs of a $2\ \mu m$ fully-depleted SOI CMOS technology with $W = 20\ \mu m$ and $L = 10\ \mu m$ for different temperatures: $T = 25°C$ (∗), $T = 125°C$ (⋆) and $T = 225°C$ (△). $V_D = 1.5\ V$, $V_S = 0\ V$.

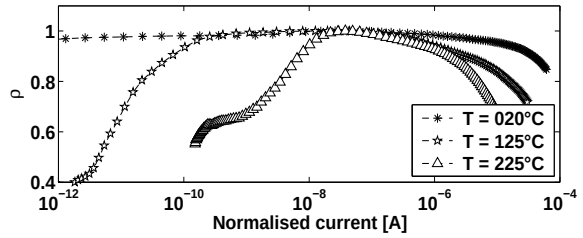

Figure 4.7: Correlation coefficient ρ $[-]$ extracted from measurements vs. $Inorm\ [A]$ for n-type MOSFETs of a $2\ \mu m$ fully-depleted SOI CMOS technology with $W = 20\ \mu m$ and $L = 10\ \mu m$ for different temperatures: $T = 25°C$ (∗), $T = 125°C$ (⋆) and $T = 225°C$ (△). $V_D = 1.5\ V$, $V_S = 0\ V$.

4.4 A new term to improve the mismatch models in weak inversion

In section 4.2, in the bulk case, we concluded that ρ diverges from 1 very quickly for gate biases lower than *Vth* or corresponding *Inorm* values (Fig. 4.3). Even in moderate inversion, ρ differs from 1 in the bulk case. In the SOI case, ρ stays close to 1 at moderate temperature (Fig. 4.7) even in very weak inversion (Fig. 4.6). Only when the temperature increases, ρ becomes less than 1 at higher and higher *Inorm* but for any temperature, ρ nevertheless shows a constant value on a wide bias range corresponding to the moderate inversion regime and only decreases for currents lower than the maximum or plateau value of $\frac{gm}{I_D}$, i.e. in very weak inversion.

On the other hand, it is well known that for FD SOI MOSFETs, the *n* body factor remains constant even in moderate inversion as the width of the depletion region is equal

to the silicon film thickness [18]. Only in very weak inversion or as the temperature is increased, n starts to increase as the device is in an intermediate operating condition between partially- and fully-depleted. Whereas in bulk CMOS, for gate biases immediately below Vth the depletion width shrinks as the surface potential drops below $2\Phi_F$, the n factor in turn increases and strongly depends on the gate bias.

To better fit the measured drain mismatch, we propose to add a new term to the right-hand side of (4.5) such that, in weak and moderate inversion,

$$\frac{\Delta I_D}{I_D} = -\frac{gm}{I_D}\Delta Vth + f(V_G)\Delta n \tag{4.12}$$

From the formula proposed in [19] to model the n dependence on V_G, we empirically propose a function $f(V_G)$, which adequately models the mismatch in weak inversion to be like

$$f(V_G) = \frac{1}{\left[\alpha_1 + \left(\frac{V_G}{\alpha_2}\right)^{\alpha_3}\right]} \tag{4.13}$$

where α_1, α_2 and α_3 are fitting parameters. Δn is computed from the values of n extracted by equating the measured maximum $\frac{gm}{I_D}$ to $\frac{1}{n*U_T}$, where U_T is the thermal voltage. Fitting $f(V_G)$ to the measured mismatch of the bulk transistors, an excellent agreement is obtained in weak inversion (Fig. 4.8, for $W = 5\ \mu m$ and $L = 0.8\ \mu m$ as an example).

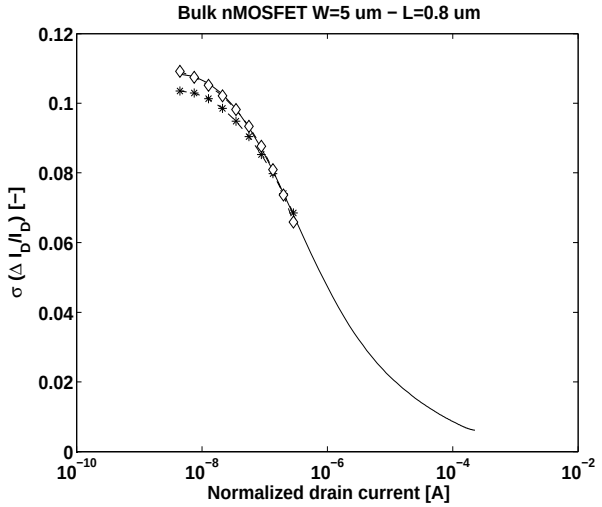

Figure 4.8: $\sigma_{(\Delta I_D/I_D)}\ [-]$ **vs.** $Inorm\ [A]$ **for a n-type MOSFET of the** $0.35\ \mu m$ **bulk CMOS technology with** $W = 5\ \mu m$ **and** $L = 0.8\ \mu m$**. The solid line is the measured** $\sigma_{(\Delta I_D/I_D)}$ **for** $V_D = 1.5\ V$, $V_S = 0\ V$**. In weak and moderate inversion, (**$\Diamond$**) is our proposed new term:** $f(V_G)\Delta n$ **and (**$*$**) is the classical assumption:** $\frac{gm}{I_D}\Delta Vth$**.**

ΔVth is extracted using a current criterion, i.e. Vth is defined as the gate bias at an a priori defined current level I_{cc}. As we are interested in the validity of (4.5) and not on the exact value of ΔVth, we choose, for each size, the value of I_{cc} which best fits the measured $\sigma_{(\Delta I_D/I_D)}$ to $\frac{gm}{I_D}\sigma(\Delta Vth)$. This ensures that the differences we observe between the two terms of (4.5) are not related to errors in the measurement procedure, but only the adequacy of (4.5). As an example in Fig. 4.9, we compare the measured $\sigma_{(\Delta I_D/I_D)}$ of n-type

bulk MOSFETs ($W = 40\ \mu m$ and $L = 5\ \mu m$) with various values of $\frac{gm}{I_D}\sigma(\Delta Vth)$ corresponding to different values of Icc and hence different $\sigma(\Delta Vth)$. The adequacy between the two terms is clearly valid only in a small region in moderate inversion (Fig. 4.2 and Fig. 4.4) even in the best fit case of $\sigma(\Delta Vth) = 3.2\ mV$. The inadequacy of $\frac{gm}{I_D}\sigma(\Delta Vth)$ to describe the mismatch in weak and moderate inversion is thus not related to any errors in the measurement procedure.

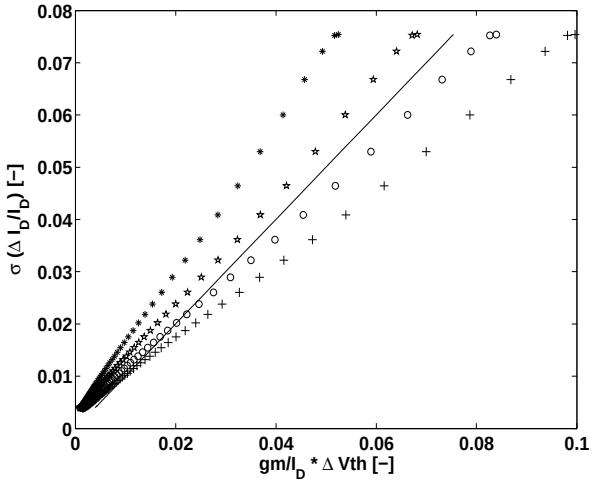

Figure 4.9: Measured $\sigma_{(\Delta I_D/I_D)}\ [-]$ vs. $\frac{gm}{I_D}\sigma(\Delta Vth)\ [-]$ for a n-type MOSFET of the $0.35\ \mu m$ bulk CMOS technology with $W = 40\ \mu m$ and $L = 5\ \mu m$. $\frac{gm}{I_D}$ is obtained from the measurements as $\sigma_{(\Delta I_D/I_D)}$ for $V_D = 1.5\ V$, $V_S = 0\ V$. The different values of $\frac{gm}{I_D}\sigma(\Delta Vth)$ corresponds to $\sigma(\Delta Vth) = 2.0\ mV\ (*)$, $2.6\ mV\ (\star)$, $3.2\ mV\ (\circ)$ and $3.8\ mV\ (+)$.

Once ΔVth estimated, the parameters α_1, α_2 and α_3 in (4.13) are extracted by fitting. Table 4.1 shows that the values of the parameters of $f(V_G)$ for different MOS sizes stay rather similar, with α_2 fairly close to Vth, which suggests a certain physical adequacy of our empirical additional term. Included in a complete mismatch model, the α's and Δn should be extracted together with the other parameters. Width and length dependence of Δn must also be assessed. We will here however not go further into details here as it requires a complete mismatch model, which is beyond the scope of our analysis.

Table 4.1: Values of the fitting parameters of $f(V_G)$ for the different W/L ratios

Parameter	$\frac{\mathbf{W}}{\mathbf{L}} = \frac{\mathbf{5\ \mu m}}{\mathbf{0.8\ \mu m}}$	$\frac{\mathbf{W}}{\mathbf{L}} = \frac{\mathbf{20\ \mu m}}{\mathbf{5\ \mu m}}$	$\frac{\mathbf{W}}{\mathbf{L}} = \frac{\mathbf{40\ \mu m}}{\mathbf{2\ \mu m}}$
α_1	0.0372	0.0287	0.0205
α_2	0.9314	0.9087	1.0354
α_3	8.9192	8.4778	8.2048

Even if the difference between the measured drain current mismatch and the approximate model (4.5) is not that big, it seems worth to add our new term since accurate modeling of mismatch in moderate inversion is important to design high-performance

analog circuits as we will show here below. Moreover, as temperature is considered, the importance of the additional term strongly rises.

4.5 Mismatch data in a top-down design methodology

Analog design is well known to result from the trade-off between different performance parameters such as the gain-bandwidth product (GBW), the power consumption, the linearity, ... [20]. Mismatch is one of them. Ever improved mismatch models are useless if they do not provide the analog designer with the adequate information on how to size and how to bias transistors in order to optimize mismatch along with the other analog performance parameters. The use of mismatch models in practical designs often remains based on complicated sensitivity analysis or lengthy Monte-Carlo simulations. Moreover, when this methodology is applied to a particular design case, only the mismatch is optimized. For example, in [21], the mismatch of a current mirror is optimized whereas e.g. the position of the pole-zero doublet associated to the mirror is not guaranteed to lie beyond the transition frequency of the circuit to which this mirror belongs. We will here include basic mismatch data into a $\frac{gm}{I_D}$ based top-down design methodology [22], showing that we are able to efficiently guide the analog designer when dealing with mismatch constraints among others. In a second design step, more accurate foundry models can be used to fine tune the devices biases and sizes. This two step method results in design time savings and increased circuits performance.

As an example, we will go through the design of a nMOSFET current mirror. We suppose the current mirror is part of a one-stage differential input amplifier (Fig. 4.10), e.g. the first stage of a Miller type two-stage amplifier. If the amplifier is intended to be part of a high-precision circuit, we expect the first stage to be low-noise, low-offset and possibly low-voltage. The following example uses the experimental mismatch data of the 0.35 μm bulk CMOS and the MOSFET behavior is described by measured $\frac{gm}{I_D}$ vs. $Inorm$ characteristics. The stage targets a GBW of 2 MHz on a load capacitance (C_L) equal to 2 pF (Fig. 4.10).

Focusing on the design of the current mirror, we suppose the designer will take the necessary decisions to lower the offset of the differential pair and we will then assume that the offset of the stage is determined by the mismatch of the current mirror. The bias current ($Ibias$) is fixed by the choices made on the input differential pair to fulfill the frequency requirements on the stage (GBW). The mirror is then designed for a constant bias current.

The lengths of transistors M_3 and M_4 (L_3) must be sufficient compared to the length of the input differential pair pMOS transistors in order to minimize the added $1/f$-noise of the nMOS mirror [4]. As the length of M_1 and M_2 is a compromise between, for example, offset and speed, we thus have to consider different values of L_3. Too long mirror devices may however cause the emergence of a pole-zero doublet, linked to the capacitance existing at the mirror node (C_1, Fig. 4.10), which is given by

$$C_1 = C_{db1} + C_{db3} + C_{gg3} + C_{gso3} + C_{gg4} + C_{gso4} \tag{4.14}$$

where C_{db1} (C_{db3}) is the drain-to-substrate capacitance of M_1 (M_3), C_{gg3} (C_{gg4}) is the total gate capacitance of M_3 (M_4) and C_{gso3} (C_{gso4}) is the gate-source overlap capacitance of M_3 (M_4). A continuous expression from weak to strong inversion for C_{gg} can be obtained

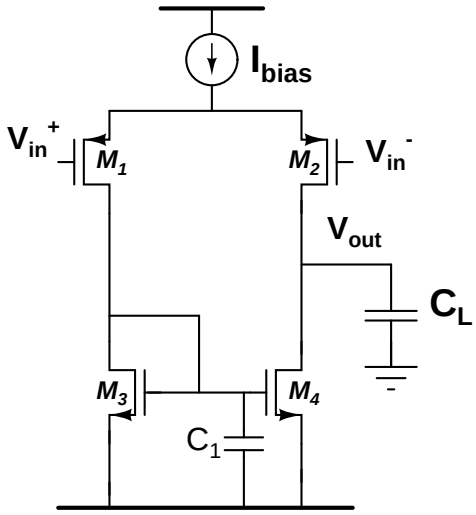

Figure 4.10: Current mirror included in an input stage of a two-stage amplifier biased by a DC current source (*Ibias*) and loaded by a capacitance (C_L). C_1 is the parasitic capacitance associated to the mirror.

through the EKV model [19] or estimated from measurements. All other capacitances are parameters from the technology. The frequency of the pole associated to the mirror is given by

$$f_{\text{pole,mirr}} = \frac{gm_3}{2\pi C_1} \tag{4.15}$$

where gm_3 stands for the transconductance of M_3 and M_4. The mirror zero is at twice $f_{\text{pole,mirr}}$. As an arbitrary design criterion to minimize the phase losses related to the mirror zero, we decide that in this case of study

$$f_{\text{pole,mirr}} \geq 4 \times GBW \tag{4.16}$$

The impact of the finite output resistance of M_3 and M_4 could be easily introduced but is beyond the scope of the presented analysis. Using (4.8) and (4.12), the current mismatch of long devices occupying a relatively small area can be described as [9]

$$\sigma\left(\frac{\Delta I_D}{I_D}\right) = \frac{gm}{I_D}\sigma(\Delta Vth) + f(V_G)\sigma(\Delta n) + \sigma\left(\frac{\Delta\beta}{\beta}\right) \tag{4.17}$$

For short lengths, the above mismatch model might not be 100% correct but would still yield a correct qualitative trend in order to select the more appropriate length and bias ranges in a first step. Once this is known, the analog designer could use more accurate mismatch models to fine tune his design.

In our case, we extracted from the bulk measurements the parameters A_{Vth} and A_β ((4.9) (4.10)) to determine (4.17) and as the dependence of the new term on the device width and length was not investigated we did not include this term in the design example. On another hand, for the available MOSFET sizes, we also included the mismatch measurement data directly into the methodology without the support of any model.

Fig. 4.11 demonstrates that, when designing our current mirror to satisfy (4.16), for a constant *Ibias* fixed by the design of the differential pair, the mismatch for a given mirror length decreases, contrarily to the classical belief, when biasing the device towards the weak inversion region i.e. high $\frac{gm}{I_D}$ ratios. These conclusions moreover do not depend on the model used as the trend is confirmed by the predictions based on the measured mismatch directly.

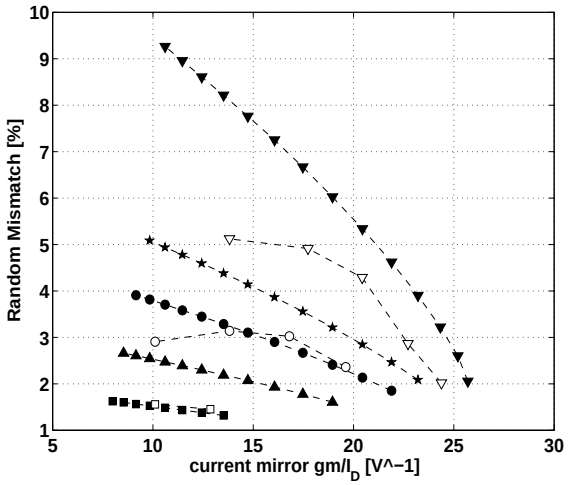

Figure 4.11: Random mismatch $[\%]$ **of the current mirror of Fig. 4.10 vs. nMOSFET** $\frac{gm}{I_D}$ $[V^{-1}]$**. Random mismatch is predicted by model with parameters extracted from measurements (full symbols) and by measured mismatch data (void symbols) for different lengths:** $L = 0.8\ \mu m$ **(▼),** $L = 1.5\ \mu m$ **(★),** $L = 2\ \mu m$ **(●),** $L = 3\ \mu m$ **(▲) and** $L = 5\ \mu m$ **(■).** $Ibias = 1.68\ \mu A$**;** $GBW = 2\ MHz$ **for** $C_L = 2\ pF$ **and the** $\frac{gm}{I_D}$ **of the pMOSFET differential pair equal to** 15**.**

This $\sigma_{(\Delta I_D/I_D)}$ evolution with the inversion regime is due to the fact that as we move from strong to weak inversion and from a design perspective (i.e. constant current), two balancing phenomena occur: the mismatch increases for a given transistor size as $\frac{gm}{I_D}$ increase (4.17) but decreases with increasing transistor area (4.9)(4.10), the last phenomenon being far more dominant (Fig. 4.12). In Fig. 4.12 A, $\sqrt{WL}$ indeed increases by a factor of 10 (i.e. $\sigma(\Delta Vth)$ and $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ decrease) while $\frac{gm}{I_D}$ increases only by a factor of 2 (i.e. $\frac{gm}{I_D}\sigma(\Delta Vth)$ increases). Even if the difference can be less important, the transistor area plays a role in both parameters: $\sigma(\Delta Vth)$ and $\sigma\left(\frac{\Delta\beta}{\beta}\right)$; and $\frac{gm}{I_D}$ only multiply one of the two terms of (4.17). The possible use of high $\frac{gm}{I_D}$ is obviously of high interest for low-voltage low-power applications for it additionally lowers the flicker noise and increases the output dynamic range as the drain-to-source saturation voltage of the current mirror transistor gets smaller [3].

4.6 Conclusion

We started by reviewing the existing mismatch models and concluded that they are insufficient to describe the mismatch in weak inversion. Mismatch measurements on two

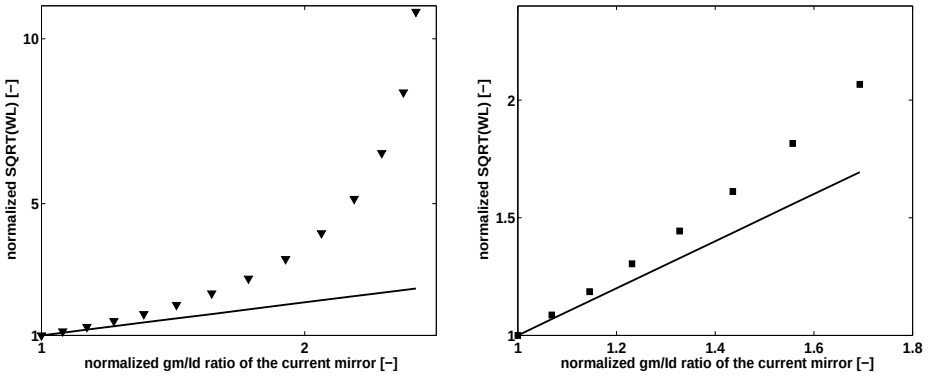

Figure 4.12: Relative increase of the square root of area vs. the relative increase of the $\frac{gm}{I_D}$ ratio for the nMOSFET of the current mirror with $L = 0.8\ \mu m$ (A) and $L = 5\ \mu m$ (B). The $\frac{gm}{I_D}$ values considered here are the same as in Fig. 4.11. The transistor area are predicted by the $\frac{gm}{I_D}$ design methodology based directly on measured characteristics. $\frac{gm}{I_D}$ and $\sqrt{WL}$ are normalized to their smallest value. $Ibias = 1.68\ \mu A$; $GBW = 2\ MHz$ for $C_L = 2\ pF$ and the $\frac{gm}{I_D}$ of the pMOSFET differential pair equal to 15.

very different technologies were presented. First, the drain current mismatch is examined for various device sizes in a 0.35 μm bulk CMOS technology. Then MOSFET mismatch is investigated in a wide temperature range ($25 - 225°C$) in a 2 μm fully-depleted SOI technology. The analysis of the measurements confirms that the mismatch on the threshold voltage is not the only relevant effect in moderate and weak inversion, contrarily to what is generally assumed. The comparison of the measurements in the two technologies further helps to better understand and identify the additional phenomena playing a role in the determination of the drain current mismatch in the moderate and weak inversion region. **We then proposed a semi-empirical term, based on the gate voltage dependence of the *n* factor, to more accurately model the MOSFET mismatch in the weak and moderate inversion regimes.**

Further, we included basic mismatch information into an analog top-down design methodology and apply it to the practical design of the current mirror of an amplifier input stage. Based on drain-current mismatch measurements, we predicted non-obvious behavior and design rules. **For the practical design targets considered here (i.e. taking the position of the pole into account and fixed *Ibias*), the random mismatch on the drain current of the two transistors of the mirror was indeed predicted to decrease as the mirror is biased more towards the weak inversion thanks to the decrease of the mismatch with the transistor sizes.** The practical design targets considered here make the difference between our analysis and [21] or [23], more recently, in which the current mirror is designed as a stand-alone analog block for current signal processing, i.e. not considering its design for an amplifier input stage in which *Ibias* is fixed by the differential pair.

The analysis of the MOSFET mismatch done here can thus be considered as the third item of the device analog ID card (Fig. 1.4) as it improves the modeling of the mismatch

in weak and moderate inversion and as through its inclusion in analog top-down design methodology provides important information to the analog cell designer.

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Part II

From analog cells to system performance : VHDL-AMS modeling

Chapter 5

Mixed-signal systems modeling and simulation with VHDL-AMS

5.1 Introduction

Design of electronics for harsh environments specifically requires methodologies to better predict the circuit/system performance at high temperatures as already stressed in chapter 1. Moreover, the required effort to reduce the power consumption in nowadays electronic systems must be undertaken at different levels during the design of mixed-mode signal processing systems (Fig. 1.4). In part I, we showed that using our design-oriented characterization methodology, the power consumption can be reduced by choosing the adequate device for a given application and by reducing the risk margins by an improved modeling and associated design methodology of two MOSFET imperfections: harmonic distortion in the triode regime and MOSFET mismatch in weak and moderate inversion. In this second part, we move one level up, from analog cells to mixed-signal circuits (Fig. 1.4). A great amount of power can be saved at this level by properly dividing the power budget among the different subcircuits. It is also important that the influence of the temperature on the different blocks is accurately modeled to ensure the correct operation of the system in the whole temperature range. The goal is here to develop tools allowing us to rapidly identify the critical blocks in order to assign them an important part of both the power budget and design effort, reducing overall power consumption, design time and hence cost. We use a mixed-signal hardware description language (HDL), VHDL-AMS, for that purpose. To be more specific, we will illustrate this in the case of the simulation and design of continuous-time $\Delta\Sigma$ analog-to-digital converters (ADC). The $\Delta\Sigma$ ADC is indeed a small mixed-signal system as composed of a series combination of a modulator, a mostly analog block, and a decimator, i.e a digital filter (Fig. 5.1).

The modulator is already in itself a mixed-signal system composed of an analog loop filter, an internal quantizer and feedback digital-to-analog converters (DAC) (Fig. 5.1). In this context behavioral simulations are indeed unavoidable. The use of VHDL-AMS and its benefits may however be extended to mixed-signal circuits. Mixed-signal HDL's furthermore provide the possibility to include thermal behavior. This aspect will however not be treated here.

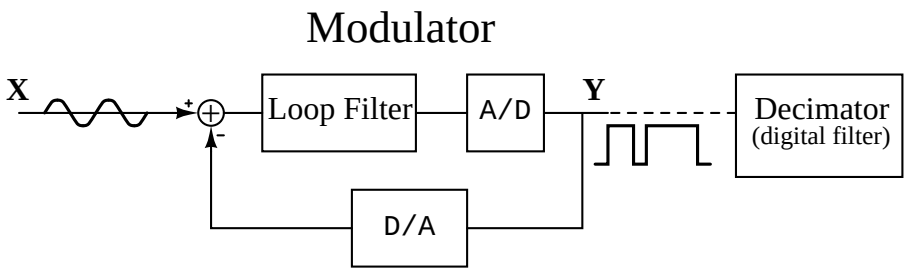


Figure 5.1: A ΔΣ analog-to-digital converter is the series combination of a mixed-signal modulator and a digital filter, the decimator. The modulator is composed of an analog loop filter, an internal analog-to-digital converter and a feedback digital-to-analog converter.

We start by motivating our choice of mixed-signal HDL's to model and simulate mixed-signal circuits and more particularly the ΔΣ analog-to-digital converters. Then we present VHDL-AMS in a brief overview. We also detail design-oriented models corresponding to different critical analog cells: amplifier, comparator and integrator. A model to generate white noise is also presented.

5.2 Motivation of the use of mixed-signal HDLs

The test of IC's is nowadays one of the major cost factors [1]. In applications where the reliability constraints are severe, its importance is even bigger. The test also slows down the time-to-market as the test set-up is only validated when the chip has been realized. HDLs provide a description detailed enough to be used commonly by the circuit and the test designer. The development and validation of the test set-up could start earlier in the design cycle, shortening the time-to-market [2].

We further focus on the simulation of the analog part of ΔΣ ADC's, the modulator. More details on the ΔΣ architectures and operation will be given in chapter 6. We here only present the specificities which affect the simulation. The ΔΣ loop filter (Fig. 5.1) can be implemented using discrete-time (DT) or continuous-time (CT) circuitry. In this thesis, we focus on CT implementations and the implications of this choice on the simulation will also be highlighted.

The ΔΣ modulators, also called noise shapers, are oversampled and their internal behavior is strongly non-linear [3]. Their sampling frequency (F_{samp}) is indeed given by $F_{samp} = OSR * 2f_b$, where OSR is the oversampling ratio and f_b is the signal bandwidth. Due to their non-linear internal behavior, the influence of each building block is not straightforward and, most of the time, cannot be evaluated analytically. During the design of a ΔΣ the designer must nonetheless distribute the available power budget among the different building blocks (Fig. 5.1) (i.e. integrators constituting the loop filter , internal quantizer, feedback digital-to-analog converters) to reach the targeted conversion resolution and signal bandwidth. Extensive simulations are then usually necessary.

The time-domain waveforms analysis is of limited interest and the performance of ΔΣ converters is mainly specified in the frequency domain, requiring the simulation of multiple signal periods ($T_b = 1/f_b$) to obtain an accurate enough spectrum estimation using the fast-fourier transform (FFT). The required simulation time is further increased

due to the oversampling of ΔΣ ADC's. For most of the design parameters, the classical transistor-level simulations are known to be accurate but also lengthy as they rely on complicated device models. The number of transistor-level simulations must be reduced to its minimum, replacing it whenever possible by simulations with behavioral models [4][5][6].

In order to implement behavioral models, several possibilities do exist. We have to make a distinction here between CT and DT implementations of the loop filter. In DT implementations, the major part of the phenomena only depends on the values of voltages, charges or currents around the sampling instants as the signal is sampled at the ΔΣ input (Fig. 5.2 a), while in the CT case, the value of each signal at any moment influences the modulator performance as sampling only occurs inside the loop, at the quantizer (Fig. 5.2 b).

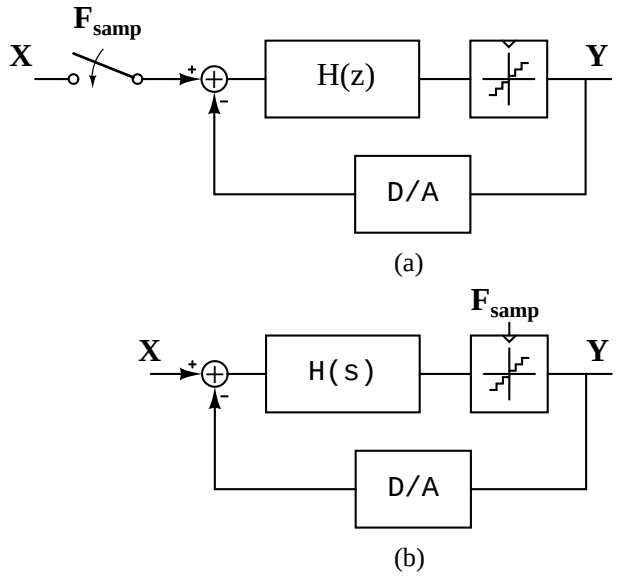


Figure 5.2: A discrete-time (DT) (a) and a continuous-time (CT) (b) ΔΣ modulator. For simplicity, only the first place where sampling occurs is indicated. The DACs (for both DT and CT), the DT loop filter and the internal ADC (DT) are also triggered by the sampling frequency $Fsamp$

DT implementations are well described using discrete-time languages like Matlab/Simulink [7][8], C [9][10][11] or VHDL [12]. On the other hand, some other possibilities have to be explored in order to take into account the true mixed-mode operation of CT ΔΣ (i.e. sampling occurring inside the loop) using C [4] or hardware description languages (i.e. VHDL/VERILOG or VHDL-AMS/VERILOG-AMS, their mixed-signal extensions) [13][14]. It is also possible to compute a DT equivalent of the CT modulator [15][16] and simulate this DT equivalent using one of the possibilities cited here above for DT modulators.

We will not go further into details of DT equivalent models here as these methods result in quite poor results accuracy, although with very fast simulation. Moreover, only the quantizer inputs and outputs are accessible. The two remaining approaches; C-based special-purpose and HDL-based simulation environments, are benchmarked in Tab. 5.1.

Table 5.1: Simulation approaches of $\Delta\Sigma$ modulator continuous-time implementations: pros and cons.

Characteristic	special-purpose simulation environment	HDL based simulation environment
Simulation speed	Very fast	Fast
Simulation accuracy	High	High
Extensibility	Low	High
Integration in mixed-mode chip	No	Yes

Modern HDLs support the description of both behavior and structure [17]. Structural models partition systems into subsystems and subsubsystems. Behavioral models describe the operation of a system (or subsystem) at various levels of abstraction starting from highly abstract to very detailed. The combination of these two descriptions make the HDLs a very good support for top-down methodologies, possibly allowing top-down specifications and bottom-up verifications. So, even if the simulation time can be much longer in HDL-based simulators, they have the big advantage to be part of the classical design flow of a mixed-mode chip. It allows to simulate the modulator jointly with the decimator and more generally, as part of a wider system. Using VHDL [18] or Verilog [19] would require to approximate the continuous-time behavior of each building block by its discrete-time equivalent. On the contrary, the use of VHDL-AMS [20] or Verilog-AMS [21]: the analog and mixed-signal extension to VHDL/Verilog is straightforward as it supports the description of systems of differential and algebraic equations (DAE's) of the form [17]

$$\bar{F}(\bar{x}, d\bar{x}/dt, t) = 0 \tag{5.1}$$

where $\bar{F}$ is a vector of expressions and $\bar{x}$ is a vector of unknowns. It can hence handle continuous-time signals. Moreover, the VHDL-AMS (Verilog-AMS) simulation tools [22] [23] [24] [25] [26] allow to connect and jointly simulate cells described in HDLs and cells described at the transistor level (SPICE-like netlists) making them a complete top-down design tool. The use of mixed-signal HDLs seems then the best solution to us for the objectives considered here. It may be discussed a lot on the pros and cons of VHDL-AMS and Verilog-AMS as both fit our needs [27]. Preferring a standardized language, we select VHDL-AMS and we chose to model the CT $\Delta\Sigma$ modulator using VHDL-AMS.

5.3 A brief overview of VHDL-AMS

VHDL-AMS is a strict superset of the standard IEEE 1076-1993, better known as VHDL'93. It has been normalized in 1999 as IEEE 1076.1-1999. AMS stands for *Analog and Mixed Systems* as VHDL-AMS supports the description, documentation and simulation of systems with a behavior continuous in time and in amplitude. It is a multi-abstraction, multi-domain description and simulation language (Fig. 5.3). Speaking about VHDL-AMS, we must be careful to separate the issues related to the norm itself from the issues related to its implementation in a design suite [22][23][24]. The available tools indeed do not implement the full language capabilities[20].

A VHDL-AMS model consists of one entity describing the model interfaces together with its generic parameters and of one or more architectures containing the model implementation [17]. The entity defines the *ports* through which the model is connected to

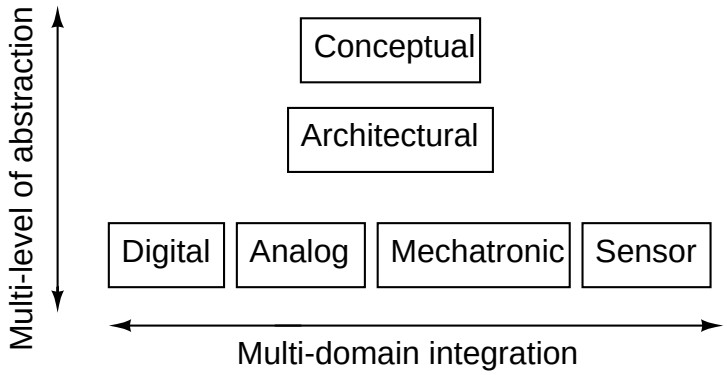


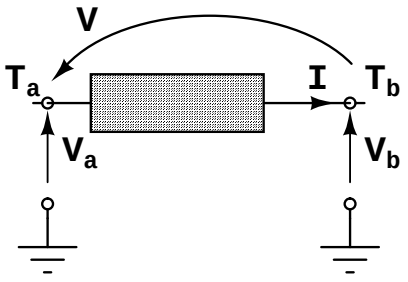
Figure 5.3: VHDL-AMS is a true multi-abstraction, multi-domain description and simulation tool

other models. A *port* can be described using different objects, which carry the information : *signals*, *quantities* or *terminals*. Signals carry the discrete-time information as in VHDL. Quantities and terminals are new objects introduced by VHDL-AMS. Quantities represent the unknown in the DAEs (5.1) and thus describe the continuous-time information. There exist *source*, *free* or *branch* quantities. Source quantities are not implemented by today's simulators and we will not go further into detail here, more information can be found in [28][29]. A quantity is free if it is not associated to any terminal. They can also be used to describe ports in signal flow modeling and are in this case associated to a *mode* (IN or OUT) indicating the direction of the signal flow. Terminals and the associated branch quantities describe conservative systems.

Conservative systems are systems obeying to generalized Kirchoff's laws like electrical systems but also thermal, mechanical or fluidic systems. The terminals have some *nature* corresponding to the energy domain: electrical, thermal, etc. Branch quantities are then the unknows in DAE's describing conservative systems and can be of two kinds: *across* and *through* quantities. Across quantities represent effort-like effects such as voltage, temperature, or pressure [17] while through quantities represent flow-like effects such as current, heat flow rate or fluid flow rate. The conservative aspects of such conservative systems are implicitly described in VHDL-AMS. The VHDL-AMS simulator then implicitly assumes that, in the case of an electrical system for example, the sum of all through quantities (currents) connected to the same terminal is zero while all across quantities (voltages) connected to the same terminal share the same value. The syntax used to describe the branch quantities is illustrated in Fig. 5.4.

Moreover, VHDL-AMS also provides, among other mechanisms, two commands to describe the action of the analog solver on the digital solver and vice-versa: *'above* and *break*, respectively. As they are fundamentally different, the analog and digital solvers are generally governed by separate clocks but indeed have to be synchronized to ensure the reliability of a mixed-signal simulation.

If the interfaces are properly defined, a system including blocks from different energy domains, described at different behavioral abstraction levels in continuous-time as well as in discrete-time can be jointly modeled and simulated using VHDL-AMS. In this way, it is a true multi-abstraction, multi-domain description and simulation language.




```
quantity V across I through Ta to Tb;
quantity Va across Ta;
quantity Vb across Tb;
```

Figure 5.4: Branch across (*Va*, *Vb*, *V*) and through (*I*) quantities associated to the terminals *Ta* and *Tb*. If the nature of the terminals are defined as electrical, then the across quantities are voltages and through quantities are currents. The reference (electrical ground) is intrinsically defined (see *Va* and *Vb* declarations.)

5.4 Analog cells models

In the following section, we review VHDL-AMS models emulating analog cells at different levels of description. The analog cells are the constituting blocks of a continuous-time $\Delta\Sigma$ modulator (see chapter 6) but were developed to be applicable in the description of other circuits. Here again, the models were developed with the designer point of view, to support a top-down methodology. The different analog cells and the related characteristics described by the models are summarized in Tab. 5.2. We describe them in more details in the next sections.

Table 5.2: Different analog cells included in the models and the corresponding modeled characteristics

BUILDING BLOCK	NON-IDEALITY
INTEGRATOR (TRANSFER FUNCTION)	finite gain
	finite gain-bandwidth product
	output voltage saturation
COMPARATOR	delay
	offset
	hysteresis
	jitter
DIGITAL-TO-ANALOG CONVERTER	rise/fall times
	jitter
RESISTOR (ACTIVE RC INTEGRATOR)	white noise
	distortion
AMPLIFIER (ACTIVE RC INTEGRATOR)	finite gain or transconductance
	finite bandwidth
	finite output impedance
	output voltage limitation
	output current limitation
	gm, gd non-linearity (OTA only)
	offset (OTA only)
	output common-mode voltage (OTA only)

5.4.1 Behavioral models for the designer

As already said, the available VHDL-AMS simulation suites [22][23][24] offer, aside from the already stressed multi-level modeling and simulation capabilities, the possibility to connect and jointly simulate VHDL-AMS models and circuits described at the transistor level (SPICE-type netlists). They can then be considered as a complete top-down design tool. In order to fully benefit from this potential, we have however to pay special attention when modeling the output stages. The available amplifier models, [30][22] for example, usually transfer the load capacitance value to the model through a generic parameter in the entity. The amplifier transfer function is then modified by an output pole. It is modeled by the following DAE :

$$Vout + \frac{dVout}{dt}\tau_p = AvVin \tag{5.2}$$

where *Vout* (*Vin*) is the output (input) voltage, τ_p is the pole time constant and *Av* is the low-frequency voltage gain of the amplifier. This model approach, although correct, is unappropriate if used in top-down design methodologies. Suppose that we want to simulate this amplifier followed by another analog cell, already (or being) designed at the transistor level (i.e. using SPICE-type simulator). To obtain accurate simulation of the two cells, we would have first to fully characterize the input capacitance of the transistor-level analog cell, then modify the value of the amplifier generic parameter accordingly and finally simulate the two circuits together. On the contrary, in our case, we assume that the outside world is a priori unknown by our model. There may not be any generic parameter related to something the designer does not control such as the load characteristics. The model must then adapt itself to the changes in the outside world.

5.4.2 Amplifier

We develop two types of amplifier models: operational amplifier (OpAmp) and operational transconductance amplifier (OTA), depending if the output is described as a voltage or a current. Both are fully-differential as most of today's implementations use fully-differential architectures for increased robustness and signal range. Below, we describe only the OTA models, the OpAmp ones being quite similar.

The entity corresponding to the fully-differential OTA (Fig. 5.5 and Listing 5.1) defines four ports through which the model communicates with the outside world: Tinm, Tinp, Toutm, Toutp, corresponding respectively to the negative and positive inputs and to the negative and positive outputs. They are all defined as terminals of nature electrical.

Note that the names *inputs* and *outputs* are purely conceptual as terminals don't have any mode (in, out or inout) in VHDL-AMS and in the reality they model. A change at the output of an amplifier will indeed influence the internal behavior of the amplifier. The generic parameters associated to the entity are all of type real and the library *Disciplines.electromagnetic_system* is included (Listing 5.1). This library contains the definition of the conservative aspects of electrical systems, i.e. the relations that the related branch quantities must satisfy.

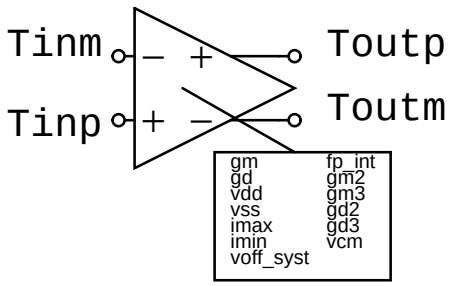


Figure 5.5: Schematic description of the entity corresponding to the fully-differential OTA. The ports are four terminals of electrical nature and the generics are of type real.

Listing 5.1: VHDL-AMS code of the entity *OtaFD* corresponding to a fully-differential OTA. The entity is composed of four ports described as terminals of electrical nature and of generics of real type.

```
library Disciplines; use Disciplines.electromagnetic_system.all;

entity OtaFD is
  generic(gm : real;          -- OTA transconductance [S]
          gd : real;          -- OTA output conductance [S]
          imax : real;        -- OTA max. output current [A]
          imin : real;        -- OTA min. output current [A]
          voff_syst : real; -- OTA input-referred offset [V]
          fp_int : real;      -- OTA internal pole [rad/s]
          vdd : real;         -- OTA positive supply voltage [V]
          vss : real;         -- OTA negative supply voltage [V]
          gm2 : real;         -- OTA 2nd order non-lin for gm [A/v^2]
          gm3 : real;         -- OTA 3rd order non-lin for gm [A/v^3]
          gd2 : real;         -- OTA 2nd order non-lin for gd [A/v^2]
          gd3 : real;         -- OTA 3rd order non-lin for gd [A/v^3]
          vcm : real          -- OTA common mode [V]
          );
        port(terminal Tinp, Tinm, Toutp, Toutm : electrical);
end entity OtaFD;
```

The model of the OTA is composed of two identical sub-models, corresponding to the positive and negative outputs of the fully-differential OTA (Fig. 5.6). The present description of the amplifier concerns single-stage architectures; models for two-stage amplifiers compensated by a Miller capacitance can however be easily obtained by cascading two single-stage models.

The differential input voltage ($Vin,dm = Vinp - Vinm$, $Vinp$ and $Vinm$ being respectively the positive and negative input voltage) is sensed (Listing 5.2) and is processed through a computational block which outputs two currents $Ilocp$ and $Ilocm$. This block, which takes a possible internal pole (fp_int, in Fig. 5.5) into account, is described in a signal flow style as $Ilocp$ ($Ilocm$) is defined as a free quantity (Listing 5.2). $Ilocp$ then controls the transconductance current ($Igmp$), driving the second block, the output stage. The positive and negative output stages of the OTA are described using conservative connections, all nodes are defined as terminals of nature electrical (Listing 5.2 and Listing 5.3). So does $Ilocm$ for the negative output stage. We will now only detail the

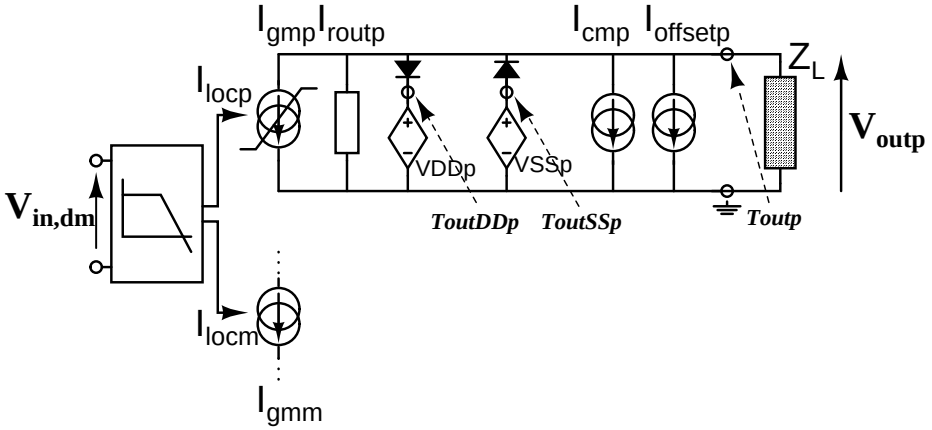


Figure 5.6: Schematic description of the part describing the positive output ($Voutp$) of the architecture of a fully-differential OTA. A similar part, not drawn here, exists for the negative output. Vin,dm is the differential input voltage and Z_L is the load impedance connected externally. $ToutDDp$, $ToutSSp$ and $Toutp$ are terminals of nature electrical. $Igmp$, $Iroutp$ are the currents corresponding to the OTA transconductance and output conductance, respectively. $Icmp$ and $Ioffsetp$ are two additional currents used to model the common-mode output voltage and offset voltage. $Vddp$ and $Vssp$ are the positive and negative supply voltages.

positive output stage for simplicity reasons.

Two local terminals (*ToutDDp* and *ToutSSp*) are defined as well as the related branch quantities following the syntax of Fig. 5.4. The six through branch quantities corresponding to the six parallel branches of the OTA output stage are also defined: *Igm*, *Irout*, *IdiodeDDp*, *IdiodeSSp*, *Icmp* and $Ioffsetp$. The description of the output stage using conservative semantics allows us to write an amplifier model, which doesn't have any information on the outside world prior to its execution.

Ilocp is computed using the *'dot* attribute ($x'dot \equiv \frac{dx}{dt}$) to take the internal pole into account (Listing 5.3, line 14).

The kernel of the OTA model consists of the two branches corresponding to *Igmp* and $Iroutp$. *Igmp*, in a basic model, would be equal to *Ilocp*. In our model, we add a limitation on the value of *Igmp* (Listing 5.3, lines 20-26) on which we will come back later on. Using conservative connections, the output conductance *gd* will be automatically associated to the load impedance Z_L. It will give a pole with frequency ($f_{\mathrm{pole,C_L}} = \frac{gd}{2\pi C_L}$) if the load is capacitive ($Z_L = C_L$) and will cause the gain to drop if the load is resistive or a combination of the two effects if the load has both an imaginary and real part. This can be seen in the AC frequency response of an OTA emulated with our model simulated in two cases: 1) with a 10 *pF* capacitive load (C_L) and 2) with a 100 $k\Omega$ (R_L) resistance (Fig. 5.7). In both cases, the OTA *gm* and *gd* are of 800 μS and 10 μS, respectively and $fp\_int = 1\ GHz$. While the internal pole is visible in the two cases, a second pole is visible in the case of the capacitance load at $f_{\mathrm{pole,C_L}} = \frac{gd}{2\pi C_L} = 159\ kHz$. On the other hand, the gain drops by $6dB$ accordingly to the simulated values ($R_L = 1/gd$) for a resistive load.

In order to emulate the OTA slew rate (SR) using design parameters, we impose a positive (*imax*) and a negative (*imin*) saturation limit on *Igmp* (Listing 5.3, lines 20-26). This limit only exists for time-domain analysis (Line 17) in order not to disturb the small-signal AC analysis. The maximum slope that the OTA output signal can afford is thus depending on the capacitive value of the load, without any a priori information on this

Listing 5.2: VHDL-AMS code of the declaration part of the architecture *struct_ota* of entity *OtaFD* emulating a fully-differential OTA.

```
library Disciplines; use Disciplines.electromagnetic_system.all;
library IEEE; use IEEE.math_real.all;

architecture struct_ota of OtaFD is
-- Local terminal and associated branch
  -- Positive signal path
    terminal ToutDDp : electrical;
    terminal ToutSSp : electrical;
    quantity VDDp across IDDp through ToutDDp;
    quantity VSSp across ISSp through ToutSSp;
  -- Negative signal path
    [...]
-- Branch quantities
  -- Inputs
    quantity Vindm across Tinp to Tinm;
  -- Outputs
   -- Positive signal path
    quantity Voutp across Igmp, Iroutp, Icmp, Ioffsetp through Toutp;
    quantity VdiodeDDp across IdiodeDDp through Toutp to ToutDDp;
    quantity VdiodeSSp across IdiodeSSp through Toutp to ToutSSp;
   -- Negative signal path
    [...]
  -- Free quantities
    quantity Ilocp : real;
    [...]
  -- Constants
    constant tau_int : real := 1.0/(math_2_pi*fp_int);
begin
  -- Computation of internal pole as signal flow
    [...]
  -- Output stage in kirchoff mode (Norton equivalent)
    [...]
end architecture struct_ota;
```

load. This limitation on the current also implies a limitation of the output voltage. The output voltage must nonetheless also be constrained by the positive and negative supply voltages. The semantics used to model the current limit can however not be used here as $Igmp$ and $Voutp$ are intrinsically linked by the Kirchoff's laws. We then define two branches composed of a series combination of a voltage source and an ideal diode, defined as a short-circuit when the voltage across it is superior to $0\ V$ and as an open-circuit otherwise (Fig. 5.6) to limit $Voutp$. As the voltages sources are fixed to the supply voltages values (Listing 5.3, lines 10-11), these two branches indeed maintain $Voutp$ clipped to Vdd (resp. Vss) if it is going too high (resp. low) (Listing 5.3,lines 28-32). If we simulate the OTA model loaded by a capacitance of $10\ pF$ and driven by a fully-differential input signal with an amplitude of $0.4\ V$, its parameters being as following: $gm = 800\ \mu S$,$gd = 10\ \mu S$, $vdd = 10\ V$, $vss = -5\ V$, $imax = 100\ \mu A$ and $imin = -80\ \mu A$, $Voutp$ is limited to $8\ V$ due to the limitation on the current and to $-5\ V$ due to the action of the ideal diodes (Fig. 5.8).

The distortion of the OTA due to the non-linearity of its transconductance and/or of its output conductance can also be modeled by replacing the $Igmp$ and $Iroutp$ expressions

Listing 5.3: VHDL-AMS code of the architecture *struct_ota* of entity *OtaFD* emulating a fully-differential OTA. Only the part corresponding to the positive output is represented for simplicty.

```
library Disciplines; use Disciplines.electromagnetic_system.all;
library IEEE; use IEEE.math_real.all;

architecture struct_ota of OtaFD is
      [...]
     -- Constants
        constant tau_int : real := 1.0/(math_2_pi*fp_int);
begin
     -- Initialisation
        break VDDp => vdd;
        break VSSp => vss;
        [...]
     -- Computation of internal pole as signal flow
        Ilocp + tau_int*Ilocp'dot== -0.5*gm*Vindm;
        [...]
     -- Output stage in kirchoff mode (Norton equivalent)
        if (DOMAIN = TIME_DOMAIN) use
          -- Positive signal path
                -- Current limitation
                if Ilocp'above(imax) use
                        Igmp == imax;
                elsif not(Ilocp'above(imin)) use
                        Igmp == imin;
                else
                        Igmp == Ilocp;
                end use;
                -- Output voltage clamping
                if VdiodeDDp'above(0.0) use
                        VdiodeDDp == 1.0*IdiodeDDp;
                else
                        VdiodeDDp == 1.0e10*IdiodeDDp;
                end use;
          -- Negative signal path
                [...]
        else
                Igmp == Ilocp;
                VdiodeDDp == 1.0e10*IdiodeDDp;
                VdiodeSSp == 1.0e10*IdiodeSSp;
                [...]
        end use;
          -- Output impedance
        Iroutp == gd*Voutp;
        [...]
end architecture struct_ota;
```

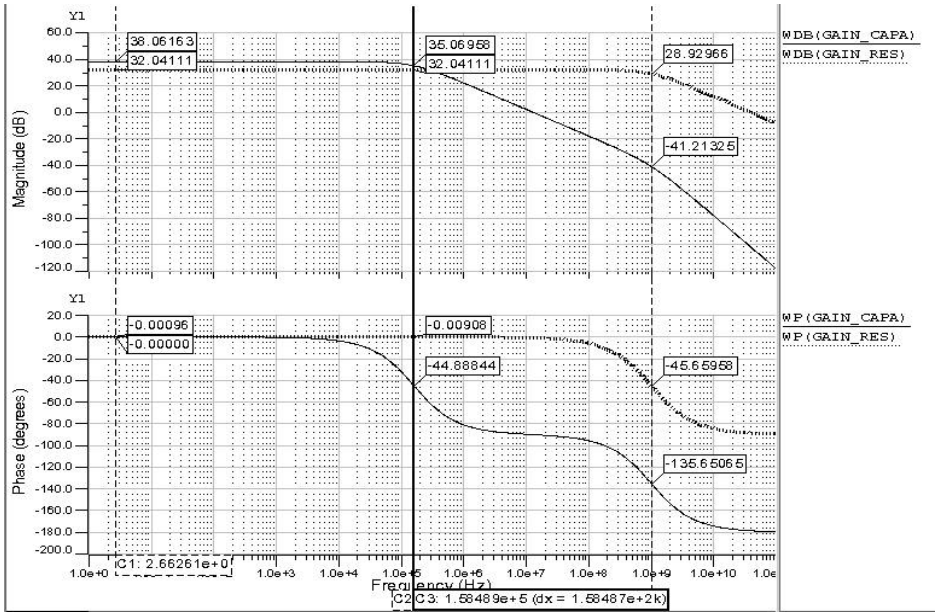


Figure 5.7: AC frequency responses in magnitude [dB] (up) and phase [°] (down) vs. frequency [Hz] for an amplifier emulated by our model. The OTA parameters are $gm = 800\ \mu S$,$gd = 10\ \mu S$ and $fp\_int = 1\ GHz$. the OTA is simulated in two cases: 1) with a $10\ pF$ capacitive load (solid lines) and 2) with a $100\ k\Omega$ resistance (dotted lines).

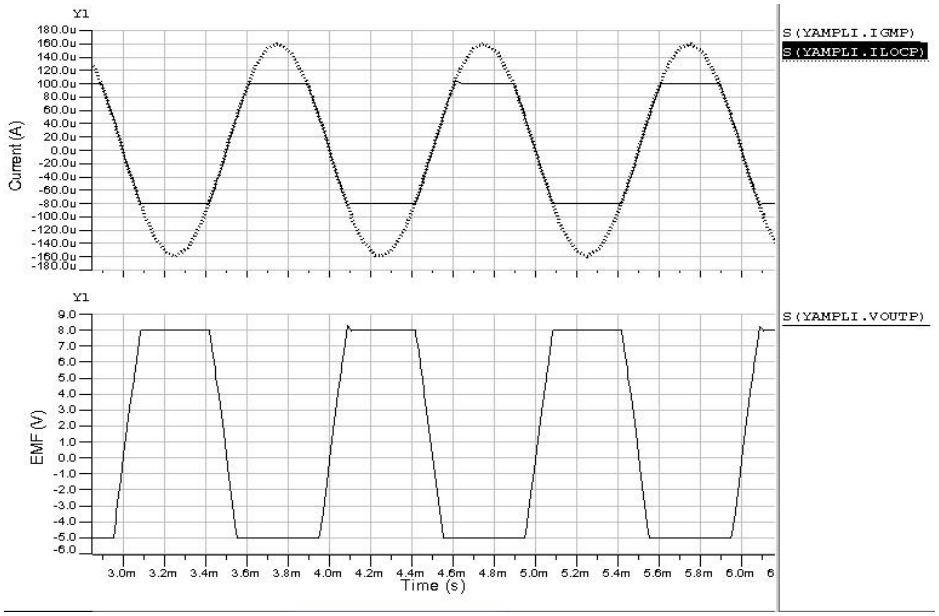


Figure 5.8: $Ilocp$ (dotted line), $Igmp$ (solid line) currents [A] (up) and $Voutp$ [V] (down) for a time-domain simulation of the OTA model loaded by a $10\ pF$ capacitor and driven by a fully-differential input signal with an amplitude of $0.4\,V$. $gm = 800\ \mu S$,$gd = 10\ \mu S$, $vdd = 10\,V$, $vss = -5\,V$, $imax = 100\ \mu A$ and $imin = -80\ \mu A$.

by the corresponding third-order Taylor series (Listing 5.4). The application of this model characteristic will be shown later on, when discussing the third-order continuous-time ΔΣ modulator, in chapter 6.

Listing 5.4: VHDL-AMS code of the architecture *struct_ota* of entity *OtaFD* emulating a fully-differential OTA. Only the modified lines in order to take the distortion are shown. *gm2* (*gd2*) is the 2nd coefficient of the *gm* (*gd*) Taylor series, while *gm3* (*gd3*) corresponds to the 3rd order coefficient. Line numbers correspond to those of Listing 5.3.

```
1  library Disciplines; use Disciplines.electromagnetic_system.all;
2  library IEEE; use IEEE.math_real.all;
3
4  architecture struct_ota of OtaFD is
7          constant tau_int : real := 1.0/(math_2_pi*fp_int);
8  begin
13       -- Computation of internal pole as signal flow
14         Igmp + tau_int*Igmp'dot == gm*(-0.5*Vindm)+
15            + gm2*(Vindm/2.0)**2 + gm3*(-0.5*Vindm)**3;
41         end use;
42           -- Output impedance
43         Iroutp == gd*Voutp+gd2*Voutp**2+gd3*Voutp**3;
44         [...]
```

Modeling the effect of the offset voltage in a fully-differential amplifier without detailing the common-mode feedback circuit is not straightforward. We may nevertheless estimate that an input-referred systematic offset (V_{off}), defined by Fig. 5.9, will shift the mean value of the positive (*Voutp*) and negative (*Voutm*) output voltages (Fig. 5.10).

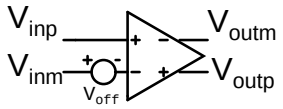


Figure 5.9: Definition of the input-referred offset voltage (V_{off}) used in the models

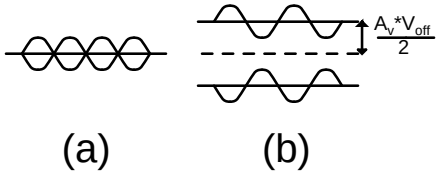


Figure 5.10: Output voltage waveforms of a fully-differential amplifier with (a) zero input-referred offset voltage (V_{off}) and (b) non-zero V_{off}. *Av* is the voltage gain of the amplifier.

The common-mode value of the OTA output voltage is modeled by *Icmp* in Fig. 5.6. The VHDL-AMS descriptions of *Icmp* and $Ioffsetp$ require to modify the architecture struct_ota (Listing 5.3) as shown in Listing 5.5. Note that this description of the common-mode value is only valid for capacitive loads as *Icm* is defined to fix the output voltage

to *vcm* when forced through a resistive load equal to $1/gd$. The description of the offset voltage is nevertheless valid on any load.

Listing 5.5: VHDL-AMS code corresponding to the description of the common-mode value of the output voltage (*vcm*) and of the input-referred offset voltage (V_{off}) for a fully-differential OTA.

```
library Disciplines; use Disciplines.electromagnetic_system.all;
library IEEE; use IEEE.math_real.all;

architecture struct_offset of OtaFD is
        [...]
begin
        [...]
     -- Output stage in kirchoff mode (Norton equivalent)
        Iroutp == gd*Voutp;
        [...]
        if (DOMAIN = TIME_DOMAIN) or (DOMAIN = QUIESCENT_DOMAIN) use
                Icmp == -1.0*gd*vcm;
                Ioffsetp == -0.5*gm*voff_syst;
                Icmm == -1.0*gd*vcm;
                Ioffsetm == 0.5*gm*voff_syst;
        else
                Icmp == 0.0;
                Ioffsetp == 0.0;
                [...]
        end use;
end architecture struct_offset;
```

The OTA model, enhanced by the common-mode and offset voltages descriptions is simulated in the time-domain. The negative input of the fully-differential OTA is clipped to the common-mode voltage value (*vcm*) and the positive input voltage (*Vinp*) is slowly varied around *vcm*. Defining $w(out)$ as the fully-differential output voltage, $w(offset\_spy)$ as $Vinp - vcm$ and t_1 as the time at which $w(offset\_spy) = 0$, the value of the input-referred offset is equal to the value of $-w(offset\_spy)$ at the time $t = t_1$ (Fig. 5.11).

The OTA, which $vcm = 2\ V$ is now driven by fully-differential sine waves first with $voff\_syst = 0\ V$ and then, with an input-referred offset voltage of 10 mV. The output voltages of the OTA with an offset (*Voutp* and *Voutm*) are clearly shifted when compared to the output voltages of the OTA without offset (*Voutp_noOffset* and *Voutm_noOffset*) by $\frac{gm*voff\_syst}{2*gd} = 400\ mV$ as wanted (Fig. 5.12)

The OTA white noise can be moreover added using the white noise generator described in section 5.4.3.

The OTA behavioral model presented above is tested against transistor-level SPICE simulations with a one-stage single-ended OTA composed of a nMOSFET input differential pair (M1-M2, with M2 connected to the OTA output) loaded by a pMOSFET current mirror (M3-M4, with M4 connected to the OTA output), the bias current is provided by a nMOSFET current mirror (M5-M6, M5 connected to the sources of M1 and M2) driven by a current source of 20 μA. We test the models in the case of a single-ended configuration for simplicity reasons; as the fully-differential models are composed of two identical

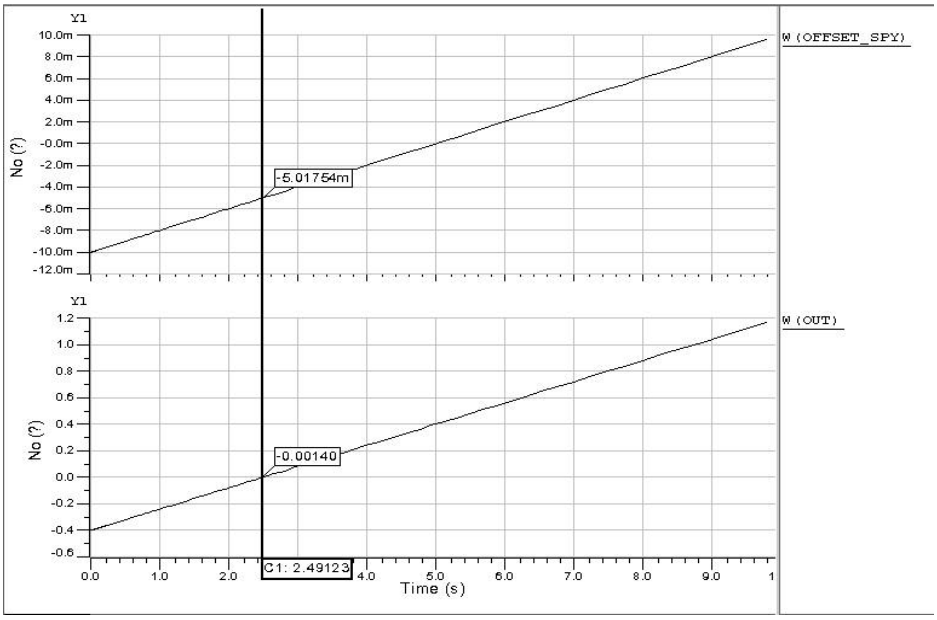


Figure 5.11: $w(offset\_spy)$ **(**$\equiv Vinp - vcm$**) [V] and** $w(out)$ $Ilocp$ **(**$\equiv Voutp - Voutm$**) [V] vs. time [s]. The input-referred offset voltage is given by** $-w(offset\_spy)$ **at the time corresponding to** $w(out) = 0$**.** $Vinp$ **is the positive input of the fully-differential OTA,** $Voutp$ **(***Voutm***) is the positive (negative) output voltage and** vcm **is the common-mode voltage value.** $Vinm = vcm = 0\ V$**, input-referred systematic offset voltage parameter (***vo f f_syst***) equal** $5\ mV$ **and the OTA is loaded by a** $10\ pF$ **capacitor.**

output branches, it should not be problematic unless for the offset voltage as it may depend on the particular implementation of the common-mode feedback. The OTA model implemented first-order behavior, slew rate and output voltage limitation. An AC analysis is first performed; the transconductance (*gm*) and output conductance (*gd*) of M2 and M4 were extracted by a SPICE simulation as: $gm,2 = 53.865\ \mu S$, $gd,2 = 0.166\ \mu S$ and $gd,4 = 87.433\ nS$. The generic parameters of the VHDL-AMS model are modified accordingly and the joint AC simulation of the VHDL-AMS model with the SPICE netlist shows that the input-output transfer function is correctly modeled (Fig. 5.13).

The OTAs are connected in voltage follower configurations and the generics of the VHDL-AMS model *imin* and *imax* are set to $\pm 20\ \mu A$; the supply voltage are $\pm 2.5\ V$. In a time-domain simulation, a voltage step is applied to the inputs of both OTAs at a time $t = 0\ s$. The slope of the output voltages vs. time is extracted at $t = 0\ s$ as a measurement of the slew rate. In both cases, the slope is, as expected, $2\ \frac{V}{\mu s}$. In an other time-domain simulation, the inputs of both OTAs are driven by a sinusoidal voltage source with an amplitude of $1.5\ V$ and a frequency of $240\ kHz$; the simulation results show that the VHDL-AMS model adequately emulates the OTA simulated by a SPICE netlist (Fig. 5.14).

Using the same voltage follower configurations, another time-domain simulation is performed with a sine wave with a $2.5\ V$ amplitude and a frequency of $20\ kHz$ in order to verify the correct modeling of the saturation of the OTA output voltage. In order to take the saturation of M2-M5 and M4 into account the generics *vdd* and *vss* of the VHDL-

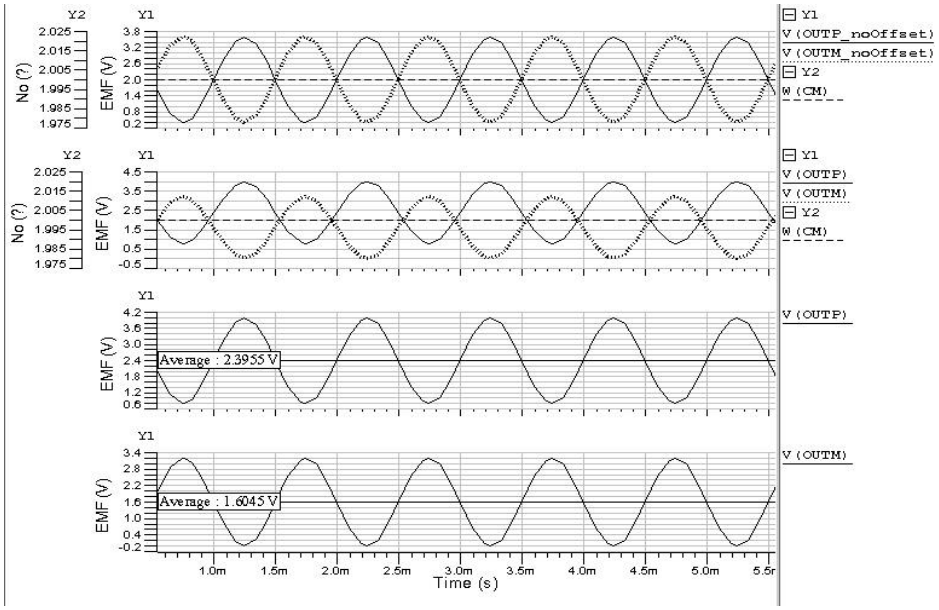


Figure 5.12: Output voltages [V] vs. time [s] of an OTA with a $10mV$ $voff\_syst$ **(**$Voutp$ **and** $Voutm$**) and with** $voff\_syst = 0\ V$ **(**$Voutp_noOffset$ **and** $Voutm_noOffset$**).** $w(cm)$ **is the common-mode output voltage [V].** $vcm = 2\ V$**,** $gm = 800\ \mu S$ **and** $gd = 10\ \mu S$**, the OTA is loaded by a** $10\ pF$ **capacitor.**

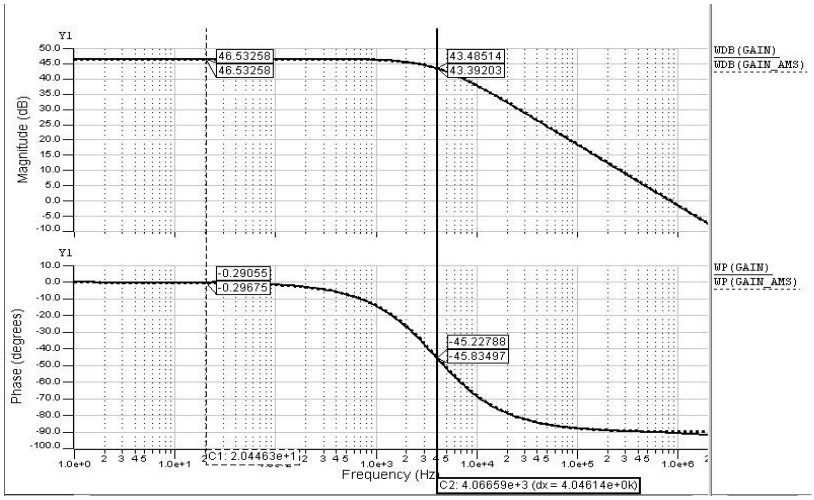


Figure 5.13: AC frequency responses in magnitude [dB] (up) and phase [$^\circ$**] (down) vs. frequency [Hz] for an OTA emulated by our model (dotted lines) and by a SPICE-like netlist (solid lines). The extracted OTA parameters are** $gm = 53.865\ \mu S$**,** $gd = 253.523\ nS$ **and the OTA is loaded by a** $10\ pF$ **capacitive load for both descriptions.**

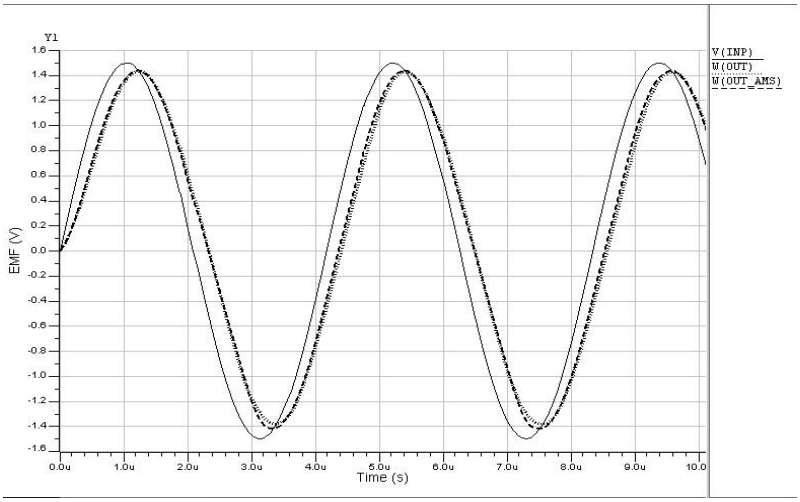


Figure 5.14: Output voltage [V] vs. time [s] of the OTA simulated by a SPICE netlist ($W(out)$, dotted line) and by the VHDL-AMS model ($W(out_ams)$, dashed line) corresponding to the same positive input voltage ($Vinp$, solid line): amplitude of $1.5\ V$ and frequency of $240\ kHz$. Both OTAs are loaded by a $10\ pF$ capacitive load. The bias current of the OTA described by a SPICE netlist is $20\ \mu A$ and the supply voltages are $pm2.5\ V$. The generics of the OTA VHDL-AMS model are $gm = 53.865\ \mu S$,$gd = 253.523\ nS$, $imin = -20\ \mu A$, $imax = 20\ \mu A$, $vdd = 2.5\ V$ and $vss = -2.5\ V$.

AMS model of the OTA are set to $2.17\ V$ and $-1.84\ V$, respectively. The simulation shows that the saturation of the OTA output voltage is adequately modeled for a behavioral model (Fig. 5.15).

5.4.3 Noise generator

In order to simulate the white noise related to different elements (resistors, amplifiers, ...), we develop an entity called *wn_source*, defined in Listing 5.6.

Listing 5.6: VHDL-AMS code of the entity emulating a white noise source.

```
entity wn_source is
 generic (Fsmp : real := 1.0e3;          -- Sampling frequency [Hz]
          PSD_dB_Hz : real := -50.0;     -- White noise PSD [dB/Hz]
          seed1 : integer := 47;         -- seed value for gaussSIG
          seed2 : integer := 449         -- seed value for gaussSIG
         );
 port    (signal Snoise : out real := 0.0
         );
end entity wn_source;
```

A white noise with a given power spectral density (*PSD*) can indeed be emulated by a

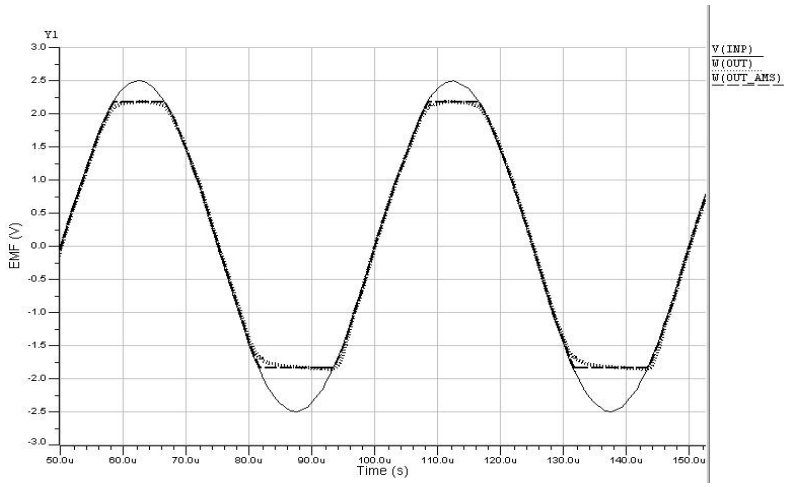


Figure 5.15: Output voltage [V] vs. time [s] of the OTA simulated by a SPICE netlist ($W(out)$, dotted line) and by the VHDL-AMS model ($W(out_ams)$, dashed line) corresponding to the same positive input voltage ($Vinp$, solid line): amplitude of $2.5\,V$ and frequency of $20\,kHz$. Both OTAs are loaded by a $10\,pF$ capacitive load. The bias current of the OTA described by a SPICE netlist is $20\,\mu A$ and the supply voltages are $pm2.5\,V$. The generics of the OTA VHDL-AMS model are $gm = 53.865\,\mu S$,$gd = 253.523\,nS$, $imin = -20\,\mu A$, $imax = 20\,\mu A$, $vdd = 2.17\,V$ and $vss = -1.84\,V$.

set of gaussian random variables with a zero mean value and a standard deviation σ given by [31]

$$\sigma = \sqrt{F_s 10^{\frac{PSD}{10}}} \tag{5.3}$$

where F_s is a sampling frequency. The standard VHDL-AMS packages do not contain any gaussian random variable generator. We could use the possibility offered by the simulation tools to jointly simulate scripts written in *C* but we prefer writing a new procedure in VHDL-AMS, ensuring the portability of our model. This procedure (Listing 5.7) emulates gaussian random variables. It is based on the Box-Muller approximation which generate *x*, a gaussian random variable following

$$x = \sqrt{-2\ln a_1} * \cos(2\pi a_2) \tag{5.4}$$

where a_1 and a_2 are $[0,1]$ uniform random variables. In our VHDL-AMS case, they are generated by the standard VHDL-AMS function *uniform*.

We use this procedure to generate 100000 samples of a gaussian random variable with $\sigma = 3$. The probability density function (PDF) is estimated by dividing the interval covered by the samples into 200 segments and computing the probability in each of these segments using the histogram. The obtained PDF is compared with the theoretical PDF of a gaussian variable (Fig. 5.16), showing the very good match of our approximation.

The white noise generator is then built on this procedure *gaussSIG*, in which the standard deviation *sigma* is defined as (5.3). Using 131072 noise samples, we emulate a

Listing 5.7: VHDL-AMS code of the procedure used to generate a random variable following a gaussian law, with a zero mean value and a standard deviation σ using the Box-Muller approximation

```
procedure gaussSIG (constant sigma : in real; [...]
  [...] variable seed1, seed2 : inout integer;[...]
  [...] variable gauss_var : out real) is
 variable unif_var1, unif_var2 : real;
begin
 uniform(seed1,seed2,unif_var1);
 uniform(seed1,seed2,unif_var2);
 gauss_var := sigma*(sqrt(-2.0*log(unif_var1))*cos(math_2_pi*unif_var2));
end procedure gaussSIG;
```

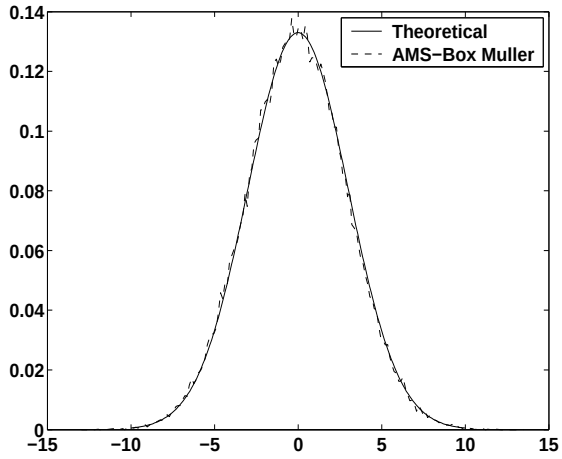


Figure 5.16: Probability density function (PDF) of a gaussian random variable with zero mean and $\sigma = 3$: from the theoretical expression of the PDF (plain line) and computed from the generated noise samples using the VHDL-AMS procedure (dotted line).

white noise with a PSD of $-50\ dB/Hz$ and $F_s = 1\ kHz$. Due to the intrinsic random signal behavior, the power spectral density is computed using the periodogram technique on sub-windows of 8192 points each (Fig. 5.17). Here again, the generated noise matches its specifications.

In a continuous-time circuit, a white noise sample must be generated at each simulation point of the analog solver (ASP). It is however not possible to trigger a model by the ASPs as they are inaccessible. We must use a discrete-time clock to trigger the generation of the noise samples. To be sure that a noise sample is generated at each ASP, the frequency of the discrete-time clock must be much higher than the highest frequency present in the operation of continuous-time circuit under consideration. An additional VHDL-AMS function, which renders the ASP instants accessible in the model would allow to avoid this time-consuming method of the discrete-time clock.

The $1/f$-noise can also be included in the VHDL-AMS models using a noise source based on fractional differentiation to generate samples with a power spectral density having a $1/f$ slope [31]. We do not go into more details here.

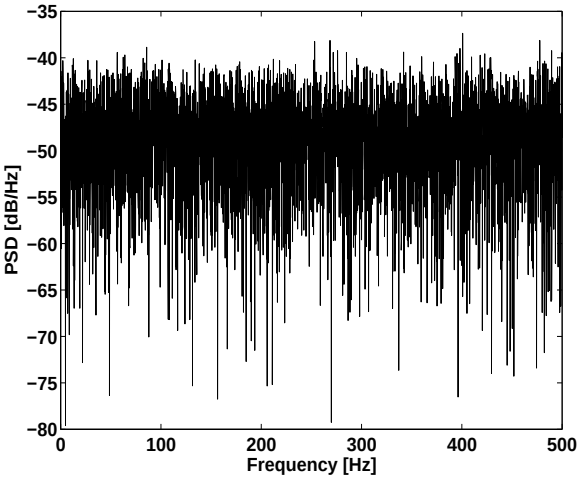


Figure 5.17: Power spectral density $[dB/Hz]$ vs. frequency $[Hz]$ of the noise samples generated using VHDL-AMS entity *wn_source* with $Fsmp = 1\ kHz$ and $PSD_dB_Hz = -50.0\ dB/Hz$.

5.4.4 Comparator

The generics associated to the model, which emulates a clock triggered single bit analog-to-digital converter (i.e. a comparator) with fully-differential inputs are listed in Fig. 5.18 together with their graphical representation.

NAME	TYPE	DESCRIPTION
up_val	real	High logic level [V]
down_val	real	Low logic level [V]
tdelay	real	Comparator delay [s]
offset	real	Comparator offset [V]
hyst	real	Comparator hysteresis [V]

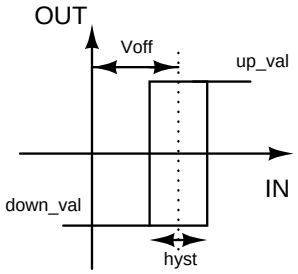


Figure 5.18: Generics associated to the VHDL-AMS entity emulating a comparator.

Apart from a model emulating the ideal behavior, the architectures *comp1bitFD_behav* and *comp1bitFD_behav2* model the following characteristics :

- comparator output delay
- comparator offset
- comparator hysteresis

The comparator hysteresis defines an input voltage range for which the output cannot be computed with determinism. If the input signal lies in this zone, the architecture

comp1bitFD_behav randomly determines the comparator output state (i.e. low or high) while in architecture *comp1bitFD_behav2* the comparator output stays identical to the output corresponding to the previous clock cycle. It is indeed the case in most practical comparator implementations, in which the stage performing the comparison is followed by a latch acting as a local memory. The comparator output state is computed by a finite state machine (FSM) implemented by the function *what_is_state* (Listing 5.8, for *comp1bitFD_behav2*). *comp1bitFD_behav* uses the same structure but calls the *uniform* function to randomly determine the output state for inputs in the hysteresis region.

In Fig. 5.19, the architecture *comp1bitFD_behav2* has been simulated with an offset voltage of 100 mV and a comparator hysteresis of 10 mV. We observe the comparator output when a fully-differential DC voltage (*Vinp*, *Vinm*) is applied to the comparator inputs during 10 clock cycles. This observation is repeated for different values of *Vinp*: 0.046, 0.047, 0.0477, 0.048, 0.050, 0.052, 0.0523, 0.053, 0.054 and 0.056 V; *Vinm* being modified accordingly. The obtained input-output characteristic shows the hysteresis region for $Vin \in [95\ mV, 105\ mV]$. The simulation performed on architecture *comp1bitFD_behav* gives similar input-output characteristics.

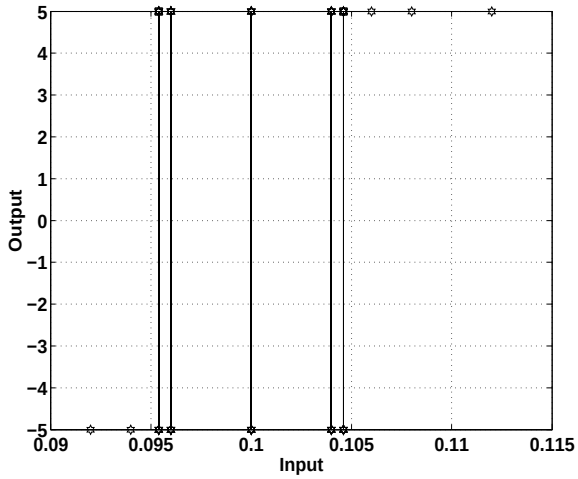


Figure 5.19: Comparator fully-differential output vs. fully-differential input simulated with architecture *comp1bitFD_behav2* with $offset = 100\ mV$, $hyst = 10\ mV$, $up\_val = 2.5$ and $down\_val = -2.5$. Different DC voltages are applied to the comparator fully differential inputs (*Vinp*, *Vinm*): for $Vinp\ [V]$: $[0.046, 0.047, 0.0477, 0.048, 0.050, 0.052, 0.0523, 0.053, 0.054, 0.056]$, *Vinm* being set accordingly. For each DC value, the simulation lasts 10 clock cycles.

In a second experiment, the comparator inputs are driven by a sine wave with a larger period than the clock frequency, again over multiple clock cycles. Both the offset voltage and the hysteresis are now set to 100 mV. For inputs in the hysteresis region ($[50\ mV, 150\ mV]$), the comparator output indeed stays identical to its value at the preceding evaluation, as modeled (Fig. 5.20).

Listing 5.8: VHDL-AMS code of the architecture describing a comparator. The comparator output state is computed by the FSM *what_is_state* and the digital and analog outputs are updated accordingly. *Tinp* **and** *Tinm* **are the, respectively, positive and negative electrical terminals modeling the positive and negative analog comparator inputs.**

```
architecture comp1bitFD_behav2 of comp1bit is
-- Types
        type states is (high,low);
-- Functions
pure function what_is_state (vin,offset,hyst:real;prec_state:states)...
                ... return states is
        variable input : real := vin - offset;
begin
        if absval(input) > (hyst/2.0) then
                if input > (hyst/2.0) then
                        return high;
                else
                        return low;
                end if;
        else
                if prec_state = high then
                        return high;
                else
                        return low;
                end if;
        end if;
end function what_is_state;
[...]
-- Branch quantities
 -- Inputs
        quantity Vindm across Tinp to Tinm;
        [...]
-- Signals
        signal Scurrent_state : states;
        signal Smemory_state : states;

begin
-- Determine the comparator output state
 new_state : process
        begin
         Scurrent_state <= what_is_state(Vindm,offset,hyst,Smemory_state);
         Smemory_state <= Scurrent_state;
         wait on Sclock until Sclock='1';
        end process;
-- Update the digital outputs
 digital_out : process(Scurrent_state)
        begin
         [...]
        end process;
-- Update the analog outputs
 break on Scurrent_state;
 analog_out :
        if Scurrent_state = high use
         [...]
        else
         [...]
        end use;
end architecture comp1bitFD_behav2;
```

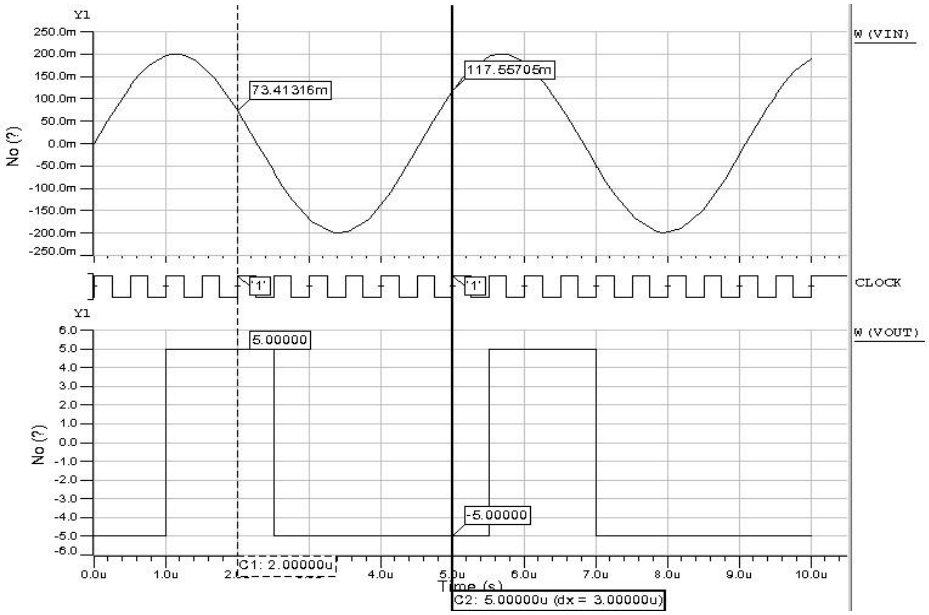
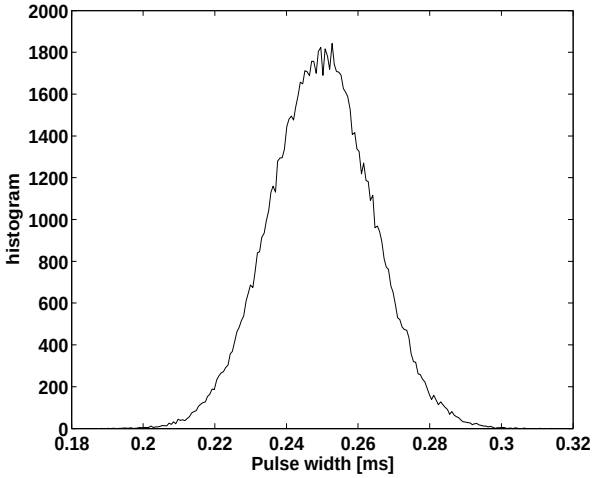


Figure 5.20: Architecture *comp1bitFD_behav2* fully-differential output ($w(vout) \equiv Voutp - Voutm[V]$) when driven by a fully-differential sine wave ($w(vin) \equiv Vinp - Vinm[V]$) where $Voutp$ (*Voutm*) and $Vinp$ (*Vinm*) are the positive and negative outputs and inputs, respectively. $offset = 100\ mV$, $hyst = 100\ mV$, $up\_val = 2.5$ and $down\_val = -2.5$. clock is the triggering clock.

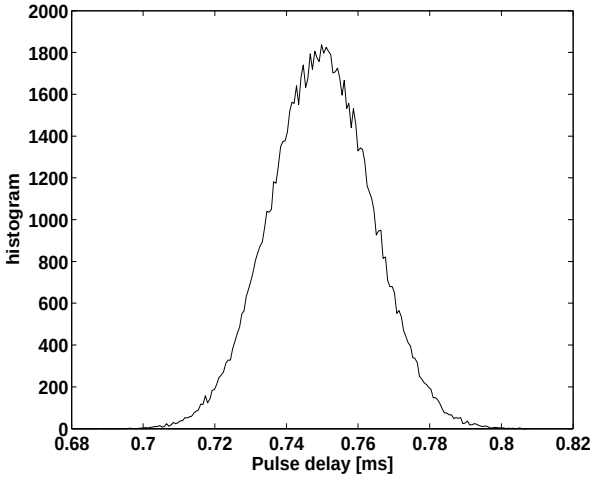
5.4.5 Clock

The clock is a crucial block in any mixed-signal circuit. The clock pulse is described by its period (generic *period*) and duty cycle (generic *tau*). Apart from an ideal clock, straightforward modeled, we develop an architecture *jitter* (Listing 5.9) to emulate a clock with uncertainties on the sampling instant (i.e. the sampling jitter).

The time uncertainties are modeled through the gaussian random variable generator *gaussSIG* (section 5.4.3). The clock used in mixed-signal circuits generally exhibits limited accumulative jitter, i.e. the sampling instants uncertainties build up with time only up to a certain level. The clock generators are indeed usually implemented by phase-locked loops (PLL), which limits the accumulation of the jitter. The model then resynchronizes the jittered clock with a jitter-free clock at each sampling instants by mean of two supplementary variables *synchro_td* and *synchro_tw*. The model is able to generate a clock with uncertainties on the pulse delay or on the pulse width, as these two types of jitter have different effects in a continuous-time modulator (chapter 6). In order to verify the behavior of the model, we perform two transient simulations of a clock emulated by the architecture *jitter* with $tau = 0.25$ and $period = 1\ ms$. First, $jitter\_width$ is set to $1e-5$ and $jitter\_delay$ to 0 (i.e. constant pulse delay) and then, $jitter\_delay$ is set to 10^{-5} and $jitter\_width$ to 0 (i.e. constant pulse width). The analysis of the histograms of the clock pulses widths and delays (Fig. 5.21) gives, in the first case and for the pulse width, a mean value (μ) of 0.25 *ms* and a standard deviation (σ) of 1.42×10^{-5} while for the second experiment and for the pulse delay, $\mu = 0.75\ ms$ and $\sigma = 1.41 \times 10^{-5}$, indicating the correct behavior of our model.



(a)



(b)

Figure 5.21: Histogram of 100000 **simulation points for the pulsewidth (a) and pulsedelay (b) jitter vs. time for a clock emulated with architecture *jitter*.** $tau = 0.25$ **and** $Fsamp = 1\ kHz$**.** $jitter\_width$ **(**$jitter\_delay$**)** $= 5.0e-12\ (0.0)$ **and** $0.0\ (5.0e-12)$**, for the (a) and (b) cases, respectively.**

Listing 5.9: VHDL-AMS code of the architecture describing a clock generator with non-accumulative jitter. The procedure *gaussSIG* generates a gaussian distributed random variable (section 5.4.3) and function *real2time* converts an object of type real into an object of type time with the same value.

```
architecture jitter of Clock is
 constant tw : time := real2time(period)*tau;          -- pulsewidth
 constant td : time := real2time(period)*(1.0-tau);    -- pulsedelay
 signal Sclock_loc : bit := '1'; -- local copy of the output signal
begin
 pulse : process is
    variable init1 : integer := seed1;
    variable init2 : integer := seed2;
    variable jit_delay, jit_width : real := 0.0;    -- jitter
    variable td_jitter : time := td;    -- jittered pulsedelay
    variable tw_jitter : time := tw;    -- jittered pulsewidth
    variable synchro_td : time := 0 ns; -- td jitter at prev. clk cycle
    variable synchro_tw : time := 0 ns; -- tw jitter at prev. clk cycle
 begin
  if Sclock_loc = '0' then
    gaussSIG(jitter_delay,init1,init2,jit_delay);
    td_jitter := td + real2time(jit_delay)-synchro_td;
    Sclock_loc <= '1' after td_jitter;
    synchro_td := real2time(jit_delay);
  else
    gaussSIG(jitter_width,init1,init2,jit_width);
    tw_jitter := tw + real2time(jit_width)-synchro_tw;
    Sclock_loc <= '0' after tw_jitter;
    synchro_tw := real2time(jit_width);
  end if;
    Sclock <= Sclock_loc;
    wait on Sclock_loc;
 end process pulse;
end architecture jitter;
```

5.4.6 Integrator: behavioral and structural descriptions

In order to study the transfer function level of the ΔΣ, we also developed models of the integrators described by their transfer function using signal-flow syntax. Although port quantities would be appropriate for this kind of modeling syntax, we define the fully-differential inputs and outputs as four terminals of nature electrical: *Tinp*, *Tinm*, *Toutp* and *Toutm* (Listing 5.10). This way, it is compatible with the other analog cells models and allow us to use the VHDL-AMS potential for the simulation of different levels of abstraction.

At this abstraction level, the integrator is described as a voltage source characterized by a s-domain transfer function. The transfer function may be modified to describe the influence of the amplifier finite gain and finite bandwidth (Tab. 5.3).

The different transfer functions are described using the VHDL-AMS *Q'dot* implicit quantity defined as $Q'dot \equiv Q.s \equiv \frac{dQ}{dt}$ where Q is an arbitrary quantity, s is the Laplace quantity and t is the time (Listing 5.11 for the case of the finite amplifier gain).

Additionally, for time-domain simulations, the output voltage is limited to the supply rails using the same construction with which we limit the current in the OTA model of section 5.4.2. The three different architectures implementing the transfer functions of Tab. 5.3 are benchmarked in an AC simulation with $gain\_int = 2.0e6\ Hz$, $gain\_ampli =$

Listing 5.10: VHDL-AMS code of the entity describing the behavior of a fully-differential active RC integrator.

```
entity integFDsyst is
 generic (gain_int : real := 2.0e6;    -- Integrator gain [/s]
          gain_ampli : real := 4.0e2; -- Amplifier gain [-]
          fp_ampli : real := 1.0e9;   -- Amplifier dominant pole [Hz]
          vdd : real := 2.5;          -- Positive supply voltage [V]
          vss : real := -2.5          -- Negative supply voltage [V]
          );
 port(terminal Tinp, Tinm, Toutp, Toutm : electrical);
end entity integFDsyst;
```

Table 5.3: Different s-domain active RC integrator transfer functions and related amplifier imperfections. A_{int} is the integrator gain, Av and wp are, respectively, the gain and dominant pole ($[rad/s]$) of the amplifier around which the integrator is constructed.

Amplifier imperfection	Integrator transfer function
-	$\frac{A_{int}}{s}$
Amplifier finite gain	$\frac{A_{int}Av}{A_{int}+(1+Av)s}$
Amplifier finite bandwidth	$\frac{A_{int}Av\ wp}{A_{int}wp+(wp(1+Av)+A_{int})s+A_{int}wp}$

40 and $fp\_ampli = 100.0\ MHz$. The simulated gain pole frequencies and gain magnitude values indeed correspond to the values predicted by the transfer functions of Tab. 5.3 (Fig. 5.22).

A structural description of the integrators can evidently be realized by connecting the OTA model of section 5.4.2 with capacitors and resistors. Non-linearities of the resistors and capacitors can be modeled very easily by the techniques used in the OTA model for the *gm* and *gd* non-linearities. The resistor noise can be added by combining the description of a resistor with the white noise source of section 5.4.3. Examples of application of this model will be presented in section 6.

5.5 Conclusion

In this chapter, behavioral models of analog cells have been developed and detailed. Moreover, our models are design-oriented as the influence of the environment is taken implicitly into account. All the parameters of the models are quantities on which the designer can act like the bias current and contrarily to the load capacitance for example. The models are detailed enough to be efficiently compared with transistor-level simulations. They are thus a tool to make the link between the analog cells and the mixed-signal circuit. As our application target is a continuous-time modulator and contrarily to existing models, our models include VHDL-AMS entities taking the noise and distortion into account.

Listing 5.11: VHDL-AMS code of the architecture emulating a fully-differential active RC integrator with a finite amplifier gain. For time-domain simulations, the output voltage is limited to the supply rails. For the sake of simplicity, we only represent the positive branch of the fully-differential outputs

```
library Disciplines; use Disciplines.electromagnetic_system.all;
library IEEE;use IEEE.math_real.all;

architecture behavAvVout of integFDsyst is
        -- Branch quantities
          -- Inputs
        quantity Vindm across Tinp to Tinm;
          -- Outputs
        quantity Voutp across Ioutp through Toutp;
        [...]
        -- Free quantities
        quantity Voutp_loc : real;
        [...]
        -- Constants
        constant alpha : real := gain_int*gain_ampli;
        constant beta : real := 1.0+gain_ampli;
        constant gamma : real := gain_int;
begin
        0.5*Vindm*alpha == Voutp_loc'dot*beta + Voutp_loc*gamma;
        [...]
        -- Output Stage
        if (DOMAIN = TIME_DOMAIN) use
                if Voutp_loc'above(vdd) use
                        Voutp == vdd;
                elsif not(Voutp_loc'above(vss)) use
                        Voutp == vss;
                else
                        Voutp == Voutp_loc;
                end use;
                [...]
        else
                Voutp == Voutp_loc;
                [...]
        end use;
end architecture behavAvVout;
```

The VHDL-AMS models of this chapter are an efficient link between the analog cells and the mixed-signal circuit (Fig. 1.4). Critical blocks can be better identified using their specification-power trade-offs. Moreover, they can be used to start the design of the test setup earlier in the design flow by providing a common description for the design and test engineers. It would reduce both the cost and design delays.

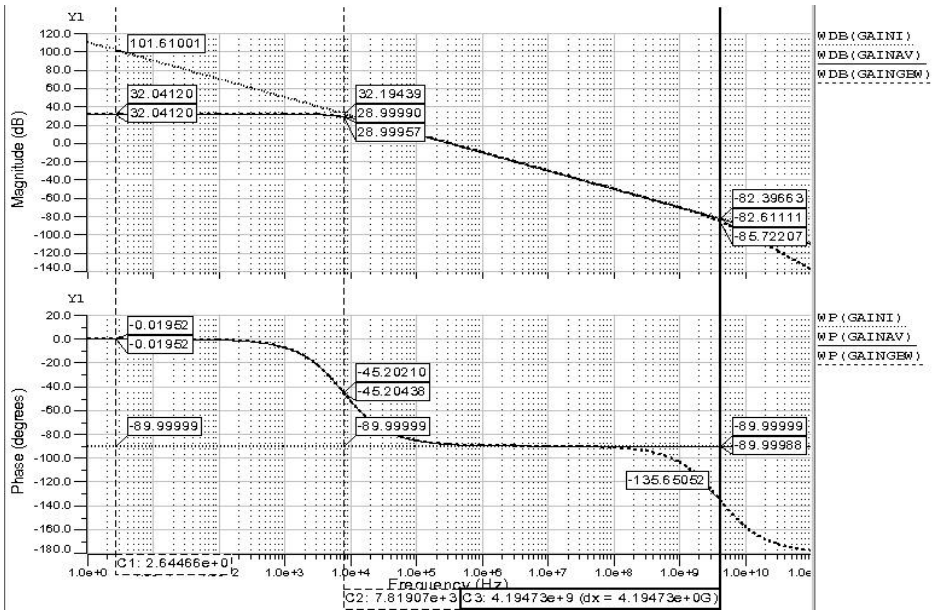


Figure 5.22: Magnitude $[dB]$ **(up) and phase** $[\circ]$ **(down) for** $GAINI$**,** $GAINAV$ **and** $GAINGBW$**.** $GAINI \equiv \frac{Voutp-Voutm}{Vinp-Vinm}$ **for the ideal integrator,** $GAINAV$ **and** $GAINBW$ **are defined in the same way but for the amplifier with finite gain and bandwidth, respectively.** $gain\_int = 2.0e6$**,** $gain\_ampli = 40$ **and** $fp\_ampli = 100.0e6$**.**

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Part III

Design case

Chapter 6

Continuous-time ΔΣ A/D converter

As announced in chapter 1, we show how the VHDL-AMS models of chapter 5 can be used in the case of a continuous-time (CT) ΔΣ analog-to-digital converter (ADC). We focus on the modulator, the mixed-mode part of the ADC (Fig. 6.1) and on the following specifications: medium resolution (14-16 bits) and a low signal bandwidth ($\approx 10\ kHz$).

The ΔΣ CT modulators have a great potential to digitize analog signals at high temperature and low power consumption for such signal specifications. It justifies their use as test vehicle. We derive a design optimization methodology to possibly integrate the CT ΔΣ modulator in the improved analog design flow presented in chapter 7.

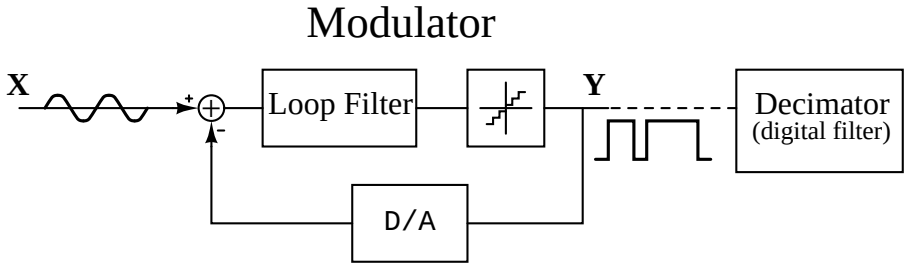


Figure 6.1: A ΔΣ analog-to-digital converter is the series combination of a mixed-signal modulator and of a digital filter, the decimator. The modulator is composed of an analog loop filter, an internal analog-to-digital converter and a feedback digital-to-analog converter.

We first introduce the ΔΣ modulators and the associated terminology in section 6.1. Based on the current state-of-the-art, we justify our interest for a third order continuous-time ΔΣ modulators in the case of our specifications (section 6.2) and for operation at high temperature (section 6.3). We also review the imperfections of the continuous-time ΔΣ modulators known in the literature (section 6.2). The continuous-time ΔΣ modulators are based on continuous-time integrators for which different topologies exist: $gm-C$, $MOSFET-C$ and active RC with passive resistors. Using the results of our study of the distortion of MOSFETs in triode regime (chapter 3) and the state-of-the-art of continuous-time ΔΣ modulators targeting our specifications, we conclude that the active RC integra-

tors with passive resistors are the most appropriate in our case (section 6.4.6). After some considerations on the topology of the loop filter, we investigate more deeply the ΔΣ modulator sensitivity to the feedback digital-to-analog converter signal asymmetry (section 6.4.3) and clock jitter (section 6.4.4), its tolerance to the variation of the value of the passives (resistors, capacitors) (section 6.4.7.1) and the impact of the imperfections of the integrators (section 6.4.7.2 and 6.4.7.3). We propose an optimization method to design the active RC integrators with passive resistors (section 6.4.7.4) that could be included in the analog design flow (Chap. 7).

The VHDL-AMS analog cells models (Chap. 5) are used in this chapter to carry on the study. They support the design methodology of a continuous-time ΔΣ modulator and ensure the methodology can be inserted in an efficient analog design flow (Chap. 7). Existing behavioral models of continuous-time ΔΣ modulators [1][2] focus on the internal quantizer and feedback digital-to-analog converters (DAC) and describe them at a rather high level of abstraction. Our model, on the contrary, is design-oriented and detailed enough to be compared with transistor-level realizations and support the top-down design methodology.

6.1 Introduction to the ΔΣ modulators

Before going more into details we will define a number of terms concerning the ΔΣ modulator architectures. We will focus here only on low-pass architectures, referring the interested reader to [3] and [4] for further information on band-pass and high-pass architectures, respectively.

The ΔΣ ADC is composed by the series combination of a mixed-mode modulator and a digital filter called the decimator (Fig. 6.1). Any analog-to-digital conversion involves sampling of the analog signal. The minimal sampling frequency ($Fsamp$) is set by the Nyquist criterion: $Fsamp \geq 2.f_b$, where f_b is the signal bandwidth. In a ΔΣ ADC, the modulator $Fsamp$ is much higher than the Nyquist frequency by a factor called the **oversampling ratio** ($OSR = \frac{Fsamp}{2f_b}$). The decimator performs digital filtering and resampling of the signal. The modulator is composed of a loop-filter, an internal ADC or quantizer and a digital-to-analog converter (DAC), which feeds back the quantized output (Y in Fig. 6.1) to substract it from the input signal.

In the case of low-pass ΔΣ architectures, the loop filter has a low-pass characteristic with high gain in the signal frequency band and low gain outside this band. The feedback of the output to the input forces the average value of the quantized output to track the average input for the frequencies at which the loop filter has a high-gain [3]. If we describe the modulator using the linear model of Fig. 6.2, in which the quantization error is described as an independent random noise source E [5] we can write the output Y as

$$Y = \frac{H}{1+H}.X + \frac{1}{1+H}.E \quad (6.1)$$

$$Y \equiv \mathrm{STF}.X + \mathrm{NTF}.E \quad (6.2)$$

where X is the input signal and H is the loop filter transfer function. STF and NTF, the signal and noise transfer function respectively depend on H.

The oversampling spreads out the frequency spectrum to allow the shaping of the noise outside the frequency band by the loop filter (Fig. 6.3) while the signal is ideally

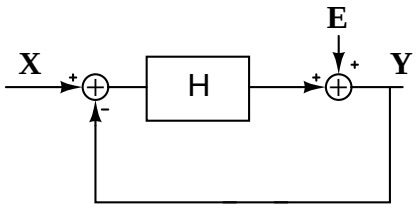


Figure 6.2: Linear model of a ΔΣ modulator, in which the 1-bit internal quantizer is modeled by a additive noise source. H is the loop filter transfer function.

left unmodified as the loop filter has high gain in the signal frequency band and low gain outside this band. The quantization noise will then be filtered out by the decimator.

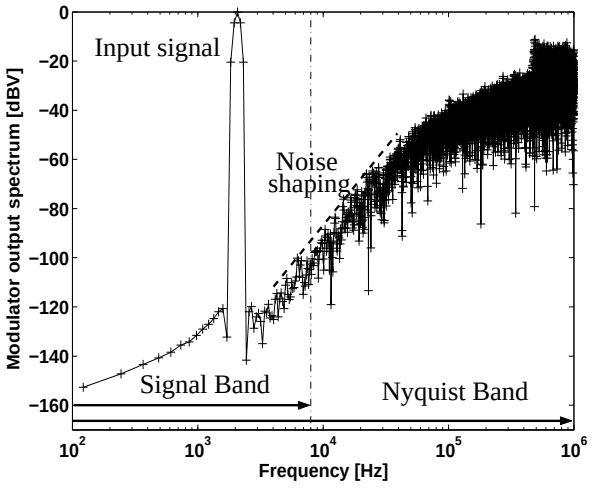


Figure 6.3: Spectrum of the modulator output $[dBV]$ vs. frequency [Hz] for a single-bit 3rd order modulator, with $OSR = 128$ and $F_{samp} = 2\ MHz$. A signal at $2.075\ kHz$ is applied at the modulator input.

The slope of the noise shaping spectrum (Fig. 6.3) is related to the order of the filter by slope $=$ filter order $* 20\ dB/dec$ (Fig. 6.3, 60 $[dB/dec]$ in this case). The loop filter order is also called the **order of the ΔΣ modulator**. The higher the ΔΣ order, the steeper the noise shaping and the higher the resolution at the price of a loss of stability. As the stability of the ΔΣ modulators, which are highly non-linear circuits, is a research topic in itself, we will not go further into details here. Further information can be found in [3], for example. In order to increase the ΔΣ order while maintaining the stability advantages of low-order modulators, the **cascade (or MASH) architectures** have been developed ([6], for example). In these architectures, low-order modulators are cascaded and their respective outputs are digitally combined to produce a final result corresponding to a modulator order roughly equal to the sum of the orders of the cascaded modulators.

"Non-cascaded" modulators are referred to as **single-loop topologies**. If the number of bits of the internal quantizer and of the feedback DACs as a consequence (Fig. 6.1) is higher than one, we talk about **multi-bit architectures**. Increasing the number of bits of the internal quantizer also increases the converter resolution but here at a price of DAC design complexity. Indeed, while 1-bit DACs are intrinsically linear, multi-bit DACs are not. They are moreover in the feedback loop and their resolution must match the resolution of the whole modulator. Digital techniques can however be applied to fulfill these objectives [7]. If the signal is sampled at the input of the modulator and the loop filter operates in the **discrete-time (DT)** domain (z-domain), the modulator is said to be a discrete-time modulator (Fig. 6.4 a) while, if the sampling only occurs at the internal quantizer and the loop filter is a continuous-time filter, we talk about **continuous-time (CT)** ΔΣ modulators (Fig. 6.4 b). While for DT architectures, all the signals inside the modulators are in discrete-time, the CT architectures are really mixed-signal (Fig. 6.4).

The resolution of a ΔΣ converter is usually specified in terms of signal to noise ratio (SNR), signal to noise and distortion ratio (SNDR), dynamic range (DR) at the input and DR at the output [5][7]. The **SNR** is measured at the output of the converter for a given converter input signal amplitude and is the ratio of the signal power to the noise power, containing both quantization noise due to the finite length of the digital coded data and extra random noise due to the converter imperfections. The **SNDR** is also measured at the output and corresponds to a certain input signal amplitude and is the ratio of the signal power to the power of the noise and distortion components. The **DR** can be specified at the output or at the input of the converter. When measured at the input, it is the ratio between the power of the largest input signal that can be treated by the converter without jeopardizing the converter resolution and the power of the smallest detectable input signal. The DR at the output is the ratio between the maximum and minimum output power. All these figures-of-merit are expressed using dB as units or in terms of *number of bits*. The two are linked by

$$\#\,\text{bits} = \frac{DR_{dB} - 1.76}{6.02} \tag{6.3}$$

6.2 Potentials and challenges of continuous-time ΔΣ modulators

Continuous-time ΔΣ are first known for their advantages concerning the digitalization of fast analog signals, i.e. signal bandwidth equal to $\approx 10\ MHz$ or more, and are popular for telecom applications [8] [9] [10]. They also offer advantages concerning low-power operation for applications with lower signal bandwidths [11] comparable to our specifications. In this section, we benchmark the CT and DT implementations of the ΔΣ modulator regarding the specifications under consideration in this thesis: resolution of $14\ldots16\ bits$, $f_b < 100\ kHz$ and low power consumption. We also present the state-of-the-art of CT ΔΣ and compare their performance.

6.2.1 Potential advantages

Here below, we summarize the main advantages of ΔΣ CT modulators known from the literature.

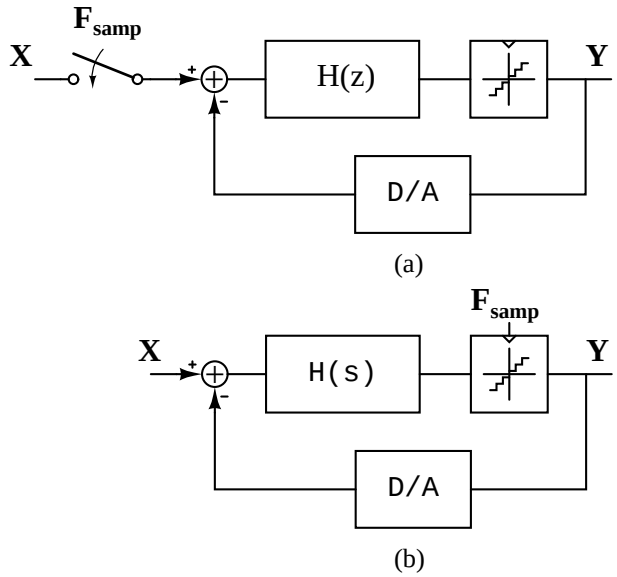


Figure 6.4: A discrete-time (DT) (a) and a continuous-time (CT) ΔΣ modulator. For simplicity, only the first place where sampling occurs is indicated. The DAC's (for both DT and CT), the DT loop filter and the internal ADC (DT) are also triggered by the sampling frequency $Fsamp$

• The absence of sampling switches in CT implementations presents major advantages for designs in nowadays and future deep sub-micron CMOS processes as the supply voltage is decreasing [12]. In conventional DT designs, special techniques like clock bootstrapping [13] or switched-opamp [14] must indeed be used to obtain satisfactory switches on-resistance ($Ron, switch$). The absence of sampling switches could also be an advantage concerning operation at high temperature as developed in section 6.3.

• As sampling of the input signal is moved to the quantizer (i.e. inside the loop)
(i) the sampling errors, possibly due to charge injection, clock feedthrough or switch non-linearity are shaped out of band like the noise of the quantizer [11];
(ii) the thermal noise aliasing occurring in the switched-capacitor integrators [15] also disappears.

• The CT loop filter strongly reduces out-of-band signals aliasing, thereby relaxing the specifications of the anti-alias filter in front of the ΔΣ, or even replacing it [16].

• In DT implementations, the errors associated to the integrator output voltage settling impose the amplifiers' GBW to be $2 \ldots 5$ times higher than the sampling frequency, leading to high bias currents. This constraint on amplifier GBW is less severe for CT implementations, in which $GBW = 1 \ \ldots \ 2 * F_{samp}$ [17]. It results in power savings in the CT integrators. Further power savings can be achieved at the system level as the specifications on the anti-alias filter are strongly relaxed in the case of CT ΔΣ implementations.

• Finally, the CT implementations appear as a very good candidate for further integration in larger mixed-mode systems as they were reported to be less sensitive to the asynchronous interferences coming from the substrate [18]. In CT implementations the signal is indeed processed during the whole sampling period contrarily to the DT case in which the signal is processed mainly at the beginning of the clock cycle; the asynchronous

interferences are averaged and have less influence.

6.2.2 Design challenges

Some difficulties must however be overcome during the design of CT ΔΣ modulators.

- The CT circuitry indeed shows more process variations.
- The intrinsic delay of the feedback signals leads to a less stable modulator [19]. This excess loop delay is defined as the non-zero time between the entry of the signal into the quantizer and the stabilization of the corresponding DAC output. If the excess loop delay becomes too large, it will eventually increase the modulator order and stability issues will rise, depending on the resolution of the internal quantizer, on the loop filter order and on the *OSR* of the modulator. The problems associated to this excess loop delay can be solved at the architectural level by an additional feedback loop around the quantizer [20] [10] or by selecting a return-to-zero (RTZ) coding type for the feedback DACs [21].
- The CT implementations are moreover well-known to be more sensitive to clock jitter than their DT counterparts.
- The DAC output voltage waveforms shape can also have an impact on the modulator resolution [16][22]. This can be understood as in the DT case, most of the feedback signal power is transferred at the beginning of the clock cycle while in CT, the feedback power is transferred at a constant rate during the whole DAC pulse duty cycle.
- Finally, the first amplifier is directly connected to the input signal which imposes that its linearity must correspond to the converter resolution [17].

We will further come back in more details on these aspects in section 6.4 devoted to the ΔΣ design issues. All the above cited pros and cons are summarized in Tab. 6.1.

Table 6.1: Summary of the pros and cons of CT vs. DT implementations of ΔΣ modulators.

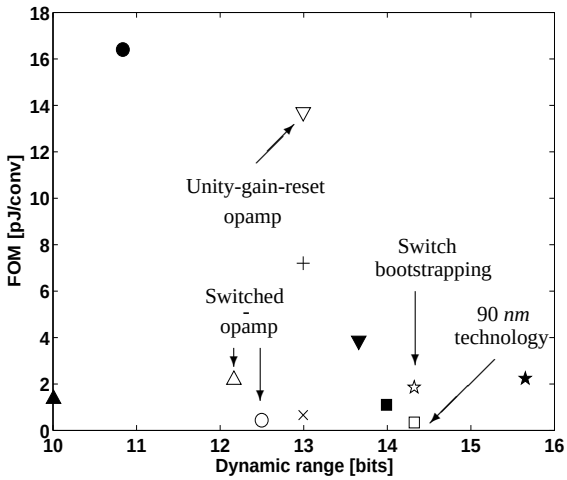
	Discrete-time	**Continuous-time**
Sampling errors	Critical	shaped out of band
Settling errors	$GBW_{\text{ota}} \approx (2\ldots5) * F_{samp}$	$GBW_{\text{ota}} \approx (1\ldots2) * F_{samp}$
Finite comparator and DAC response time	almost no effect	less stability
DAC waveform	almost no effect	noise level increase and/or harmonic distortion introduced
DAC driving clock jitter	quite insensitive	sensitive
Low-voltage applications	quite inappropriate	appropriate
Sensitivity to asynchronous substrate noise	high	low
Constraints on amplifier linearity	low	high
Sensitivity to process variations	low	high

6.2.3 Benchmarking based on the state-of-the-art

In order to fairly compare the different modulators, we use the figure-of-merit (*FOM*) defined as [15]

$$FOM[pJ] = \frac{\text{Power consumption}}{2^{\text{resolution}} * f_b} \tag{6.4}$$

where *resolution* is the modulator resolution in number of bits. The FOM vs. dynamic range characteristic of the different published CT ΔΣ modulators with a signal bandwidth lower than $100kHz$ is plotted in Fig. 6.5 and Tab. 6.2 gives additional details on the modulators.



			FOM $[pJ/conv]$
+	[16]	CT	7.197
★	[18]	CT	2.230
■	[23]	CT	1.104
▼	[11]	CT	3.860
x	[24]	CT	0.661
▲	[25]	CT	1.361
●	[26]	CT	16.398
○	[14]	DT	0.432
⋆	[13]	DT	1.851
□	[27]	DT	0.341
▽	[28]	DT	13.703
△	[29]	DT	2.176

Figure 6.5: FOM [pJ/conv] vs. dynamic range [bits] of the published continuous-time (CT) and discrete-time (DT) ΔΣ modulators targeting low to medium signal bandwidth $(< 100\ kHz)$**. [30] (CT) is not present to improve graph readability (**$FOM = 102.93$ **[pJ/conv] for** $f_b = 72\ kHz$ **and** $DR = 8.66$ **[bits]).**

To assess the intrinsic potential of CT implementations vs. DT, we better consider DT implementations which do not use special techniques like the bootstrapping of the switches and implemented in comparable technologies. The benchmarking of the different published ΔΣ modulators indicates the benefit of the continuous-time implementations for moderate resolution ($14 \ldots 16$ *bits*) power-aware designs (Fig. 6.5). Indeed, the highest resolution is attained by [18] (★), which uses continuous-time circuitry. Moreover, among the three other modulators reaching a dynamic range superior to 14 bits [13] (⋆) [27] (□) [23] (x), the two DT implementations have a low power consumption thanks to clock bootstrapping [13] (⋆) or thanks to the use of a more advanced technology [27] (□) which offers a low power supply in combination with a low threshold voltage.

The benchmarking of published CT and DT ΔΣ realizations (Fig. 6.5 and Tab. 6.2) confirms the potential of the continuous-time implementations for power-aware low-frequency and moderate resolution ($14 \ldots 16$ *bits*) modulators as it was first pointed out for different parameters in Tab. 6.1.

6.3 A/D converters at high temperature

The resolution vs. temperature characteristics of published [31] [32] [33] [34] modulators for high temperature and of the one commercially available [35] are plotted in Fig. 6.6 and the corresponding signal bandwidth (f_b), oversampling ratio (OSR) and modulator order are gathered in Tab. 6.3 As power consumption was not reported in most of the designs, we are unable to fairly compare the realizations from a power consumption point-of-view.

Table 6.2: Additional parameters of the published $\Delta\Sigma$ modulators targeting low to medium signal bandwidth $(< 100\,kHz)$. All discrete-time (DT) implementations are using switched-capacitor (SC) techniques.

ADC	DT/CT	Implementation technique	OSR [-]	modulator order	technology
[16]	CT	$gm-C$	64	4	0.5 μm CMOS bulk
[18]	CT	RC, $gm-C$	128	4	0.5 μm CMOS bulk
[23]	CT	RC, $gm-C$	64	4	0.35 μm CMOS bulk
[11]	CT	$gm-C$, current-mode	128	3	0.18 μm CMOS bulk
[24]	CT	RC	48	3	0.5 μm CMOS bulk
[25]	CT	RC	32	3	0.5 μm CMOS bulk
[26]	CT	RC	195	3	0.35 μm CMOS bulk
[30]	CT	$gm-C$	128	1	2.0 μm CMOS bulk
[14]	DT	SC-switched-opamp	48	3	0.5 μm CMOS bulk
[13]	DT	SC-switch bootstrapping	100	3	0.35 μm CMOS bulk
[27]	DT	SC	100	3	0.09 μm CMOS bulk
[28]	DT	unity-gain-reset opamp	256	2	0.35 μm CMOS bulk
[29]	DT	SC-switched-opamp	64	2	0.18 μm CMOS bulk

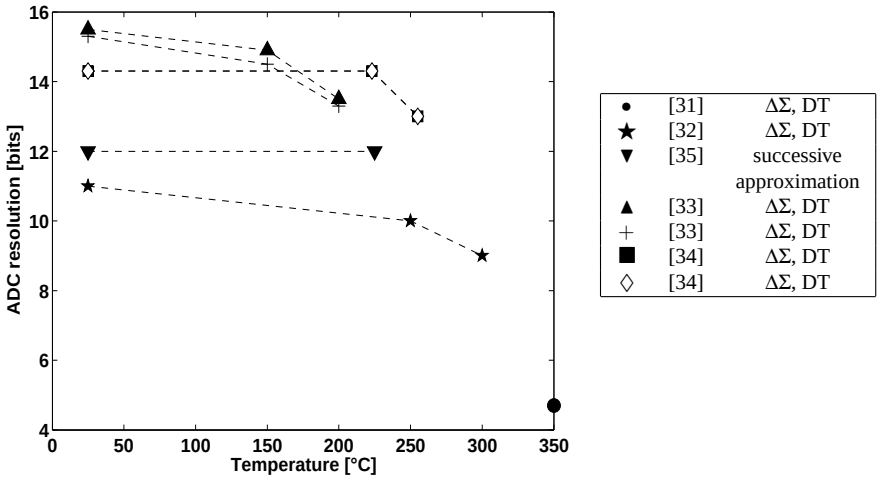


Figure 6.6: Resolution [bits] vs. Temperature [$^{\circ}C$] of the different published or commercially available ADC's targeting high temperature operation

Except for [35] (▼), which is a converter based on successive-approximation techniques, all ADC's are discrete-time $\Delta\Sigma$ modulators implemented by switched-capacitor techniques. The modulator orders range from one [31] (•) to four [33] (▲), two modulators use cascaded topologies [33] (▲) [34] (◊) while the others are single-loop $\Delta\Sigma$.

The technologies used for the different designs are 2 μm fully-depleted (FD) silicon-on-insulator (SOI) [31] (•) [32] (★), 0.35μm partially-depleted (PD) SOI [35] (▼), 0.5μm FD silicon-on-sapphire (SOS) [33](▲ and $+$) and 1.5μm bulk CMOS [34] (■ and ◊). Single-loop architectures seem to better perform over temperature than cascade modulators, which suffer from increased circuit impairment at high temperature [34]. Resolutions of 15.3 *bits* at room temperature, 14.9 *bits* at 150$^{\circ}C$ and 9 *bit* at 300$^{\circ}C$ are attained at best. For each converter, the resolution suddenly drops with a higher rate above a certain limit temperature. As pointed out in [34], the resolution droop above 220$^{\circ}C$ of [34] is caused

Table 6.3: Additional parameters of the published or commercially available ADC's targeting high-temperature operation and based on a ΔΣ architecture with a discrete-time implementation using switched-capacitor techniques.

ADC	f_b [kHz]	OSR [-]	modulator order	technology
[31] (•)	0.39	128	1	2μm FD SOI
[32] (★)	7.81	64	2	2μm FD SOI
[33] (+)	1.00	256	2	0.5μm SOS
[33] (▲)	1.00	256	4 (2-2 MASH)	0.5μm SOS
[34] (■)	0.50	256	2	1.5μm Bulk
[34] (◇)	0.50	256	3 (2-1 MASH)	1.5μm Bulk

by the increase of leakage current in the amplifier common-mode feedback. We believe that the leakage current increase in the MOS switches at high temperature could be the reason of the other converters resolution droop, as will be discussed here below.

In discrete-time ΔΣ, the loop filter is composed of switched-capacitor integrators, usually designed in fully-differential topologies for increased robustness and improved signal dynamics (Fig. 6.7).

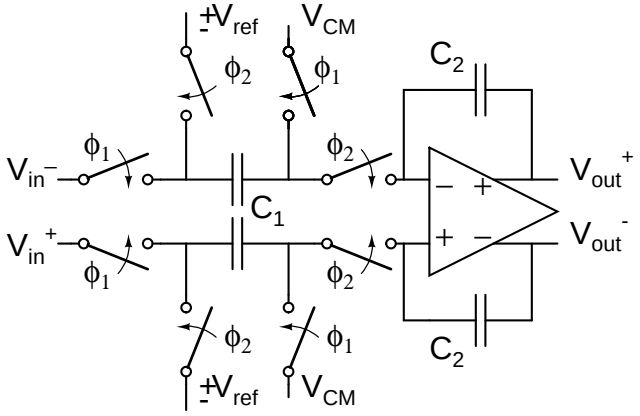


Figure 6.7: Fully-differential switched-capacitor integrator. ϕ_1 and ϕ_2 are non-overlapping clocks. V_{in}^+ and V_{in}^- (V_{out}^+ and V_{out}^-) are the fully-differential inputs (outputs). V_{ref} is the feedback DAC output voltage and V_{CM} is the common-mode voltage.

During the first clock phase ϕ_1, the input voltage (*Vin*) is sampled on the capacitors C_1 and, during the second clock phase ϕ_2, the difference $Vin - Vref$ is transferred on the integrating capacitor C_2, $Vref$ being the feedback DAC output voltage. The switches are usually implemented as transmission gates for increased signal dynamics (Fig. 6.8).

Leakage currents are known to be the most limiting parameter in transmission gates at high temperature [36]. Their temperature dependence depends on the technology as the underlying physical phenomena differ from one technology type to the other. The physical leakage current (*Ileak*) indeed originates from reverse-biased diodes in the MOSFETs. *Ileak* is caused by two different physical junction phenomena: 1) generation mechanisms in the depletion region of the junctions (*Ileak* proportional to the intrinsic carrier concentration (*ni*) and to the volume of the depleted junctions) and 2) diffusion mechanisms in the undepleted part of the silicon film ($Ileak \propto ni^2$). In FD SOI, as the film is fully

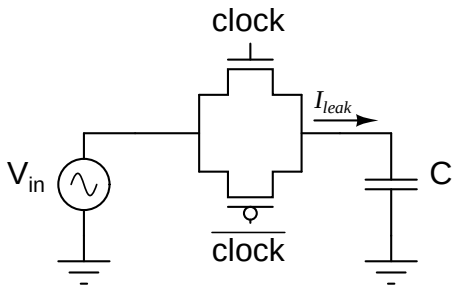


Figure 6.8: Transmission gate composed of a n-type and a p-type MOSFET's. n-type is driven by the clock signal (clock) and the p-type by its logic complement ($\overline{clock}$). I_{leak} is the total leakage currents originating from the n and p-type MOSFETs.

depleted, only generations mechanisms take place and then $Ileak$ is proportional to ni and to the depletion region volume (i.e. $W.L.t_{si}$, where W and L are the device width and length, respectively and t_{si} is the silicon film thickness, equal to the depletion width). In bulk or PD SOI, $Ileak$ is usually first dominated by generation mechanisms and then by diffusion mechanisms (above $150°C$, generally). Note that, in advanced deep-submicron technologies, the relative importance of these mechanisms may be different [37] (see Appendix A). These differences between bulk and PD SOI on one hand, and FD SOI on the other hand generally imply a much lower value of $Ileak$ in FD SOI.

If we consider the case of a transmission gate driven by a voltage source and charging/discharging a capacitor (Fig. 6.8) during the hold phase (i.e. switch open), the net leakage current of the pMOSFET and nMOSFET will, accordingly to its sign, charge or discharge the capacitor and will cause the voltage across the capacitor to ramp or drop. Note that using FD SOI MOSFETs and depending on the relative voltage values, we may still see the weak inversion current and not the physical leakage current, whose value may be very low [38]. This charging/discharging phenomenon is negligible at room temperature as the total leakage currents ($Ileak$) is small. But with increasing temperature, $Ileak$ increases and may cause the switched-capacitor integrator to stop working properly as the stored value on C_1 will not correspond anymore to Vin (Fig. 6.7) [36]. Note that this phenomenon can be mitigated using minimum-size switches [34]. If the leakage current to the transistor bulk is dominant, the use of fully-differential topologies [39] can also improve the situation. Above a given temperature depending on the temperature dependence of $Ileak$ and hence depending on the technology, the voltage increase or decrease is however thought to be too big for the solutions proposed above. The only remaining solution is then to increase the sampling frequency in order to decrease the hold time and, accordingly, the voltage droop accordingly. On the other hand, to work properly, DT $\Delta\Sigma$ impose the gain-bandwidth product (GBW) of the amplifier in the integrator to be higher than $K * Fsamp$ where $K = 2 \ldots 5$ [15]. The reachable GBW is however limited by the technology and by the design, facing a speed/resolution tradeoff [36], limiting to our meaning, the resolution of DT $\Delta\Sigma$ at high temperature. It would also explain why the temperature at which the resolution drops is higher for FD SOI design than for others (Fig. 6.6).

To check the validity of this assumption, we compared the measured nMOSFET and pMOSFET leakage currents in the $0.5\ \mu m$ FD SOS and $2\ \mu m$ FD SOI technologies, corre-

sponding respectively to the designs of [33] and [32]. We consider that the total leakage current $Ileak$ is given by $IleakN + IleakP$ as, due to the presence of the insulating layer in the considered technologies, there is no leakage to the bulk. We focus on these two designs as we dispose of measured data in the case of these two technologies. We extract $IleakN + IleakP$ for minimum length and 20 μm wide MOSFETs at the temperature corresponding to the higher rate droop of the converter resolution: $150°C$ for the SOS case and at $250°C$ for the SOI case. In the SOS case, we have $IleakN + IleakP = 1.096\ nA$ for a drain voltage $V_D = 1\ V$ at $150°C$ and in the SOI case, $IleakN + IleakP = 5.599\ nA$ for $V_D = 2\ V$ at $250°C$. In both cases, $V_S = 0\ V$ and V_G is chosen such that the extracted current is in the plateau. These extractions are however performed at different V_D and $Ileak$ depends on the drain voltage: $Ileak \propto \sqrt{V_D}$ if the generation mechanisms in the junction are dominant and $Ileak \propto \exp(V_D)$ if the diffusion from the undepleted part of the body dominates [40]. The considered SOI devices at $250°C$ are nearly fully-depleted [41], i.e. in a transition state between full and partial depletion. It is then difficult to determine which phenomenon (diffusion or generation) dominates in this case. To compare the SOI and SOS cases at same $V_D = 1\ V$, we start from the value at $V_D = 2\ V$ for SOI. We compute the expected $IleakN + IleakP$ in the SOI devices at $V_D = 1\ V$ either considering diffusion (i.e. $Ileak \propto \exp(V_D)$) which gives an estimation of 2.060 nA, or considering generation (i.e. $Ileak \propto \sqrt{V_D}$) which gives an estimation of 3.959 nA. As the considered SOI devices are, at $250°C$, in a transition state between full and partial depletion, we expect that $IleakN + IleakP$ in these SOI devices lies between these two values at $V_D = 1\ V$, 2.060 nA and 3.959 nA. The values of the total leakage current $IleakN + IleakP$ at same $V_D = 1\ V$ in the two different technologies have similar values at the temperature at which the converter resolution starts to drop at a higher rate. The droop of resolution can thus possibly be linked to the increase of the leakage current in the switches. Continuous-time ΔΣ modulators are then a good candidate for digitizing analog signals at high temperature as no switch is present in these implementations.

6.4 Design considerations for continous-time ΔΣ modulators

In the next sections, we review with more detail the design challenges of the continuous-time ΔΣ modulators pointed out in section 6.2. Each of the design challenges is assessed by simulations using the VHDL-AMS models of chapter 5. It shows that using these models we can go through the entire design flow in a single simulation environment (the VHDL-AMS simulator) and hence, make it more efficient; we come back in full details on this last subject in chapter 7.

We briefly deal with the trade-offs of the loop filter implementation and with its stability. The choice for return-to-zero (RTZ) codes for the DAC output waveforms in place of non-return-to-zero (NRTZ) is justified and specifications for the jitter of the clock are derived in that case. The sensitivity of the modulator performance on the comparator imperfections is only briefly reviewed as they are less important. Based on the state-of-the-art of continuous-time ΔΣ modulators targeting $14 \ldots 16\ bits$ of resolution for a signal bandwidth smaller than 100 kHz and on the results of chapter 3, we show that active RC integrators with passive resistors and capacitors are the right choice concerning the implementation of the loop filter for our specifications. For that particular integrator im-

plementation, the imperfections of the amplifiers as well as the mismatch of the passive elements are assessed and an design optimization methodology is derived. We finally deal with the implementation of the feedback DACs in the case of active RC integrators with passive resistors and capacitors.

A third-order continuous-time ΔΣ modulator with an internal quantization of 1 *bit* will be used as example to evaluate the effects of all these imperfections. The loop filter is in our particular case stabilized by feedback as will be justified below (Fig. 6.9). We choose to study a third-order ΔΣ as it seems to be a good trade-off between resolution of $14\ldots16$ *bits* or higher and reasonable design complexity (Tab. 6.2). A single-bit internal quantization is chosen for the same design complexity reasons. The remaining specifications of the modulator are: $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$.

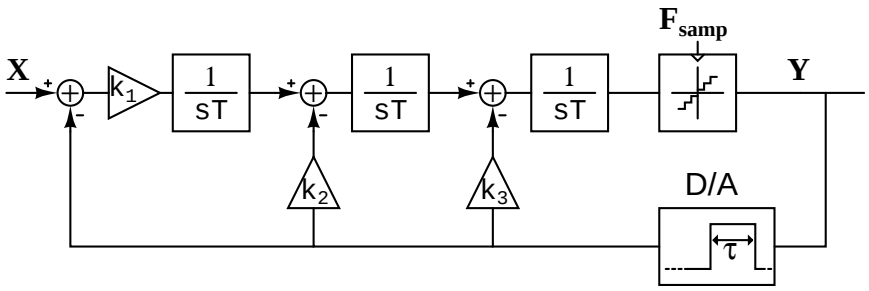


Figure 6.9: 3rd order CT ΔΣ modulator stabilized by feedback. $k1$, $k2$ and $k3$ are the loop filter coefficients

As the main purpose of this CT modulator is to be a test vehicle of the VHDL-AMS models (Chap.5) in a top-down design methodology (Chap. 7), we will not go into too much details, pointing out the key issues and where there is room for improvement.

6.4.1 Loop filter topology: feedback vs. feedforward

We chose to stabilize the loop filter by feedback (Fig. 6.9) as it is expected to be more robust than a corresponding loop filter stabilized by feedforward compensation [17]. An other benefit of feedback topologies is an improved performance of the ΔΣ intrinsic anti-alias filter [17] and hence a lower power consumption if we consider the power consumption of both the ΔΣ modulator and anti-alias filter. In a n^{th} order feedback compensated loop filter (Fig. 6.9, in the particular case of $n = 3$), the signal transfer function (STF) has indeed generally n poles, yielding a n^{th} order low-pass anti-alias filter [17]. On the other hand, the STF of a feedforward compensated loop filter (Fig. 6.10, in the particular case of $n = 3$) is only a 1^{st} order low-pass as it has n poles and $n-1$ zeros.

In feedback compensated topologies, the gain of the first loop filter integrator has to be small in order to keep the output signal swing within the supply range. As a result, the higher-order integrator imperfections will have more impact on the modulator performance and the corresponding amplifiers may not be scaled down. It may then result in a higher power consumption, especially for low oversampling ratios [17]. There is thus a possible trade-off between the power consumption reduction obtained by relaxing the

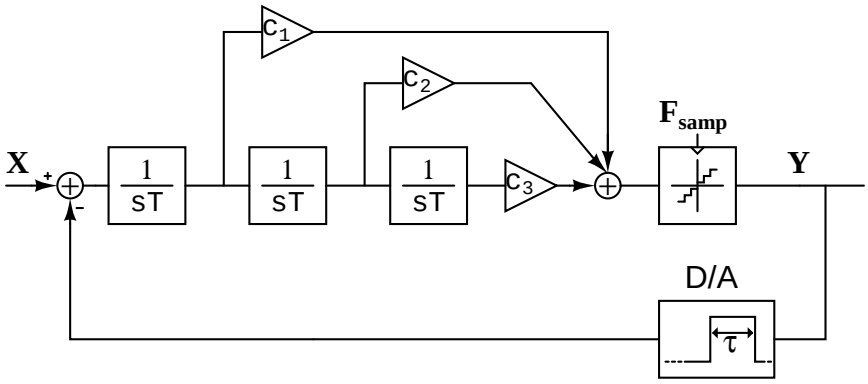


Figure 6.10: 3rd order CT ΔΣ modulator stabilized by feedforward compensation. $c1$**,** $c2$ **and** $c3$ **are the loop filter coefficients**

specifications on the anti-alias filter and the power consumption increase due to the higher contribution of higher order integrator imperfections.

There is room for improvement of the modulator efficiency at this level for example by adding local feedforward or feedback loops [3] [17] but, as it is not the main purpose of our study of the ΔΣ modulator, we will not go further into details.

6.4.2 Stability: sizing of the loop filter

The stability of the modulator is ensured by the proper sizing of the loop filter coefficients ($k1$, $k2$ and $k3$ in Fig. 6.9). These coefficients are determined by simulations. For DT modulators, dedicated tools exist [42]. The CT modulator loop filter coefficients can be determined by first computing an equivalent discrete-time loop filter. The loop filter coefficients for the DT equivalent filter are then determined. Finally, the CT coefficients are obtained by mapping the coefficients of the two equivalent filters [43] [44]. Alternatively, the loop filter can be sized by studying the loop filter stability directly in the time-domain [17]. We use the first approach, finding the discrete-time loop filter coefficients using the Schreier's toolbox [42] and further mapping them to the CT implementation using the modified Z-transform [44]. The DT equivalent loop filter transfer function depends on the coding of the DAC waveform: return-to-zero (RTZ) (Fig. 6.11), non-return-to-zero (NRTZ),.... In our case, we use RTZ codes as will be argumented in section 6.4.3. The coefficients for a third-order loop filter stabilized by feedback with the DAC output voltage coded as RTZ pulses with a pulse duty cycle (Fig. 6.11) of $\frac{3}{4}T_{samp}$ (Fig. 6.11) are presented in Table 6.4.

The third-order ΔΣ continuous-time modulator stabilized by feedback (Fig. 6.9) using the loop filter coefficients of Table 6.4 is simulated for different input signal amplitudes using the VHDL-AMS models of chapter 5. The DAC output waveform is a RTZ pulse with a duty cycle of $\frac{3Tsamp}{4}$ (Fig. 6.11). The integrators are described by a s-domain transfer function emulating an ideal integrator and all other components are ideal. We perform a time-domain simulation for different input signal amplitudes ranging from $-70\ dBFS$ (i.e. dB relative to the comparator input full-scale) to $0\ dBFS$. The signal-to-noise ratio

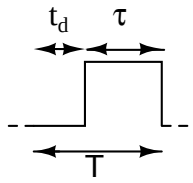


Figure 6.11: Generic feedback DAC return-to-zero pulse (RTZ). T is the sampling period, t_d is the pulse delay and τ is the pulse width or duty cycle.

Table 6.4: Coefficients for a 3rd-order loop filter stabilized by feedback with all poles at zero for a discrete-time implementation using [42] and for a continuous-time implementation by applying the modified z-transform [45]. The indexing of the loop filter coefficients refers to Fig. 6.9

Loop filter coefficient	**Discrete-time**	**Continuous-time** RTZ pulse - $\tau = 0.75$
$k1$	0.0138	0.0184
$k2$	0.1273	0.1535
$k3$	0.5217	0.6363

(SNR) corresponding to each input signal amplitude (*Ain*) is extracted by a 2^{14}-points Fast-Fourier Transform (FFT) of the output data stream of the modulator and represented vs. *Ain* in Fig. 6.12. For *Ain* larger than $-6.43\ dBFS$, the quantizer is overloaded and the modulator is hence unstable

The maximum SNR (SNR_{max}) obtained by simulation is 101.26 dB corresponding to an input signal amplitude of $-6.43\ dBFS$ (Fig. 6.12). A dynamic range (DR) of 103.6 dB is obtained by extrapolation of the SNR vs. Ain characteristic. As the SNR vs. Ain characteristic saturates for an *Ain* of $-6.43\ dBFS$ corresponding to 48 % of the comparator full-scale, the implemented loop filter is very stable [3]. A higher *SNR* could be obtained by selecting another set of loop filter coefficients corresponding to a higher NTF out-of-band gain at the expense of a loss of stability [3].

6.4.3 Coding of the digital-to-analog converter output waveform

As announced above, the actual coding (return-to-zero (RTZ), non-return-to-zero (NRTZ)) of the DAC output waveform matters in CT ΔΣ designs. Apart from its influence on the sizing of the loop filter coefficients (section 6.4.2), the RTZ coding of the DAC output voltage has also

(1) a **positive effect** on the **excess loop delay** as already discussed (section 6.2);

(2) a **negative effect** on the sensitivity of the modulator performance to the **jitter** of the clock driving the DACs [46] as will be explained in section 6.4.4;

(3) a **positive influence** on the modulator sensitivity on the **asymmetries of the DAC waveform** as detailled below.

Let us take a generic NRTZ DAC waveform (Fig. 6.13) exhibiting non-zero and possibly different rise and fall times (t_{rise} and t_{fall}), causing the waveform to be asymmetrical. At the integrator inputs (Fig. 6.9), the power of the DAC output waveform is substracted from the input signal power and yields the quantization error. It is crucial to the ΔΣ princi-

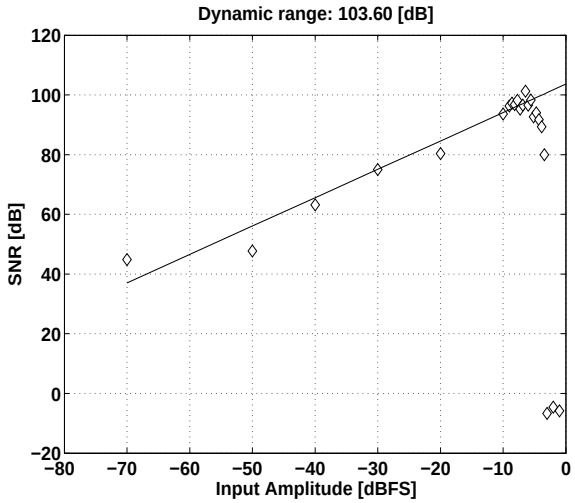


Figure 6.12: Signal-to-noise ratio (SNR) $[dB]$ **vs. input signal amplitude (Ain)** $[dBFS]$ **for the 3rd order CT** $\Delta\Sigma$ **with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit,** $Fsamp = 2\,MHz$**,** $\mathbf{OSR} = 128$ **and hence** $fb = 7.8\,kHz$**. Each point corresponds to a VHDL-AMS simulation of the modulator using a behavioral description of the integrators. The dynamic range (DR) is obtained by extrapolation. A** $-6.43\,dBFS$ **input signal amplitude corresponds to the maximum SNR of** $101.26\,dB$**. The SNR is extracted by a** 2^{14} **points FFT of the output data stream.**

ple. The actual shape of the waveform influences the estimation of the quantization error and hence, the modulator performance (i) on one hand due to different t_{rise} and t_{fall} and (ii) on another hand due to the non-zero t_{rise} and t_{fall}.

In the case of **different pulse rise and fall times**, the integrated area of a DAC output pulse corresponding to a $'1'$ DAC digital input is different from the one corresponding to a $'0'$ input (Fig. 6.13). The power transmitted to the loop filter by the DAC (i.e. the integrated pulse area) during the sequence $'1010'$ will then be different than in the $'1100'$ sequence, although they include the same number of $'1'$ and $'0'$ and hence should feed the same power back into the loop filter. The transmitted power depends on the DAC input signal, generating harmonic distortion. This effect is usually referred to as inter-symbol interference (ISI) or memory effect [47] [16] [11]. The positive effect of RTZ codes for the DAC in the case of asymmetrical t_{rise} and t_{fall} is quite straightforward as the waveforms are reseted to a zero level during each clock signal and the pulse integrated area is then equal for a $'1'$ and for a $'0'$. However, fully-differential codes also relax the DAC waveform symmetry requirements as the waveforms are in this case intrinsically symmetrical, except for the mismatch between the positive and negative signal paths. Fully-differential non-return-to-zero codes could then be sufficient but require steep waveforms and careful design and layout [47] possibly leading to higher power consumption. On the other hand, RTZ codes intrinsically compensate for ISI [11][22], making it a power-conscious solution and confirming the benefit of using RTZ codes in this context.

In the case of **non-zero pulse rise and fall times**, the DAC output pulse integrated area is smaller than the area corresponding to an ideal square DAC output pulse (Fig. 6.13). The power transmitted by the DAC is then accordingly reduced, increasing the relative input signal level of the modulator. Depending on the noise sources in a particular imple-

mentation, it can decrease the converter resolution by increasing the harmonic distortion if it is dominant or, alternatively, decrease the maximum input signal level at which the modulator is stable without decreasing the corresponding maximum resolution. The two effects may be modeled in a very efficient way in the case of a $1-bit$ DAC by replacing the DAC by a series combination of a gain stage and a DC-level shift [22]. The use of RTZ codes does not improve the robustness of the modulator to non-zero pulse rise and fall times but their use is largely justified by the benefits concerning ISI.

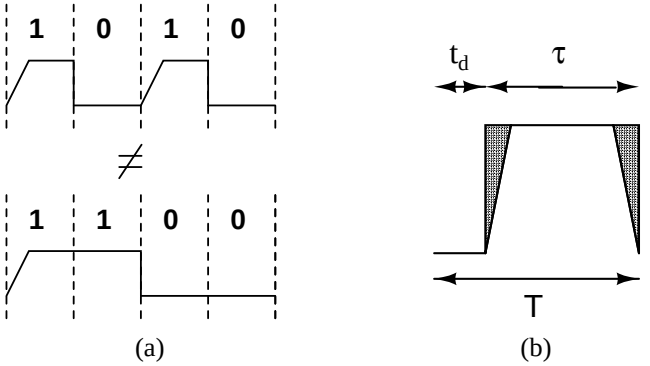


Figure 6.13: DAC waveform imperfections: (a) unequal rise and fall times of a non-return-to-zero pulse generate ISI and (b) finite settling time reduces the energy transmitted to the loop filter by the DAC.

6.4.4 Sensitivity to clock jitter

The CT ΔΣ modulators are well-known to be very sensitive to jitter on the clock driving the feedback DACs [46]. Intuitively, the reason is that, in continuous-time designs, the feedback signal is integrated continuously during the whole period and an error on the sampling instant yields a large error in the power fed back into the loop filter by the DAC. On the contrary, in switched-capacitor DT implementations, most of the power is transmitted at the beginning of the clock cycle after the triggering pulse; an error on the sampling instant yields only a small error as the majority of the power has already been transmitted.

On the other hand, jitter on the comparator clock has a relatively small influence as the related errors are shaped out-of-band by the loop filter similarly as what is happening in a DT implementation.

The RTZ coding of the DAC output waveform moreover increases the sensitivity of the modulator to jitter. By definition, a RTZ code returns to zero at each clock period and hence involves more transition in the DAC output voltage than in the non-return-to-zero case.

Using a RTZ feedback DAC, we can distinguish different jitter mechanisms (Fig. 6.14): the pulse-width jitter denotes the random variations of the width of the clock pulse (constant t_d) while the pulse-delay jitter describes the random variations of the clock pulse delay (constant τ).

The modulators are rather insensitive to the pulse delay jitter as it does not influence the amount of power transmitted by the DAC to the loop filter because of the constant

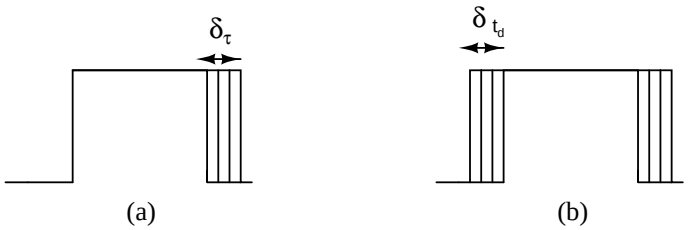


Figure 6.14: Different jitter mechanisms in a return-to-zero DAC pulse: (a) pulse width jitter (constant t_d) and (b) pulse delay jitter (constant τ).

pulse width [11][48]. We simulated the influence of pulse width jitter for the 1-bit feedback compensated third-order CT modulator (Fig. 6.9) with ideal integrators emulated by their s-domain transfer function and ideal comparator and DACs, all described using the models of chapter 5. As expected, the CT ΔΣ modulator imposes as expected (Fig. 6.15) severe constraints on the pulse-width jitter, requiring a clock generator with a pulse width jitter lower than 0.004 % of the sampling period (i.e. 20.67 *ps*) following our simulations. These are quite tough constraints for the phase-locked loop which generates the clock. Published designs however report the same constraints on the phase-locked loops ensuring the feasibility of such clock generators [49] [9].

6.4.5 Sensitivity to the quantizer imperfections

Due to the position of the quantizer in the loop, the modulator performance is quite insensitive to the quantizer imperfections as they are suppressed by the gain of the integrators. As in our case we use a single bit quantizer, it is implemented by a comparator. A typical comparator [24] exhibits offset, hysteresis and non-zero response delay. All these imperfections are implemented in the corresponding VHDL-AMS models (Chap. 5), which can then be used to set the specifications on the comparator. The non-zero delay of the comparator causes the *loop delay* which can lead to instability but can be adressed at the transfer function level (section 6.2). We do not go more into details here as it is not dominant at all.

6.4.6 Which implementation for the integrators: gm-C, MOSFET-C or active RC with passive resistors ?

In this section, we move one step further towards the implementation and we refine the obtained modulator behavioral description of Fig. 6.9 by discussing the integrator implementation. The integrators can indeed be implemented using different known continuous-time filters implementations: $gm-C$, $MOSFET-C$ and active *RC* with passive capacitors and resistors. To elect the best option, we use the state-of-the-art of CT ΔΣ modulators targeting a resolution of $14-16$ bits and $fb < 100kHz$. We identify the integrator linearity as the key performance parameter and show how it influences the performance of the modulator. We finally benchmark the different implementations and show that active *RC* with

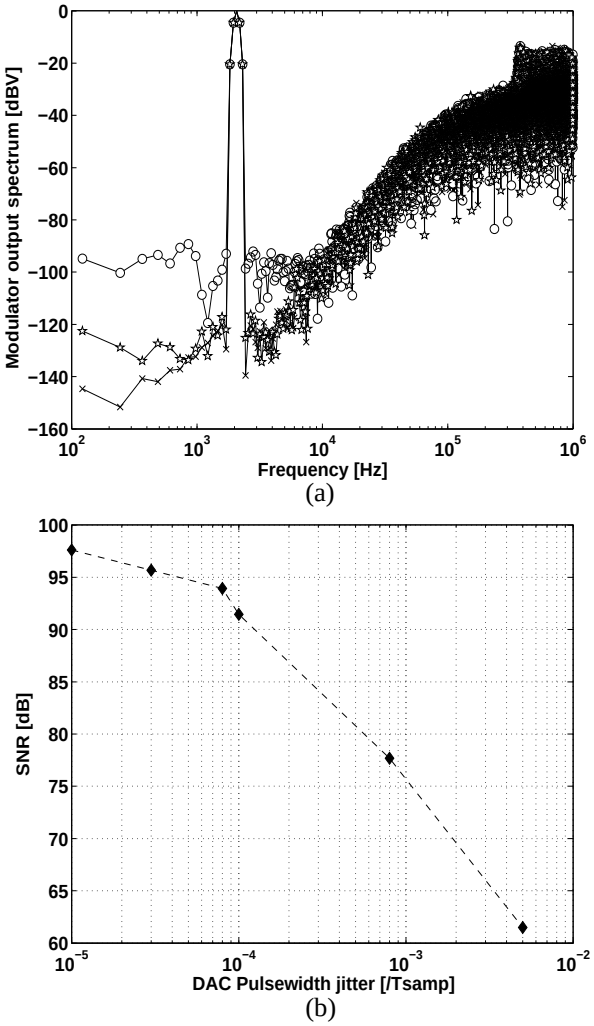


Figure 6.15: DAC pulsewidth jitter effect on the performance of the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4 and with the integrators implemented as transfer function. (a) Normalized magnitude of the ΔΣ modulator output $[dBV]$ vs. frequency $[Hz]$ for a pulsewidth jitter of $0s$ (×) $200\ ps$ (○) and $5\ ps$ (⋆) and (b) SNR evolution vs. pulsewidth jitter $[s]$. Spectrum obtained by an FFT on 2^{14} points, $F_{samp} = 2\ MHz$ and input signal frequency $Fin = 2.075\ kHz$.

passive capacitors and resistors is the best option for our specifications ($Fsamp = 2\ MHz$, OSR $= 128$ and $14-16$ bits of resolution).

Looking again at the different published CT ΔΣ modulators focusing on $f_b < 100kHz$ (Fig. 6.16), we identify the best candidate for high dynamic range as the active *RC* implementation, at least for the first integrator of the loop filter. The modulators in [16] and [18] are based on the same architecture and only differ in the implementation of the first integrator: $gm-C$ in [16] and active *RC* with passive resistors in [18]. The increase in the dynamic range between [16] and [18] is due to the better linearity of the passive *RC*-type integrator as explained hereafter (Tab. 6.1).

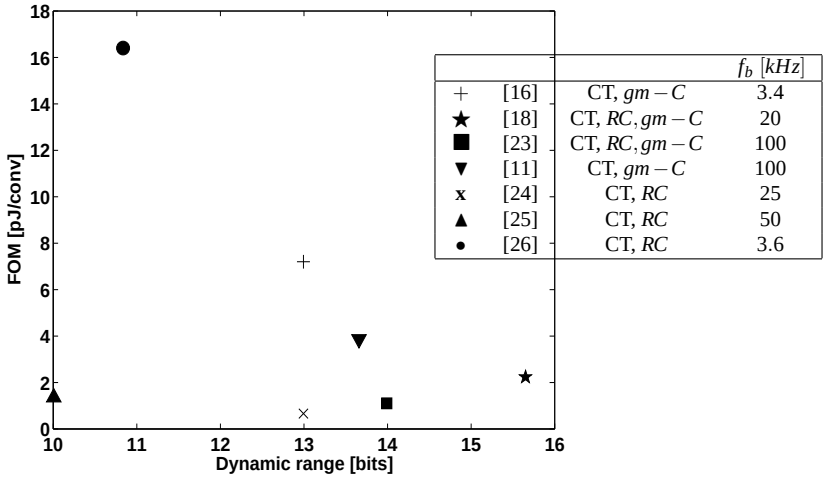


Figure 6.16: FOM [pJ/conv] vs. dynamic range [bits] of the published continuous-time (CT) ΔΣ modulators targeting low to medium signal bandwidth $(< 100\ kHz)$**. [30] is not present to improve graph readability (**$FOM = 102.93$ **[pJ/conv] for** $f_b = 72\ kHz$ **and** $DR = 8.66$ **[bits]).**

The sensitivity on the first integrator linearity seems surprising as the integrator is located in the forward path of a feedback system and as the linearity of such systems is supposed to be dominated by the linearity of the feedback path provided that the forward path has a sufficiently high gain. The usual behavioral representation of CT ΔΣ (Fig. 6.9) is actually misleading as the first amplifier influences the summing point of the input and feedback signals and can be seen as a voltage-to-current (V/I) converter. A close-up of the modulator input is represented in Fig. 6.17 for both a $gm-C$ and an active *RC* first integrator. In the case of the $gm-C$ implementation, the OTA is clearly outside the loop and its linearity influences the current, which is further processed by the ΔΣ modulator. The amplifier of the active *RC* integrator is inside the loop (i.e. after Σ, the summing point) but its linearity influences the behavior of Σ and hence the V/I conversion performed by the resistors *Rin* and *Rdac* (Fig. 6.17). Moreover, in a continuous-time ΔΣ the gain of the forward path is not infinite and in our case of $1-$bit internal quantization the feedback DAC is intrinsically linear further increasing the sensitivity of the modulator to the first integrator linearity.

The poor linearity of $gm-C$ integrators is well-known and they are mainly used in ΔΣ modulators for low resolution and high speed telecommunication applications. The

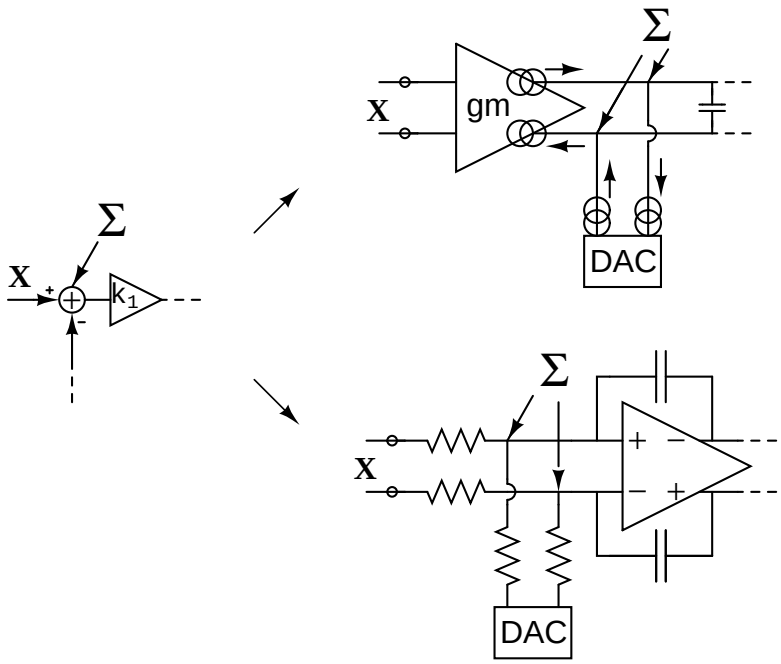


Figure 6.17: Position in the loop of the amplifier of the first integrator in the case of a $gm-C$ type (up) and active RC (down) implementation of the integrators. Σ refers to the summing point as represented in the $\Delta\Sigma$ loop schematics of Fig. 6.9 or Fig. 6.10

$MOSFET-C$ is very attractive as it would be tunable on-chip. The linearity of well-designed $MOSFET-C$ integrators is given by the linearity of the MOSFET in triode used to emulate the resistance. In chapter 3, the linearity of such MOSFETs is thoroughly analyzed and based on measured characteristics, it is shown that the best third order harmonic distortion (HD3) reachable under practical design conditions is $-60\ dB$. As in the CT $\Delta\Sigma$ modulator, the circuits are implemented using fully-differential techniques for improved robustness and dynamic range, the HD3 determines the linearity performance. The best resolution we could reach with $MOSFET-C$ integrators is $-60\ dB$; although this value is valid only in the particular case of the technology of chapter 3, it can be used as an indicator for other technologies and the 60 dB are too far from our specifications. Active RC implementations with passive resistors and capacitors in nowadays deep-submicron technologies offer the required combination of speed and linearity (Fig. 6.16). The influence of the poor accuracy of the integrated capacitors and resistors, drawback of active RC integrators is assessed in section 6.4.7.1. Subsequent integrators may be implemented using $gm-C$ techniques in order to lower the power consumption for the requirements on their linearity performance are reduced. For simplicity reasons, we decide to implement the whole loop filter as active RC integrators with passive resistors (Fig. 6.18). The resistors and capacitors are sized according to the loop filter coefficients and integrator gains. RC products determine the integrator gains and each ratio of the resistances $\frac{R_{in,j}}{R_{dac,j}}$ sets the corresponding loop filter coefficient k_j. We come back in more details on that in section 6.4.7.

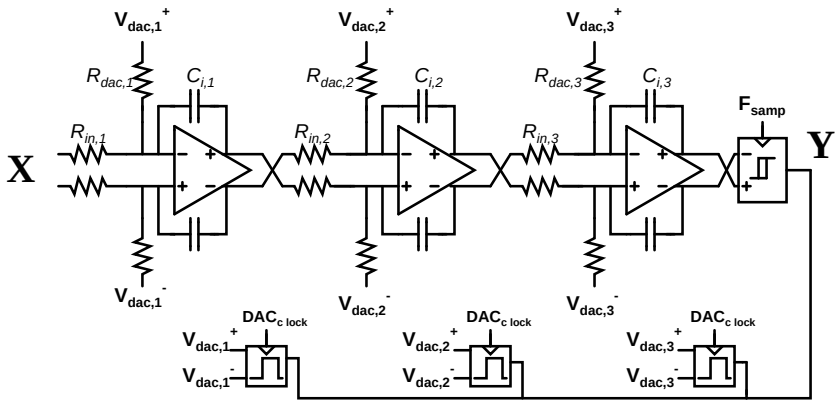


Figure 6.18: 3rd order CT ΔΣ modulator stabilized by feedback and implemented using active RC integrators.

The third-order modulator (Fig. 6.9) with all integrators implemented as active *RC* (Fig. 6.18) can be simulated by our VHDL-AMS models using a structural description for the integrators. The loop filter coefficients are the ones of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$.

The corresponding *SNR* vs. input signal amplitude (*Ain*) characteristic is represented in Fig. 6.19. Each SNR point is obtained by a 2^{14}-points fast-fourier transform (FFT) of the modulator output data stream. The amplifiers are described as operational amplifiers with a sufficiently high gain to be considered as infinite. The resistors, capacitors, comparator and feedback DACs are, in this case, described using ideal behavioral models. The resistances and capacitances are chosen to adequately implement the loop filter coefficients and integrator gains, we come back on the sizing of these elements in the next section devoted to the design methodology. The SNR vs. *Ain* characteristic exhibit a SNR_{max} of 89.31 dB corresponding to an input signal amplitude of $-8.14\ dBFS$. Compared to the results obtained with the behavioral description (Fig. 6.12), it is a performance loss of about 10 dB. As we focus here on the design methodology and on the tools, which support it, we will not go deeper into details. We however think that the resistances ($R_{\text{in,i}}$ and $R_{\text{dac,i}}$ in Fig. 6.18) have to be more finely tuned to implement more accurately the loop filter coefficients.

The linearity of the first integrator in the loop filter determines the resolution of the ΔΣ modulator. For our specifications ($Fsamp = 2\ MHz$, OSR $= 128$ and target resolution of $14-16\ bits$), only the active RC integrators with passive resistors can yield so low harmonic distortion.

6.4.7 Active RC integrator with passive resistors

In this section, we investigate in more detail the impact of the imperfections of active RC integrators with passive resistors and capacitors. In the following sections, we study

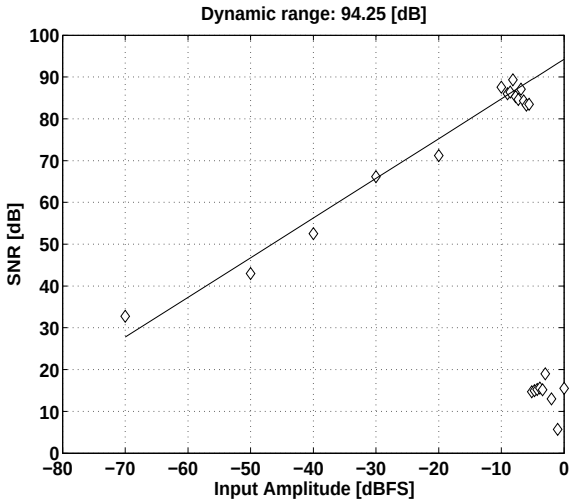


Figure 6.19: Signal-to-noise ratio (SNR) $[dB]$ vs. input signal amplitude (Ain) [dBFS] for the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$. Each point corresponds to a VHDL-AMS simulation of the modulator using a structural description of the active RC integrators (Fig. 6.18). The dynamic range (DR) is obtained by extrapolation. A $-8.14\ dBFS$ input signal amplitude corresponds to the maximum SNR of $89.31\ dB$. The SNR is extracted by a 2^{14} points FFT of the output data stream obtained by an input signal with a frequency $Fin = 2.075\ kHz$.

the influence of the integrated passives variations and determine the amplifier gain, gain-bandwidth product and slew-rate needed to correctly implement the loop filter. We focus more closely on the sizing of the first integrator as it is the most critical. We look at the integrator linearity and thermal noise along with the sizing of the resistances and capacitances. Based on this analysis, a design optimization methodology is presented. This methodology is derived to be implemented in an improved design flow of the integrators (Chap. 7) and is supported by our VHDL-AMS models. We also detail the implementation of the feedback DAC.

6.4.7.1 Mismatch of the passive elements

Passive elements implemented in CMOS processes usually exhibit large chip-to-chip variations for corresponding devices (ΔR, ΔC) but also mismatch from device to device inside the same chip (δR, δC). The implemented resistances or capacitances are then described by $R = R_{nom} + \Delta R + \delta R$ and $C = C_{nom} + \Delta C + \delta C$, where R_{nom} and C_{nom} correspond to the nominal value of the resistor and capacitor, respectively. The influence of the *local* mismatch of the passives is usually assessed separately by Monte-Carlo simulations. It should be interesting to include this mismatch in a top-down design methodology as was done in the current mirror case in section 4.5 but the strong non-linear operation of the ΔΣ modulator renders it particularly tough in this case. In a CT ΔΣ modulator using active RC with passive resistors and capacitors, the loop filter coefficients are set by a ratio of resistances (section 6.4.7.4). The coefficients should be rather resistant to variations of the process. Deeper investigation requires Monte-Carlo simulations, which are not

implemented in the tool yet.

Focusing on chip-to-chip variations (ΔR, ΔC), the integrator transfer function is then accordingly modified as [24]

$$H_{int}(s) = \frac{1}{sRC} \approx \frac{1}{sR_{nom}C_{nom}(1+\Delta RC)} \tag{6.5}$$

where ΔRC represents the combined influence of the variation of R and C and is given by

$$|\Delta RC| = \sqrt{(\Delta R)^2 + (\Delta C)^2}, \tag{6.6}$$

if we assume that ΔR and ΔC are not correlated. Considering a typical chip-to-chip variation of the resistance and capacitance of ± 10 %, ΔRC equals ± 14 %. Tuning of the RC time constant is needed to avoid costly in-factory trimming or calibration. If we moreover consider the operation at high temperature, tuning becomes unavoidable.

The behavioral simulations of the modulator for different integrator time constants nevertheless show that ΔRC values of ± 14 % can be afforded without problems (Fig. 6.20). The SNR vs. normalized *RC* time constant characteristic indicates that for decreasing RC product (i.e. increasing integrator gain) the SNR first improves and then suddenly drops due to stability problems (Fig. 6.20).

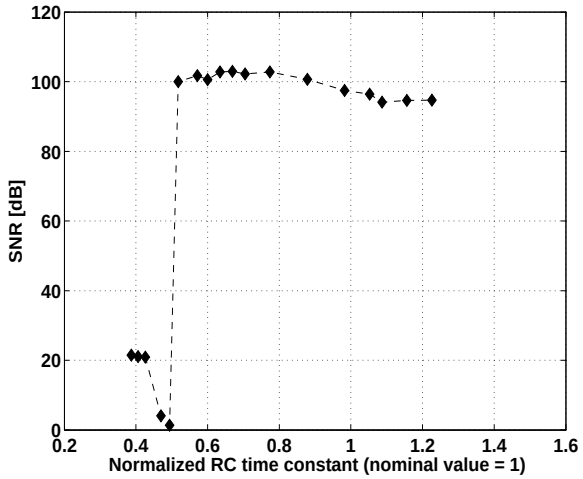


Figure 6.20: Signal-to-noise ratio (SNR) $[dB]$ vs. normalized RC time constants of the integrators $[-]$ for the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$. Each point corresponds to a VHDL-AMS simulation of the modulator using ideal integrators described by their Laplace-domain transfer function (Fig. 6.9). Spectrum obtained by an FFT on 2^{14} points for an input signal amplitude of $-6.45\ dBFS$ and frequency $Fin = 2.075\ kHz$ for each simulation.

In our particular case, some resolution could be won by repositioning the integrator time constant to for example $0.7 \times R_{nom}C_{nom}$ yielding still sufficient robustness against chip-to-chip *RC* variations. It may seem surprising that the computed loop filter coefficients (Tab. 6.4) do not yield an optimal modulator, i.e. maximum SNR corresponding to

a normalized RC time constant of 1. The loop filter coefficients are obtained by mapping the coefficients of a stable DT ΔΣ modulator to another discrete-time ΔΣ modulator equivalent to the CT (section 6.4.2). The DT equivalent is however not exactly identical to the CT ΔΣ modulator. Moreover, the loop filter coefficients of the stable DT ΔΣ modulator are the result of a trade-off between the aggressiveness of the NTF and the stability of the modulator. Finally, the CT-DT transformation and the computation of the loop filter coefficients both rely on the linear model (Fig. 6.2) of the modulator and single-bit loops are known to slightly deviate from this model unless the model of the comparator is refined [50]. The slightly non-optimal SNR for the nominal RC time constant may then be understood.

The quite low sensitivity of the modulator on the time constant variation however allow the use of cheap and rather simple discrete capacitor tuning (Fig. 6.21), in which the number of bits of the control word are determined according to the required precision on the RC time constant [51] [52] [53].

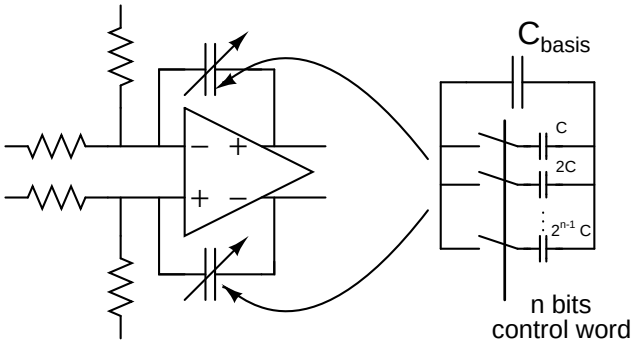


Figure 6.21: Discrete tuning of the capacitance for an active RC integrator. Algorithms to set up the n-bits control word can be found in [51][52][53]

Although mismatch on the passive resistors and capacitors may at first sight seem a big issue for active RC integrators with passive resistors and capacitors, we showed that the CT ΔΣ modulator tolerates mismatch levels compatible with actual technologies characteristics. Moreover, the loop filter can be adjusted to be more robust to these mismatches if needed. Efficient on-chip tuning can be performed by discrete-time tuning of the capacitance.

6.4.7.2 Amplifier finite gain and finite bandwidth

The finite gain (*Av*) and gain-bandwidth product (*GBW*) of the amplifiers implementing the integrators, introduce phase errors in the integrator transfer function. In order to minimize them, the amplifiers of the active RC integrators must have sufficient *Av* and sufficiently high *GBW*. The rather low sensitivity of the CT ΔΣ modulators on the amplifier gain [11][24] is confirmed by our simulations (Fig. 6.22). In the case of a behavioral description of the integrator, a gain of only 45 dB is indeed sufficient to minimize the associated errors. The steep increase of the CT ΔΣ SNR with the amplifier GBW [11][24] is also confirmed here (Fig. 6.23); as a *GBW* of approximately $2 \times Fsamp$ suffices to reach

an *SNR* of 3 *dB* below the ideal value. In these last simulations, *Av* is set to 300 and the amplifier pole is swept to yield the required *GBW* variation.

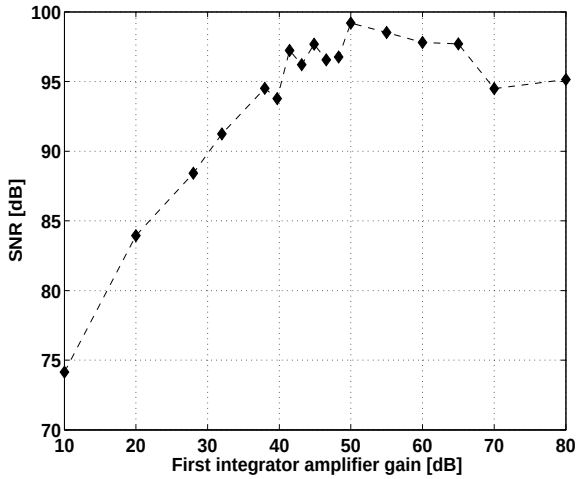


Figure 6.22: Signal-to-noise ratio (SNR) $[dB]$ vs. amplifier gain $[dB]$ of the first integrator for the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$. Each point corresponds to a VHDL-AMS simulation of the modulator using integrators described with the Laplace transfer function emulating the amplifier finite gain (Fig. 6.9). Spectrum obtained by an FFT on 2^{14} points for an input signal amplitude of $-6.45\ dBFS$ and frequency $Fin = 2.075\ kHz$ for each simulation.

6.4.7.3 Amplifier slew rate and limited output swing

The amplifier must track signals varying quite rapidly and there must be sufficient current to charge and discharge the integrating capacitors. The limit imposed by the implementation of the ΔΣ on the amplifier slew rate (*SR*) is assessed by the simulation of a modulator implemented by active *RC* integrators (Fig. 6.18), showing that a $SR = 6\ V/\mu s$ is sufficient to track the modulator signals. The corresponding minimal amplifier output current is 10.6 μm and was obtained by the simulation of the output current limited amplifiers.

The limited output swing of the amplifiers will also limit their capability to track the modulator signals. Moreover, as high level signal will be clipped to the maximum and minimum output voltage of the amplifier, the limited output swing will cause an increase of the noise level and introduce a high amount of harmonic distortion as can be seen in Fig. 6.25. For the supply ranges of $\pm 2.5V$ considered here, the amplifier maximum (minimum) output voltages must be lower (higher) than $2.2\ V$ ($-2.2\ V$). Note that these values correspond to the loop filter coefficient of Tab. 6.4. The amplifier output voltage levels may indeed be scaled to fit the amplifier performance [45]. As the level of the signals are in this case modified, the *SR* and output swing analysis must be of course reconsidered.

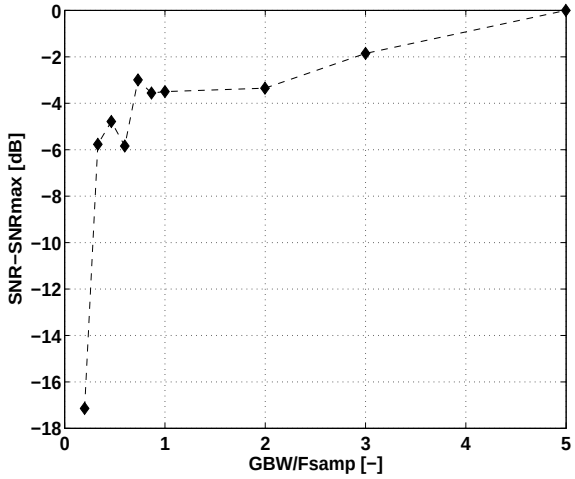


Figure 6.23: Signal-to-noise ratio (SNR) $[dB]$ vs. the gain-bandwidth to sampling frequency ratio ($GBW/Fsamp$, $[-]$) of the integrators for the 3rd order CT $\Delta\Sigma$ with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, $\mathbf{OSR} = 128$ and hence $fb = 7.8\ kHz$. Each point corresponds to a VHDL-AMS simulation of the modulator with the integrators described by their Laplace transfer function emulating the case of amplifiers with finite gain-bandwidth (Fig. 6.9). Spectrum obtained by an FFT on 2^{14} points for an input signal amplitude of $-6.45\ dBFS$ and frequency $Fin = 2.075\ kHz$ for each simulation. The integrators gain is set to 300 and $SNRmax$ corresponds to the SNR of a modulator with $Av = 300$ and infinite GBW.

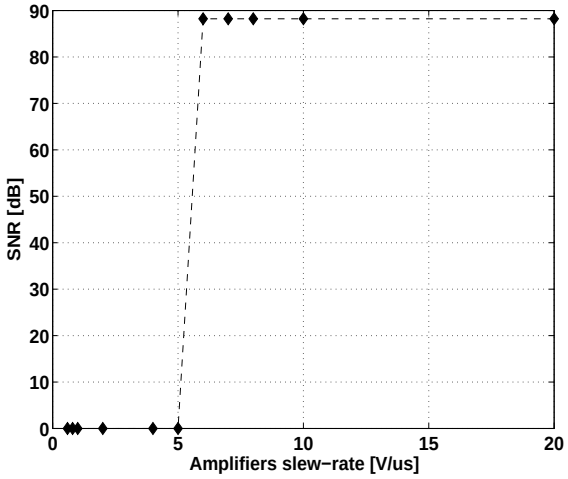


Figure 6.24: Signal-to-noise ratio (SNR) $[dB]$ vs. amplifier slew rate (SR) $[V/\mu s]$ for the 3rd order CT $\Delta\Sigma$ with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, $\mathbf{OSR} = 128$ and hence $fb = 7.8\ kHz$. Each point corresponds to a VHDL-AMS simulation of the modulator using an RC implementation of the integrators (Fig. 6.18), with SR limited amplifiers. Spectrum obtained by an FFT on 2^{14} points for an input signal amplitude of $-6.45\ dBFS$ and frequency $Fin = 2.075\ kHz$ for each simulation.

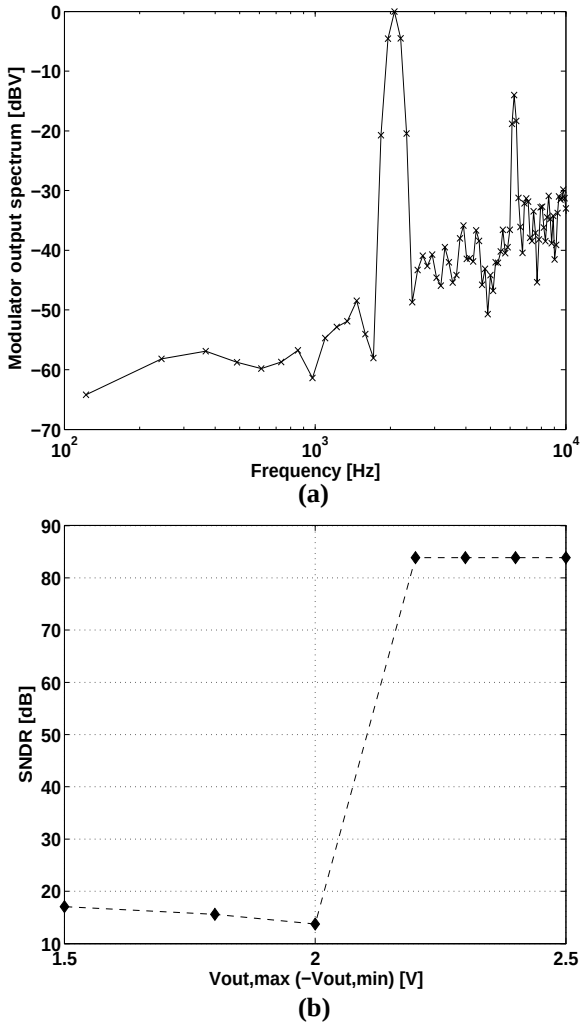


Figure 6.25: Effect of the amplifier output clipping on the resolution of the modulator or the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4. The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$. Each point corresponds to a VHDL-AMS simulation of the modulator using an RC implementation of the integrators (Fig. 6.18). (a) Normalized magnitude of the ΔΣ modulator output $[dBV]$ vs. frequency $[Hz]$ for a clipping level of $2\ V$ and (b) SNDR evolution vs. clipping level $[V]$. The modulator is Spectrum obtained by an FFT on 2^{14} points, $F_{samp} = 2\ MHz$ and input signal frequency $Fin = 2.075\ kHz$. $Ain = -8\ dBFS$

6.4.7.4 An optimization methodology for the design of active RC integrators, based on noise and linearity performance

Besides these limitations of ΔΣ modulators already implemented in other published behavioral models [1] [2] [48], the continuous-time implementations impose restrictions on the loop filter input-referred noise and on the integrator linearity as already explained. The errors related to high order integrators are reduced by the loop filter gain and the first stage will be the most critical. We focus in a first time on the first integrator and we use the VHDL-AMS models to support a design optimization methodology including noise and linearity while targeting minimal power consumption. The design optimization methodology to be included in an improved analog design flow (Chap. 7) is summarized in Fig. 6.26 and described here below.

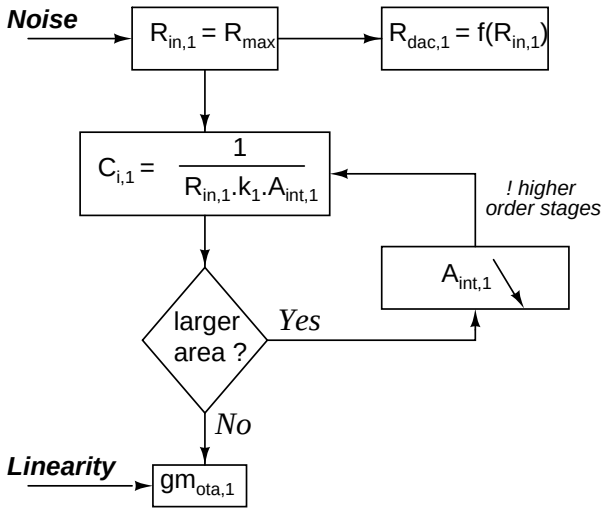


Figure 6.26: Design optimization methodology of the active RC integrators of a CT modulator supported by our VHDL-AMS models.

As sampling occurs inside the feedback loop, the **input-referred noise of the loop filter** and of the DAC are indeed directly added to the input signal (Fig. 6.18). In practical design cases, the thermal noise is the dominant error source [18]. The input-referred noise must be such that the target resolution is attained, i.e. $\frac{\text{Signal power}}{\text{Thermal noise power}} \geq SNR_{\text{target}}$ where SNR_{target} is the target converter resolution [17]. The total in-band input-referred noise $P_{noise,int}$ can be computed as [24]

$$\frac{P_{noise,int}}{8kT\,f_b} = R_{in,1} + \frac{R_{in,1}^2}{R_{dac,1}} + \frac{\kappa}{4g_m}\left(1 + \frac{R_{in,1}}{R_{dac,1}} + R_{in,1}C_{i,1}s\right)^2 \tag{6.7}$$

where $R_{in,1}$ and $R_{dac,1}$ are the resistances connected between the first amplifier and, respectively, the input signal and the DAC, $C_{i,1}$ is the first integrating capacitance, κ is the amplifier excess noise factor, k is the Boltzmann constant, T is the absolute temperature and gm is the amplifier transconductance. The noise of the OTA can usually be neglected

as its *gm* can be chosen large enough to provide an accurate enough virtual ground at its inputs. The $1/f$-noise of the amplifier can be neglected in a first approximation but must be included when fine tuning the design. In order to lower $P_{noise,int}$ we thus better choose low values for $R_{in,1}$ and $R_{dac,1}$. The increase of the noise floor by the white noise of the resistances is emulated by the VHDL-AMS models in Fig. 6.27

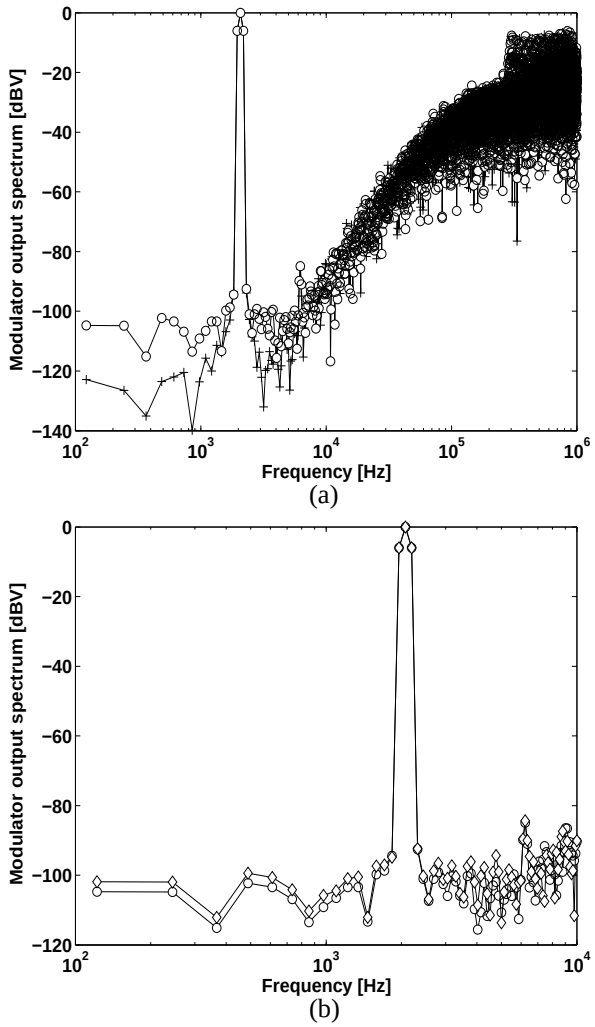


Figure 6.27: Normalized output spectrum of the ΔΣ modulator $[dBV]$ vs. frequency $[Hz]$ for the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4 and with the integrators implemented as active RC (Fig. 6.18). The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$. Spectrum obtained by an FFT on 2^{14} points, $F_{samp} = 2\ MHz$ and input signal frequency $Fin = 2.075\ kHz$. The spectrum is represented in the Nyquist frequency band (a) and in the signal band (b) with ideal resistors $Rin1 = Rin,nom = 451\ k\Omega$ and $Rdac1 = Rdac,nom = 503\ k\Omega$ (+), with noisy $Rin1 = Rin,nom$ and $Rdac1 = Rdac,nom$ (○) and with noisy $Rin1 = 2 * Rin,nom$ and $Rdac1 = 2 * Rdac,nom$ (◇)

The **linearity** of the input V/I converter must also be so low that it does not jeopardize the converter resolution, i.e. $\frac{\text{Signal power}}{\text{Total harmonic distortion}} \geq SNR_{\text{target}}$ where SNR_{target} is the target

converter resolution (Fig. 6.17). Assuming we have small signal amplitudes, the non-linear OTA output current may be described by its Taylor expansion $i_{out}(t) = g_m v_{in}(t) + g_{m,2} v_{in}(t)^2 + g_{m,3} v_{in}(t)^3$, v_{in} being its input voltage. Further assuming fully-differential circuitry, we suppose the third-order harmonic distortion ($HD3$) is dominant and it may be expressed as [17]

$$HD_3 \approx \frac{gm_3}{16 g_m'^4} \left(\frac{1}{R_{in,1}} + \frac{1}{R_{dac,1}} \right) \left(\frac{\widehat{V_{in}}}{R_{in,1}} \right)^2 \tag{6.8}$$

where $g_m' = gm - \frac{1}{2}\left(\frac{1}{R_{in,1}} + \frac{1}{R_{dac,1}}\right)$. Low $HD3$ can be obtained through high values of $R_{in,1}$ and $R_{dac,1}$.

Focusing on the sizing of the passives, we must choose R_{in} and R_{dac} large , for linearity reasons (6.8), but not too large to comply with the noise requirements (6.7). The **design optimization methodology** must guide to the best value for R_{in} and R_{dac} according to this trade-off. As the evaluation of the converter performance is assessed by simulations, the design optimization methodology is an iterative process.

1) The *ratio of the resistances* is fixed such that the power of the input signal and the feedback signal are comparable:

$$\frac{R_{in,1}}{R_{dac,1}} = \frac{\sqrt{(2)}\widehat{A_{in}}}{(1-\tau)V_{dac}} \tag{6.9}$$

where $\widehat{A_{in}}$ is the input signal amplitude, τ is the duty cycle of the return-to-zero feedback pulse (Fig. 6.11) and V_{dac} is the magnitude of a DAC output corresponding to a $'1'$ digital input. We set the *absolute value of the resistances* such that the input-referred noise fixes the converter resolution (6.7).

2) The integrating capacitance ($C_{i,1}$) is then determined to implement the first loop filter coefficient (k_1, Fig. 6.9) as

$$C_{i,1} = \frac{1}{A_{int,1} R_{in,1} k_1} \tag{6.10}$$

where $A_{int,1}$ is the gain of the first integrator.

3) Once the passive components have been sized, the amplifier *gm* must be made large enough to reach the wanted HD3 performance (6.8), resulting in a power-linearity trade-off. This power-linearity trade-off is illustrated in Fig. 6.28 , where different *gm* and $gm,3$ values are combined. On the other hand, the integrator linearity can also be improved by decreasing its gain (i.e. increasing the *RC* product) [17][11]. The OTA *gm* could be lowered, saving power. It would however imply a larger $C_{i,1}$ as the resistance is limited due to noise (6.7), resulting in an area-performance trade-off. If the first integrator gain is reduced, the NTF and STF must be preserved by proper scaling of the loop filter coefficients [45]. Care must also be taken that the first integrator gain remains sufficiently high to cancel the higher-order stages imperfections. The final *gm* yields the minimum power consumption as it is the result of these power-linearity and power-area trade-offs (Fig. 6.26), which can be assessed through the VHDL-AMS models.

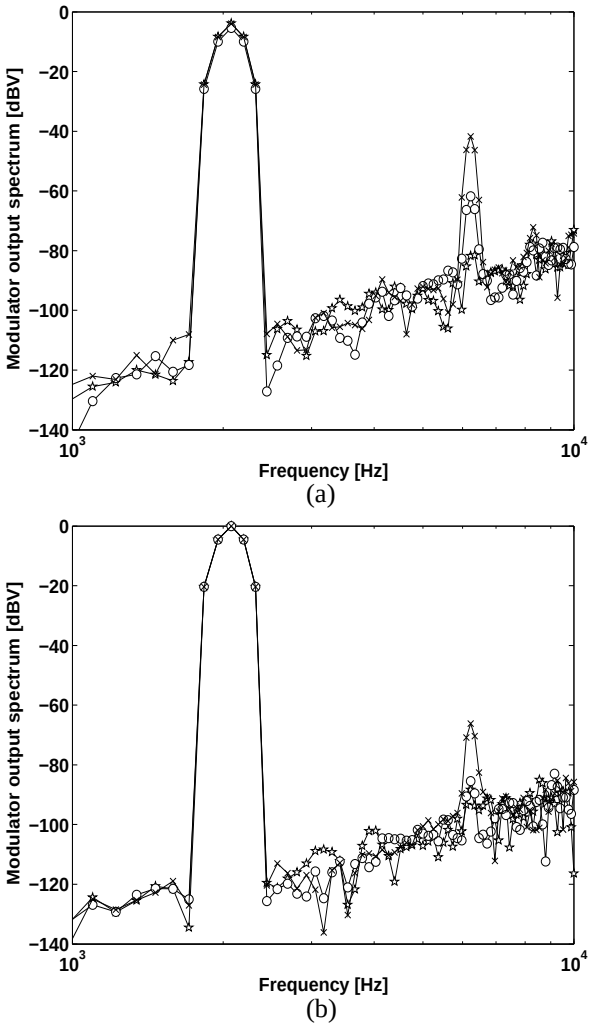


Figure 6.28: Normalized magnitude of the ΔΣ modulator output $[dBV]$ vs. frequency $[Hz]$ for the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4 and with the integrators implemented as active RC Fig. 6.18). The internal quantizer has a resolution of a single bit, $Fsamp = 2\ MHz$, OSR $= 128$ and hence $fb = 7.8\ kHz$. Spectrum obtained by an FFT on 2^{14} points, $F_{samp} = 2\ MHz$ and input signal frequency $Fin = 2.075\ kHz$. The first integrator OTA gm is $gm \approx 1/R$ (a) and $gm \approx 10 * 1/R$ (b) ($1/R = 1/Rin1 + 1/Rdac1$). In each case, the $gm3$ generic is: gm_3 : $0.001g_m(\star)$, $0.1g_m(\circ)$ et $g_m(\times)$.

The higher-order integrators can be designed using the same design methodology. The constraints should nevertheless be less stringent as their imperfections are substantially relaxed by the previous integrators gain. The ratio of the resistances here implements the loop filter coefficients while the integrating capacitances $C_{i,j}$ fix the integrator gain

$$\frac{R_{in,j}}{R_{dac,j}} = k_j \tag{6.11}$$

$$C_{i,j} = \frac{1}{A_{int,j} R_{in,j}} \tag{6.12}$$

where $R_{in,j}$ and $R_{dac,j}$ are, respectively the input and the feedback resistors of the j-th integrator, k_j is the corresponding loop filter coefficient.

The specification-power trade-off for a given set of $R_{in,1}$ and $R_{dac,1}$ values is finally obtained by the evaluation of the influence of the OTA transconductance on the ΔΣ modulator when the noise and linearity constraints are taken into account. In Fig. 6.29, the OTA gm is swept from $\frac{1}{R}$ up to $\frac{20}{R}$ for a $gm3 = 0.05\ gm$, corresponding to an OTA HD3 of $-66\ dB$ for a 200 mV amplitude. The power-specification trade-off is clear in Fig. 6.29, yielding a SNDR of $\approx 14\ bits$ for an OTA gm of 84 $\mu A/V$.

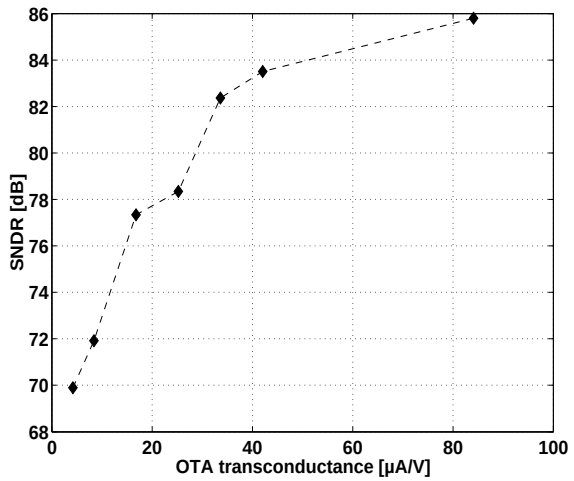


Figure 6.29: Signal-to-noise-and-distortion ratio (SNDR) $[dB]$ vs. the transconductance of the first OTA (gm) $[\mu A/V]$ for the 3rd order CT ΔΣ with the loop filter coefficients of Tab. 6.4. Each point corresponds to a VHDL-AMS simulation of the modulator using an RC implementation of the integrators. The first OTA has a $gm3 = 0.05\ gm$, its output current is limited to $\pm 20\ \mu A$, the finite output impedance is $250\ k\Omega$ corresponding to $R_{in,2}$. The noise of $R_{in,1} = 451\ k\Omega$ and $R_{dac,1} = 503\ k\Omega$ are also taken into account. The other integrators are RC integrators with ideal amplifiers. The input signal amplitude is $-8\ dBFS$.

6.4.8 A feedback DAC for active RC integrators

The use of return-to-zero (RTZ) coding allows us to relax the specifications on the feedback DACs (section 6.4.1). The DACs will then include some logic to generate the RTZ code. As the rest of the modulator, they are implemented using fully-differential circuitry

for it helps in this particular DAC case to further reduce the DAC output waveforms asymmetry (section 6.4.1). The DAC output signals must also be synchronized with the comparator so that the modulator output stabilizes when the DAC output is set to zero ($t_d = Tsamp/4$, in our particular case). We then choose to generate the comparator clock internally starting from the DAC driving clock.

The DAC architecture is quite simple and consists of six transmission gates, driven by three clock signals: *rtz*, *up*, *down* (Fig. 6.30). The positive (resp. negative) DAC outputs are connected to the common-mode voltage of the circuit (V_{CM}) during t_d and to the positive ($Vref,p$) or negative ($Vref,m$) reference voltage during τ_d depending on the comparator output.

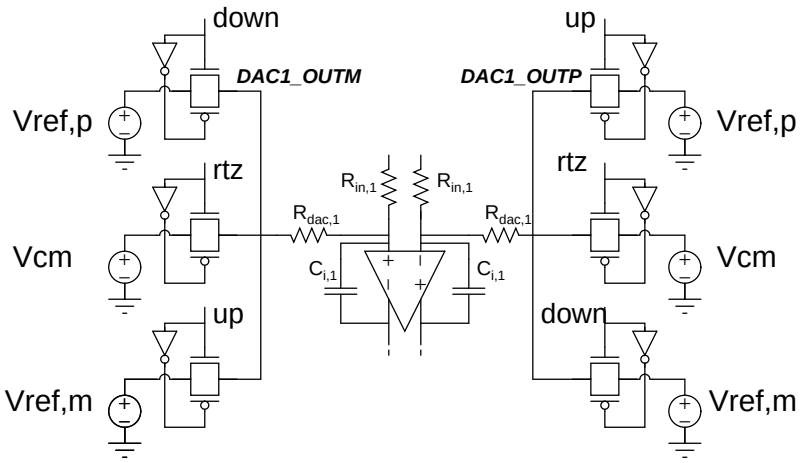


Figure 6.30: Architecture of the fully-differential DAC, whose outputs ($Vdac,outp$ and $Vdac,outm$) are connected to the first amplifier input through resistances $R_{dac,1}$. $Vref,p$ ($Vref,m$) is the DAC output high (low) level value and $Vref,cm$ is the common-mode value to which the outputs are connected during the return to zero. rtz, up and $down$ are the clock signals and are generated by a logic circuit.

As an example, the time diagram of the DAC control signals corresponding to a comparator output sequence $'0110'$ is drawn in Fig. 6.31.

The DAC outputs are connected to the amplifier inputs through the feedback resistances ($R_{dac,j}$). The switches on-resistance is small compared to $R_{dac,j}$. $R_{dac,j}$ will thus set the amount of current flowing from the reference voltage to the amplifier input nodes. The speed and noise of the DAC is mainly determined by the $R_{dac,j}$, provided that the output current of $Vref,p$ and $Vref,m$ is sufficient. If the DAC happens to be too slow, the value of $Vref,p$ ($Vref,m$) may be decreased (increased) and $R_{dac,j}$ may be lowered accordingly. This also yields a lower noise contribution of the DAC but the designer must verify that the integrator output levels are still correct. Voltage-based DACs will however remain *slow*. It is not a problem in our case as we target relatively low signal bandwidth but for higher $Fsamp$, the use of current based DAC is more appropriate [9] [10] [54].

In section 6.3, we showed that continuous-time ΔΣ modulators are a good candidate for operation at high temperature due to the absence of switches. The influence of the

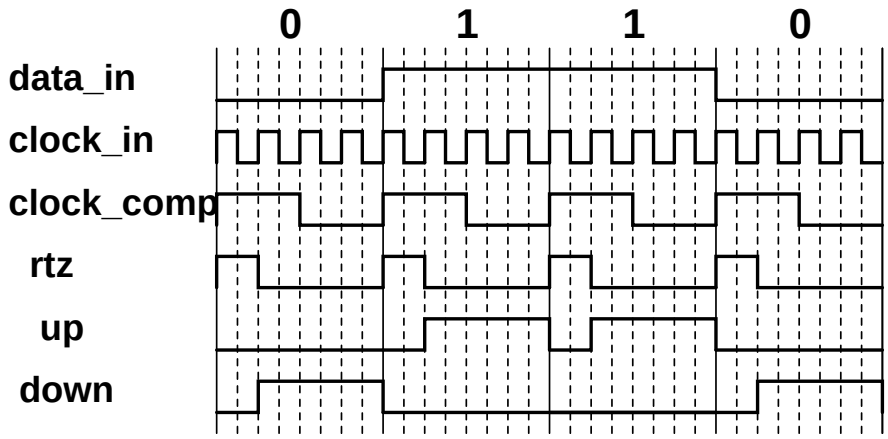


Figure 6.31: Time-diagram of the DAC control signals corresponding to a $'0110'$ *data_in* **sequence.** *clock_in* **is the input clock at** $4 \times Fsamp$**.** *rtz*, *up* **and** *down* **are the three DAC control signals.** *clock_comp* **oscillates at** $Fsamp$ **in order to trigger the comparator.**

DAC transmission gate leakage should not be critical due to the relative low sensitivity of the modulator on the RTZ DAC performance.

To generate the five clock signals, we propose the logic circuit of Fig. 6.32, which is driven by a clock, which frequency is equal to $4 \times Fsamp$. The circuit additionally generates a clock at the sampling frequency, synchronized with the DAC control signals, to drive the comparator. It ensures that the comparator output data will be stable after t_d, provided the comparator has been properly designed. A DAC clock at $4 \times Fsamp$ is preferred to a DAC clock at $2 \times Fsamp$ in order to be triggered only by positive edges and the signals are furthermore synchronized using D-type latches in order to be independent of the delay of the gates.

Fig. 6.33 shows a sequence of DAC input and output signals for a DAC connected to the first integrator. The transmission gates are described at the transistor level using models of a 1.2 μm partially-depleted SOI CMOS technology, the first integrator and the DAC control logic are emulated by the VHDL-AMS models. The behavioral simulations show that the obtained t_{rise} and t_{fall} of ≈ 700 ps can be afforded. The digital gates are available in the technology library and the sizing tools are available for the logic circuit. Moreover, our timing constraints are not critical for the technology under consideration. We then do not go further into details as it is not the purpose here.

6.5 Conclusion

In this chapter, we show how the developed VHDL-AMS models can be used in a practical mixed-signal design case using a continuous-time $\Delta\Sigma$ modulator as test vehicle. After reviewing basic concepts of the $\Delta\Sigma$ analog-to-digital converter, we motivate the use of a

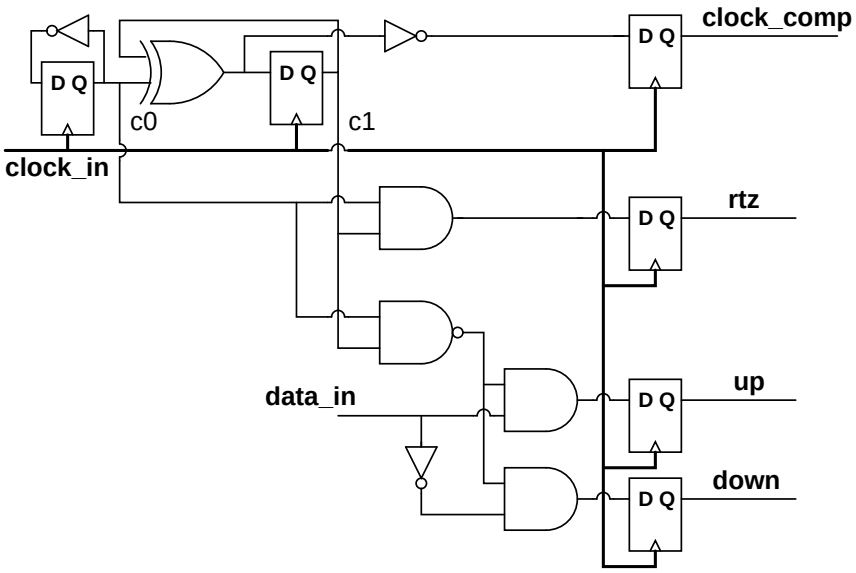


Figure 6.32: DAC RTZ logic. $clock\_in$ **is the input clock at** $4 \times Fsamp$ **and** $data\_in$ **is the comparator output data.** rtz**,** up **and** $down$ **are the three DAC control signals.** $clock\_comp$ **oscillates at** $Fsamp$ **in order to trigger the comparator**

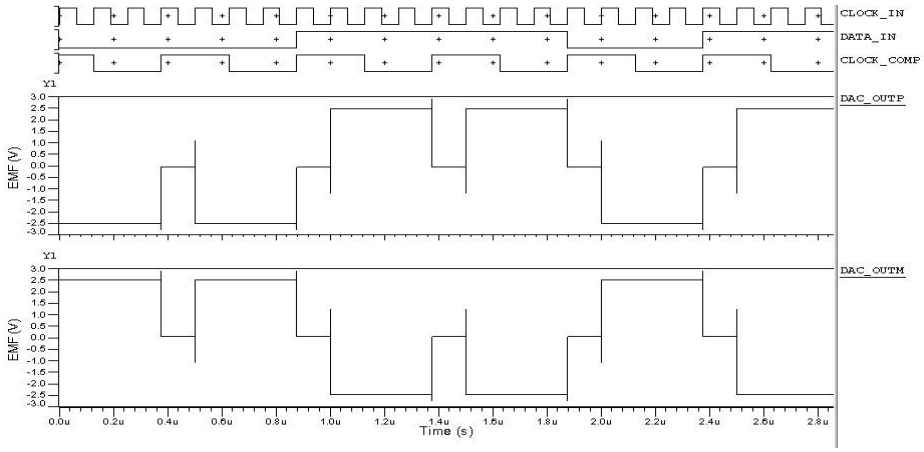


Figure 6.33: Time domain simulation of the DAC driving the first amplifier of the loop filter as in Fig. 6.30. The transmission gates are simulated at the transistor level using models from a PD SOI $1\ \mu m$ **technology. The nMOSFETs have minimal size (**$W = 4\ \mu m$ **and** $L = 1\ \mu m$**) while the pMOSFETs width and length are respectively,** $8\ \mu m$ **and** $1\ \mu m$**.** $R_{dac,1} = 503\ k\Omega$ **and** $C_{int,1} = 60\ pF$**. The amplifier gain is equal to** 1000 **and its output impedance is** $250\ k\Omega$**.**

continuous-time implementation of the $\Delta\Sigma$ as test vehicle by pointing out its potential for our application targets: low-power consumption and operation at high-temperature. Investigation of the behavior of the $\Delta\Sigma$ modulator indeed revealed key potential of continuous-time implementations concerning low-power operation. This was further confirmed by the state-of-the-art of $\Delta\Sigma$ focusing on medium to high resolution and on signal bandwidth below 100 kHz. The analysis of published analog-to-digital converters targeting high-temperature operation also stressed key potential of continuous-time $\Delta\Sigma$ for operation at high-temperature. The test vehicle has the following specifications: medium resolution (14-16 bits) and a low signal bandwidth ($\approx 10\ kHz$) with an oversampling ratio OSR$=128$. We reviewed the methods available for the design of the transfer function of the continuous-time $\Delta\Sigma$ and point out the design trade-offs. The different options to implement the integrators ($gm-C$, $MOSFET-C$ and active RC with passive capacitors and resistors) are also reviewed based on the state-of-the-art of published continuous-time modulators.

Using the VHDL-AMS models we assess the influence of the analog cells imperfections on the modulator performance. Classical amplifier parameters like the gain, the gain-bandwidth product, the slew-rate are taken into account but also the jitter on the clock, the white noise and the amplifier non-linearity. Continuous-time $\Delta\Sigma$ impose specific constraints on the feedback DAC, which are also assessed. We finally propose an implementation for the feedback DACs.

Through the continuous-time $\Delta\Sigma$ test vehicle, our VHDL-AMS models are shown to be an efficient link between the analog cells and the mixed-signal circuits (Fig. 1.4). Using the models and the design optimization methodology we can include the design of the CT $\Delta\Sigma$ modulator in the improved analog design flow that we investigate in chapter 7.

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Part IV

Conclusions

Chapter 7

The Analog Design Flow: status and personal contributions

Electronic systems include ever more features. Their increased potential mainly comes from the huge improvements of device fabrication technologies and from the combination of analog and digital signal processing on the same chip. State-of-the-art applications possibly gather electronical, mechanical, optical and thermal subsystems. At the same time, cost and development time are reduced; stressing the need for an efficient design flow for fast and reliable design of multi-domain mixed-signal systems.

We focus in this chapter on the analog design flow in the context of multi-domain, mixed-signal systems. We start from the current design flow to highlight the breakthroughs enabled by the mixed-signal hardware description languages (HDL-AMS). We deal with both the top-down synthesis and bottom-up validation as part of this design flow and emphasize our contribution by integrating the analog ID card (part I) and the design methodology of chapter 6.

7.1 Analog Design Flow using HDL-AMS

The design of an electronic system results of a top-down synthesis, from the specifications to the physical realizations, and of a bottom-up validation, from the test of the functional entities up to the test of the system (Fig. 7.1).

In the top-down path (Fig. 7.1), the system specifications are propagated downwards. There is currently no formal methodology to generate the specifications of a system and even less methodology to propagate them from up to down and vice-versa. It is a research area by itself. The designers recursively divide the system into functional subsystems; choose an architecture for each of them and end with the physical realization of the basic cells which compose these subsystems. In a second, bottom-up step (Fig. 7.1), the realizations of the basic cells are tested. If they comply with their specifications, they are assembled to form the complete electronic system and if not, the corresponding top-down design step must be revised. The test and validation steps are then propagated up to the electronic system, level by level. This design flow ensures the adequacy of the realized system and its specifications.

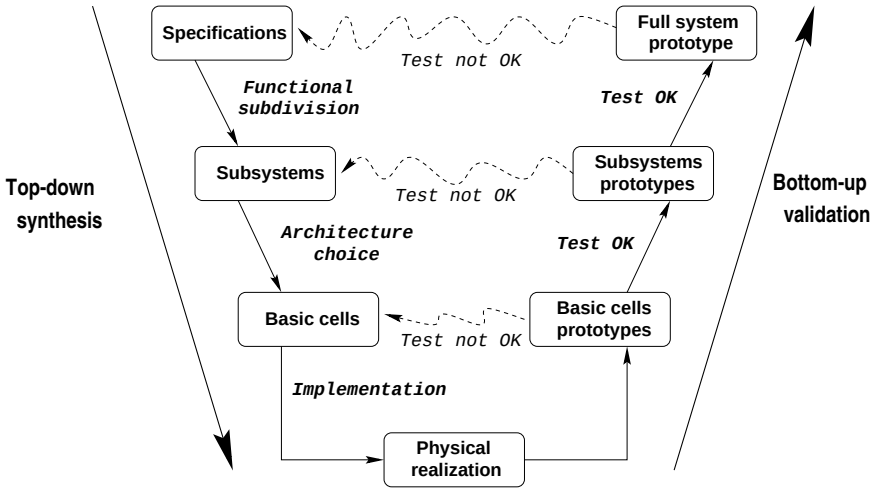

Figure 7.1: Traditional top-down design and bottom-up validation design flows of analog circuits, usually referred to as the V-cycle.

Different levels of abstraction correspond to the description of the system and subsystems at the different stages of the design flow. While for digital applications these abstraction levels are well defined, the situation is different for analog applications as the number of design parameters are far more important. The models can be divided in two classes whether they are used to describe or predict the behavior of a system. We define three types of models to support the analog design flow: behavioral, structural and physical models [1]. A behavioral model describes a system as a black-box, defining only the link between the system inputs and outputs (Fig. 7.2). It is very fast but limited and can not predict the possible failures which were not explicitly modeled. It corresponds for example to the description of a continuous-time filter using a Laplace transfer function. The structural description identify the subsystems and define the link between them (Fig. 7.2). In this case, the filter would be described as an interconnection of subsystems like amplifiers, resistors, capacitors and inductances. Each subsystem can be described by a behavioral model, further subdivided into basic cells described by a physical model. The physical model describes the internal mechanisms as accurately as possible so that it can predict the system behavior and its parasitic effects (Fig. 7.2). If the amplifiers of the filter are further subdivided into an interconnection of transistors, these can be described using compact transistor models for example.

Tools or languages are also associated to each model level. Currently, at the behavioral level, the digital circuits are described using C/C++ or SystemC [2] for more abstract and HW/SW systems and Verilog [3] or VHDL [4] for smaller ones. The analog part is modeled in Matlab/Simulink or in C using a discrete-time equivalent. The system also possibly includes parts from other physical domains (mechanical, thermal or optical, ...) like e.g., an accelerometer or a parallel optical module [5]. In order to have a description compatible with the electronic circuits, the detailed models of these parts of other physical domains are approximated using electrical equivalents. Increased efficiency would require a language, common to all parts of a complete electronic systems to fill the gaps between

the detailed descriptions of the different physical domains (Fig. 7.2). HDL-AMS provide such multi-domain feature; [6] emulates for example an airbag system using the physical domains associated to each subsystem.

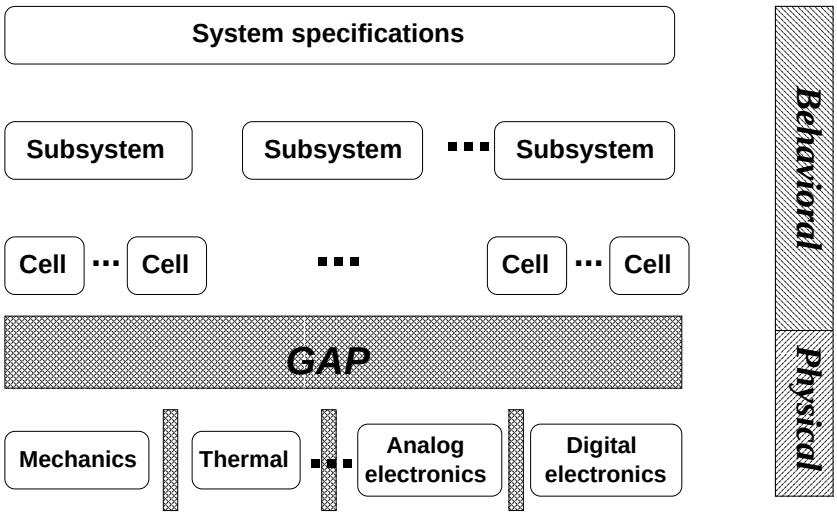

Figure 7.2: Top-down division of a multi-domain multi-signal electronic system and associated level of abstraction; from the system down to the basic cells implemented in various physical domains. Current gaps between 1) the different physical domains 2) the behavioral and physical levels of abstraction.

In order to efficiently implement the top-down design and bottom-up validation flows, we also need a language common to all the abstraction levels, which allows to mix the description levels in a single simulation. Focusing on analog electronics, the behavioral models are typically written in Matlab/Simulink while the physical models are implemented in SPICE-like electrical simulators. The results of the electrical simulations cannot be efficiently compared to the behavioral models. This may imply the realization of a large quantity of prototypes to ensure the reliability of the system (Fig. 7.1). In the current design flow, there is thus also a gap between the behavioral and physical models (Fig. 7.2), which can be bridged by the multi-level of abstraction HDL-AMS. Finally, the design flow can be improved by using HDL-AMS as will be detailed here below, focusing on the gap between the behavioral and physical models in the case of mixed-signal electronic systems.

HDL-AMS provide a common frame to the different levels of description. The top-down analysis can be efficiently supported by these HDL-AMS models starting from a behavioral description of the system, going through behavioral models of the subsystems and ending with the subsystems physical descriptions. Moreover, as the different models are tested and compared to the higher level descriptions they also adequately support the bottom-up validation flow (Fig. 7.1). In this case the validation, based on models and not on prototypes anymore [1], may take place after each top-down step, revealing as fast as possible the errors in the design (Fig. 7.3). Provided that the physical models are accurate, the influence of each subsystem imperfections on the system performance can be accurately evaluated. The design flow supported by HDL-AMS languages avoids the costly production of intermediate prototypes, or at least reduces their number (Fig. 7.3).

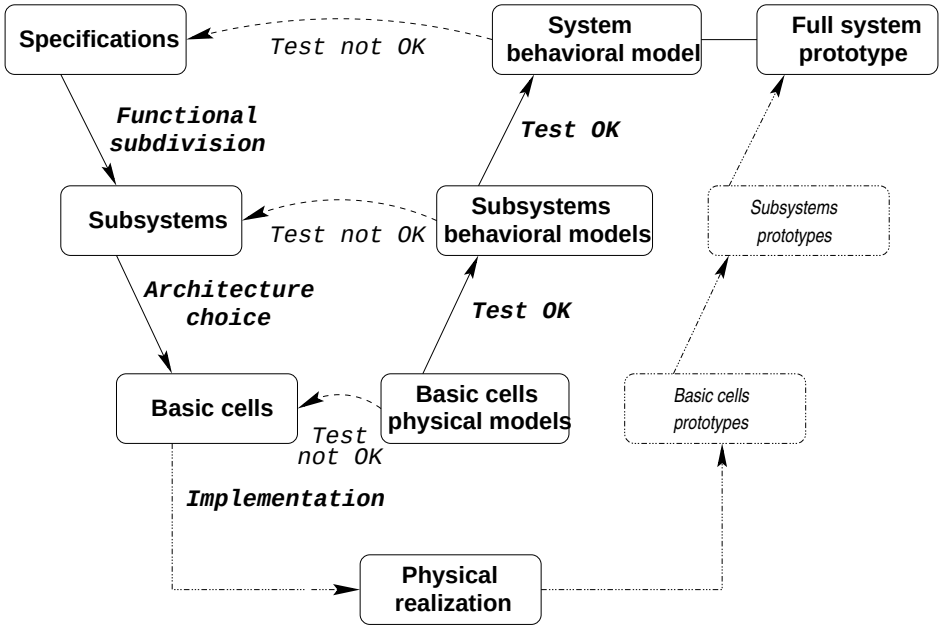

Figure 7.3: Improved top-down design and bottom-up validation design flows of analog circuits using HDL-AMS with less prototype realizations and enhanced reliability. Dotted lines indicate prototypes that could be avoided using HDL-AMS. The V-cycle of Fig. 7.1 is modified and it is called the *Virtual Prototyping Cycle* in the case all the intermediate prototypes are avoided [7].

The use of HDL-AMS also brings additional benefits. Due to their multi-domain characteristic, the system can be simulated in its real environment, possibly including thermal or mechanical effects for example. As it is a common language for all the parts of a mixed-signal system, it also facilitates the interactions between designers as well as external collaborations (IP cells, ...). Finally, it fixes a common behavioral description of the system which is the reference for everyone. The system specifications and associated test benches can be defined unambiguously with the design teams and customers.

7.2 Challenges for guided top-down synthesis and bottom-up validation

Apart from the improvement of the design flow concerning modeling and simulation issues, HDL-AMS could also use the same design flow to automatically propagate the specifications in the top-down flow. We will here more focus on tools guiding the designer to the most relevant solutions rather than on fully automatized synthesis. We start by pointing out the key issues and by formalizing the processes. We will then highlight our contribution by integrating the analog ID card (part I) and the design methodology of chapter 6 in this guided top-down synthesis and bottom-up validation flows. We focus more closely on VHDL-AMS [8] as it is the language we used (chapter 5).

According to a particular performance criterion, we must derive the best implemen-

tation starting from the system specifications. Following the top-down flow, the specifications must be propagated downwards and the realization performance must be upwards compared to the specifications [9]. A performance is measured by simulating a particular test bench. The system is as already said divided into subsystems. Each subsystem gets its specifications from the (sub)system it is part of and its performance is the aggregate of the measured performance of all the subsystems in which it is further divided (Fig. 7.4) [9]. If the performance meets the specifications, the subsystem model is well-tuned.

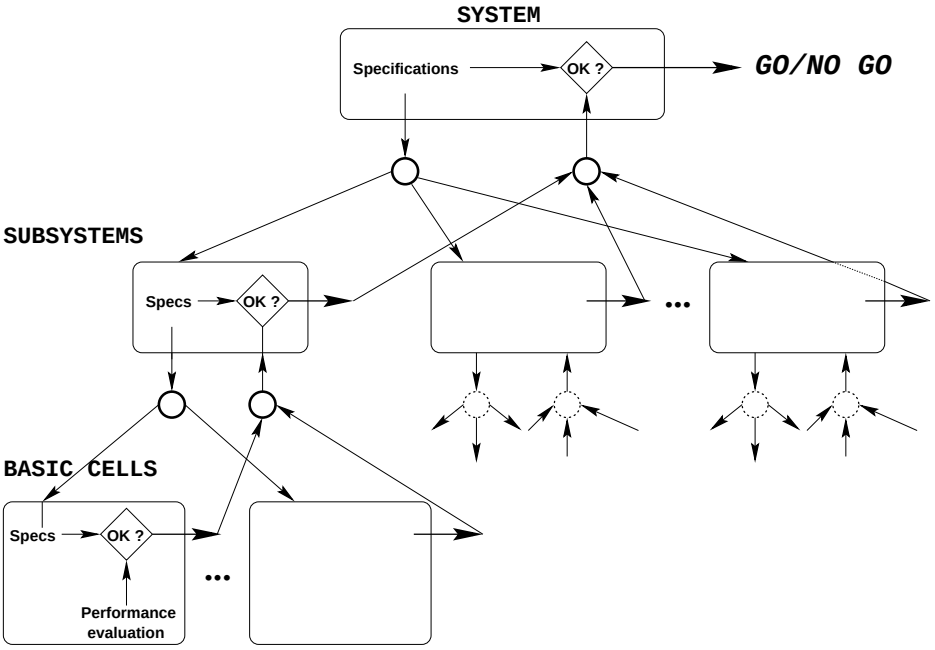

Figure 7.4: Guided top-down design and bottom-up validation flows of analog circuits using HDL-AMS. The specifications are downwards propagated to the different subsystems while the performance of these subsystems are aggregated to verify locally if the performance and specifications are adequate [9].

Moreover, different topologies may exist for a given (sub)system; this process must be done for each topology. Using VHDL-AMS, an ENTITY (VHDL-AMS language syntax[1]) corresponds to each subsystem and its behavior can be tuned through its GENERIC parameters. The goal of guided top-down sizing can then be refined as: 1) for each specification and for each topology, determine the set of the values of the GENERICS such that the measured performance of the model agrees with the specification; 2) determine the subset of values of GENERICS which fulfills all specifications and 3) using an external optimizer, identify the best solution for each topology and hence the best topology for the (sub)system.

The specifications must be clearly defined and organized hierarchically so that a performance criterion can be identified. An efficient classification method is the MoSCoW technique [10], an acronym defining four levels of hierarchy which can be associated to e.g. four VHDL-AMS severity levels [9] as follows

[1] In this chapter, words in small capital letters refer to VHDL-AMS language syntax

M	*MUST have* fundamental to the project	*Failure* severity level
S	*SHOULD have* important but the project success doesn't depend on it	*Error* severity level
C	*COULD have* if it does not affect anything else	*Warning* severity level
W	*WON'T have* this time round but would like in the future	*Note* severity level

Next to the specifications related to the performance of the system, one must add specifications related to the actual implementation (minimal and maximal transistor dimensions, for example) ensuring the feasibility of the solutions. The optimization criterion is defined based on the set of prioritized specifications.

The tuning of the subsystem GENERICS depends on the link which exists between the specification and the GENERICS [11]:

- There is an explicit analytical link between the specification and a set of GENERICS; i.e. specification $= f(\text{GENERICS})$ is known. The GENERICS can be directly computed.
- There is an implicit analytical link between the specification and a set of GENERICS; i.e. $0 = f(\text{specification}, \text{GENERICS})$ is known. The GENERICS can be directly computed.
- There is no analytical link between the specification and a set of GENERICS; their relationship is only known by data sheets or measurements and can be expressed by a look-up table. The GENERICS can then be found using an heuristic approach, coarse or knowledge-based optimization.

Obviously, the link between specification and GENERICS may also be a combination of the above types and in a given model, the different types may coexist. In the next subsection, we show how our work can be used in practical cases.

7.3 Our contribution

We will here below show how our work can be integrated in the efficient analog design flow using HDL-AMS (Fig. 7.3). For this purpose, we start from a practical design case: a continuous-time $\Delta\Sigma$ modulator (chapter 6) for which we can identify three subsystems (Fig. 7.5): the integrators, the internal quantizer and the feedback digital-to-analog converter (DAC). In the context of this application, we will show how our work contributes to the construction of a guided top-down sizing and bottom-up validation flow concerning current bottlenecks: (1) given a resolution specification, efficient choice of the type of integrator; (2) design of the integrators in a semi-automated procedure, with respect to the continuous-time $\Delta\Sigma$ modulator specifications; and (3) top-down design methodology for active RC integrator topologies.

We focus on the integrators and consider their possible implementations: $gm-C$, MOSFET-C or active RC techniques with integrated resistors (Fig. 7.6). We show how the analog ID card of part I and the study of chapter 6 are able to guide the designer to the best implementation for its specifications. For applications with a resolution of $14-16$ *bits*, we show that the active RC integrators with passive resistors are the most appropriate while the MOSFET-C integrators may be used for lower resolution only. This conclusion can only be drawn using the methodology developed in chapter 3 as the linearity of these integrators can hardly be predicted using traditional MOSFET models. We also detail the top-down design of active RC integrators. In the case of the active RC integrators

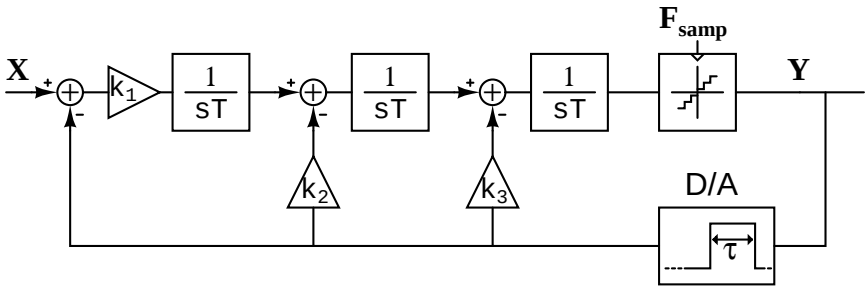

Figure 7.5: 3rd order ΔΣ modulator with continuous-time integrators stabilized by feedback. $k1$**,** $k2$ **and** $k3$ **are the loop filter coefficients**

with passive resistors, we use the study made in chapter 6 to propose a knowledge-based optimization method for the design of such integrators with respect to the ΔΣ modulator specifications. Chapter 5 provides the VHDL-AMS models to implement the improved design flow (Fig. 7.3 and Fig. 7.4). This way we can tune the integrator model as in this case there is no analytical link between the specifications of the modulator and the parameters of the integrator subsystems. In the case of the MOSFET-C integrator, we go down to the transistor level using the results of part I.

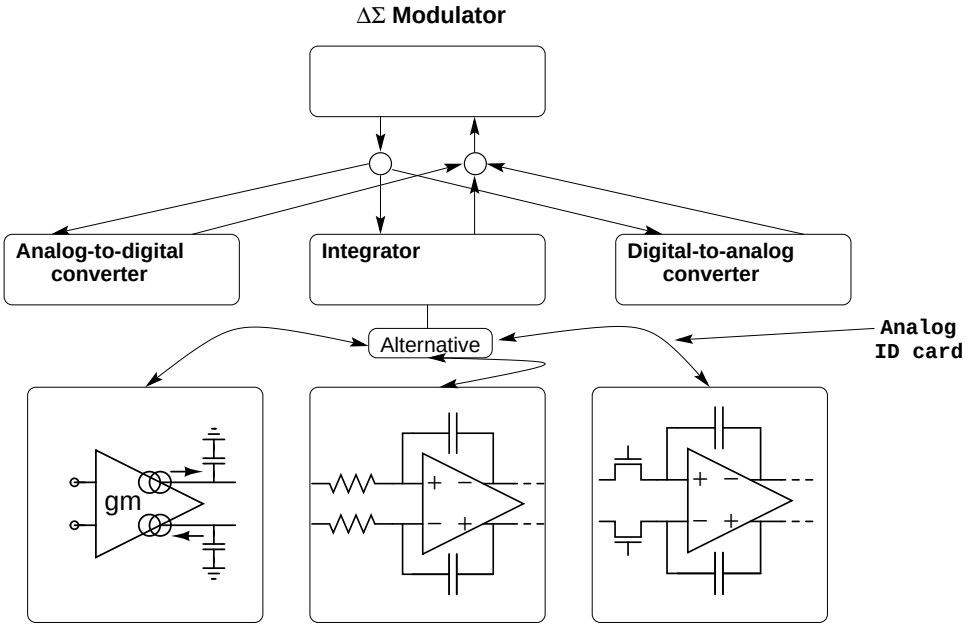

Figure 7.6: Top-down structural division of a ΔΣ modulator with continuous-time integrators. Three subsystems are identified: integrator, analog-to-digital converter and digital-to-analog converter. We focus on the three different topologies for the integrators.

7.3.1 Continuous-time ΔΣ modulator

A structural description of a third-order continuous-time ΔΣ modulator is presented in Fig. 7.6 where the integrators, internal quantizer and feedback digital-to-analog converter (DAC) are identified. We focus here on the integrators which can be implemented using $gm-C$, MOSFET-C or active RC techniques with passive resistors. In a top-down design, the best topology must be identified. Based on the study of chapter 6, we can put the speed and linearity on top of the hierarchy of the integrator specifications. Depending on the modulator speed and resolution, one technique will prevail. To evaluate the potential of the MOSFET-C technique, we will review the design of such integrators and propagate the performance back to the ΔΣ modulator.

7.3.1.1 MOSFET-C integrator top-down sizing and bottom-up validation

The behavior of an integrator (Fig. 7.7) can be described at first order by a Laplace transfer function

$$\frac{V_{out,\text{int}}}{V_{in,\text{int}}} = \frac{Gain_{\text{int}}}{s} \tag{7.1}$$

where s is the Laplace quantity, $Gain_{\text{int}}$ is the integrator gain, $V_{out,\text{int}}$ and $V_{in,\text{int}}$ are the integrator output and input voltage, respectively. Using an active RC implementation for the integrator, we can refine (7.1) using

$$Gain_{\text{int}} = \frac{1}{RC} \tag{7.2}$$

where R is the resistance and C is the capacitance.

The specifications for such an integrator (Fig. 7.8) include $Gain_{\text{int}}$, the load impedance, the linearity and the maximum, minimum and typical signal amplitude (A_{signal}). Process variations, temperature of operation as well as minimum and maximum transistor sizes must also be taken into account. Focusing on fully-differential implementations for increased dynamic and robustness, the linearity is determined by the third-order harmonic distortion (HD3). The integrator is divided into three subsystems (amplifier, resistor and capacitor) and the specifications are propagated downwards accordingly (Fig. 7.8). We suppose that the linearity of the filter is dominated by the resistor HD3, i.e. we suppose that the amplifier provides a sufficiently high gain and that the linearity of the passive capacitor can be neglected. If this would not be verified, we could detect it when reporting the performance of the subsystems to the filter (Fig. 7.7) and take the appropriate actions (increasing amplifier gain or selecting an other capacitor type). Here below, we design the amplifier and resistor from the specifications down to the physical, transistor level.

Fig. 7.7 illustrates the different levels of abstraction used to describe the amplifier, starting from the behavioral Laplace transfer function down to the transistor-level schematic. We use here the case of a simple common-source amplifier for clarity reasons. The results may however be extended to more elaborated topologies. We first deal with the basic analog parameters: gain (Av) and gain-bandwidth product (GBW). In this very simple case, the structural decomposition of the amplifier into a transconductance (gm) and an output conductance (gd) is not mandatory. We however keep it as in more elaborated topologies it may be useful. The *sizing* box of Fig. 7.7 is further detailed in Fig. 7.9 which schematically presents the *sizing* box having as inputs the specifications and the analog ID card; and as outputs, the bias current ($Ibias$) and the transistor width (W) and length (L) .

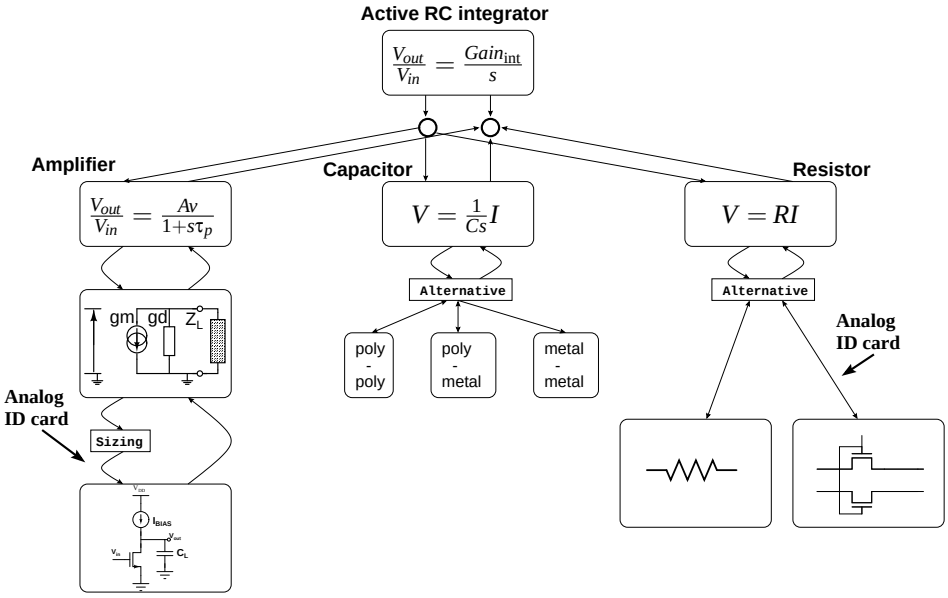

Figure 7.7: Top-down structural division of an active RC integrator starting from the *system* behavioral description down to the physical realization for the three subsystems: amplifier, resistance and capacitance. The interaction of the analog ID card is highlighted.

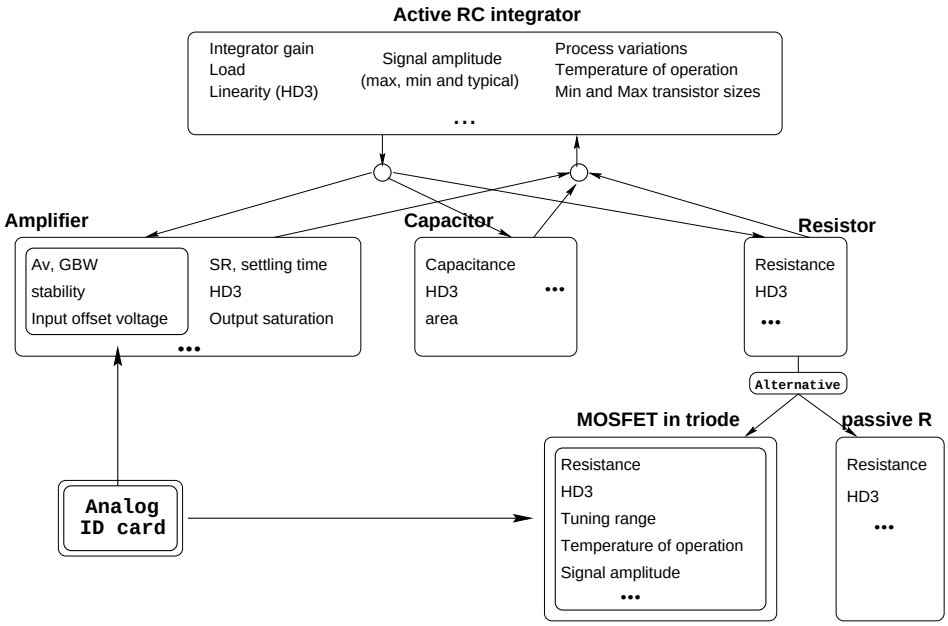

Figure 7.8: Top-down propagation of the specifications and bottom-up characterization in the case of an active RC integrator. The contribution of the analog ID card is highlighted.

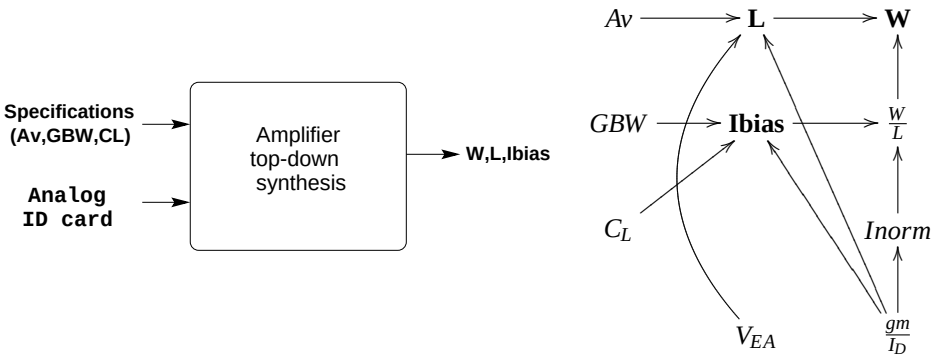

Figure 7.9: Top-down $\frac{gm}{I_D}$ design methodology which takes the analog ID card as input and gives as result the transistor sizes (W, L) and bias current ($Ibias$).

The well-known used top-down design methodology [12] based on the analog ID card is further detailed for the particular case of the common-source amplifier (Fig. 7.9). In this methodology, the bias point of the transistors are characterized by their $\frac{gm}{I_D}$ ratio. The $\frac{gm}{I_D}$ vs. $Inorm$ characteristic can be moreover considered as unique for a given transistor type in a given technology and there is a bijection between $\frac{gm}{I_D}$ and $Inorm$. In the case of the common-source amplifier (Fig. 7.9), for each possible $\frac{gm}{I_D}$ (i.e. bias point):

- gm is computed as $gm = 2\pi GBW C_L$;
- $Ibias$ can be derived from gm as $Ibias = \frac{gm}{\frac{gm}{I_D}}$;
- $Inorm$ is obtained through the $\frac{gm}{I_D}$ vs. $Inorm$ characteristic;
- $\frac{W}{L} = \frac{Ibias}{Inorm}$ by definition;
- $L = \frac{10^{\frac{Av[dB]}{20}}}{\frac{gm}{I_D} V_{EA,L}}$ as $Av = \frac{gm}{I_D} V_{EA,L} L$ (chapter 2);
- $W = \frac{W}{L} L$.

Listing 7.1 illustrates the implementation of the design methodology in the current VHDL-AMS tools as a PROCEDURE. The use of the PROCEDURAL would be more appropriate but it is not implemented in the current version of the tools. The PROCEDURAL indeed allows to simulate a set of sequential statements at each analog solution point (ASP), i.e. each evaluation of the analog solver.

Having determined W, L and $Ibias$ we can perform an electrical simulation using the MOSFET compact model provided by the semiconductor foundry, extract the performance of the amplifiers at the transistor level and propagate it one level above to verify that it complies with the specifications. This sizing methodology has been successfully used in practical designs [13] [14] [15] and was shown to efficiently size amplifiers with various specifications as Av, GBW, slew-rate, settling time [16] [17], ... In chapter 4, we

Listing 7.1: VHDL-AMS code of the entity corresponding to the one-stage amplifier and the *TopDown* architecture implementing the top-down sizing methodology schematically represented in Fig. 7.9 as a procedure .

```
entity OneStage is
  generic(gbw_min : real := 1.0e6;       -- gain bandwidth product [Hz]
          av : real := 20.0;             -- voltage gain [dB]
          cl : real := 10.0e-12;         -- load capacitance [F]
          vea : real := 10.0;            -- Early voltage [V/um]
          size_gmi : integer := 25       -- length of input vector
          );
       port(signal gmi, inorm : in real_vector(0 to 158);
            signal ibias, W, L : out real_vector(0 to 158)
            );
end entity OneStage;

architecture topdown of OneStage is

procedure computeL (variable param: in real_vector(0 to 3);
    variable gmi_array: in real_vector;
    variable inorm_array : in real_vector;
    variable ibias_array : inout real_vector;
    variable W_array : out real_vector;
    variable L_array : inout real_vector) is
variable ft_min : real := param(0);
variable gain : real := param(1);
variable load_capa : real := param(2);
variable early_voltage : real := param(3);
variable end_of_loop : integer := gmi'length;
variable wonl : real_vector(0 to end_of_loop);
    begin
    for kk in 0 to end_of_loop loop
        ibias_array(kk) := (math_2_pi*ft_min*load_capa)/gmi_array(kk);
        wonl(kk) := ibias_array(kk)/inorm_array(kk);
        L_array(kk) := (10.0**(gain/20.0))/(gmi_array(kk)*early_voltage);
        W_array(kk) := L_array(kk)*wonl(kk);
    end loop;
    end procedure computeL;
begin
        [...]
end architecture topdown;
```

extended this methodology to include measured mismatch data and hence predict the offset. This extension can also be easily implemented in a VHDL-AMS procedure but is not presented here. In this case, the transistor performance is characterized by the data from the analog ID card: Early voltage ($V_{EA} \equiv V_{EA,L}$), the transconductance over drain current ratio ($\frac{gm}{I_D}$) vs. the normalized drain current (*Inorm*) characteristics and in the drain current mismatch vs. Inorm characteristics. As it was shown in part I, the extension of the analog ID card for operation at high temperature is straightforward. All these characteristics can be moreover obtained by simple measurements which is critical for designing state-of-the-art circuits without waiting for exhaustive and accurate transistor models.

Concerning the linearity of the MOSFET-C filters, the resistor is the key building block. The specifications on this subsystem (Fig. 7.7) are the resistance (*Ron*), the temperature range of operation and the signal amplitude (A_{signal}). The resistance must be

moreover tunable to compensate for on-chip variations of the process. The resistance in a fully-differential architecture can be implemented using two different topologies including respectively two and four transistors operating in the triode regime [18] [19] [20](chapter 3). In both topologies, the tuning of the resistance occurs through the gate voltage. The HD3 of these two structures can hardly be predicted by most of the MOSFET models available in electrical simulators, except the MOSFET model MM11 [21]. Up to now, the semiconductor foundries however rarely provide the parameter set associated to this model; and the extraction of the model parameter set is too costly. We therefore developed a measurement-based design methodology in chapter 3 to efficiently predict the HD3 performance of transistors under practical design optimization targets (Fig. 7.8). The sizing process using this methodology takes as inputs the specifications (*Ron*, A_{signal}, process variations and temperature range of operation) and the analog ID card and yields, for the two different topologies, the minimum and maximum HD3 obtained for the whole tuning range in the temperature range of operation. Here again, the obtained HD3 can be propagated one level above to verify if the resistor linearity comply with the specifications.

7.3.1.2 Best integrator implementation

We now come back to the integrators of a $\Delta\Sigma$ modulator for which we must elect the best topology: $gm-C$, MOSFET-C or passive RC techniques (Fig. 7.7). Based on the study of chapter 6, we form the set of specifications of the integrator into a hierarchy, placing speed and linearity on top. Depending on the modulator speed and resolution, one technique will prevail. In chapter 6, we focus on low-frequency modulators with a resolution of 14 to 16 bits. The $gm-C$ technique was already shown inappropriate for so high resolution [22]. The passive RC technique is the most linear of all but is sensitive to process variations. The MOSFET-C technique is very attractive as it can be tuned on-chip to compensate for process variations but as said in the previous section, it is rather difficult to predict its linearity using classical MOSFET compact models. Using the design methodology developed in chapter 3 and used in the previous section, we are able to verify that the linearity of the MOSFET-C topology is not compatible with the considered linearity specifications (i.e. resolution) using the semiconductor process of chapter 3. For the design targets and process considered here, the use of passive resistors in the active RC topology is the most appropriate. We review the top-down design of such an integrator in the next section.

7.3.1.3 Passive RC integrator top-down sizing and bottom-up validation

The first integrator of the continuous-time $\Delta\Sigma$ modulator is the most critical (chapter 6). It is structurally divided as shown in Fig. 7.7 and there exists no reliable analytical link between the integrator specifications (mainly noise and linearity) and the specifications of the subsystems: resistors, capacitors and amplifier. In chapter 6, we therefore developed a design methodology which can be used in this context as a knowledge-based optimization method to adequately size the subsystems starting from the integrator specifications (section 7.2). Once the specifications of the subsystems are specified, the amplifier can be sized down to the transistor level using the $\frac{gm}{I_D}$ sizing methodology as done in the previous section in the case of the MOSFET-C filter for most of the analog parameters. In further developments, the Volterra series [23] could be used to size the amplifier according to its

linearity specifications. Here again, a transistor-level simulation of the amplifier is used to measure its performance and propagate it to the upper level.

7.4 Conclusions

We started from the typical design flow of electronics systems resulting from combined top-down design and bottom-up validation flows. In the context of state-of-the-art electronic systems including sensors and actuators from different physical domains and mixed-signal electronics, we pointed out the gaps existing in the implementation of this design flow using current tools. Typical tools are indeed inappropriate to jointly handle different domains as well as different levels of abstraction. These gaps are bridged by the analog and mixed-signal extensions of hardware description languages (HDL-AMS). Based on these languages, it is possible to implement a more efficient design flow for increased reliability and requiring less prototypes, i.e. reducing costs.

The efficient handling of different levels of abstraction also allows to build semi-automated design methodologies upon the HDL-AMS design flow. To implement these design methodologies, specifications must be put into a hierarchy to define a performance metric. Following the HDL-AMS structures, we identify one ENTITY to each subsystem. The subsystem is tuned to comply with the specifications through the ENTITY GENERICS. Depending if the specifications and GENERICS are linked by analytical expressions or by data tables, the GENERICS are computed directly or by optimization, based on previous knowledge or not. The extraction of the subsystem performance is done by a simulation of the corresponding model; the model is well-tuned if the simulated performance meets the specifications.

Our work contributes to the development of semi-automated design methodologies for analog electronics. The analog ID card (part I) indeed allows to efficiently characterize the transistor performance and as it is design oriented, its integration in top-down design methodologies is quite straightforward. Our work deals with major analog performance parameters: gain and gain-bandwidth product, the random mismatch which can be applied to the determination of the offset voltage and the third-order harmonic distortion of transistors operating in triode regime. We illustrate these contributions through the design of a MOSFET-C integrator as an example. The study of the continuous-time $\Delta\Sigma$ modulator of chapter 6 helps to put the specifications into a hierarchy and proposes as result a knowledge-based optimization method for the design of the integrators with respect to the $\Delta\Sigma$ modulator specifications. Our work contributes to the set-up of a semi-automated choice of the integrator architectures. We proposed, for current bottlenecks of analog designs, different semi-automated design methodologies for cases where an analytical link exist between the specifications and the GENERICS (amplifier) and for case where the link is only known by data tables (mismatch, third-order harmonic distortion, integrators of continuous-time $\Delta\Sigma$ modulators).

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Chapter 8

Conclusions

State-of-the-art high-performance electronic systems impose severe restrictions on the power consumption due to the move to portable applications. A highly competitive market moreover imposes ever shorter time-to-market and continuous pressure for lowering the costs. The downscaling of the technologies drastically improves the speed of the devices but also reduces the dynamic range available in analog applications. On the other hand, focusing on electronics to be operated in harsh environments, cost and safety reasons impose hard constraints on the reliability. Methodologies and tools are thus needed to ensure proper operation of electronic systems mixing analog and digital circuits but also possibly sensors and actuators. For increased efficiency, the cost and the power issues must be assessed at all hierarchical description levels of a system. Efficient design should be the result of concurrent top-down design starting from the system specifications and ending with the sizing of the MOSFETs as well as bottom-up validation, converting the actual device power-speed characteristics trade-offs into the system performance. A lot of power and cost can indeed be saved by efficiently partitioning the specifications among the different subsystems but this is only possible if the different subsystem and technology power-specification trade-offs are known and can be simulated together.

This thesis contribution has been to fill still existing gaps in this ideal design flow for analog circuits, first by defining and characterizing MOSFETs analog figures-of-merit, which enable the efficient, pertinent, reliable transmission of the information on the device to the analog cell designer (part I) and secondly by developing VHDL-AMS models of various analog cells, which allow the evaluation of the influence of the analog cells in a mixed-signal circuit (part II). The use of these models has been studied using a third-order continuous-time $\Delta\Sigma$ modulator as test vehicle (part III).

In part I, the MOSFET figures-of-merit have been gathered in a MOSFET analog ID card intented to provide design relevant information on the device performance to the analog cell designer. The basic analog parameters like the gain (Av) and the gain-bandwidth product (GBW) have been studied as well as two important MOSFET imperfections: the third-order harmonic distortion (HD3) of MOSFETs biased in the triode regime and the MOSFET mismatch in weak and moderate inversion.

We started from a common-source amplifier to define the figures-of-merit concerning the gain (Av) and gain-bandwidth product (GBW) of analog circuits and used the transconductance over drain current ratio $\frac{gm}{I_D}$ vs. normalized current ($Inorm$) as pivot

of our characterization methodology. It is indeed a design-oriented characteristic obtained from measurements, which we proved still relevant in deep-submicron CMOS technologies and in a wide temperature range to efficiently assess and compare different devices. The analog figures-of-merit for Av and GBW are thus $\frac{gm}{I_D}$ and the Early voltage V_{EA}. The figures-of-merit were first used to compare the performance of bulk, partially-depleted (PD) and fully-depleted (FD) silicon-on-insulator (SOI) MOSFETs on technologies with a nominal gate length ($Lnom$) of 0.12 μm. It has been shown that the benefit of the FD SOI are maintained even for the shorter transistors. In deep-submicron CMOS technologies, as additional implantations (HALO dopings) are used to better control the threshold voltage (Vth) and maximize the on-to-off current ratio for very short channel transistors, we assessed their influence in the case of the three mentioned technologies. The predicted negative influence of the HALO doping has been here confirmed for long-channel transistors targeting high-gain and for devices targeting high-frequency operation and biased in strong inversion on various technologies. On another hand, the characterization methodology has also been applied to investigate the possibility of using a deep-submicron ($Lnom = 0.15$ μm) multi-Vth FD SOI technology for applications up to 250°C. The figures-of-merit indicate that, surprisingly, the short-channel MOSFETs can be safely used for analog applications up to 250°C. Moreover, digital figures-of-merit also indicate that the most heavily doped MOSFETs are suitable for digital applications at maximum temperature. This extends the advantage of FD SOI for operation in harsh environments in the case of short-channel transistors. The figures-of-merit were shown to efficiently compare different device types in various practical bias configurations and temperature range and provide a quick and accurate insight into the device performance for a given analog application.

We next focus on the linearity of applications in which MOSFETs are biased in the triode regime and used as tunable resistors. Focusing on fully-differential continuous-time MOSFET-C filters, we defined the third-order harmonic distortion (HD3) as figure-of-merit. Based on measurements of a multi-Vth PD SOI technology with $Lnom = 0.12$ μm in a wide temperature range, the HD3 was extracted for the 2-MOS and the 4-MOS resistive structures. Multi-Vth process allowed a discussion of the scaling of the oxide thickness (t_{ox}), channel doping (N_A) and hence Vth, mobility, mobility reduction with vertical field and body factor, on the HD3 performance of MOSFETs in the triode regime. The extractions performed on the 2-MOS structure using various device types and from 25°C up to 225°C highlight the interaction of body and mobility reduction related effects. A design-oriented comparison methodology was developed to help the analog designer in selecting the best device type, gate bias range and resistive structure in practical design conditions, i.e. ensuring the optimal or targeted HD performance can be reached in the whole tuning range, necessary to compensate on-chip for process and temperature variations. This measurement-based methodology can be applied to any device on any technology without the need for still lacking precise models. Applied to this particular case, the methodology revealed that HD3 levels of at least -60 dB can be reached by all the device types in the whole temperature range for a dynamic range (DR) of 400 mV under low supply voltage condition (1.5 V). Surprisingly, for the optimization targets considered here, the devices normally designed for digital applications (thin gate oxide, low Vth) exhibit the best performance.

The last MOSFET imperfection with which we dealt is the MOSFET mismatch in the weak and moderate inversion. We started from drain current mismatch measurements for

various MOSFET sizes on a 0.35 μm bulk CMOS and from a 2 μm FD SOI in a wide temperature range ($25°C - 225°C$). The drain current mismatch in weak inversion is usually said to be determined only by threshold voltage mismatch. Based on our mismatch measurements on very different technologies, we checked the validity of this assumption and showed that additional parameters should be included in the mismatch models. The comparison of the measurements on the two technologies furthermore allowed us to identify the additional physical phenomena playing a role in determining the drain current mismatch in moderate and weak inversion. We consequently proposed a semi-empirical term based on the dependence of the n body effect factor on the gate voltage V_G to better model the mismatch in the weak and moderate region of inversions. Finally, we included the measured mismatch data in an analog top-down design methodology and applied it to the design of a current mirror for the input stage of an amplifier. This analysis predicts that, for a constant bias current, the random mismatch between the drain currents of the two MOSFETs constituting the mirror may actually decrease when they are biased towards the weak inversion. The mismatch indeed decreases if its increase linked to the higher $\frac{gm}{I_D}$ in weak inversion is compensated by the decrease associated to larger transistor dimensions, contrarily to the conclusion of traditional simple design guidelines.

In part II, we developed behavioral models for different analog cells to be combined to form a continuous-time $\Delta\Sigma$ modulator, which will be used as a test vehicle for the application of the models in a mixed-signal circuit. These basic analog cells are the amplifier described both as OTA and Opamp, the comparator and the digital-to-analog converter. The analog cell models describe the imperfections at the behavioral level in order to assess their influence on the mixed-signal circuit performance. Aside the classical imperfections like amplifier finite gain, amplifier finite bandwidth or comparator hysteresis, the models include the jitter on the clocks, the white noise associated to the different elements as well as the amplifier linearity. A white noise generator was developed in VHDL-AMS for increased portability of the models. Moreover, models are design-oriented as they implicitly take into account the influence of the cell environment, i.e. input and output impedances of following and preceding cells. For describing our cells, we took care to use only parameters on which the designer has an influence. For example, in the case of an amplifier and to describe the pole on the output node, the model only fixes the output resistance while the capacitance, and accordingly the pole position, is defined by the input capacitance of the subsequent stage. The models are detailed enough to be compared with transistor-level simulation or realization and can then also be used in the design of the test set-up. This would allow to start the test development earlier in the design cycle, shortening the time-to-market.

These behavioral models are used in a practical case in (part III). The mixed-signal test vehicle is a continuous-time $\Delta\Sigma$ modulator. In the context of operation at high temperature and reduction of the power consumption, the analysis of the operation of continuous $\Delta\Sigma$ modulators indeed reveals interesting possibilities; these are confirmed by the benchmarking of the recently published $\Delta\Sigma$ modulators targeting medium to high resolution for a signal bandwidth lower than 100 kHz. The detailed analysis of state-of-the-art analog-to-digital converter targeting high-temperature applications further stresses the potential benefits of continuous-time $\Delta\Sigma$ modulators. The design of the $\Delta\Sigma$ modulators at the transfer function level has been briefly reviewed and trade-offs pointed out as well as issues related to the integrator implementation. We used VHDL-AMS models to evaluate the influence of analog cells imperfections on the modulator performance. The models were

shown to be able to support a top-down design methodology of the integrators targeting low power consumption. Continuous-time ΔΣ imposes specific constraints on the feedback DAC, which have also been assessed.

In summary, in this thesis, we have demonstrated that in the search for top-down analog design flow :

- The link between the technology or device characteristic and the analog cell performance could be efficiently done for deep-submicron devices and in a wide temperature range using the $\frac{gm}{I_D}$ characteristic for the major analog parameters. Furthermore, this link can include two MOSFET imperfections: the mismatch and the linearity in triode regime using the developed characterization methodologies.
- The link between the analog cell and the mixed-signal system can be made through behavioral models written in VHDL-AMS and including the analog block imperfections.
- The analog ID card in combination with VHDL-AMS enables a more efficient analog design flow.

Focusing on analog design in deep-submicron technologies, we applied the improved top-down analog design flow to practical cases and

- we showed that silicon-on-insulator transistors of a well-optimized process with short channels of 0.15 μm can safely be used for mixed-signal operation up to $250^{\circ}C$ and we recommend (i) to avoid in analog transistors, if possible, the use of HALO dopings, except for short-channel devices targeting low-frequency of operation and high gain; and (ii) to use fully-depleted silicon-on-insulator instead of bulk transistors even in deep-submicron technologies.
- we showed that in a particular silicon-on-insulator process, 0.1% of linearity can be attained in a wide temperature range ($25 - 150^{\circ}C$) using MOSFETs in triode and we recommend to use the resistive structure based on four transistors in deep-submicron processes.
- the mismatch between the drain current of the transistors of a current mirror can be possibly improved by biasing the transistors of the current mirror in weak or moderate inversion instead of strong inversion.
- we recommend to use active RC integrators with passive resistors and capacitors to implement the loop filter of continuous-time ΔΣ modulators targeting a resolution superior to 10 *bits*.

8.1 Suggestions for future work

To go further, we briefly point out some directions in which we think further research should be carried on.

- While the mutual influence of the body effect and of the reduction of the mobility was clearly identified for the 2-MOS resistive structures, the 4-MOS still need improved

modeling and understanding. The HD3 trends vs. gate bias and temperature are indeed less clear than for the 2-MOS structure and require a deeper physical insight.

- The proposed semi-empirical term to better model the mismatch in the moderate and weak inversion should be included in a complete drain current mismatch description. Additionally, chip-to-chip variations and more particularly, the inclusion of yield information into analog top-down design methodologies also deserve a special attention.

- A big advantage of mixed-signal hardware description languages is to finally define a common description and documentation for the analog circuits. Additional constraints must be added to make it a design tool. The mixed-signal circuit should be described by a well-defined hierarchical system, starting from a highly abstract description of the system and ending with a detailed description of the different cells. The parameters of the abstract description should be moreover expressed as a combination of the cell parameters in order to support the top-down design and bottom-up validation. This kind of methodology has been applied to determine the specifications of the blocks of a frequency synthesizer starting from the requirements of a telecommunication standard [1]. The link between the analog cells and the mixed-signal circuits would be furthermore improved if besides its actual outputs the model would evaluate the power-specifications trade-offs. At each level of description, a model should output a *cost* parameter, reflecting the power needed to reach the specifications and possibly the cell design and test complexity. If the costs are propagated to the most abstract level, it would enable the designer to evaluate high-level trade-offs taking implementation costs into account. Then, as proposed in [2], an optimization algorithm at the most abstract description level would be able to determine the specifications for each block while minimizing the global cost.

- The developed VHDL-AMS models describe the $\Delta\Sigma$ modulator on one side at the integrator transfer function level and on another side as a structural description of an active RC amplifier. A link between these two descriptions should be made, as proposed here above, in order to directly convert the results of the design at the transfer function level into sizing guidelines for the structural description. The evaluation of design trade-offs is particularly tricky in this case of $\Delta\Sigma$ modulators as the modulator performance evaluation for different cell parameters can be lengthy. These models should then be associated to an optimizer, showing both the trends and the most sensitive parameters to the designer. Combined with the approach proposed here above, it could then be the basis of a tool assisting the designer and guiding him to the right choices.

- Concerning the $\Delta\Sigma$ the next step is evidently the implementation of the continuous-time modulator to experimentally verify the identified potential. The improvement of the performance by a better design of the transfer function seems worth to be carried on. Local feedback loops could decrease the linearity constraints and improve the resolution. For much higher resolution at high temperature, the multi-bit approach should be preferred to the cascade option. Indeed, cascade modulators have been shown to be useless in discrete-time $\Delta\Sigma$. Dynamic element matching could indeed help to lower the modulator sensitivity to circuit impairment at high temperature, provided the digital circuits would work at high temperature. This should however not be a problem if the operating frequency is not too high. Moreover, multi-bit modulators would reduce the modulator sensitivity to the jitter, one of the major drawbacks of continuous-time

$\Delta\Sigma$. Multi-bit continuous-time $\Delta\Sigma$ modulators have already been validated at room temperature [3] [4] [5].

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Part V

Appendices

Appendix A

Mixed-mode applications in $0.15\mu m$ CMOS at $250°C$

In section 2.2.2, we already showed that 0.15 μm FD SOI devices could be safely used for analog applications up to $250°C$. Here, we will focus on digital applications showing the potential of 0.15 μm FD SOI devices for mixed-signal applications at high temperature. We also point out some particular temperature dependence mechanisms of the physical leakage current ($Ileak$) and the threshold voltage (Vth) in advanced deep-submicron processes.

The device parameters are as defined in section 2.2.2. We here focus on the high speed (low Vth) and low leakage (high Vth) device types as undoped devices with $Vth \approx 0\ V$ preferably target analog applications. Even if the process is FD, low-leakage devices exhibit partial depletion in normal circuit condition (i.e. when $0\ V$ is applied at the back gate) already at room temperature. For such back gate bias, the drain current vs. gate voltage (V_G) characteristics corresponding to different back gate biases are indeed superposed (Fig.A.1) and the devices become fully-depleted when a positive voltage is applied to the back interface.

We use the evolution with temperature of the on-to-off drain current ratio ($Ion/Ioff$), $Ileak$ and Vth as figures-of-merit to assess the potential of a technology for digital applications.

Ion and $Ioff$ are extracted for a drain voltage (V_D) of $1\ V$ and for a gate voltage $V_G = 1.5\ V$ and $0\ V$, respectively. If we consider that $Ion/Ioff = 10^4$ is sufficient for reliable digital cell operation, the 5 μm long-channel devices exhibit satisfactory performance in almost the whole temperature range for both low leakage and high speed devices (Fig.A.2). While high speed short-channel MOSFETs ($L = 0.15\ \mu m$) stop working correctly above around $125°C$, the 0.15 μm long low leakage devices can be safely used up to around $250°C$ in digital applications (Fig.A.2).

$Ileak$ is extracted at V_G such that it corresponds to the negative V_G plateau of I_D. For 10 μm long MOSFETs, at $250°C$, $Ileak = 10\ [pA/\mu m]$ and for 0.15 μm long transistors at the same temperature, $Ileak$ is still equal to $0.1\ [nA/\mu m]$, a remarkably low value for deep-submicron devices. Concerning the leakage current, short-channel devices of both types can safely be used up to the maximum temperature. Fig.A.3 presents the measured leakage currents for high speed and low leakage devices with gate lengths of 0.15 μm and

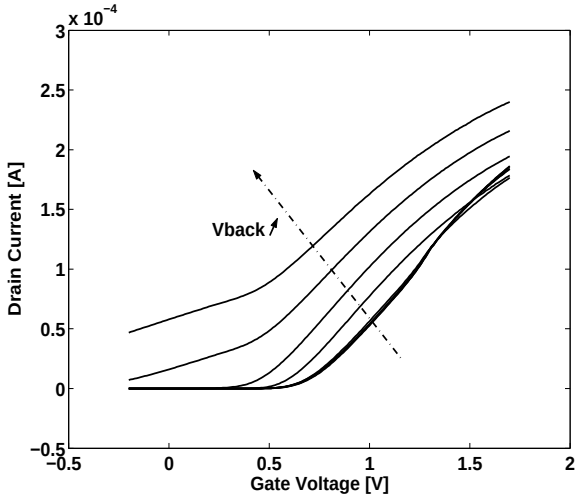

Figure A.1: Measured I_D vs. V_G corresponding to a back gate voltage ($Vback$) varying from $-40\ V$ to $40\ V$ in $10\ V$ steps. nMOSFET low leakage with $L = 0.5\ \mu m$ and $W = 10\ \mu m$, $V_D = 50\ mV$ and $V_S = 0\ V$.

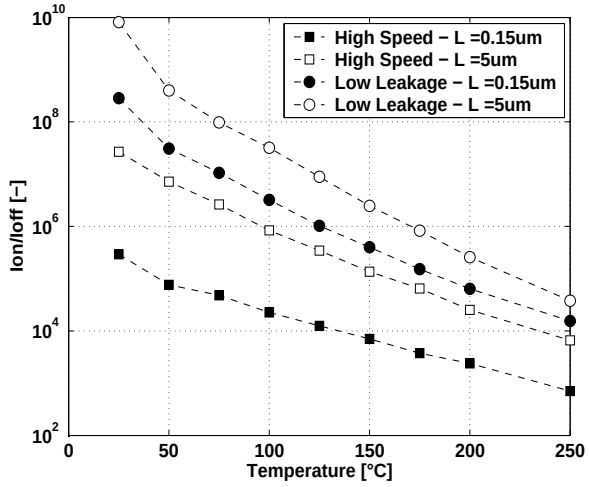

Figure A.2: Measured $Ion/Ioff$ ratio vs. temperature for n-type high speed (□) and low leakage (○) MOSFETs. Ion is measured for $V_G = 1.5\ V$, $Ioff$ for $V_G = 0\ V$. $L = L_{nom} = 0.15\ \mu m$ (full symbols) and $L = 5\ \mu m$ (void symbols). $W = 10\ \mu m$, $V_D = 1\ V$ and $V_S = 0\ V$.

5 μm from room temperature up to 250°C.

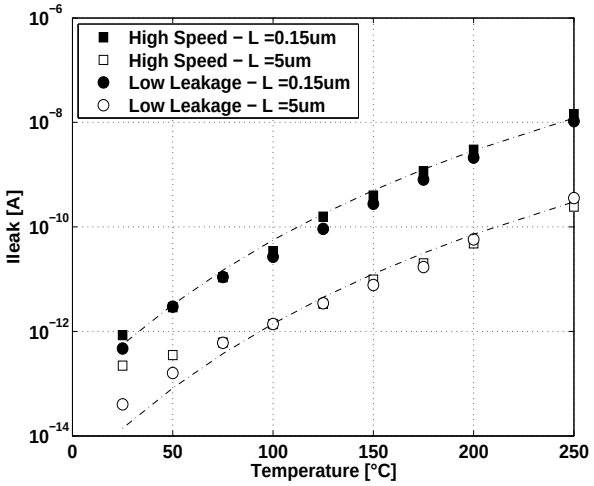

Figure A.3: Measured $Ileak$ **[A] vs. temperature for n-type high speed (□) and low leakage (○) MOSFETs. The dotted lines show the proportionality to** ni**.** $Ileak$ **is measured for** V_G **such that we are in the plateau region.** $L = L_{nom} = 0.15\ \mu m$ **(full symbols) and** $L = 5\ \mu m$ **(void symbols).** $W = 10\ \mu m$**,** $V_D = 1\ V$ **and** $V_S = 0\ V$**.**

In general, the leakage current of SOI MOSFETs is made of two components: generation current in the depletion region and diffusion current from the undepleted part of the silicon film. As it can be seen from the figures, even if the device sizes are scaled down to the deep-submicron level, the leakage current at high-temperature keeps the same tendencies as long channel devices and follows a dependence proportional to the intrinsic carrier concentration (*ni*), which is attributed to the generation mechanisms. Moreover, the same dependency is observed for both high speed FD devices and low leakage PD devices. So, whereas the low leakage devices are partially depleted, the mechanism, which dominates the leakage currents at high temperature and for $V_D = 1\ V$, is the generation in the reverse-biased drain-body junctions and not the diffusion from undepleted body at least up to 250°C. This is probably due to the higher doping concentration N_A in advanced deep-submicron processes, rejecting the transition from generation to diffusion mechanisms to higher temperature [1].

Measured Vth of the different devices are also represented vs. temperature (Fig.A.4), showing a limited degradation of Vth. The temperature dependence of Vth with temperature is given next to the curves.

From the threshold voltage point-of-view, short-channel devices can also be used in digital applications up to 250°C. The PD low leakage devices exhibit surprising small dependence on the temperature. This is due to the fact that the Vth evolution with temperature is determined for a bulk or PD device by

$$\frac{\partial Vth}{\partial T} \propto \frac{\Phi_F}{\partial T} + \frac{1}{C_{ox}} \frac{\partial Q_{depl}}{\partial T} \tag{A.1}$$

where Φ_F is the Fermi potential, C_{ox} is the front oxide capacitance and Q_{depl} is the depletion charge. In deep submicron devices, N_A is increased and thus, $\frac{\Phi_F}{\partial T}$ is decreased

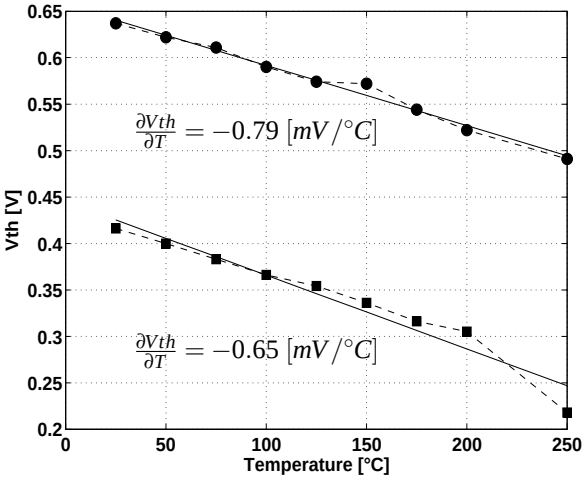

Figure A.4: Measured Vth [V] vs. temperature for n-type high speed (■) and low leakage (•) MOSFETs. $W = 10\ \mu m$ **and** $L = L_{nom} = 0.15\ \mu m$**.** $V_D = 50\ mV$ **and** $V_S = 0\ V$**.**

and $\frac{\partial Q_{depl}}{\partial T}$ is increased. Two antagonist phenomena are thus taking place, $\frac{\partial Q_{depl}}{\partial T}$ being weighted by $\frac{1}{C_{ox}}$, smaller with thinner gate oxide [1]. With thinner front gate oxide, the Vth dependence with temperature of the PD and Bulk will be more and more similar to FD devices for which

$$\frac{\partial Vth}{\partial T} \propto \frac{\Phi_F}{\partial T} \tag{A.2}$$

Using Ion-to-$Ioff$ ratio, $Ileak$ and Vth as figures-of-merit for the digital applications, we may conclude that short-channel low leakage devices can safely be used in digital applications up to $250^{\circ}C$. Following section 2.2.2, we conclude that these deep-submicron devices are suitable for mixed-signal operation up to $250^{\circ}C$.

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Appendix B

Peculiarities of MOSFET HD3 in triode

The third-order harmonic distortion (HD3) of MOSFETs in the triode regime has been investigated in chapter 3 for the 2-MOS and 4-MOS resistive structures (Fig.3.1). This section first provides additional information on the device parameters, which are not included in chapter 3 for the sake of conciseness and then investigate more deeply the influence of the connections between the PD SOI MOSFET body and other terminals. Finally, we start from the EKV expression of the drain current to obtain a description of HD3 in triode, symmetrical with respect to the MOSFET source and drain and show that the actual EKV drain current model is unable to correctly predict the HD3 in triode.

A) To complete the discussion on the evolution of the *n* body effect factor, we here below represent the *n* factor for the GO1 LL (thin-gate oxide, high Vth) and the GO2 (thick-gate oxide) devices (Fig.B.1).

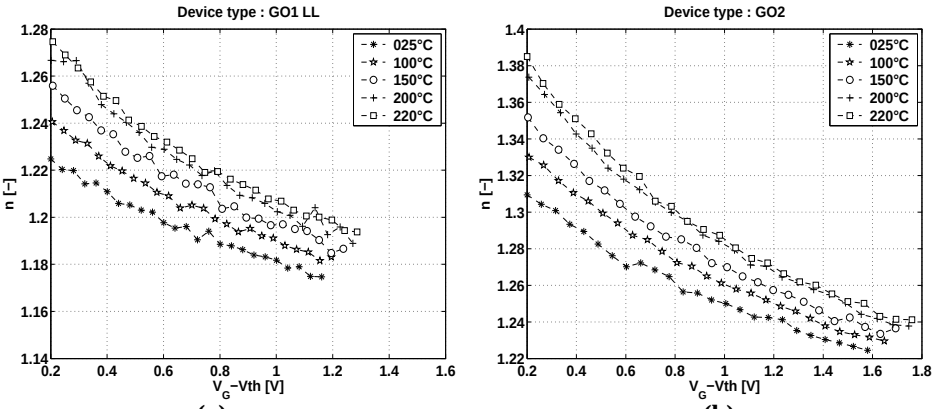

Figure B.1: *n* **body effect factor in strong inversion [-] vs.** $V_G - Vth$ **for (a) GO1 LL device (thin-gate oxide, high** Vth**) and (b) GO2 (thick-gate oxide) device at different temperatures.** $W = 10\ \mu m$ **and** $L = 10\ \mu m$**.**

B) In analog applications and in order to avoid floating body effects, the body of partially-depleted (PD) SOI MOSFETs is usually connected to their source. In our partic-

ular case, the MOSFET terminals corresponding to the source and the drain are connected on one side to the input signal and on the other side to the amplifier inputs (Fig.3.1). The input signal is a varying voltage source with an amplitude (*Va*) around a fixed DC bias (*Vo* in Fig.3.1). If the amplifier gain is sufficient, the amplifier inputs can be considered as a fixed potential. The usual connection of the body to the source is then irrelevant as the source and drain alternatively move from one terminal to the other, depending if the voltage source has a positive or negative value with respect to the virtual ground of the amplifier. In Fig.B.2 and Fig.B.3 we compare the HD3 performance of the 2-MOS and 4-MOS structures in two different configurations: when the body is connected to the fixed potential and when it is connected to the varying signal source. In all cases, the measured gate current was negligeable.

For all devices and for the 2-MOS structure, the HD3 improves if the body is connected to the varying signal source (Fig. B.2). In this case, the body potential indeed tracks the input. Let us denote fix the fixed potential terminal and *var*, the varying one.

For positive input signals, the junction between the body and fix (i.e. source) will be forward bias. The Vth is then decreased and an additional current is flowing in the device, increasing the current for same input voltage (Fig.B.4); the linear region of the $I_D - V_D$ characteristic is extended. For negative input signals, the Vth is on the contrary increased and less current is flowing through the device (Fig.B.4). Moreover, as in the resistive structures, the voltage across the MOSFET terminal is varied around $0\ V$, our HD3 analysis starts from $I_D - V_D$ characteristics with V_D varying from $-0.5\ V$ to $0.5\ V$. While for positive V_D, the characteristic is like a common $I_D - V_D$ characteristic, the curve corresponding to negative V_D is in fact closer to a $I_D - V_G$ characteristic. In this last case, V_G is indeed fixed at a positive value, V_S is set to $0\ V$ and V_D has a varying negative value. The results presented here thus show that the HD3 of MOSFET in the triode regime is in fact dominated by the behavior in the first quadrant, i.e. for positive V_D. The HD3 indeed improves as the linear region is extended when we connect the body to *var*. The HD3 behavior is however not strongly modified and the conclusions drawn in chapter 3 are still valid. For the 4-MOS structure using thick oxide GO2 devices, the HD3 is also decreased when connecting the body to *vary* (Fig.B.2). HD3 of GO1 devices (thin oxide) in the 4-MOS configuration exhibit a compensation peak. The HD3 of devices with a body-to-*vary* connection is here slightly higher for V_G after the compensation peak due to differences in the peak location for the two different body connections. This further stresses the need for improved understanding and modeling of the 4-MOS structure.

C) In [1], the HD3 of a bulk MOSFET biased in triode is described as

$$HD3 \propto \frac{-1}{V_{GS} - Vth}\left(\frac{\theta}{2} - \frac{\gamma}{12\,(V_{SB} + \phi_b)^{3/2}}\right) \tag{B.1}$$

where θ is the mobility reduction coefficient, γ is the body effect coefficient, V_{SB} is the source-to-bulk voltage and ϕ_b is the surface potential in strong inversion. This expression is however based on an asymmetrical description of the MOSFET, i.e. if we swap the source and drain terminals, we don't obtain the same expression for HD3. This is unrealistic and unappropriate as in the applications under concern here, the drain and source are swapped continuously as explained just above. Here below, we report an unsuccessful attempt to derive the HD3 of MOSFET in triode using the EKV formalism. We identify the assumption in the EKV formalism leading to its impossibility to correctly model the HD3 in triode.

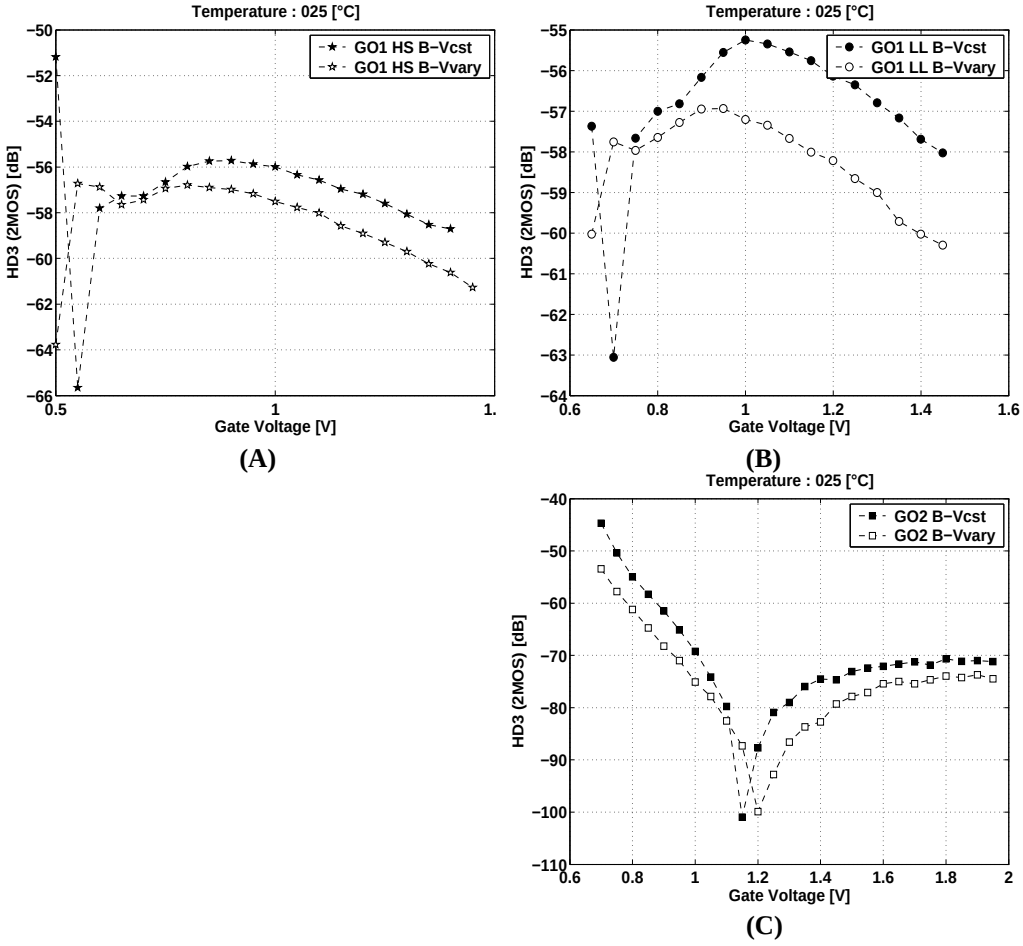

Figure B.2: HD3[dB] vs. V_G for 2-MOS structures composed of devices GO1 HS (thin-gate oxide, low Vth)(A), GO1 LL (thin-gate oxide, high Vth)(B) and GO2 (thick-gate oxide) (C) with body connected to the fixed potential terminal (full symbols) and with body connected to the varying signal source (void symbols). All devices are $10\ \mu m$ long and $10\ \mu m$ large. $Va = 200\ mV$ around $Vo = 0\ V$, at room temperature.

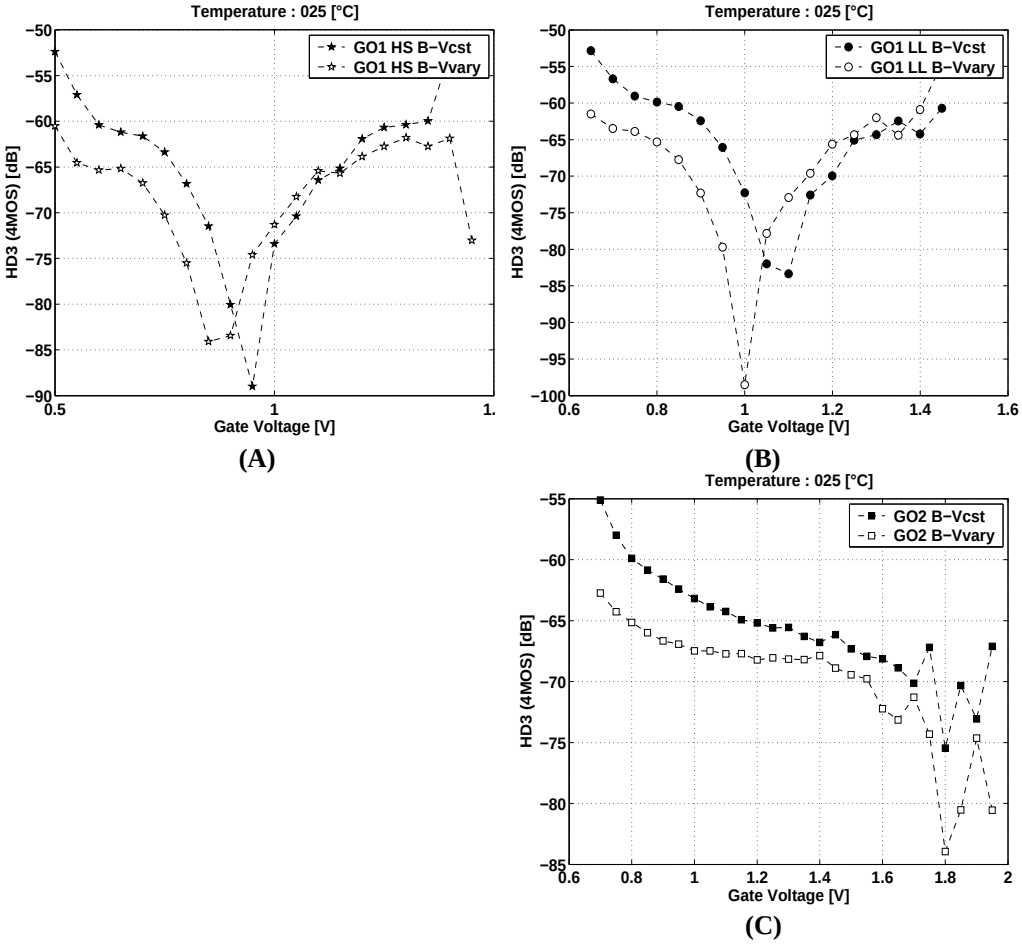

Figure B.3: HD3[dB] vs. V_G for 4-MOS structures composed of devices GO1 HS (thin-gate oxide, low Vth)(A), GO1 LL (thin-gate oxide, high Vth)(B) and GO2 (thick-gate oxide) (C) with body connected to the fixed potential terminal (full symbols) and with body connected to the varying signal source (void symbols). All devices are $10\ \mu m$ long and $10\ \mu m$ large. $Va = 200\ mV$ around $Vo = 0\ V$, at room temperature.

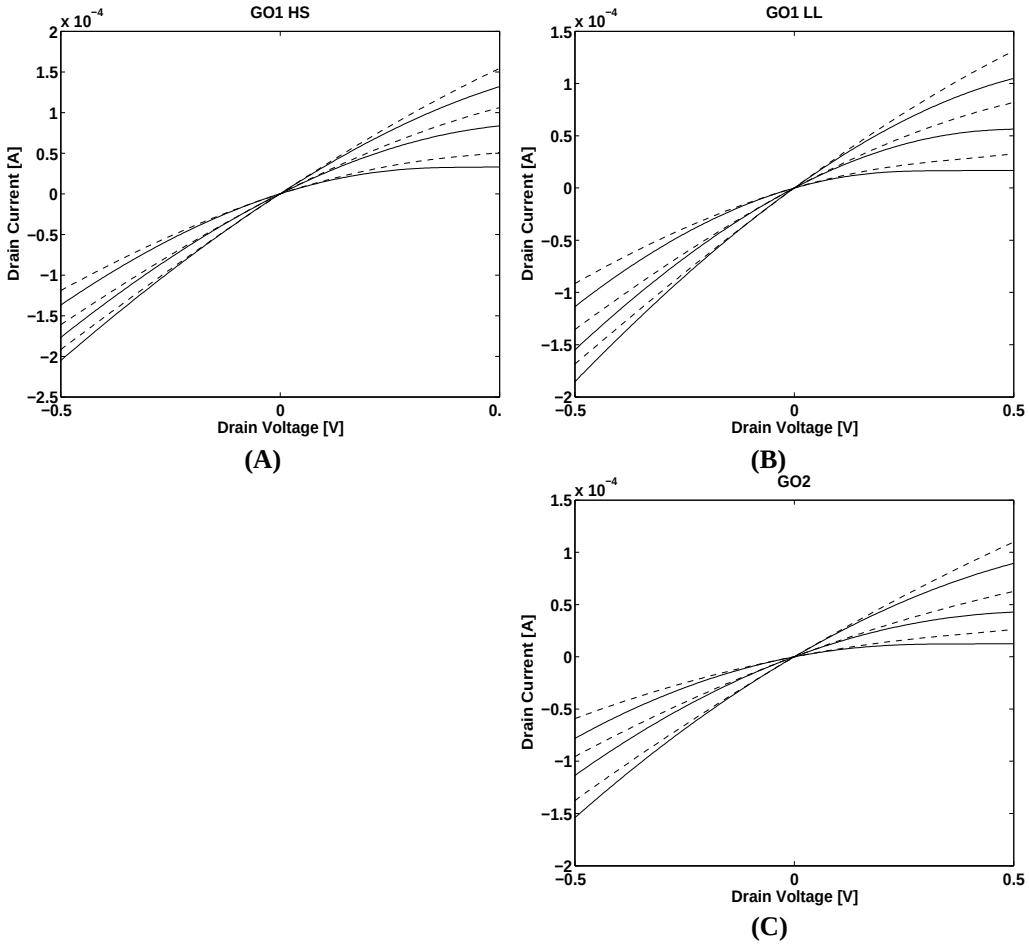

Figure B.4: $I_D\ [A]$ **vs.** $V_D\ [V]$ **at different** V_G **for GO1 HS devices (thin-gate oxide, low** Vth**)(A), GO1 LL (thin-gate oxide, high** Vth**)(B) and GO2 (thick-gate oxide) (C) with body connected to the fixed potential terminal (full line) and with body connected to the varying signal source (dashed line). The different** V_G **are:** 0.7**,** 1 **and** $1.3\ V$ **for the thin-oxide GO1 and** 0.8**,** 1.15 **and** $1.6\ V$ **for the thick-oxide GO2 devices. All devices are** $10\ \mu m$ **long and** $10\ \mu m$ **large;** $V_S = 0\ V$**, at room temperature.**

The EKV expression for the current in triode regime is [2]

$$I_D = I_F - I_R \tag{B.2}$$

$$I_{F(R)} = \frac{n\mu C_{ox}}{2}\frac{W}{L}\left(V_P - V_{S(D)}\right)^2 \tag{B.3}$$

$$I_D = n\mu C_{ox}\frac{W}{L}\left[V_P - \frac{V_S + V_D}{2}\right](V_D - V_S) \tag{B.4}$$

where V_P is the pinch-off voltage and I_F and I_R are respectivey called the forward and reverse current. In our case, $V_S = 0\ V$, V_G is kept at a fixed bias, ensuring that the device is working in the triode regime and the input signal is applied to the drain. The mobility dependence on the vertical field may be introduced in (B.4) by [2] $\mu = \frac{\mu_0}{1+\theta V_P}$ where μ_0 is the low-field mobility and θ is the mobility reduction factor. On another hand, for rather weak non-linearities $HD3 \propto \frac{T_3}{T_1}$ where T_1 and T_3 are, relatively, the first and third-order coefficients of the Taylor expansion of the output-input characteristic, i.e. I_D-V_D in our case. Finding the Taylor expansion coefficients of (B.4), we find that HD3 is infinite as the derivatives $\frac{d^n I_D}{dV_D^n}$ are equal to zero for $n > 2$. To solve this problem, a description of μ and n depending on V_D and V_S must be included. Such a description for μ can be found in [3] e.g. but it is not possible for n in the EKV formalism as it indeed defines n as [2]

$$n = \frac{\partial V_G}{\partial V_P} = 1 + \frac{\gamma}{2\sqrt{\psi_0 + V_P}} \tag{B.5}$$

$$V_P = V_G - Vth - \gamma\left[\sqrt{V_G - Vth + (\psi_0 + \frac{\gamma}{2})^2} - (\psi_0 + \frac{\gamma}{2})\right] \tag{B.6}$$

where γ is the body-effect factor and ψ_0 is equal to $2\phi_F +$ several U_T, ϕ_F being the fermi potential and U_T is the thermal voltage. V_P and thus n are then independent of V_S and V_D in the EKV formalism. It is then impossible to derive an expression for the HD3 using the EKV formalism in which n would play a role. We saw however how the HD3 characteristic, in the case of the 2-MOS structure, is determined by the mutual influence of the body-effect and mobility reduction coefficients (Fig. 3.2). The HD3 for a MOSFET in triode is then impossible to obtain in the EKV formalism unless a dependence of the pinch-off voltage V_P on the drain and source voltage is added.

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Appendix C

State-of-the-art of drain current mismatch models

The mismatch in a certain component is defined as the variation in the value of identically designed components. When examining measurements of identically designed devices placed all over a wafer, one can distinguish two different mismatch types. These two mismatch types are called systematic and random, respectively.

A deterministic trend can first be observed in the measured data as a deterministic function of the position of transistors far away from each other, this is the systematic mismatch. The underlying phenomena causing systematic mismatch are variations in gate dimensions, gate-oxide thickness gradients, variations in channel doping, micro-loading effects among others [1] [2]. Since the systematic mismatch is a deterministic phenomenon, it is possible to predict it precisely. The deterministic trend can indeed be approximated by a gradient-like function. For small and medium sized wafers, these gradients can be represented by planes [3] [1] (Fig. C.1).

Modeling the systematic mismatch can then be done by finding the best plane which fits the measured data. In section C.2, we will deal more precisely with systematic mismatch and with the underlying causes.

Transistor parameter mismatch caused by systematic mismatch can be minimized by layout techniques. One has to follow a set of *good layout* rules [4] [5] [2]. We will then focus on the random mismatch in the following.

The remainder of the mismatch is called random mismatch. The causes of this second type of mismatch are [6] edge effects, implantation charges profile variations, local oxide thicknesses and mobility effects. Given the stochastic nature of this second type of mismatch, it cannot be predicted accurately. The aim of a random mismatch model is hence to characterize the mismatch variance as precisely as possible. This kind of mismatch deals with devices close to each other.

The value of a transistor parameter P, supposing the transistor is located at coordinates

(i, j) on the wafer, can then be expressed as

$$P_{(i,j)} = \overline{P_{(i,j)}} + \sigma(P) \times (rand) \tag{C.1}$$

where $\overline{P_{(i,j)}}$ is the parameter P mean value at coordinates (i, j), *rand* is a random number distributed as a normal variable with zero mean and unity variance and $\sigma(P)$ is the standard deviation of P determined by the random mismatch model. $\overline{P_{(i,j)}}$ can be calculated using the best fit plane as explained above. In [2], the systematic part of the mismatch is estimated to contribute for approximately 40% [1] of the total mismatch. It is then important not to underestimate this part. On the other hand, there is little discussion about modeling systematic mismatch using best fit planes as long as the wafer size is not too large. We will then focus on random mismatch modeling here.

This appendix is organized as follows. We will begin with a review of four major existing theories (Section C.1). Most of these theories deal as we will see with transistors working in strong inversion. These models are sometimes said to be continuous from weak to strong inversion as the fitting of the corresponding mismatch model parameters is performed across the different regions of operation.

C.1 Existing theories

We will start this section with Pelgrom's mismatch model [6]. Following the model developed by Bastos in [5], we will then show that Pelgrom's model can be not appropriate anymore when devices dimensions are scaled. We will then present an other model which

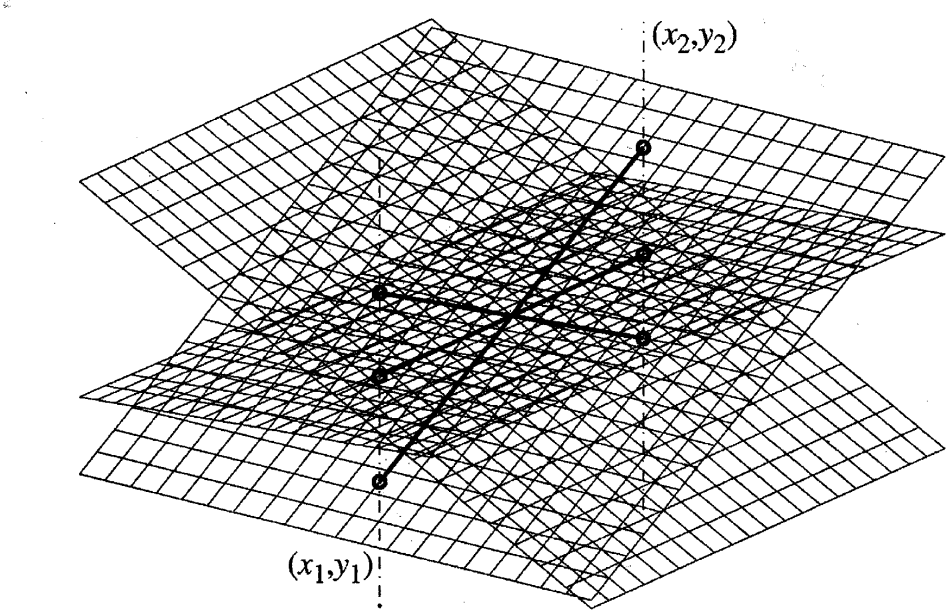


Figure C.1: The deterministic trend in the parameters value can be approximated by planes for small and medium sized dies [3]

was developed by Serrano [3]. In the last part of this section we will briefly review a last model developed by Croon [7]. These two last models are presently the most *continuous* across the different inversion regimes. Note that for the sake of simplicity we will use the term *mismatch* even if *random mismatch* is the correct terminology.

C.1.1 Pelgrom's model

For Pelgrom, the mismatch in a parameter P is modelled as a mismatch generating source filtered by a spatial filter function called *geometry function* [6]

$$\sigma^2_{(\Delta P)} = \frac{1}{4\pi^2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} |G(\omega_x,\omega_y)|^2 S_p(\omega_x,\omega_y)d\omega_x d\omega_y \tag{C.2}$$

where $S_p(\omega_x,\omega_y)$ is the mismatch source spectral density and $G(\omega_x,\omega_y)$ is the Fourier transform of the geometry function. This last function depends on the layout of the transistors. ω_x and ω_y are the Fourier representations of the spatial variables x and y.

The mismatch source represents all the different physical phenomena responsible of mismatch.

Random mismatch source spectral density can be considered as a constant like white noise. Random mismatch indeed results of a large amount of processes so small that their effects can be summed. It is equivalent as saying that their correlation distance is much smaller than transistors dimensions.

Pelgrom doesn't model the systematic mismatch by finding the best fit plane as we explained above. He rather models the deterministic trend observed in the measured data as an additional stochastic process with a long correlation distance. We will not go deeper into details here.

We here below derive the expression of the variance of a parameter P for a pair of transistors occupying an area $W.L$ (Fig. C.2).

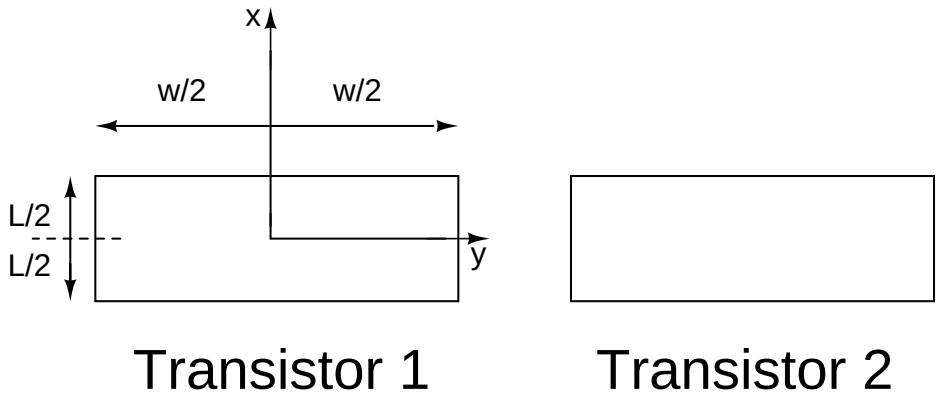


Figure C.2: Approximation of the transistors used to determine the corresponding geometry function

Assuming we only want to model the random part of the mismatch, let us begin with the geometry function. Because we focus here on random mismatch we can neglect the influence of the position of the two transistors. Looking at Fig. C.2 and taking the two-dimensional Fourier transform of the transistors, one finds

$$G(\omega_x,\omega_y) \propto \frac{sin(\frac{\omega_x L}{2})}{\frac{\omega_x L}{2}}.\frac{sin(\frac{\omega_y W}{2})}{\frac{\omega_y W}{2}}. \tag{C.3}$$

Combining this last expression and (C.2) with a constant spectral density yields

$$\sigma^2_{(\Delta P)} = \frac{A_p^2}{WL} \tag{C.4}$$

where A_p is a process depending constant, determined experimentally . This is the well-known $\frac{1}{\text{area}}$ dependence. Using (C.4), one can determine σ^2_{Vth}, $\frac{\sigma^2_\beta}{\beta^2}$, ...

Our interest, from a designer point of view, is to develop a drain current mismatch model $\sigma_{(\Delta I_D/I_D)}$. First of all, one must choose the parameters the model will depend on. Pelgrom uses therefore the well-known long channel drain current expression for bulk Si MOSFETs. In linear mode of operation, this model gives

$$I_D = \beta\left(\frac{\left(V_{GS}-Vth-\frac{V_{DS}}{2}\right)V_{DS}}{1+\theta\,(V_{GS}-Vth)}\right) \tag{C.5}$$

where $Vth = Vto + K\left(\sqrt{V_{SB}+2\phi_F}-\sqrt{2\phi_F}\right)$ and θ takes into account the mobility reduction with the vertical electrical field. In [6], the parameters on which the mismatch model depends on is Vto, β et K.

The way we determine the constant A_p from (C.4) requires also a lot of attention. The measurement setup used in [6] is illustrated in Fig. C.3. The drain current in triode regime of each transistor is first measured. Based on the current model given by (C.5), the parameters Vto, β et K are then extracted. Next, the parameter differences ΔVto,$\Delta\beta$ et ΔK are computed for each transistor pair. The constants A_p are finally computed by a statistical treatment of the extracted data. Note that the values for Vto, β et K are extracted for a transistor in triode regime but that they are used to characterize the drain current mismatch in saturation regime as well.

As highlighted in [5], the main advantage of Pelgrom's model i.e. formula (C.2) is the generality. The mathematical treatment proposed here can be applied to capacitances, resistors, ... It also provides a unique frame for the two kinds of mismatches.

The method used to determine the A_p constants is based on a drain current model and computes the mismatch on a parameter P from its nominal value. The validity of the mismatch model then depends on the validity of the drain current model. This could be a big disadvantage considering less known devices, deep sub-micron devices or subthreshold operation. We will indeed show in the next part that this model was reported to [5][8] fail when devices dimensions are scaled.

C.1.2 Bastos current mismatch model

The model developed by Bastos mainly introduces two new features. First, he studies the matching behavior of submicron transistors. And he uses an other measurement setup for extracting the mismatch data. Using this new extraction methodology, the data is extracted more precisely. We begin here by reporting and interpreting the mismatch behavior of submicron devices as reported in [5]. We will next present the method used to extract the mismatch data.

Experiments carried out by Bastos first confirm the conclusions drawn by Pelgrom for long transistors. The mismatch on the different P parameters indeed behaves as predicted by (C.4). Pelgrom's model fails on the other hand when predicting the mismatch behaviour of small dimensions devices.

Consider the mismatch on the threshold voltage σ^2_{Vto} as an example. One must distinguish here the short and the narrow-channel transistors. Indeed, in this particular technology, for devices having a length shorter than $2\mu m$ the mismatch on the threshold voltage σ^2_{Vto} is larger than what is predicted by the $\frac{1}{WL}$ law (Fig. C.4). On the other hand, for narrow-channel transistors ($W \leq 2\mu m$, in this particular case), the mismatch is better than what is predicted by (C.4) (Fig. C.4). These observations are explained by a model developed in [5] and briefly described here below.

The threshold voltage of a standard bulk MOS transistor can be expressed as

$$Vth = V_{FB} + 2\phi_F + \frac{Q_B}{C_{ox}} - \frac{Q_f}{C_{ox}} \pm \frac{Q_I}{C_{ox}} \tag{C.6}$$

where Q_B is the charge density in the depletion region, Q_f are the parasitic charges located in the oxide and at the oxide-silicon interface (we assume these are fixed) and Q_I is the threshold-adjust implanted charge density. They are all expressed in $[C/m^2]$. Calculating the different parameters variance and retaining only the most significant terms from the expression above, one finds [5]

$$\sigma^2(Vth) \simeq \frac{1}{\overline{C_{ox}}^2}\left(\sigma^2(Q_B) + \sigma^2(Q_I)\right) \tag{C.7}$$

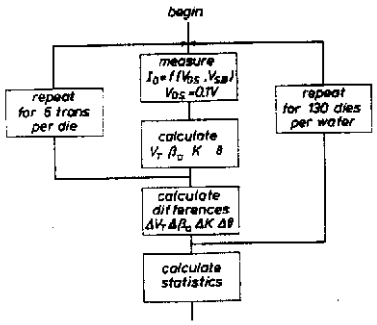


Figure C.3: Measurement procedure used by Pelgrom[6]

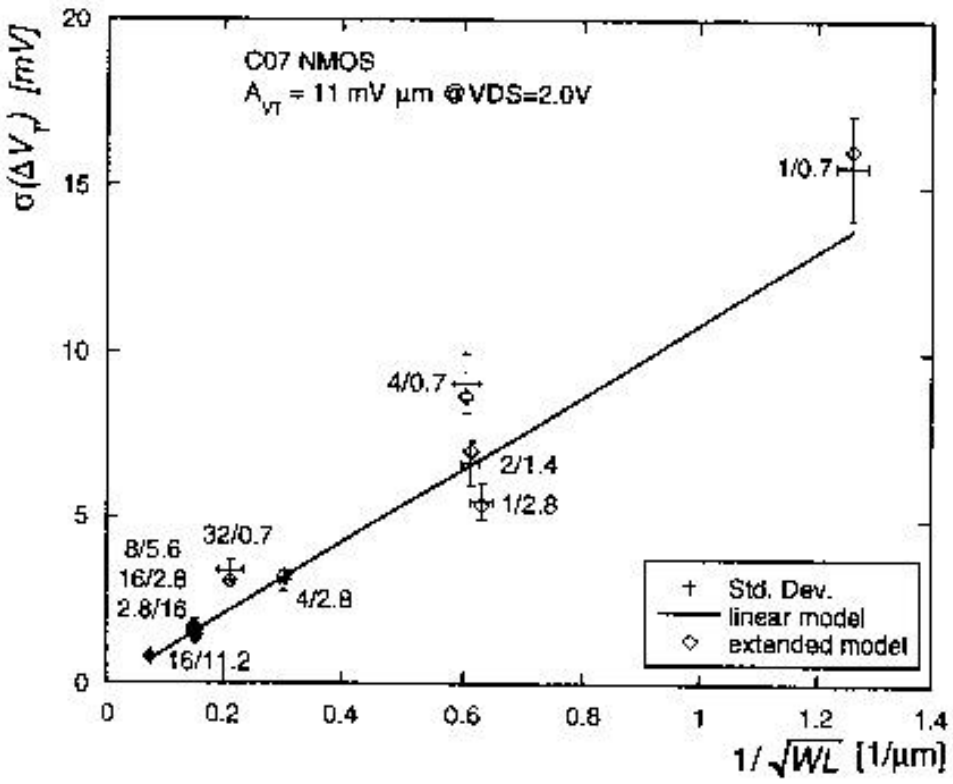


Figure C.4: Threshold voltage mismatch for NMOS transistors in saturation [5]

For a long-channel transistor [5],

$$\frac{\sigma^2(Q_B)}{\overline{Q_B}^2} = \frac{1}{4\overline{WLW}_D\overline{N}_A} \tag{C.8}$$

$$\sigma^2(Q_I) = \frac{\overline{Q}_I}{\overline{WL}} \tag{C.9}$$

where $\overline{N}_A$ is the average doping and $\overline{W}_D$ is the average value of the depletion region depth. Inserting these last two expressions in (C.7), the expression of the threshold voltage mismatch becomes

$$\sigma^2(V_T) \simeq \frac{1}{\overline{C}_{ox}^2}\left(\frac{\overline{Q}_B^2}{4\overline{WLW}_D\overline{N}_A} + \frac{\overline{D}_I}{\overline{WL}}\right) \tag{C.10}$$

Fluctuations in the depletion region charge is well-known for being the principal cause of the threshold voltage mismatch. Let us then look at (C.8). The $\sigma^2(Q_B)$ dependence on $\overline{W}_D$ is the key to understand why Pelgrom's theory fails when devices dimensions are shortened.

When width and length become shorter, the gate controlled depletion charge, i.e. the one to be considered when evaluating the threshold voltage, can no longer be approxi-

mated like we were used to for long transistors (Fig. C.5 and C.6). For a long transistor indeed the depletion charge was estimated by

$$Q_B = qN_A WLW_D \tag{C.11}$$

with -that is precisely the point- W_D considered as a constant.

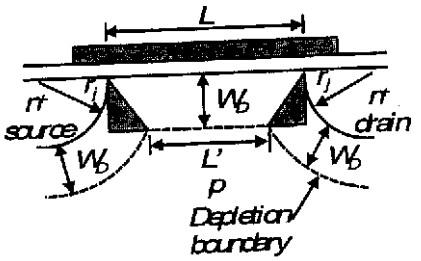


Figure C.5: When the transistor length is small, W_D is no longer uniform [5]

Looking at Fig. C.5, it is possible to rewrite the preceding expression in the case of short-channel transistor. Assuming V_{DS} is small so that the depletion region at the drain and the one at the source are identical, one finds

$$Q_{B,L} = qN_A WLW_{Dshort} \tag{C.12}$$

where $Q_{B,L}$ is the depletion charge and W_{Dshort} is the depletion region depth, both are calculated for a short-channel transistor. An expression for W_{Dshort} is found in [5]

$$W_{Dshort} \simeq W_D \left(1 - \frac{\kappa_1}{L}\right) \tag{C.13}$$

where κ_1 is an empirical parameter to be determined experimentally. The shortest the length becomes, the less the gate controls the depletion charge.

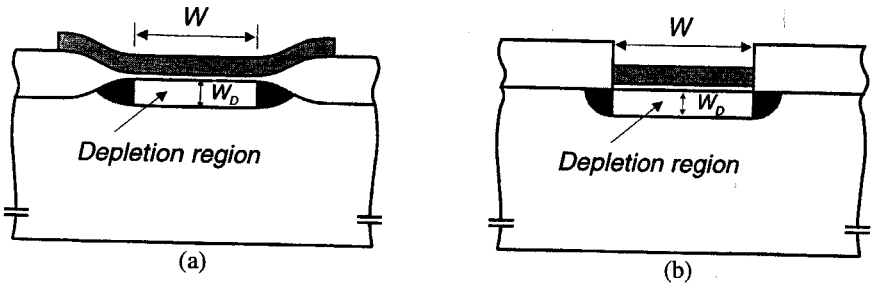


Figure C.6: Depletion region depth when transistor width is small. Real situation (a) and approximation (b) [5]

Same results can be found for narrow-channel devices (Fig. C.6),

$$Q_{B,W} = qN_A WLW_{Dnarrow} \tag{C.14}$$

where

$$W_{Dnarrow} \simeq W_D \left(1 + \frac{\kappa_2}{W}\right) \tag{C.15}$$

and κ_2 is also determined experimentally. When the transistor becomes narrower, the charge located in the *bird's beak* can not be neglected anymore. There is then more charge controlled by the gate comparing to the long-channel approximation. Combining expressions (C.12) and (C.14), an expression for the depletion charge for short dimensions transistors can be found [5]

$$\overline{W}_{Dsmall} \simeq \overline{W}_D \left(1 - \frac{\kappa_1}{\overline{L}} + \frac{\kappa_2}{\overline{W}}\right) \tag{C.16}$$

where $\overline{W}_D$ is the long-channel approximation of the depletion depth. Using the expression of $\overline{W}_{Dsmall}$ in (C.10) yields if we neglect high-order terms in a Taylor expansion [5]

$$\sigma^2(Vth) = \frac{A^2_{1,Vth}}{\overline{WL}} + \frac{A^2_{2,Vth}}{\overline{WL}^2} - \frac{A^2_{3,Vth}}{\overline{W}^2\,\overline{L}} \tag{C.17}$$

where $A^2_{1,Vth}, A^2_{2,Vth}$ and $A^2_{3,Vth}$ are determined experimentally . This model explains the results of the measurements cited above. If length becomes smaller the gate controls less depletion charge. Fluctuations in the dopant concentration have a stronger influence than in the long-channel behavior. On the other hand, the gate relatively controls more charges for narrow-channel devices. Hence, the fluctuations in the dopant concentration are more averaged and they have a weaker influence on mismatch than in the long-channel transistor. This explains the negative term in (C.17).

The theory developed by Bastos seems to explain the threshold voltage mismatch behavior. On the other hand, if one tries to explain the mismatch behavior of other parameters like the current factor β, the model becomes uncertain. To match the data, the theory has to be refined. This is done in [5], we will not go into further details here.

One of the main breakthrough of Bastos' model is the method he uses to extract the mismatch data.

First note that in [5] one specific model is used for each transistor region of operation (weak inversion, strong inversion triode regime and strong inversion saturation regime). For each region of operation, a drain current mismatch $\frac{\Delta I_D}{I_D}$ model is derived. This model depends on other mismatch parameters

$$\frac{\Delta I_D}{I_D} = f(\Delta Vto, \frac{\Delta\beta}{\beta}, \ldots) \tag{C.18}$$

As seen in Fig. C.3, Pelgrom computes the mismatch parameters (e.g.ΔVto, $\frac{\Delta\beta}{\beta}$) from an *absolute* value of the transistor parameters (e.g.Vto, β). Here, we first measure the drain currents of a transistor pair at different V_{GS} and V_{SB}. Then $\frac{\Delta I_D}{I_D}$ is computed as $\frac{I_{D1}-I_{D2}}{I_{D1}}$. These values are further interpolated to fit the mismatch model developed (C.18). This model is specific to the operating region of the transistor in which the measurements were made. The fitting operation yields the wanted mismatch parameters.This extraction method yields more precise results than Pelgrom's.

ΔVth, $\frac{\Delta\beta}{\beta}$, $\Delta\theta$ and $\Delta\gamma$ are the parameters chosen in [5] to characterize the drain current mismatch between transistors. $\Delta\theta$ models the mobility reduction mismatch and γ is the substrate-effect parameter.

Bastos then extrapolates the results obtained at all the transistor regions of operation. Bastos justifies this way of doing saying parameters are varying linearly from one region to the other. This assumption is not true. This becomes evident looking at the mobility behavior (Fig. C.7) [9].

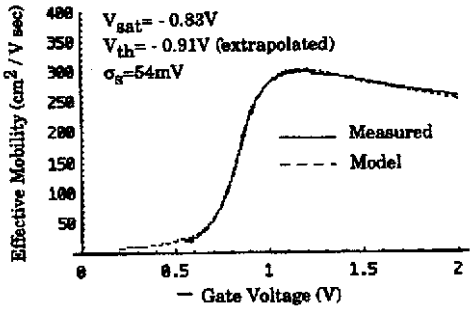


Figure C.7: The hole mobility (here : Pchannel) doesn't vary linearly from one region to the other [9]

As a conclusion, this model shows submicron transistors behave differently. It also uses an interesting extraction method. But, the transistor mismatch behavior is determined by three parameter sets, one for each region of operation. When designing a circuit, it is interesting not to fix the region of operation a priori.

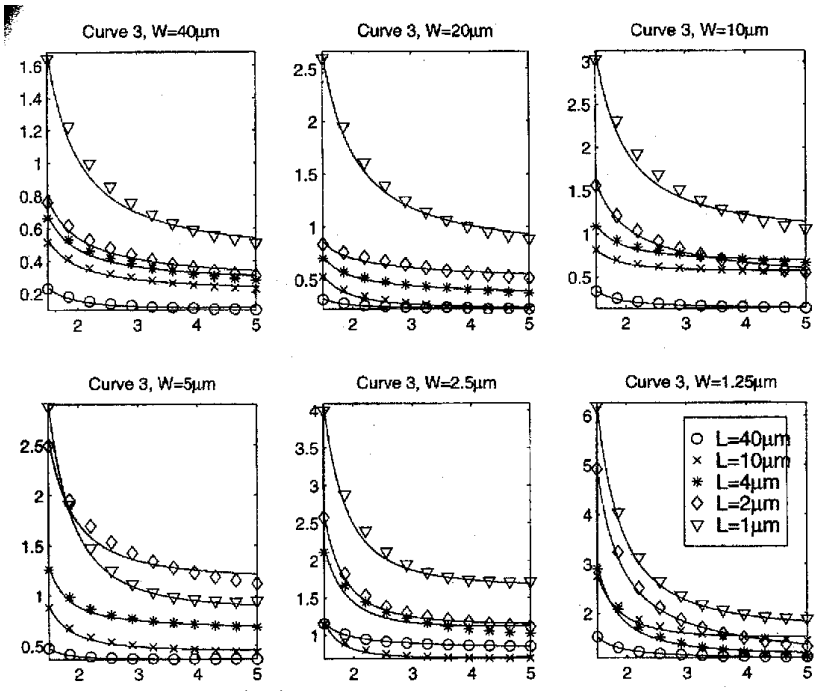
C.1.3 Serrano's model

In [3], the current mismatch is linked to the transistors dimensions using a method based on fitting. The extraction method used is of the same type as the one used by Bastos.

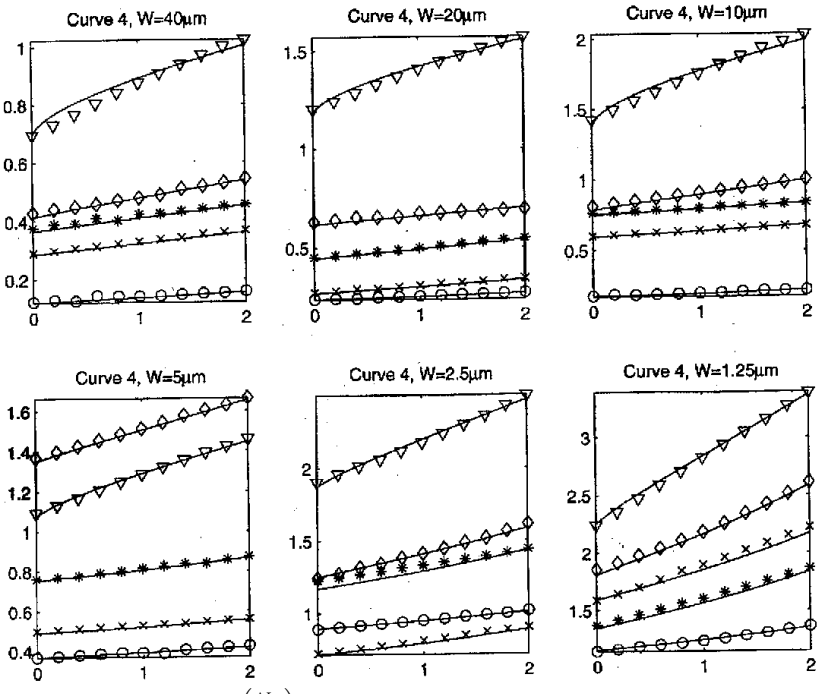
We will start this section by explaining the different mismatch parameters on which this model is based. We will then explain the procedure proposed in [3] for determining the mismatch model parameters. We will also present some results.

The Serrano's drain current mismatch model depends on five mismatch parameters. These are ΔVto, $\frac{\Delta\beta}{\beta}$, $\Delta\gamma, \Delta\theta_o, \Delta\theta_s$. $\Delta\gamma$ models the mismatch on the substrate effect. $\Delta\theta_o$ and $\Delta\theta_s$ represents the mismatch on the mobility reduction. $\Delta\theta_o$ corresponds to a transistor operating in triode and $\Delta\theta_o + \Delta\theta_s$ to one operating in saturation. Transistors are all biased in strong inversion mode. The model based on these five chosen parameters has a very good agreement with the measured data. (Fig. C.8(a) and C.8(b))

To determine the five mismatch parameters, the measurement and extraction procedure is as follows [3]. For each pair of transistor, the drain current I_{DS} of each transistor



(a) $\sigma^2\left(\frac{\Delta I_D}{I_D}\right)$ in % in function of $V_{GS} = (1.5 - 5.0\,V)$



(b) $\sigma^2\left(\frac{\Delta I_D}{I_D}\right)$ in % in function of $V_{SB} = (0.0 - 2.0\,V)$

Figure C.8: Serrano's mismatch model adequately fit the measured data [3]

is first measured. The drain current mismatch is then computed as

$$\frac{\Delta I_D}{I_D} = 2\frac{I_{DS1} - I_{DS2}}{I_{DS1} + I_{DS2}} \tag{C.19}$$

where I_{DS1} and I_{DS2} are the drain currents of the two transistors of one pair. For each transistor, I_{DS} vs. V_{GS} and I_{DS} vs. V_{SB} are measured in triode and in saturation regime of operation. That is four measurements per transistor.

Take the $(I_{DS}\text{vs.}V_{GS})_{triode}$ curve as an example. For each transistor, β_{triode}, Vto_{triode} and $\Theta_{eff,triode}$ are extracted from this curve. A drain current mismatch model for this region of operation is then derived [3]

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} + X_{1a}\Delta Vto + X_{2a}\Delta\theta_o \tag{C.20}$$

where the $X's$ depend on the extracted parameters (e.g. Vto_{triode}). Those $X's$ can then be calculated.

This procedure is done for the four different curves yielding each several X parameters. At this point, the four mismatch models developed for the four curve types are simultaneously fitted using the $X's$ calculated above and $\left(\frac{\Delta I_D}{I_D}\right)_{measured}$. This fitting operation is done by means of a Least Square Minimum algorithm. The results of the fit are the five mismatch parameters.

The measurement procedure explained above is applied on transistors with different widths and lengths. To find the mismatch parameters size dependence, the measured data is fitted to a nonlinear function. The chosen function is a very general one [3]

$$\sigma^2_{(\Delta P)} = \sum_{m,n} \frac{C_{mn}}{(W - \varepsilon_w)^m (L - \varepsilon_l)^n} \tag{C.21}$$

where C_{mn}, ε_w and ε_l are computed for each of the five parameters.

Some results are presented in Fig. C.8(a). Note the model is in very good agreement with the measured data.

In [10], the model is extended to weak inversion and presents the best mismatch prediction up to now with an accuracy on the drain current mismatch of 5 % in strong inversion regime and of 13.5 % in weak inversion.

C.1.4 Croon's model

In this section, we first describe how the different drain current mismatch sources are modeled by Croon. We then depict the total current mismatch model. We also discuss how the mismatch dependence on transistor sizes is taken into account. We finally conclude.

The drain current mismatch coming from a variation in the threshold voltage is expressed as [7]:

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{gm}{I_D}\Delta Vto \tag{C.22}$$

It comes from the differentiation of a very simple current model ($I_{DS} = f(V_{GS} - Vth)$).

The drain current mismatch due to the variation of the current factor value is more complex to describe. The expression of the mismatch used here is based on the following drain current expression :

$$I_{DS} = \beta(V_{GS} - Vth - \frac{V_{DS}}{2}) \tag{C.23}$$

with

$$\frac{1}{\beta} = \frac{1}{\beta_0} + \frac{V_{GS} - Vth - \frac{V_{DS}}{2}}{\beta_{sr} + \frac{V_{DS}}{\beta_{sat}}} \tag{C.24}$$

where β_0 is the long channel current factor and β_{sr} and β_{sat} model the mobility degradation due to V_{GS} and V_{DS} respectively. The two last terms take also the effect of the series resistances into account [7]. The drain current mismatch can then be expressed as

$$\frac{\Delta I_{DS}}{I_{DS}} = \alpha_1 \frac{\Delta(\beta_0)}{\beta_0^2} + \alpha_2 \frac{\Delta(\beta_{sr})}{\beta_{sr}^2} + \alpha_3 \frac{\Delta(\beta_{sat})}{\beta_{sat}^2} \tag{C.25}$$

where the α parameters are found by differentiating (C.23). These parameters do not depend on the current factors themselves but on the drain current well. This is important because the extraction of the current factor, which is a difficult operation does not need to be carried out. Not however that this model is the same as the model of Serrano, described in the previous section, by doing the following parameter mapping (left side: Croon's notation and right side: Serrano's notation)

$$\frac{1}{\beta_{sr}} = R_D + R_S + \frac{\theta}{\beta} \tag{C.26}$$

$$\frac{1}{\beta_{sat}} = \frac{\mu}{2L\beta v_s} - R_D \tag{C.27}$$

where R_D and R_S are respectively the drain and sources series resistance, θ is the mobility reduction parameter and v_s is the velocity saturation.

The complete drain current mismatch model is obtained by summing the two contributions (C.22) and (C.25). (C.22) is well-known to be continuous from weak to strong inversion. But (C.25) is only valid in strong inversion. Following Croon, this is not a real problem because mismatch in the weak inversion inversion region is dominated by threshold voltage fluctuations. The model is then made continuous by assuming the current factor part of the mismatch to be constant in moderate and weak inversion regions [7]. We however saw in section 4 that this assumption is not true. It would explain the large fitting errors of the model of Croon in weak inversion [8].

The width and length dependence of the drain current mismatch is taken into account by the spatial Fourier transform method developed by Pelgrom [6].

C.2 Systematic mismatch

In this section, we will shortly explain how to deal with the systematic mismatch. In the introduction we said that the actual value of a parameter P could be seen as

$$P_{(i,j)} = \overline{P_{(i,j)}} + \sigma(P) \times (rand)$$

In this last equation, the systematic mismatch is responsible for the parameter mean value $\overline{P_{(i,j)}}$. In the introduction, we also said the effects of this kind of mismatch could be reduced by appropriate design rules. There exist indeed several types of layout (Fig. C.9).

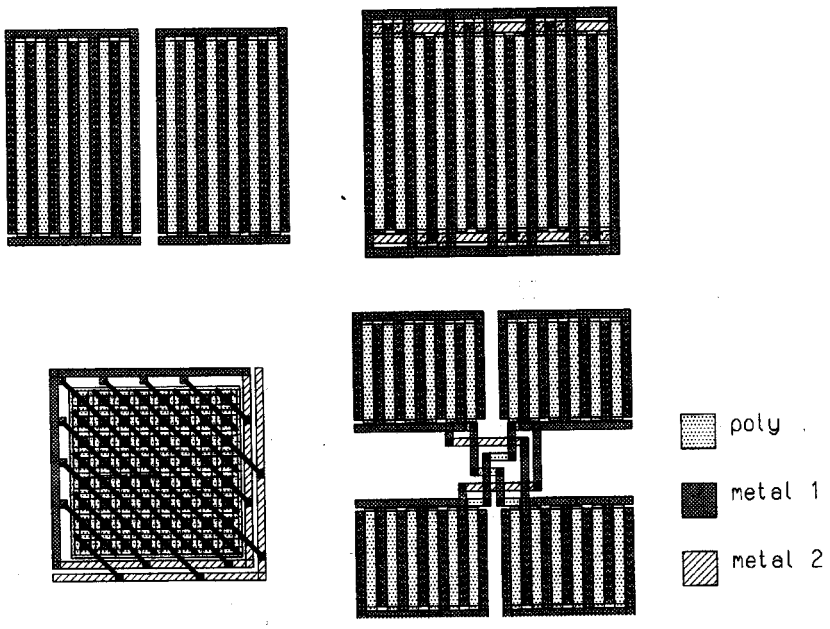


Figure C.9: Different possible layouts for the same differential pair [5].

As we already said, the deterministic variation of a parameter on small or medium wafers can be approximated by planes [3] [2] [1]. For a transistor located at a position (i, j) on a wafer, one finds then

$$\overline{P}_{(i,j)} = \overline{P}_{wafer} + G_P^{(x)} i + G_P^{(y)} j \tag{C.28}$$

where $\overline{P}_{wafer}$ is the mean value of parameter P on a specific wafer. $G_P^{(x)}$, $G_P^{(y)}$ are the coefficients used to represent the planes

$$z = G_P^{(x)} x + G_P^{(y)} y + n \tag{C.29}$$

where x and y represent the coordinates on the wafer, z the value of the parameter and n an offset. The coefficients $G_P^{(x)}$, $G_P^{(y)}$ and n are found by minimising the mean square error from the actual value.

Given those planes for each parameter P of interest, one can easily place the transistors of a given circuit so that $\overline{P}_{(i,j)}$ terms (C.28) of the different transistors cancel each others (Fig.C.10).

Among the different parameters influencing the systematic mismatch, let us say a few words about the *micro-loading effect* [11][12]. This effect models the difference

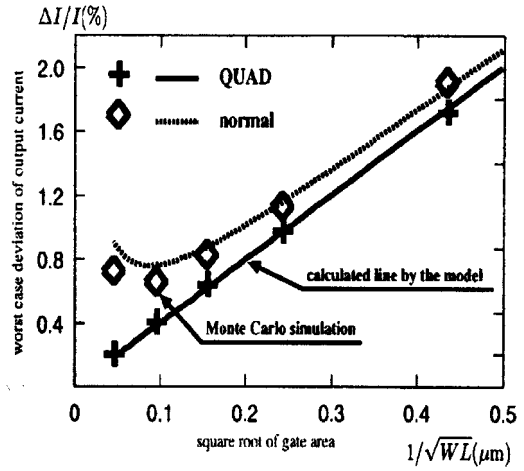


Figure C.10: The layout type has an impact on the performance of a current mirror [2]

existing between the actual and drawn dimensions of a polysilicon or a metal line. This difference depends on the line dimensions (size effect) and also on the distance to other lines (proximity effect). This mismatch cause can have a dramatical impact on the final performance of the circuit. It can also be modeled like the other causes. Models of the micro-loading effect can be found in [2] and [11].

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Appendix D

MOSFET parameter extraction methods

D.1 The Integral function method (IFM)

The integral function method (IFM) [1] [2] [3] extracts the DC non-linear behavior of a MOSFET from the drain current (I_D) vs. gate or drain voltage (V_G, V_D). The IFM provides the same information on the device non-linearity than a Taylor expansion but doesn't require the computation of high-order derivatives. We will not go into details here and focus on the main advantages of the method as well as its principle. We refer the interested reader to [4] for a comprehensive review of the subject as well as the extension of the method to high frequencies.

Our goal is to compute the distortion introduced by a MOSFET when a signal described by $X_{dc} + X_{amp} sin(\omega t)$ is applied. Depending on the situation, the signal can be a current or a voltage. The main advantages of the IFM are the following.

- It is more robust to measurement noise as no higher-order derivatives are computed.
- It starts from DC characteristics.
- It depends on the signal DC level (X_{dc}) and amplitude (X_{amp}).

The IFM extracts the device non-linearity as follows.

1.) Based on the application, the DC characteristic on which the extraction will occur is chosen. In the case of an amplifier for example, the signal is applied to the gate, the I_D vs. V_G will be elected and the effect of the drain bias is studied by measuring I_D vs. V_G corresponding to different V_D. On the contrary, in the case of a MOSFET-C resistor (chap. 3), I_D vs. V_D for various V_G will prevail to take the effect of the gate bias into account. In the following, we refer to Y vs. X characteristics to be more general.

2.) We select the region of the Y vs. X characteristic corresponding to the input signal characteristics: DC level (X_{dc}) and amplitude (X_{amp}).

3.) Y vs. X is normalized in both axis from 0 to 1. The normalized characteristic which we note y vs. x, appears in a square of area equal to 1 in the first quadrant (Fig. D.1) and defines two areas: *area1* below and *area2* above y vs. x. Intuitively, a perfectly linear transfer characteristic would be a straight line, i.e. $y = x$. The difference between *area1* and *area2* quantifies the difference of a particular y vs. x characteristic with the linear

case. This difference is thus proportional to the total harmonic distortion (THD).

4.) Mathematically, we define the integral function D corresponding to the difference between the two areas as

$$D = 2\int_0^1 y(x)dx - 1 \tag{D.1}$$

and it is proportional to the THD including the DC shift (THD_0) [2] $THD_0 = 1.06D$. To avoid the integral cancellation when y vs. x crosses the $y = x$ curve, it is preferable to use the modulus of y yielding a function D_s which is also proportional to THD_0.

5.) To isolate the different orders of harmonic distortion, the IFM computes the Y_r vs. X characteristic with $Y_r(X) = Y(X) - Y(-X)$ which eliminates the even harmonics in the output signal. Y_r vs. X is normalized; a integral function D_r is defined

$$D_r = 4\int_0^{0.5} y_r(x)dx - 0.5 \tag{D.2}$$

Again, to avoid the integral cancellation, a function D_{rs} using modulus is defined. $D_r = HD3$ if the orders of harmonic distortion higher than three are neglected.

6.) The principal harmonic parameters can be extracted as :

$$THD = \sqrt{\frac{(1.06D_s)^2}{2} + \frac{D_{rs}^2}{2}} \tag{D.3}$$

$$HD2 = \sqrt{\frac{(1.06D_s)^2}{2} - \frac{D_{rs}^2}{2}} \tag{D.4}$$

$$HD3 = D_r \tag{D.5}$$

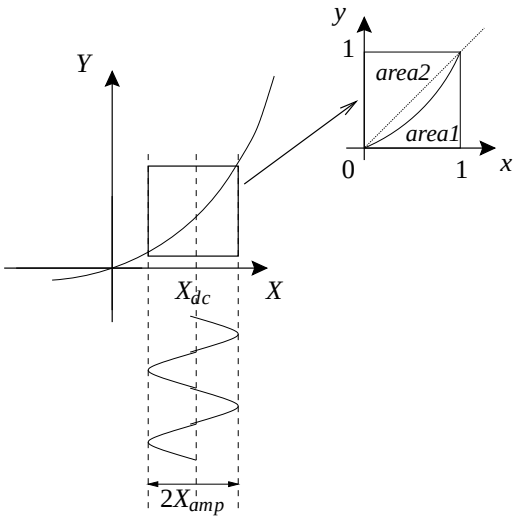

Figure D.1: The zone of interest of the Y vs. X characteristic is normalized in the first quadrant into a y vs. x characteristic.

The IFM also extracts the intermodulation distortion under restrictive assumptions. We do not go into details here and again refer to [4].

D.2 Vth and n extraction with the EKV method

Numerous methods exist to extract the threshold voltage (Vth). An extensive review on the subject is presented in [5]. Here we focus on an extraction method [6] [7] not covered in [5] based on the EKV formulation of the drain current (I_D). We briefly review the EKV formulation of I_D, give the principle of the extraction of Vth in this context and finally, the associated measurement methods.

In the EKV formulation, I_D is given by the sum of a forward (I_F) and a reverse (I_R) current, depending on the gate voltage (V_G) and, respectively, on the source (V_S) and drain (V_D) voltages [8]:

$$I_D = I_F - I_R = I_0 \left[F\left(\frac{V_P - V_S}{U_T}\right) - F\left(\frac{V_P - V_D}{U_T}\right)\right] \quad \text{(D.6)}$$

$$I_0 = 2n\beta U_T^2 \quad \text{(D.7)}$$

$$F(x) = \ln\left[1+\exp\left(\frac{x}{2}\right)\right]^2 \quad \text{(D.8)}$$

$$V_P \cong \frac{V_G - Vth}{n} \quad \text{(D.9)}$$

where F is an interpolating function continuous from weak to strong inversion, n is the linearized body factor, β is the current factor, U_T is the thermal voltage and V_P is the pinch-off voltage, i.e. the voltage at which the inversion charge disappears in old MOSFET models considering only the strong inversion regime. All voltages are referred to the transistor bulk.

From (D.6), **Vth corresponds to $\mathbf{V_G}$ at which $\mathbf{V_P = 0}$ and n is the inverse of the slope of $\mathbf{V_P}$ vs. $\mathbf{V_G}$**. Our goal is to measure the V_P vs. V_G characteristic. For a transistor in saturation, (D.6) reduces to $I_D = I_0\left[F\left(\frac{V_P - V_S}{U_T}\right)\right]$; if additionally $V_S = V_P$:

$$I_D = 2n\beta U_T^2 \ln 2^2 \cong n\beta U_T^2 \equiv I_{\text{spec}} \quad \text{(D.10)}$$

I_{spec} being the specific current. Finally, we can summarize it as: for a transistor in saturation, $V_S = V_P \Leftrightarrow I_D = I_{\text{spec}}$. **If we impose $\mathbf{I_D = I_{spec}}$ for a transistor in saturation, V_P can be measured at the source terminal for any $\mathbf{V_G}$.**

To extract I_{spec}, I_D of a transistor in saturation and strong inversion is measured. From (D.6), $I_D = I_0 \ln\left[1+\exp\left(\frac{V_P - V_S}{2U_T}\right)\right]^2$; under these conditions $\exp\left(\frac{V_P - V_S}{2U_T}\right) >> 1$ so that finally (D.6) (D.10)

$$\sqrt{I_D} = \sqrt{\frac{I_{\text{spec}}}{2U_T^2}}\,(V_P - V_S) \quad \text{(D.11)}$$

$\mathbf{I_{spec}}$ is obtained by the maximum slope of the $\mathbf{\sqrt{I_D}}$ vs. $\mathbf{V_S}$ characteristic.

At first sight, this method may seem tricky as it requires the extraction and injection of I_{spec}. The technique was however proved to be rather insensitive to an error in I_{spec} [7]. Moreover, several important parameters are extracted from the V_P vs. V_G characteristic: Vth, n and $n\beta$ by definition of I_{spec} (D.10).

The extraction procedure is the following

1. Measure I_S for different V_S for a transistor in saturation and in strong inversion (Fig. D.2 a). Extract the maximum slope (e.g. the maximum of the first derivative) of $\sqrt{I_S}$ vs. V_S and compute I_{spec} as the maximum slope is equal to $\sqrt{\frac{I_{\text{spec}}}{2U_T^2}}$.

2. For a transistor in saturation, impose $I_S = I_{\text{spec}}$ and measure V_P at the source terminal (Fig. D.2 b). Vth corresponds to V_G for which $V_P = 0$ and $n = \frac{\partial V_G}{\partial V_P}$. For short-channel transistors, the circuit configuration of Fig. D.2 b may be inappropriate as the drain-to-source voltage V_{DS} is not kept constant, which results in a small error due to channel-length modulation [6]. It can be circumvented by the configuration of Fig. D.2 c [6] as in this case V_{DS} is kept constant at RI_R by the opamp and can be adjusted by modifying I_R.

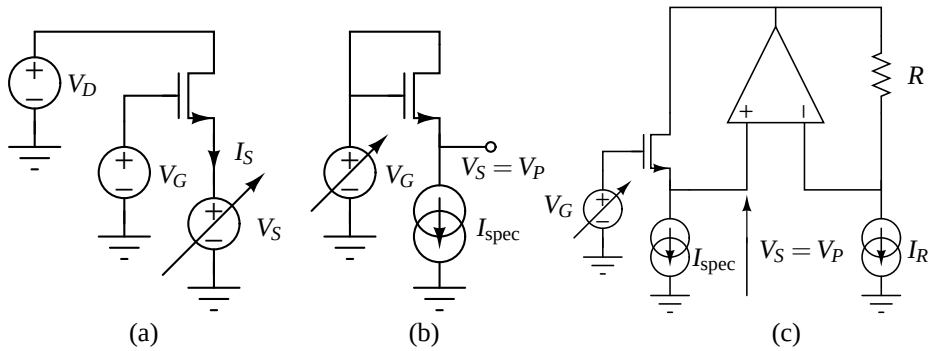

Figure D.2: Configuration for the measurement of (a) I_S vs. V_S and extraction of I_{spec}; (b) V_P vs. V_G; and (c) V_P vs. V_G for short-channel transistors.

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