RF SOI CMOS Technology on Commercial Trap-Rich High Resistivity SOI Wafer

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I. INTRODUCTION

As CMOS technology continues to scale down, allowing operation in the GHz range, it provides the opportunity of low cost integration of analog, digital and RF functions on the same wafer for System-on-Chip (SoC) applications [1]. SoC circuits on Si are prone to substrate losses and coupling, especially when RF analog and digital functions are integrated together into the same chip. In digital circuits, substrate coupling can also cause fluctuations in the propagation delay of logic gates by changing the threshold voltage of devices through the body effect [2]. The development of SOI technology presents the major advantage of providing high resistivity silicon (HR-Si) substrate capabilities, which are mandatory for high-performance RF integrated circuits [3], leading to substantially reduced substrate RF losses and crosstalk [4]. However, oxidized HR-Si wafers suffer from parasitic surface conduction (PSC) due to fixed charges (Q_{ox}) within the oxide which attract free carriers near the Si/SiO_2 interface, hence reducing the substrate effective resistivity (ρ_{eff}) and increasing substrate losses [5]. In addition, PSC increases the non-linearities originating from the substrate [6] and RF devices are more sensitive to variations of the DC voltage [7]. Several techniques have been developed to reduce these parasitic effects and to enhance the HR properties of Si material. The introduction of a trap-rich layer has been proved as the most effective technique while being compatible with industrial SOI wafer fabrication and with the important thermal budget of standard CMOS process [5]. The traps capture the free carriers at the Si/SiO_2 interface, thereby enabling the substrate to recover its nominal resistivity [5], linearity, eliminating the DC dependency [6], [7], and leading to a substantial reduction of RF losses and crosstalk [8].

In this paper we aim at comparing the static and RF performances of passive and active fully-depleted (FD) SOI MOSFETs fabricated on top of either a standard or a trap-rich HR-SOI UNIBOND wafer both provided by SOITEC.

II. DEVICES DESCRIPTION

The passivation efficiency of trap-rich HR-SOI substrates was investigated on commercially available 200 mm industrial SOI wafers. The tested devices were 1 µm-thick aluminum coplanar waveguide (CPW) and nMOS FD SOI transistors fabricated using a standard CMOS process [9]. The dimensions of the 50-Ω CPW line are respectively 38, 18 and 213 µm for the central conductor, slot space, and ground. The cross-section of the FD SOI MOSFETs is shown in Fig. 1, having 400 nm BOX, 80 nm for the thin active silicon film and 25 nm for the gate oxide thickness, all lying on a HR-Si handle substrate (> 1 kΩ.cm). The studied FD SOI MOSFET has a 2 µm gate length (L) with 20 gate fingers of 20 µm each (W). Both intrinsic (10^{15} at/cm^3, named NiN) and standard boron implantation ($4x10^{16}$ at/cm^3, NP2N) are considered for the channel doping.

III. MEASUREMENT RESULTS

A. Harmonic Distorsion of CPW line on trap-rich HR-SOI

The 2nd and 3rd harmonics of a 900 MHz signal at the output of a 2,000 µm-long CPW line on both HR-SOI and trap-rich HR-SOI substrates are shown in Fig. 2. A reduction of more than 25 and 35 dB is depicted on trap-rich HR-SOI for, respectively, the 2nd and 3rd harmonics. Despite its high nominal resistivity, the effective resistivity (ρ_{eff}) [10] sensed by the CPW on HR-SOI wafer is only 210 Ω.cm (Fig. 3), which explains the high harmonic level measured at the output [6]. Fortunately, the trap-rich HR-SOI substrate reduces the CPW line harmonics and fully recovers the HR properties of the substrate with measured ρ_{eff} higher than 4 kΩ.cm. A degradation of ρ_{eff} (4 times lower) was observed for the HR-SOI wafer after the CMOS process. This degradation could be explained by the impact of thermal donor generated during the processing. On the contrary, the RF performance, ρ_{eff} and benefits of the trap-rich HR-SOI wafer remain unchanged after the CMOS process (Fig. 3). Additional measurements under different DC bias conditions (not shown here) also confirm the RF performance insensitivity of CPW to the applied voltage for trap-rich HR-SOI substrates.

B. FD SOI MOSFET DC and RF characteristics

DC and RF measurements were performed on 18 dies for both HR-SOI and trap-rich HR-SOI wafers. The normalized I_D-V_G and g_m-V_G curves recorded for 2 µm-long FD SOI nMOS are presented in Fig. 4. For both wafer types the results outline similar DC behavior for both channel doping levels, NiN and NP2N FD SOI MOSFETs.

To fairly compare all types of transistors on both wafers, and to eliminate the impact of threshold voltage variations, we extracted the g_m/I_D over $I_D/(W/L)$ (Fig. 5). The low body-effect coefficient for FD SOI devices allows for obtaining almost identical high values of g_m/I_D (35 V^{-1}) on both HR-SOI and trap-rich HR-SOI technologies. High frequency measurements have been performed from 0.04 to 40 GHz using an Anritsu 37369A in combination with HP4145A. The pad parasitics were subtracted from the measurements using a set of dedicated calibration structures. Fig. 6 presents the expected

H_{21} which shows excellent similarity, respectively, for the NiN and NP2N FD SOI MOSFETs on both wafers.

IV. CONCLUSION

The excellent matching between the experimental static and RF characteristics of measured FD SOI MOSFETs on top of both HR-SOI and trap-rich HR-SOI wafers clearly demonstrates that the presence of a trap-rich layer underneath the BOX does not alter the DC or RF behavior of SOI MOS transistors. Since substrate losses and crosstalk are greatly reduced when using a trap-rich HR-SOI wafer and because those advantages are also conserve after CMOS processing, trap-rich HR-SOI technology can be considered as a excellent solution for the co-integration of digital, analog and RF devices on the same chip.

ACKNOWLEDGMENTS

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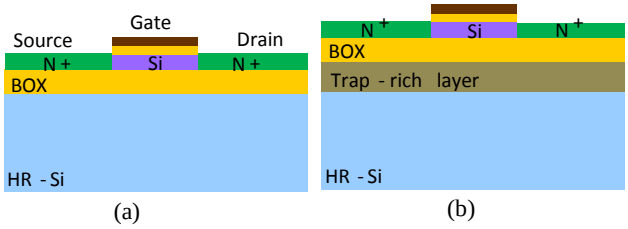

Fig. 1. Cross-section of FD SOI MOSFET on (a) HR-SOI and (b) trap-rich HR-SOI wafers.

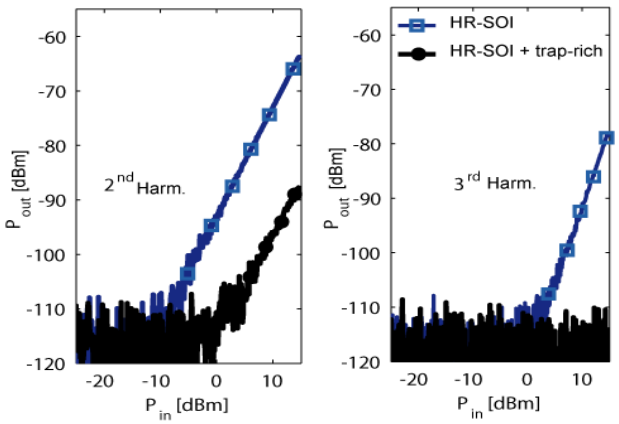

Fig. 2. Harmonics distortion of a CPW on HR-SOI and trap-rich HR-SOI.

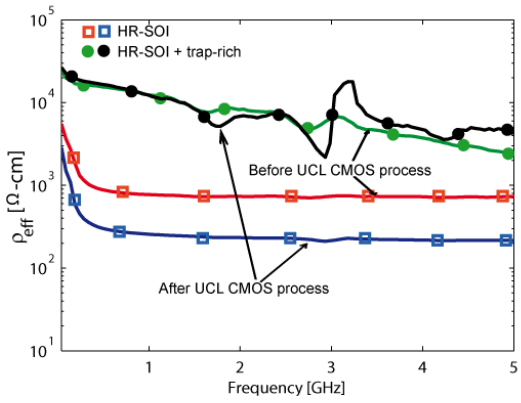

Fig. 3. Effective resistivity of CPWs on HR-SOI and trap-rich HR-SOI.

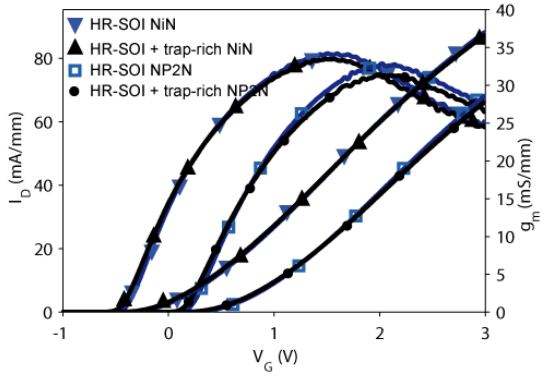

Fig. 4. Normalized I_D-V_G and g_m-V_G characteristics ,for NP2N and NiN FD SOI MOSFETs.

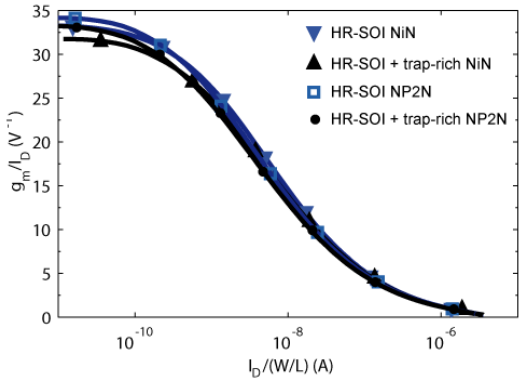

Fig. 5. g_m/I_D ratio versus $I_D/(W/L)$, for NP2N and NiN FD SOI MOSFETs.

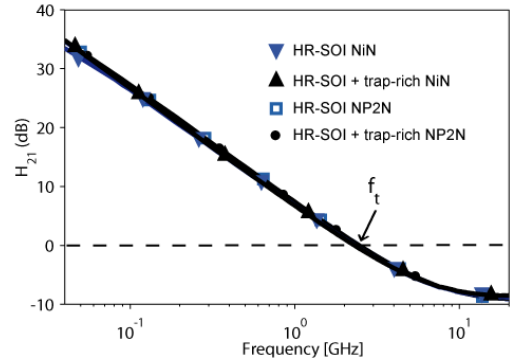

Fig. 6. Cutoff frequency as function of supply voltage (V_G) at V_D=1.5 V for NiN and NP2N FD SOI MOSFETs