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WIDE BAND AND NOISE CHARACTERIZATION OF VARIOUS MOSFETS FOR OPTIMIZED USE IN RF CIRCUITS

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To my parents,
to my wife,
and to my daughter

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ABSTRACT

Wireless, *portable* and *performance* are becoming the keywords for both the consumer electronics and the telecommunication markets. These key requirements are very demanding on the circuit design level as well as on the technology level. In fact, the circuit design is no more separated from the technology. The passage from *micro*-electronic to *nano*-electronic devices was accompanied by a great deal of revolutionary enhancements and modifications of device modeling. In order to meet the new challenges of advanced applications and circuit designs, it is indispensable for the device model to approach from the device physics, as opposed to the empirical models known earlier. This leads, *de facto*, to a more complicated device model. As a result, a good circuit designer should coercively comprehend the device physics. A profound research is indeed compulsory in this gray area between the circuit design and the device characterization conventional areas.

The first keyword, *wireless*, is intuitively interpreted by electronics engineers to *RF*. The term *RF* being an old notation of *radio frequency* is now the synonym of any high frequency application, circuit, or device. By high frequency, engineers refer to the frequency range starting from few hundreds of mega hertz to the tera hertz range. Advanced applications tend to adopt one or more forms of wireless communication schemes. Many standards already exist which include GSM, WLAN, WiFi, WiMax ... etc. Nevertheless, the inclusion of the wireless feature requires area, power and cost. These requirements contradict the second keyword; portable.

Portability compels a smaller product that consumes less power, and hence has longer battery life time. Theoretically, an optimum portable product is not optimized in terms of *performance*. Fortunately, the continuous down scaling of transistors made it possible to include enormous number of transistors on a single small chip, thus more functions and better performance. Yet, increasing the number of transistors yields to higher power consumption and certainly shorter battery life time. Another challenge is to be able to efficiently include the wireless functionality on the same chip. It is well known that digital circuitry will interfere with the analog/RF circuitry in the form of what is known as crosstalk resulting in many problems not to mention malfunctioning of the application.

Silicon-on-Insulator SOI technology is introduced as an excellent candidate to overcome the problem of crosstalk through an enhanced device isolation. SOI also provides the possibility of using high resistive substrates that help to reduce losses. Thus, the use of lower power signals becomes possible and longer battery life times can be achieved.

In this context, the work of this PhD thesis is devoted to:

- provide the link between the device engineering/characterization domain and the circuit design domain, pronouncedly for RF applications. This is achieved through an elaborated research of already existing transistor structures (floating-body and body-tied) as well as new structures (graded channel). Different technologies such as bulk, partially-depleted SOI, and fully-depleted SOI are also considered. Based on a complete flow (design of layout to on-wafer measurements), a detailed comparison of all mentioned variations of transistors is presented in order to render the RF circuit designer with adequate information for a successful RF product.
- cover the whole area of operation of the device:
  - In terms of frequency, the device characterization phase starts from dc to 40 GHz. The small-signal equivalent circuit is extracted (intrinsic and extrinsic parts). A specific tool has been developed to facilitate the extraction steps and also to verify the extracted parameters and the extraction procedures. All dc, ac, and RF figures of merit are then readily compared.
  - Nonlinear performance including harmonic distortion and intermodulation figures of merit are extracted using the well known Integral Function Method (IFM).
  - High-frequency noise performance is studied in detail. Based on Tuner measurements, a profound analytical interpretation and the extraction of the parameters of different models are achieved. A validation of the adequacy of specific noise models to specific transistor structures is presented.
  - Low voltage low power regime of operation is highlighted and compared for different transistor structures as a necessary requirement of new portable applications.
  - High-temperature dc and RF performances are measured and compared. Temperature range of 25^oC to 250^oC is considered. This includes dc, ac, RF, and nonlinear performances.
- apply the acquired knowledge and results from the device characterization phase to a sample RF circuit, namely the RF antenna switch, in order to prove and show the advantages/drawbacks of different characterized structures/technologies. This includes the design, simulation, layout, and on-wafer measurement steps. The figures of merit of RF antenna switches (isolation and insertion-loss) are then compared for different switches built using different transistor structures and technologies.

At the end of this complete cycle (from device engineering to circuit testing), the PhD thesis is meant to serve as a guideline for circuit designers to show the optimum operation regimes and conditions for a specific transistor structure.

ACRONYMS

BOX	Buried oxide
BT	Body-Tied
CMOS	Complementary metal-oxide semiconductor
DIBL	Drain-induced barrier lowering
DT	Dynamic Threshold
FB	Floating-Body
FBE	Floating Body Effects
FD	Fully-Depleted
HF	High Frequency
ISS	Impedance Standard Substrate
LVLP	Low Voltage Low Power
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PD	Partially-Depleted
RF	Radio Frequency
SOI	Silicon-on-Insulator

LIST OF SYMBOLS

A_{v0}	Low-frequency open-loop gain (intrinsic gain)	—
B_{cor}	Noise correlation susceptance ($\Im(Y_{\text{cor}})$)	Ω^{-1}
B_{opt}	Noise optimum susceptance ($\Im(Y_{\text{opt}})$)	Ω^{-1}
B_{s}	Noise source susceptance ($\Im(Y_{\text{s}})$)	Ω^{-1}
C_A	Noise correlation matrix for chain representation	—
C_Y	Noise correlation matrix for admittance representation	—
C_Z	Noise correlation matrix for impedance representation	—
C_{bd}	Body-to-drain capacitance	fF/mm
C_{bs}	Body-to-source capacitance	fF/mm
C_{D}	Channel depletion-layer capacitance	fF/μm^2
C_{ds}	Drain-to-source capacitance	fF/mm
C_{gs}	Gate-to-source capacitance	fF/mm
C_{gd}	Gate-to-drain capacitance	fF/mm
C_{gg}	Total gate capacitance	fF/mm
C_{it}	Capacitance associated with interface traps	fF/μm
C_{OFF}	Drain-to-source OFF capacitance	fF/mm
C_{ox}	Gate oxide capacitance	fF/μm^2
C_{ox1}	Front gate oxide capacitance	fF/μm^2
C_{ox2}	Back gate/buried oxide capacitance	fF/μm^2
C_{p}	Pad capacitances	fF/μm^2
C_{si}	Depleted silicon film capacitance	fF/μm^2

C_{tot}	Total gate capacitance including pad capacitances	fF/μm^2
ΔA_{d}	Impedance field of the drain which represents the noise propagation	—
ΔA_{g}	Impedance field of the gate which represents the induced noise propagation	—
ΔS	Variation of subthreshold slope with temperature	%/^{o}C
ΔV_T	Variation of threshold voltage with temperature	mV/^{o}C
D_{n}	Electron diffusion coefficient	cm^2/s
$\overline{e^2}$	Spectral density of voltage noise source	V^2/Hz
E_{g}	Energy gap	eV
ε_{Si}	Silicon permittivity ($= 1.04 \times 10^{-12}$)	F/cm
F_{50}	Noise figure for a system with a source of 50 Ω impedance	GHz
f_{MAG}	Maximum available gain cutoff frequency	GHz
f_{max}	Maximum oscillation frequency (unilateral gain cutoff frequency)	GHz
f_T	Current gain cutoff frequency	GHz
Γ_{opt}	Optimum input reflection coefficient	dB
G_{ass}	Associated gain	dB
G_{cor}	Noise correlation conductance ($\Re(Y_{\text{cor}})$)	Ω^{-1}
g_D	Output conductance extracted from dc measurements	mS/mm
G_{dsi}	Intrinsic output conductance extracted from RF measurements	mS/mm
g_m	Transconductance extracted from dc measurements	mS/mm
$g_{m\text{b}}$	Body to source transconductance	mS/mm
$G_{m\text{i}}$	Intrinsic transconductance extracted from RF measurements	mS/mm
$g_{m,\text{max}}$	Maximum transconductance extracted from dc measurements	mS/mm

G_n	Equivalent noise conductance	Ω^{-1}
G_{opt}	Noise optimum conductance ($\Re(Y_{\text{opt}})$)	Ω^{-1}
G_{s}	Noise source conductance ($\Re(Y_{\text{s}})$)	Ω^{-1}
HD	Harmonic distortion	dB
HD_n	Harmonic distortion or order n	dB
$HD2$	Second harmonic distortion	dB
$HD3$	Third harmonic distortion	dB
$\overline{i^2}$	Spectral density of current noise source	A^2/Hz
i_d	Drain noise current source	A
I_{DS}	Drain current normalized with respect to total gate width	mA/mm
I_{Dsat}	Drain saturation current normalized with respect to total gate width	mA/mm
i_g	Gate noise current source (induced gate noise)	A
I_{GS}	Gate current normalized with respect to total gate width	mA/mm
I_{Leakage}	Drain leakage current normalized with respect to total gate width	mA/mm
I_{OFF}	Drain current in OFF state normalized with respect to total gate width	mA/mm
I_{ON}	Drain current in ON state normalized with respect to total gate width	mA/mm
IP_3	Third intercept point	dBm
L_{eff}	Effective channel length	nm
L_{LD}	Lightly doped region of the channel	nm
n_{i}	Intrinsic carrier density	cm^{-3}
N_A	P-type doping density in the channel region	cm^{-3}
NF	Noise Figure	dB
NF_{min}	Minimum Noise Figure	dB
N_{finger}	Number of parallel gate fingers	—
P_{av}	Available thermal noise power	W

P_{dc}	DC power consumption	W
Φ_{MS}	Work-function difference between metal and silicon	V
ψ_{F}	Fermi potential	V
ψ_{B}	Difference between the Fermi potential and the intrinsic potential (mid-gab potential)	V
ψ_{S}	Surface potential	V
$P_{\text{1-dB}}$	1-dB compression point	dBm
Q_{D}	Depletion Charge per unit area	$\mathrm{C.cm^{-2}}$
Q_{i}	Inversion Charge per unit area	$\mathrm{C.cm^{-2}}$
Q_{ox}	Equivalent oxide charge density per unit area	$\mathrm{C.cm^{-2}}$
R_{d}	Extrinsic drain resistance	Ω
R_{g}	Extrinsic gate resistance	Ω
R_{gsi}	Intrinsic gate-to-source resistance or the input resistance of the small signal equivalent circuit of the transistor	Ω
R_{i}	Intrinsic gate-to-source resistance or the input resistance of the small signal equivalent circuit of the transistor	Ω
R_n	Equivalent noise resistance	Ω
R_{ON}	Channel ON (strong inversion) resistance	Ω
R_{s}	Extrinsic source resistance	Ω
S	Subthreshold slope	mV/dec
T_{a}	Ambient temperature	K
t_{box}	Buried-oxide thickness	nm
T_{C}	Equivalent temperature of noise source in its cold state	K
τ_{d}	Delay	s
T_d	Drain equivalent noise temperature	K
τ_{e}	Effective lifetime related to the thermal generation process in the depletion region	s
T_g	Gate equivalent noise temperature	K
T_{in}	Input equivalent noise temperature	K

THD	Total harmonic distortion	dB
THD_0	Total harmonic distortion including dc offset	dB
T_{H}	Equivalent temperature of noise source in its hot state	K
τ_{n}	Electron lifetime in p-type neutral silicon	s
T_{out}	Output equivalent noise temperature	K
t_{ox}	Gate-oxide thickness	nm
τ_{p}	Hole lifetime in n-type neutral silicon	s
t_{Si}	Silicon film thickness	nm
T_0	Standard noise temperature (=290 K)	K
μ_{eff}	Effective mobility	$\mathrm{m}^2/(\mathrm{V.s})$
V_{BS}	Body-to-source voltage	V
V_{DD}	Power supply voltage	V
V_{DS}	Drain-to-source voltage	V
$V_{\mathrm{DS,sat}}$	Drain-to-source saturation voltage	V
V_{EA}	Early voltage	V
V_{FB}	Flat-band voltage	V
V_{GS}	Gate-to-source voltage	V
V_{GT}	Gate overdrive voltage ($V_{\mathrm{GS}} - V_T$)	V
V_T	Threshold voltage	V
V_{T0}	Threshold voltage at zero body bias	V
$V_{T,\mathrm{off}}$	Threshold voltage at zero gate bias (OFF state for DTMOS)	V
X_{D}	Depletion width	nm
X_{Dmax}	Maximum depletion width	nm
Y_{cor}	Noise correlation admittance	Ω^{-1}
Y_{opt}	Noise optimum admittance	Ω^{-1}
Y_{out}	Output admittance	Ω^{-1}
Y_{s}	Noise source admittance	Ω^{-1}

AUTHOR'S PUBLICATION LIST

Journal papers

[1] **M. Emam**, J. C. Tinoco, D. Vanhoenacker-Janvier, and J.-P. Raskin, "High-temperature RF behavior of partially-depleted SOI MOSFET transistors," *Solid-State Electronics*, vol. 52, no. 12, pp. 1924–1932, Dec. 2008.

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[5] C. Urban, **M. Emam**, C. Sandow, J. Knoch, Q.-T. Zhao, J.-P. Raskin, and S. Mantl, "Radio frequency study of dopant-segregated n-type SB-MOSFETs on thin-body SOI," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 537–539, Jun. 2010.

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Research is the effort of the mind to comprehend relationships which no one has previously known, and in its finest exemplification it is practical as well as theoretical, trending always toward worthwhile relationships, demanding common sense as well as uncommon ability.

H. D. Arnold, 1925,
first research director at Bell Labs

The transistor was probably the most important invention of the 20^{th} Century, and the story behind the invention is one of clashing egos and top secret research ...

Ira Flatow, Transistorized!,
PBS (www.pbs.org)

CHAPTER 1

INTRODUCTION

The main objective of this work is to provide a link between the device level engineering and the RF circuit design world. To fulfill this objective, a wide variety of MOSFET devices are studied. The study is meant to cover different aspects of operation in order to ensure a correct choice of the device based on a complete knowledge of its characteristics. From the RF point of view, for this study to be as complete as possible, it should include dc, analog, RF, nonlinear, low voltage low power, high frequency noise, and high temperature characterizations. The dc and analog characteristics of the device form the base for the figures of merit for the RF operation. In other words, the formula of any RF figure of merit consists basically of dc and ac parameters. A good understanding of the dc and analog characteristics help to improve and optimize the RF behavior of the device. This is made clear in chapter 3 which also includes the high temperature aspect of the dc, analog, and RF characteristics. The high temperature characterization is essential for the new and emerging technologies due to the cohabitation of a large number of transistors on a small area resulting in elevated temperature operation conditions. The shift in the device characteristics due to this high temperature operation should be taken into account while designing the RF circuit to avoid failures and malfunctions. In addition, the high temperature operation conditions are gaining more grounds since the RF circuits are used more and more in applications related to harsh environments, such as

automotive electronics, on-engine, wheel-mounted, aerospace and environmental monitoring, including mining and well logging. All these applications are increasingly employing RF circuits especially for wireless communication systems and detectors.

The wireless communication is, in fact, a highly accelerating market especially the consumer applications sector. Competition pushes RF circuits to deliver better performance while minimizing its area and its power consumption. The target is to ensure portability and maximize the battery life time. Low voltage low power operation scheme is therefore a crucial solution. A complete chapter is devoted for this operation scheme including novel ideas aiming to optimize RF characteristics under conditions of low voltage low power and high temperature conditions.

The performance of RF circuits has two axes; frequency and amplitude. The frequency axis is usually limited by the cutoff frequency figures of merit (current gain cutoff frequency and maximum oscillation frequency) which are studied in chapter 3. On the other hand, the amplitude axis has a maximum and a minimum limit, or a floor and a ceiling. The minimum limit is the high frequency noise level, characterized by the noise figure NF or the minimum noise figure $NF_{\min}$ along with the other noise parameters as presented in chapter 6. The maximum limit is the linearity of the devices and the circuit. Nonlinear figures of merit such as the 1-dB compression point and the third intercept point quantify the ceiling of the performance of the RF circuit, which is the subject of chapter 5. The area between these two limits constitutes the dynamic range of the RF device or circuit. The wider this area the more adapted the device for a better performance. There are solutions to maximize the dynamic range at the circuit design level. In this work, the focus is directed to the solutions based on the device level. Novel device structures such as the Graded Channel MOSFET (GCMOS) is presented as one solution that could fulfill this task.

In order to close the loop, the RF performance of the variety of MOSFET devices considered in this work is examined through design, fabrication and, testing of one simple RF circuit, yet very important, the RF antenna switch, presented in chapter 7. Including only four transistors and four resistors, the RF antenna switch serves as a good demonstrator of the RF characteristics of the different devices. Nevertheless, not all the aspects of operation, presented through the different chapters of the thesis, could be directly verified through such a simple circuit. Thus, a table of different figures of merit is built gradually throughout the chapters in order to provide a complete comparison between the devices at the conclusion of the thesis.

It is worth noticing that all results presented in this thesis are based on real on-wafer measurements, with the exception of few ADS simulations presented for the RF antenna switch in chapter 7. All results are either published, submitted for publication, or under preparation for publication. Publications are referenced in their appropriate locations throughout the thesis and are also listed in the author's publication list.

CHAPTER 2

VARIOUS MOSFET STRUCTURES

THE understanding of the basic characteristics of the building block of any work is a key point in the success of this work. The transistor constitutes the main building block of any electronic circuit nowadays. In the context of this work, high frequency electronic circuits are concerned. Several flavours of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) are studied. This chapter introduces the characteristics of these different flavours in preparation to the next chapter where the measurements and analysis of various operation aspects as well as detailed comparisons are presented for all of the considered devices.

2.1 MOSFET

Garner, L. E., Jr. once defined the transistor as [1]:

> "The transistor is basically a current operated device. Thus, the transistor operates as a current amplifier ... The vacuum tube, on the other hand, operates as a voltage amplifier ..."

The concept of a Field-Effect Transistor (FET) was patented in the year 1926 by the polish-american physicist and inventor Julius E. Lilienfeld [2] (filed October 8^{th}, 1926 in US and earlier on October 22^{nd}, 1925 in Canada). Lilienfeld's patent described a three-electrode amplifying device based on the semiconducting properties of copper sulfide. He then added two other patents describing the

control of current in a device by means of an electric field [3, 4]. This pioneering work was followed by a patent by Oskar Heil of the university of Berlin in 1935 which contained the first description of an insulated-gate FET that hinted at the new semiconductor concepts. [5].[1]

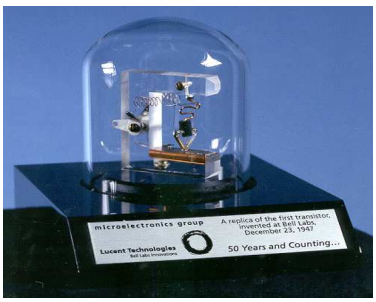
After the successful invention of the first solar cell using a *pn* junction diode by Russel Ohl [12] (patent filed May 27th, 1941), Bell labs started a research group in 1945 led by William Shockley and including John Bardeen, Walter Brattain, and others, with the target of finding a replacement of the vacuum tubes.[2] Mission was accomplished on December 23rd, 1947 when Bardeen and Brattain designed an amplifying circuit using a point contact "transfer resistance", to be known later as a "transistor". This device was patented later in 1950 (filed June 17th, 1948) as the first transistor ever: The germanium "Point Contact Transistor" [9, 10, 14–17] (see Fig. 2.1). However, this transistor was not easy to fabricate, hence, W. Shockley introduced the first junction transistor [18], patented in 1951 [19] (filed June 26th, 1948) which took its place in commercial products within few years [20].

Although the point contact transistor was not a field-effect transistor (which was the aim of the research of Shockley's group from the begining), the idea of field-effect was not completely abandoned. Shockley's group patented several field-effect devices. Bardeen's patent in 1950 [9, 10] (two complementary patents) is a sourceless MOSFET, whereas Brattain and Gibney's patent in 1950 [23] is a gated p-n junction, i.e. an inversion-channel insulated-gate FET.

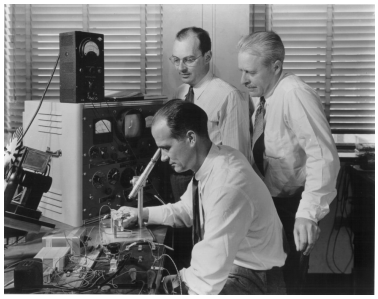
The first junction field-effect transistor (JFET) was invented and tested by W. Shockley and his group in 1952 [11]. The effort of this research group was rewarded by the Nobel prize of physics in 1956 [24]. Although, this research group started working on a FET, where Shockley failed to realize a working

[1] It has been long believed that the FET was first invented in the 1940's by Shockley, Bardeen, and Brattain. However, Robert G. Arns published a detailed article of the history of FET in 1998 [6]. Arns showed that as early as 1964, Virgil Bottom published a paper drawing the attention to the preceding work of Lilienfeld and his right to be declared the first to invent the FET [7]. Three months later, J. B. Johnson (then recently retired from Bell Labs) published a reply saying that the he tried himself to reproduce the transistor patented by Lilienfeld and it failed to work [8]. Nevertheless, in 1991 Bret Crawford, in his physics MS thesis, was able to reproduce a working version of Lilienfeld transistor, though not stable. However, in 1995, Joel Ross replicated the same transistor described by Lilienfeld and this time it was functioning and stable for several months. Arns also showed that he himself examined the files of the patents of Bardeen and Brattein [9, 10] and that of Shockley [11], and he found that a total of 65 claims were abandoned or disallowed in these two patents; the reason most frequently cited for disallowing a claim was Lilienfeld's prior art.

[2] According to the information available on the official site of Alcatel-Lucent Bell Labs [13], in the 1930s, Bell Lab's director of research, Mervin Kelly, recognized that a better device was needed for the telephone business to continue to grow. He felt that the answer might lie in a strange class of materials called semiconductors but, in order to get there, they had to pioneer a whole new class of science. After the end of World War II, Kelly put together a team of scientists to develop a solid-state semiconductor switch to replace the problematic vacuum tube. The team would use some of the advances in semiconductor research during the war that had made radar possible. A young, brilliant theoretician, Bill Shockley, was selected as the team leader.



(a) A replica of the first transistor: The "Point Contact Transistor" [21].



(b) William Shockley, (seated), John Bardeen (left), and Walter Brattain (right) invented the transistor in 1947 (Photo credit: Alcatel-Lucent/Bell Labs) [22].

Fig. 2.1.: The first transistor and its inventors.

FET in the early 1940's [20], the invention of the point contact transistor and the junction transistor took Bell Labs away from the path of FETs, as Bell Labs got committed to the silicon BJT in 1955 [6] (although they were able to solve the interface states problems at the surface of silicon by 1955 as published by G. C. Dacey and I. M. Ross in the Bell Systems Technical Journal [25]).

Nevertheless, it was Texas Instruments who introduced the first commercial silicon transistor when Semiconductor R&D chief Gordon Teal (ex-researcher at Bell Labs) presented it at the Institute of Radio Engineers National Convention in Dayton, Ohio, on May 10^{th}, 1954 [26] (see Fig. 2.2).

In 1956, M. M. Atalla was made head of a group to work on surface problems at Bell Labs. Three years later, in the Bell Systems Technical Journal, M. M. Atalla presented the first p-channel MOSFET device [27]. A year later, the p-channel MOSFET device was presented by a researcher of his group, Dawon Kahng, in the Solid State Device Research Conference in Carnegie Institute of Technology [28]. However, due to the comittement of Bell Labs to BJT, the first commercial MOS transistor was not fabricated in Bell Labs. It was fabricated by Jean Hoerni at Fairchild Semiconductor Corp in 1960 [29] (who presented it in the same conference where Kahng and Atalla described their p-channel MOSFET). Hoerni used his patented planar process which allowed transistors to be fabricated from silicon rather than from germanium [30]. Bell did not start a development project using MOS technology until 1966 [6].

The MOSFET device was then studied and characterized by Ihantola and Moll [31], Sah [32] and Hofstein and Heiman [33]. The technology, the application, and the device physics were the objective of many text books, e.g. [34–37].

The concept of the integrated circuit (IC) was first published by Geoffrey W. A. Dummer in the US Electronic Components Symposium in Washington D.C. on May 7^{th}, 1952 [38]. He stated that

> "With the advent of the transistor and the work on semi-conductors generally, it now seems possible to envisage electronic equipment in a solid block with no connecting wires. The block may consist of layers of insulating, conducting, rectifying, and amplifying materials, the electronic functions being connected directly by cutting out areas of the various layers."

However, his trial to build an integrated circuit in 1956 was not successful. Later, in 1958, Jack Kilby, a newly hired engineer at Texas Instruments, was able to build the first integrated circuit which was patented few years later [39] (filed on February 6th, 1959). In 1961, Fairchild and Texas Instruments both introduced the first commercial IC.

In 1963, Wanlass and Sah of Fairchild introduced one of the most important milestones in the transistor history, the Complementary MOSFET (CMOS) [6]. In the same year, RCA introduced the first MOS IC [38].

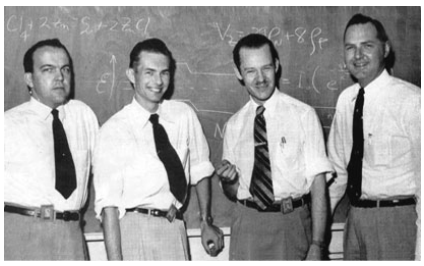
The market of MOSFET continued to grow up (mainly thanks to the computer industry) until it surpassed a $1 billion in sales in 1962, $10 billion in 1978 and $100 billion in 1994 [38]. Since the begining, the MOSFET technology has been following the famous Moore's law, given by Dr. Gordon E. Moore (then one of the founders of Fairchild Semiconductor and Director of the research and development laboratories) in 1965 [40] in which he observed that "The complexity for minimum component cost has increased at a rate of roughly a factor of two per year". Thus he predicted that the number of components the industry would be able to place on a computer chip would double every year. In 1975, he updated his prediction to once every two years. It has become the guiding principle for the semiconductor industry to deliver ever-more-powerful chips while decreasing the cost of electronics [41].[3]

2.2 SOI AND BULK

The idea of building MOSFET transistors on top of an isolator layer is nearly as old as the MOSFET transistor itself. The story started with the successful work of H. M. Manasevit and W. I. Simpson to grow a single-crystal silicon on sapphire substrate in 1964 [43]. Most probably, another research group was working on the same idea in parallel and by the end of the same year C. W. Mueller and P. H. Robinson introduced the first Silicon-on-Sapphire (SOS) transistor fabricated using standard diffusion and photoetching techniques whereas the gate oxide was thermally grown [44, 45]. This later work inspired C. A. T. Salama and L. Young to realize transistors on sapphire but using evaporation silicon films on sapphire [46]. Later, the first silicon on insulator (not yet named SOI) was introduced by C. H. Fa and T. T. Jew [47]. They called it the Poly-Silicon Field-Effect Transistor (PSFET) because the active element was fabricated in an epitaxially deposited film of polycrystalline silicon on an oxidized single crystal silicon substrate. In 1972, T. I. Kamins introduced the first Dielectric Isolation

[3] In 2005, Gordon E. Moore himself expected that his law cannot hold anymore and he declared it dead! [42]

(a) When TI announced commercial availability of the silicon transistor in 1954, this photograph of a silicon transistor superimposed on a three-cent U.S. postage stamp was used to show its relative size (Courtesy of Texas Instruments) [26].



(b) The silicon transistor development team from a photograph in the company's internal publication, Texins, in June 1954. Pictured, left to right, are Willis Adcock, Mort Jones, Ed Jackson, and Jay Thornhill. Pat Haggerty honored the team at the company's strategic planning conference in 1980 (Courtesy of Texas Instruments) [26].

Fig. 2.2.: The first commercial silicon transistor and its inventors.

(DI) technique (still not named SOI, although it is practically an SOI) using an electrochemical etching process [48]. His idea was to to form a thin silicon film from a thick single-crystal silicon wafer by an electrochemical etching technique that stops at a well-defined n-n^+ interface. As opposed to the heteroepitaxial case of SOS, the DI technique does not suffer from mismatch limitations and the minority carrier lifetime is significantly improved.

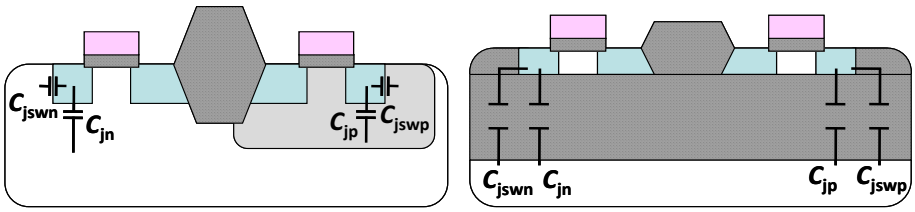
Between 1976 and 1979, a new device, attractive for its high speed switching operation, was introduced. This device used a localized buried oxide layer beneath the active area of the transistor and was called the Buried Oxide MOSFET (BO-MOS) [49–52]. In their work, they aimed to mimic the advantages of SOS MOS devices (high speed switching) while eliminating its drawbacks (expensive substrate and high junction leakage due to high defect density in the epitaxial silicon) [49]. In 1978, K. Izumi *et al.* introduced the SIMOX technique ("Separation by IMplanted OXygen") to create a buried SiO_2 layer and presented a fabricated 19 stage MOSFET ring oscillator on top of it [53].

It was not until 1979 that the term Silicon-on-Insulator was introduced by A. F. Tasch *et al.* when he introduced the first MOSFET transistor built on top of a thick SiO_2 layer which covers the whole silicon substrate [54]. He used the laser-recrystallised polysilicon films technique introduced by K. F. Lee *et al.* earlier to build a MOSFET on top of a nitride insulator layer [55]. Tasch *et al.* argued the better properties of SiO_2 as an insulator than the nitride Si_3N_4 used by Lee *et al.* [55].

Over the last 40 years, the fabrication of SOI enormously evolved through many academic and laboratory techniques including polysilicon melting and recrystallization, homoepitaxial, FIPOS, ion beam synthesis (such as SIMOX),

wafer bonding and etch back (BESOI), and finally through large scale commercialized techniques which are basically layer transfer techniques such as Smart-Cut® [56] and Eltran® [57] (see [58] for detailed description of different techniques).

The principal motivation for why researches have been giving all this attention for the development of the SOI technology is its high speed switching characterisitcs, which is direclty related to its highly reduced junction capacitance of the drain diffusion compared to bulk (conventional) MOSFET devices [49]. Depending on the buried oxide thickness, a remarkable decrease in the drain (source) junction capacitance (C_{bd} and C_{bs}) can be achieved in comparison to the bulk case, both for the bottom and the side-wall components (see Fig. 2.3) [59]. For a 1-μ m CMOS process, a reduction up to one seventh could be obtained for these capacitances. This factor can be increased to the order of 10 for recent technologies [59]. This is also manifested in the reduction of Metal-1-to-substrate capacitance, which can be reduced by 40% in SOI compared to bulk [58]. Typically, this reduction in parasitic capacitances is translated into a SOI device that can deliver 30 to 40% less power and operate faster by 30 to 40% than a bulk device [59].



(a) Bulk CMOS. (b) SOI CMOS.

Fig. 2.3.: Comparison of bulk and SOI junction capacitances for a typical CMOS process, C_{j} and C_{jsw} denote the bottom area and sidewall peripheral junction components at zero bias, respectively (Courtesy of [59]).

It is also worth mentioning that the SOI CMOS technology offers a great advantage at the level of the layout design, since a significant gain of area can be achieved using the SOI technology [60].

SOI devices are more reliable for harsh environment applications (space applications, high temperature applications, etc.) thanks to their buried-oxide. While bulk devices would fail to operate at temperatures higher than 180^{o}C, due to elevated leakage current, SOI devices can function correctly up to 300^{o}C [58].

On the other hand, the presence of the buried oxide prevents a good heat dissipation path through the substrate due to the poor thermal conductivity of SiO_2. A "Self Heating" phenomenon results due to the substantial increase in the device temperature. The dissipation of the excess heat is deviated towards the contacts and the metal layers. As a result, a negative resistance can be seen in

the output characteristics of the SOI device due to the reduction of the mobility as a direct consequence of the elevated temperature.

2.3 PARTIALLY- AND FULLY-DEPLETED

Two main categories of SOI MOSFETs exist: the Partially-Depleted (PD) and the Fully-Depleted (FD) SOI MOSFETs. The PD SOI MOSFET is more commonly used in the electronics market. This is because it is easier to fabricate than the FD SOI MOSFET. It is simply completely compatible with the traditional bulk fabrication process with the use of a SOI wafer. On the other hand, the FD SOI MOSFET is a delicate process in which the silicon film thickness t_{Si} is a very sensitive parameter and its homogeneity all over the wafer is crucial for a successful FD process.

In fact, based on the thickness of the silicon film and its doping level, and knowing that the maximum depletion width is given by (2.1)

$$X_{\mathrm{Dmax}} = \sqrt{\frac{4\varepsilon_{\mathrm{Si}}\psi_{\mathrm{F}}}{qN_A}} \tag{2.1}$$

a device could be categorized in one of three categories (see Fig. 2.4) [58]:

- Partially-Depleted (PD) SOI: in which the film thickness, t_{Si}, is larger than twice the value of X_{Dmax}; $t_{\mathrm{Si}} > 2X_{\mathrm{Dmax}}$. The body of the device (the silicon film) is never (under any biasing condition) completely depleted. On the contrary, unless a contact exits that ties the body to a certain bias, the body is kept "floating" and a series of phenomena called "floating-body effects" (FBE) take place. As a result, two sub-categories of SOI devices exist; floating-body (FB) and body-tied (BT) devices (this subject is detailed in section 2.5.
- Fully-Depleted (FD) SOI: in which $t_{\mathrm{Si}} < X_{\mathrm{Dmax}}$. Except for special bias conditions, the silicon film is entirely depleted and the device is free from FBE due to the reduction of the source barrier [59]. FD devices are considered to deliver superior characteristics as compared to PD devices thanks to a better control of the gate terminal on the channel. Based on a better front-to-back gate coupling through the Fully-Depleted film capacitance, when compared to bulk devices and even to PD devices, FD devices exhibit sharper subthreshold slope close to the ideal value of 60 mV/dec at room temperature, improved drive capability due to smaller body effect, and less mobility degradation with gate voltage [61]. On the other hand, FD devices suffer from a significant sensitivity of the threshold voltage to the film thickness and buried oxide parameters. This could also result in failures of FD devices in total-dose radiation hardness applications [59]. M. J. Sherony *et al.* reported a reduced dependence of threshold voltage on film thickness by keeping the total dose constant instead of the doping concentration [62]. This can result in a threshold voltage standard deviation being similar to the bulk case [59].

– Near-Fully-Depleted (NFD) SOI: this is an intermediate case where $X_{\mathrm{Dmax}} < t_{\mathrm{Si}} < 2X_{\mathrm{Dmax}}$. Depending on the back gate bias, the silicon film might or might not be entirely depleted.

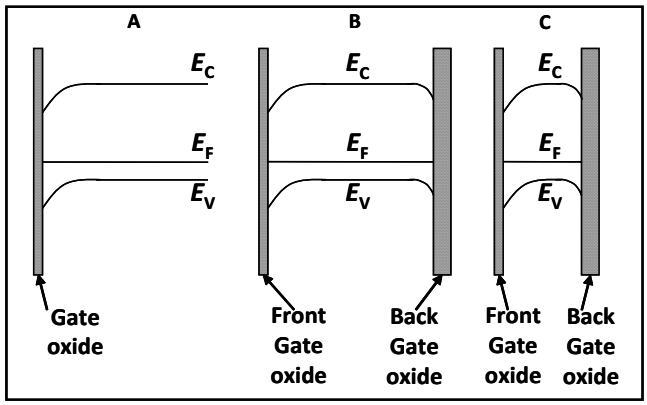


Fig. 2.4.: Energy band diagrams in bulk (A), PD SOI (B) and FD SOI (C). All devices are represented at $V_{\mathrm{GS}} = V_T$. SOI devices are represented for a condition of weak inversion (below threshold) at the back interface (Courtesy of [58]).

2.4 DNW BULK

In 1992, R.-H. Yan *et al.* raised the question of whether the technology will go back to bulk after migrating to SOI [63]. Yan based his assumption on the scaling trends which lead to excessively high doping requirements, causing undesirably large junction capacitances and degraded mobility. He then proposed a technique called "Pulse-Shaped Doping" which results in a bulk device which mimics the advantages of a SOI device for deep sub-micrometer regime.

A deep n-well (DNW) protected structure of Bulk-Si is then considered as a candidate that combines the mainstream low cost Bulk-Si technology with the advantages of the SOI technology. This special structure of Bulk-Si was presented by Su *et al.* [64] to improve RF performance in Bulk-Si transistors. Su *et al.* used a floating DNW. The high temperature RF characteristics of a grounded DNW protected Bulk-Si device was briefly compared to the PD SOI device in [65]. The device is aimed to mimic the structure of a SOI device through completely isolating the body of the transistor by using a deep n-well and a vertical n^+ implantation (known as NISO: N Isolation), as shown in Fig. 2.5. A more interesting case would be a V_{DD} connected DNW, since the body is p-type, thus connecting the DNW to V_{DD} ensures a reverse biased body-DNW junction at all time therefore highly reducing leakage currents especially at elevated temperatures as is shown in section 3.2.6.

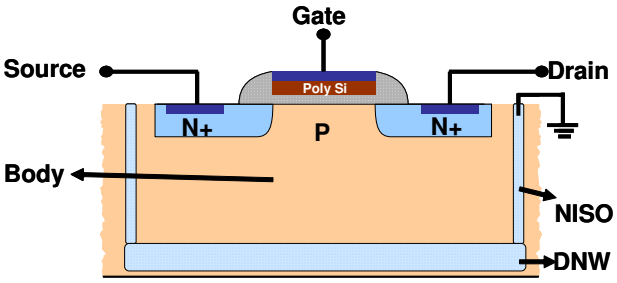


Fig. 2.5.: A cross section of a DNW protected Bulk-Si MOS transistor.

From Fig. 2.5, it can be clearly seen that the DNW bulk device would occupy more area than a conventional bulk device or even a SOI device especially if each device of the circuit is individually protected (which is the optimum case). Nevertheless, the attractive characteristics of such a device promotes it to be used for analog and RF small circuits which do not use a big number of transistors and in which the required silicon area is mostly determined by the passive components, as it is the case in the RF antenna switch circuit [65].

2.5 FLOATING-BODY AND BODY-TIED STRUCTURES

A PD SOI device in which the body is not connected to any terminal is referred to as a floating-body FB device. This results in what is known as the Floating-Body Effects (FBE), mostly manifested in the kink effect, the parasitic BJT effect, the anomalous subthreshold slope, the reduced drain breakdown voltage, and other effects [58]. In general, the FBE is only seen in PD devices whereas it is not apparent in FD device, as will be explained hereafter.

The kink effect phenomenon had already been identified for SOS devices as early as 1975 [66]. The kink effect is now mainly noticed in PD SOI devices. It can also be seen in bulk devices operated at low temperatures [67] or Deep N-Well protected bulk devices [65].

The kink effect is a direct consequence of impact ionization. At elevated values of drain voltage, the electron in the channel has enough energy in the high electric field region near the drain to generate an electron-hole pair. The generated electron is easily drained through the drain terminal, whereas the hole seeks the lowest potential point, which is the source, and it moves towards it. However, since the body-source energy barrier is high (due to the presence of the non-depleted neutral region in the PD device), the hole cannot be removed through the source terminal and it has to stay in the floating-body non-depleted neutral region. The continuous generation of electron-hole pairs by impact ionization results in an accumulated reservoir of holes in the neutral region whose potential starts to increase. The calculation of the potential of the floating-body area is not

simple and requires an iterative solution of complex equations [58, 68]. At a certain point, the floating-body acquires enough potential (∼0.7 V) to turn ON the body-source p–n junction. At this particular moment, the kink effect takes place, since a sudden increase in the net drain current occurs giving rise to a "kink" in the drain-current drain-voltage I_{DS}-V_{DS} characteristics (see Fig. 2.6). In the same time, the threshold voltage of the device is reduced since the body-source bias V_{BS} acts as the body bias (body effect) in bulk devices (see (2.3)).

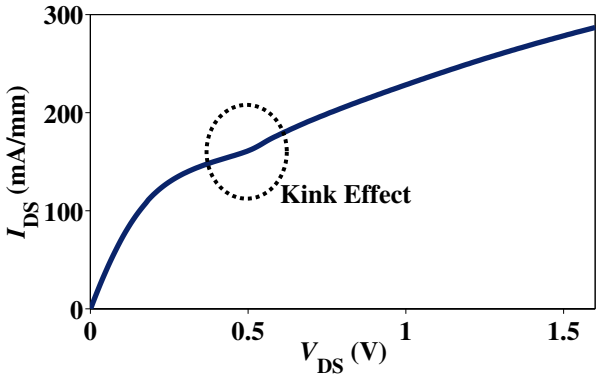


Fig. 2.6.: An illustration of the kink effect phenomenon appearing on the I_{DS}-V_{DS} characteristics of a PD FB device at a $V_{\mathrm{GS}} = 0.6$ V.

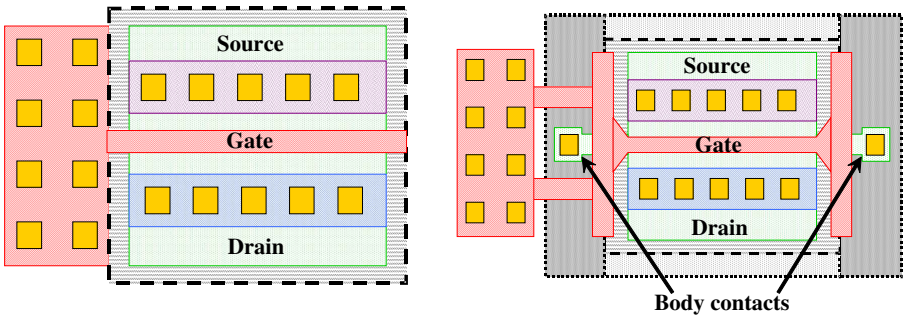
In FD devices, the kink effect is not apparent for two reasons. First, the electric field near the drain is lower than the case of the PD devices as can be seen through TCAD simulations [58]. Second, the energy barrier between the body (the thin film of Si) and the source is very low, hence, the holes generated from impact ionization are easily removed through the source terminal. Under certain bias conditions, especially for a negative back-gate bias, this energy barrier is increased, and a kink effect can appear.

The presence of the floating-body can also be problematic when combined with the parasitic BJT which exists naturally in a MOSFET. The source-body-drain junctions constitute a parasitic BJT device (NPN or PNP). In devices where a body contact exists, the body (or the base of the parasitic BJT) is always tied and the BJT is always OFF. However, for a floating-body case, the potential of the body depends on the currents flowing through it. Thus, the BJT can be triggered ON, and results in undesirable consequences like the amplification of the impact ionization, a significant reduction of the subthreshold swing (the inverse of the subthreshold slope S), and a reduced drain breakdown voltage.

A special effect can also take place due to the presence of the floating-body. In the subthreshold regime, at low values of V_{GS} but high enough values of V_{DS}, the weak inversion current can result in impact ionization in the high electric field region near the drain. The same mechanism like in the kink effect occurs where

the body potential increases leading to a reduction of V_T. The whole I_{DS}–V_{GS} characteristic shifts to the left, and the subthreshold swing shows a slope less than the theoretical limit of 60 mV/decade. If the minority carriers lifetime is high enough, the parasitic BJT can amplify the base current (or the hole current generated by impact ionization) which can then constitute a positive feedback loop on the current flowing through the device, thus the drain current suddenly increase. As a result, a subthreshold slope of zero mV/dec can be observed [58, p. 209]. This phenomenon is called the "single-transistor latchup". More problems related to the FBE can be found in [58].

The Body-Tied structure is intended to solve all these problems related to the floating-body effect. A silicide body contact is added to the traditional structure (the floating-body structure) and is then shorted to the source. As a result, the body is always tied to the source, which is in turn tied to the ground. The layouts of the two structures are presented in Fig. 2.7. The advantage of the BT structure is obviously the suppression of the floating-body effects. It also has other advantages relative to the I–V characteristics as will be detailed in section 3.2.2. However, the BT transistor occupies more area and thus is not suitable for high density circuits. It is mostly used in analog and RF circuits where the number of transistors is relatively small and the area constraint is more relaxed.



(a) FB structure layout. (b) BT structure layout.

Fig. 2.7.: Floating-Body versus Body-Tied structures.

2.6 DYNAMIC THRESHOLD MOSFET (DTMOS)

In CMOS digital circuits, the delivered power is proportional to the square of the power supply voltage according to:

$$P = CV_{DD}^2 f \tag{2.2}$$

From which it is seen that an effective method of reducing the active power in CMOS digital circuits is to reduce the power supply voltage V_{DD}. This reduction of V_{DD} is limited by the minimum threshold voltage that can be tolerated in these circuits. Normally, V_{DD} cannot go below $\sim 3V_T$, otherwise this will importantly degrade the switching speed of the gate. It will also degrade the subthreshold characteristics leading to an increased stand-by current in static circuits and may produce failures in dynamic circuits and memory arrays.

Therefore the ideal solution is to implement a MOSFET with a dynamic threshold voltage, which means that V_T is low when the device is turned ON for high gate overdrive, whereas V_T is high when the device is turned OFF for low subthreshold leakage. Dynamic Threshold Voltage MOS (DTMOS) is then considered as the best alternative for ultra low power CMOS applications.

On the other hand, the conventional scaling theory states: "The physical dimensions and applied potentials must be scaled by the same factor, whereas the impurity concentration is increased by the reciprocal of such factor" [69]. This scaling theory has some limitations [70]:

- Temperature dependence of V_T, which is mainly due to the variation of the substrate Fermi level with temperature.
- Non-scalability of the junction built-in potential, leading to a larger depletion width and worsening of the short channel effects.

These drawbacks can be solved by forward biasing of the substrate which helps to avoid short channel effects and to reduce the sensitivity of V_T to the channel length. Thus DTMOS is constructed by connecting the floating body to the gate in a short channel SOI MOSFET as shown schematically in Fig. 2.8. Usually, the floating body of the SOI MOSFET is connected to the gate using a P^+–metal contact. This is in complete compatibility with the CMOS fabrication process, as it uses the same techniques used to control the floating body by connecting it to the source terminal or to a ground pin.

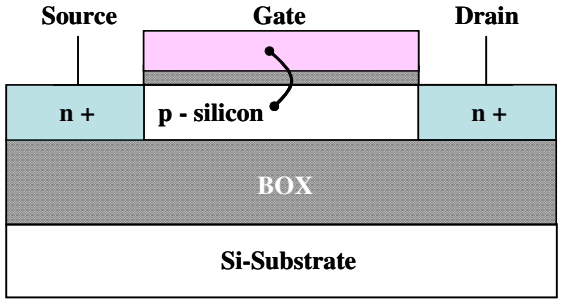


Fig. 2.8.: A cross section of the Dynamic Threshold MOS transistor.

The DTMOS was first introduced as a hybrid bipolar-MOS transistor in 1987 [71] in the form of a voltage controlled bipolar-MOS transistor. This was mainly aimed for high-speed operation as the device was capable of both reduced voltage

swing operation and high current drive. In this device, the body bias has to be relatively high ($\geqslant 0.6$ V) allowing the lateral bipolar current to be added to the current drive capabilities of the device. However, this advantage comes at the cost of increased input (base) current which results in elevated standby current. In 1994, DTMOS was explicitly introduced as a highly recommended solution for ultra-low power applications [72] where the body bias is kept below 0.6 V. Although possible in bulk devices, the advantage of highly reduced junction areas in SOI helps to impressively reduce the base current in a DTMOS. Since then, aggressive technological improvements led to successful fabrication of bulk and SOI DTMOS, and numerous efforts have been put to deeply characterize and model it [73]. Whether used for high-speed operation or for ultra-low power applications, the DTMOS merits the advantages of ideal subthreshold characteristics, reduced body effect, improved drive current [58], higher carrier mobility [72], and superior high frequency characteristics [74].

2.6.1 DTMOS Operation

2.6.1.1 DC Operation

A DTMOS device can be considered as two devices in one structure (or a twin device); a MOSFET and a bipolar junction transistor (BJT). For the case of a n-channel MOSFET device (with a NPN BJT device), when the device is OFF, i.e. $V_{GS} = V_{BS} = 0$, the potential of the body (or the base) is low, hence V_T is maximized (having the same value of V_T of a conventional MOSFET), which also results in minimum OFF current. When the device is turned ON, i.e. $V_{GS} = V_{BS} = V_{DD}$, the body-source junction is forward biased and because of the well known body effect, V_T is decreased to its minimum. As a result, the ON current is increased (compared to a conventional MOSFET) while the efficiency (gain) of the BJT device is increased and the effective neutral base width is decreased [71]. Therefore, the body-gate tie improves both the MOSFET and the BJT twin devices.

The reduced threshold voltage of DTMOS, which is also the result of the reduction in the depletion charge, leads to an increased inversion charge and higher current drive but at the cost of an increased effective gate capacitance.

To study the threshold voltage of a DTMOS, it is practical to assume that for low values of V_T, the BJT current is negligible in comparison to the MOSFET current, and hence the device can be treated as a pure MOSFET device whose V_T is modulated by the gate bias. The body effect in a DTMOS is identical to that of a bulk device and V_T can then be given by:

$$V_T = V_{T0} + \gamma \left(\sqrt{2\psi_F - V_{BS}} - \sqrt{2\psi_F} \right) \tag{2.3}$$

where γ is the body factor and is defined as:

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si} N_A}}{C_{ox}} \tag{2.4}$$

and V_{T0} is the threshold voltage at zero body bias ($V_{\mathrm{BS}} = 0$ V) and is given by:

$$V_{T0} = V_{\mathrm{FB}} + 2\psi_{\mathrm{F}} + \gamma\sqrt{2\psi_{\mathrm{F}}} \tag{2.5}$$

where V_{FB} is the flat-band voltage given by:

$$V_{\mathrm{FB}} = \Phi_{\mathrm{MS}} - \frac{Q_{\mathrm{ox}}}{C_{\mathrm{ox}}} \tag{2.6}$$

For a DTMOS, substituting $V_{\mathrm{BS}} = V_{\mathrm{GS}}$ in (2.3), the threshold voltage for a DTMOS is directly given by

$$V_T = V_{T0} - \gamma\left(\sqrt{2\psi_{\mathrm{F}}} - \sqrt{2\psi_{\mathrm{F}} - V_{\mathrm{GS}}}\right) \tag{2.7}$$

where the relation between the threshold voltage and the gate bias is clear. As V_{GS} increases, V_T decreases, and vice versa. It also shows that a DTMOS should be operated at low supply voltage since V_{GS} cannot exceed $2\psi_{\mathrm{F}}$.

The gate voltage of a DTMOS has to be limited to approximately one diode voltage ($\sim$ 0.7 V at room temperature) otherwise large body-to-source/drain junction capacitances and currents result. Large C_{bd} and C_{bs} will degrade the switching speed of DTMOS circuits. Also large diode currents will increase the static power dissipation of DTMOS circuits.

It is proved experimentally and analytically that a DTMOS can provide an ideal subthreshold swing of 60 mV/dec [75]. This means that a perfect coupling occurs between the gate bias V_{GS} and the surface potential ψ_{S}. If the interface traps are neglected, the subthreshold swing (or the inverse of the subthreshold slope) can be described by [58]:

$$S = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{\mathrm{D}}}{C_{\mathrm{ox}}}\right) \tag{2.8}$$

For PD SOI and bulk, the relation between the surface potential and the gate bias is:

$$\frac{\mathrm{d}\psi_{\mathrm{S}}}{\mathrm{d}V_{\mathrm{GS}}} = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\mathrm{D}}} \tag{2.9}$$

But in the case of a DTMOS, $V_{\mathrm{GS}} = V_{\mathrm{BS}}$, thus $\mathrm{d}\psi_{\mathrm{S}} = \mathrm{d}V_{\mathrm{GS}}$ or $\mathrm{d}\psi_{\mathrm{S}}/\mathrm{d}V_{\mathrm{GS}} = 1$. Therefore, S of a DTMOS can be simplified to:

$$S = \frac{kT}{q}\ln(10) = 60 \text{ mV/dec (at room temperature)} \tag{2.10}$$

Transconductance of the DTMOS is also significantly higher than for a conventional MOSFET. This increase of the total transconductance comes at the cost of a higher input capacitance. Indeed, the total body/gate capacitance is made of the gate capacitance of a MOSFET and the depletion capacitance.

The forward biasing of the source-substrate junction (SSJ) improves the transistor operation since the transverse electric field ($E\perp$) decreases, thus reducing

the degradation of the carrier mobility; and a higher mobility leads to a higher current drive capability which also improves the operating speed.

The amount of increased current drive in DTMOS is approximately proportional to $C_{\text{ox}}\Delta V_T$ where ΔV_T is the amount of V_T reduction caused by the forward body bias:

$$\Delta V_T \approx V_{\text{DD}} \frac{3t_{\text{ox}}}{X_{\text{D}}} \tag{2.11}$$

An increase of ΔV_T by increasing the body-effect parameter (which results from increasing the substrate concentration) also produces an undesirable increase of V_T. Thus, a trade-off between ΔV_T and V_T should be found in terms of the depletion width and the gate oxide thickness.

Using uniformly doped SOI MOSFET will have several limitations. If a laterally non-uniform well is used (with high doping concentration in the middle of the channel) large body effect can be obtained while minimizing C_{bd} and C_{bs} [76]. The sensitivity of V_T and ΔV_T to V_{BS} can also be increased using retrograde or counter-doping of the channel [77].

Standard DTMOS has a high body resistance, leading to a long RC delay of gate to body signal transmission. Dynamic operation speed of the circuit is severely restricted by this long delay. To reduce the RC delay, schemes need to be developed for connecting the gate to the body along the device width direction [76]. Another method for significantly reducing this delay is to build the DTMOS on bulk substrates using a triple-well process [78].

Therefore, in summary, as body potential ↑
⇒ vertical electric field ↓
⇒ mobility ↑
⇒ depletion region ↓
⇒ for short channel DTMOS g_D ↓
⇒ Early voltage V_{EA} ↑ (doubled)
⇒ degradation due to hot-carriers ↓ (due to the reduction of the electric field).

2.6.1.2 RF Operation

In a DTMOS, the "extrinsic" output conductance, defined by $\Re\,(Y_{22} + Y_{12})$, increases vs. frequency and the "extrinsic" transconductance, $\Re\,(Y_{21} + Y_{12})$ decreases. Therefore, it is expected that the benefits of DTMOS reduce as frequency increase [79, 80].

The useful effect of the DTMOS is related to $g_{m\text{b}}$ (the body to source transconductance). The influence of $g_{m\text{b}}$ vanishes when a signal comes from the gate. The extrinsic transconductance falls from $(g_m + g_{m\text{b}})$ to g_m. The highest gains of DTMOS for analog applications are obtained for frequencies below 200 MHz [79]. It is worth noticing that the output conductance g_D of the DTMOS is also increasing above 200 MHz. This variation of the output conductance is mainly related to the phenomena occurring in the thin film of silicon, and not in the underlying substrate. Similar variations have been observed using a high resis-

tivity substrate. Thus the variation of g_D can be related to a $g_{m\mathrm{b}}$ controlled by the drain through the body-to-drain junction.

Higher than few GHz, DTMOS acts similarly to a conventional MOSFET. But a reduction of V_T allows DTMOS to conduct more current and to have a higher transconductance than a usual MOSFET for the same bias. Practically, the contact between the gate and the floating body of the DTMOS does not bring any RF advantages as only DC bias is acting through this contact. On the contrary, it introduces real impedances at the input of the transistor, and as a consequence a loss of power. Indeed, any part of the incident power that goes through this input impedance does not bring any useful effect.

However, since the DTMOS is a device well suited for low voltage applications, its RF characteristics are better monitored at low bias levels. At low supply voltages (~ 0.7 V), DTMOS shows significantly higher f_T and $f_{\max}$ values than FB and BT conventional MOSFET transistors [74]. In 2001, the record $f_{\max}$ (185 GHz) was reported using a DTMOS device [81].

2.6.2 Channel Engineering of DTMOS

2.6.2.1 Vertical Doping Engineering for Enhancing ΔV_T

DTMOS can greatly enhance performance by engineering the vertical doping profiles to scale the depletion width X_{D} [77]. In DTMOS, the amount of increase in inversion charge ΔQ_{i} is a result of the decrease in the depletion charge:

$$\Delta Q_{\mathrm{i}} = 2\psi_{\mathrm{B}} C_{\mathrm{D}} - (2\psi_{\mathrm{B}} - V_{\mathrm{DD}})\, C'_{\mathrm{D}} = C_{\mathrm{ox}} \Delta V_T \tag{2.12}$$

where C'_{D} is the depletion capacitance when V_{BS} is charged up to V_{DD} and ψ_{B} is the difference between the Fermi potential and the intrinsic potential (mid-gap potential). This added gate-loading of $C_{\mathrm{ox}}\Delta V_T$ is beneficial to the device speed, in particular when the output loading is dominated by external capacitance and the delay is inversely proportional to I_{Dsat}. When C_{bs} and C_{bd} are small and can be ignored, the speed of the DTMOS operated at V_{DD} is effectively operated at $V_{\mathrm{DD}}+\Delta V_T$ because:

$$\tau_{\mathrm{d}} \propto \frac{C_{\mathrm{ox}} V_{\mathrm{DD}} \left(1 + \dfrac{\Delta V_T}{V_{\mathrm{DD}}}\right)}{I_{\mathrm{Dsat}}} \approx \frac{V'_{\mathrm{DD}}}{V'_{\mathrm{DD}} - V_{T,\mathrm{off}}} \tag{2.13}$$

When compared at the same delay and the same I_{OFF}, the reduction of the active power of the DTMOS is about $V_{\mathrm{DD}}/(V_{\mathrm{DD}} + \Delta V_T)$. Thus one major task in a DTMOS device design is to maximize ΔV_T. From (2.11), the key device design parameter is to reduce the depletion width X_{D}. Knowing that scaling X_{D} improves short-channel effects but results in increased subthreshold slope S in conventional MOSFET. However in DTMOS, S is always equal to the ideal value of 60 mV/decade. Low temperature epitaxy could provide a way to engineer profiles with very small X_{D}.

2.6.2.2 *Lateral Doping Engineering for Minimizing Parasitic Capacitances*

When the circuit speed is dominated by device capacitances, lateral doping engineering is important to reduce $C_{\rm bs}$ and $C_{\rm bd}$ in order to obtain performance improvements, especially in certain logic circuits where the Miller effect is important [77].

In ac conditions, the effect of $C_{\rm bs}$ and $C_{\rm bd}$ plays an important role in the device speed, particularly when the output loading is dominated by the device capacitance but not by the wiring capacitance such as in unloaded ring oscillators.

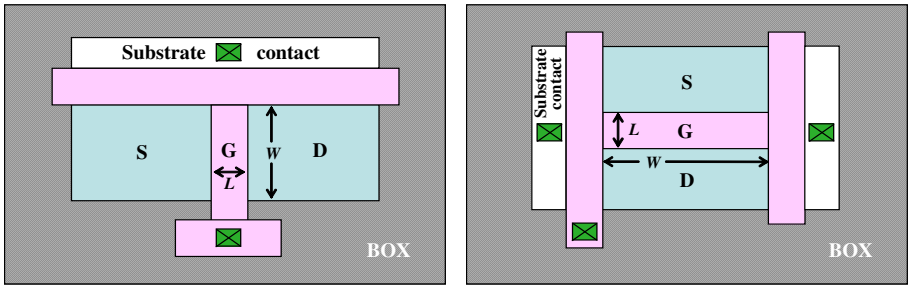
Scaling $X_{\rm D}$ increases the ratio of $C_{\rm D}$ over $C_{\rm bs}$ and $C_{\rm bd}$. $C_{\rm bs}$ and $C_{\rm bd}$ can be further reduced by using laterally-nonuniform local channel doping to reduce the overlap capacitance. The gate coupling effect is weakened when the wiring capacitance increases therefore the advantage diminishes.

Another important parasitic component is the parasitic resistance along the channel width direction because the contacts are at the sides of the device. The delay caused by the parasitic RC can be measured using body contact structures.

Using pulse measurement, the delay can be measured by monitoring the voltage rise at the drain terminal when a step voltage is applied to the body contact. The delay of a $W/L = 10/0.25$ device is approximately 100 ps [77].

2.6.3 Effect of Different Gate Structures

A H-gate structure has a larger threshold voltage reduction than a T-gate counterpart (see Fig. 2.9). This is because H-gate structures have higher body-effect factor. Since $I_{\rm Dsat} \propto (V_{\rm GS} - V_T)^2$, therefore as V_T decreases, $I_{\rm Dsat}$ increases. Thus, H-gate structures show higher saturation drain current than the T-gate ones. H-gate devices also show smaller DIBL and higher g_m in saturation region than T-gate ones due to its higher body-effect factor [82].



(a) T-gate structure. (b) H-gate structure.

Fig. 2.9.: Gate structures can strongly affect the threshold voltage.

2.6.4 Modeling of DTMOS

Conventional circuit model of MOSFETs is based on the depletion approximation, which is obviously violated by the presence of mobile charges owing to the forward biasing of the source-body junction [73].

Any MOSFET has an intrinsic BJT associated structurally with it. Under normal MOS operating conditions (reverse or zero biased body) this BJT is OFF. However, when the body is forward biased at voltages well above 0.6 V, the bipolar effect will be manifested. Most injected carriers from the source will be collected by the drain terminal; some will be recombined in the body [70]. DTMOS can be easily modeled as two transistors connected in parallel (MOSFET + BJT) [73].

A small signal equivalent circuit model for the intrinsic part of the DTMOS was proposed by T. Hirose *el al.* and is presented in Fig. 2.10 [81].

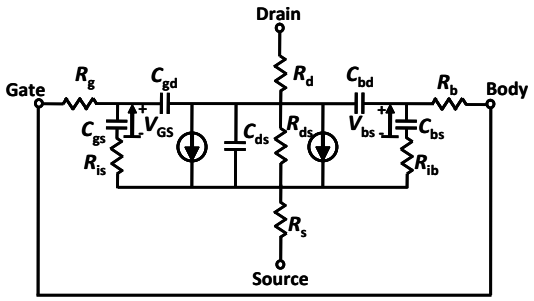


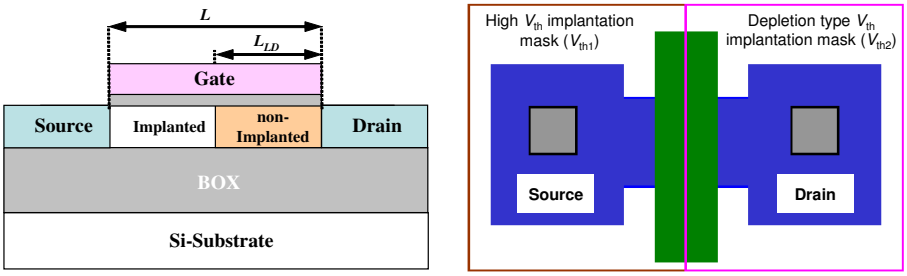
Fig. 2.10.: Small-signal equivalent circuit for a DTMOS device.

2.7 GCMOS

The idea of a Graded-Channel device was first introduced by T. A. DeMassa, G. G. Goddard, and G. T. Catalano in 1971 [83] and 1973 [84]. In 1975, T. A. DeMassa and S. R. Iyer proposed a closed form solution for a Graded-Channel Junction Field Effect Transistor (JFET) [85]. They also introduced a study of the thermal noise in the same device [86]. Later, in 1978, R. E. Williams and D. W. Shaw presented improved linearity and noise figure using a Graded-Channel FET [87]. The RF favoured performance of Graded-Channel devices over classical uniform doping devices was highlighted in 1980 by S. D. S. Malhi and C. A. T. Salama, where they reported a higher cutoff frequency for Graded-Channel FET [88]. The Metal-Oxide-Semiconductor MOS version of the Graded-Channel devices was introduced for the first time in 2000 by M. A. Pavanello *et al.* [89], and since then, it has received an increasing attention. In these academic devices, the implantation used to adjust the threshold voltage V_T is masked near the drain

over a distance L_{LD} (Lightly-Doped) (see Fig. 2.11a), yielding a high V_T region near the source in series with a low V_T region adjacent to the drain.

Nevertheless, in order to align the fabrication of GCMOS within the framework of an industrial standard CMOS process, a different procedure is used. The channel is shared between two different doping schemes introduced through two perfectly aligned masks, one for a high V_T (near the source) giving rise to V_{T1} and the other for a depletion mode MOSFET (near the drain) giving rise to V_{T2} (see Fig. 2.11b). The target is to introduce the maximum possible $\Delta V_T = V_{T1} - V_{T2}$. As a result, a lightly doped region is created near the drain over a length of L_{LD}. The high difference in V_T results in a naturally inverted region near the drain side (over L_{LD}) at approximately zero gate bias which emulates an extended drain area beneath the gate. Hence, the effective channel length is reduced from L (the drawn channel length) to $L_{\mathrm{eff}} = L - L_{\mathrm{LD}}$. The ratio L_{LD}/L defines the characteristics of the device [89].



(a) Cross-section of a PD GCMOS structure.

(b) Top view mask layout of the FD GCMOS structure.

Fig. 2.11.: PD and FD GCMOS structures.

The highly doped part of the channel at the source end improves the threshold voltage roll-off and the drain induced barrier lowering (DIBL), whereas the light doping near the drain ensures high mobility, reduced peak electric field, and lowered impact ionization [89–91]. It also results in higher Early and break down voltages [92]. As a result a better analog performance is achieved with a better intrinsic gain due to a higher dc transconductance (g_m) and a lower output conductance (g_D). In addition, the analog and RF characteristics of the GCMOS are highly improved with a higher current gain cut-off frequency (f_T) compared to classical MOSFET transistors [90–95].

The low frequency ($1/f$) noise performance of the Graded-Channel MOS (GCMOS) has also been analyzed in order to study the ability of this device to be used in the recent low-power low-noise applications [96]. In addition, using TCAD simulations, T. C. Lim *et al.* [97] showed that the minimum noise figure of the laterally asymmetric channel MOS should outperform the classical nMOS device for both bulk and partially-depleted SOI due to a higher correlation factor C in the Pucel's model [98–100]. On the other hand, Roy *et al.* described

the noise sources distribution along the channel and showed a higher correlation factor in the case of GCMOS transistor compared to classical nMOS [101].

2.8 SUMMARY OF DEVICES-UNDER-TEST

The devices considered in this work have been presented in this chapter. These device are characterized in chapter 3 in dc and RF regimes for wide temperature range (from room temperature till 250^{o}C) and also for low voltage low power applications in chapter 4. In chapter 5, the nonlinearity behavior of these devices are studied whereas in chapter 6 the RF noise performance of some of them is presented (mainly the GCMOS structure). Based on these different characterization schemes, chapter 7 shows the advantages and disadvantages of using these devices in RF circuits represented by the RF antenna switch.

All data presented throughout this work are measured data. The geometries and characteristics of the devices measured and presented in this work are summarized in Table 2.1. This table should evolve throughout with the extraction of different figures of merit.

Table 2.1.: A summary of the geometries and the characteristics of the devices considered in this work.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
t_{Si}(nm)	—	—	—	150	150	150	40	40
t_{ox}(nm)	2	2	2	2	2	2	2.5	2.5
t_{box}(nm)	—	—	—	400	400	400	145	145

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
t_{Si}(nm)	40	40	40	40	100	100	100
t_{ox}(nm)	2.5	2.5	2.5	2.5	4.5	4.5	4.5
t_{box}(nm)	145	145	145	145	400	400	400

DNW bulk devices and PD SOI devices are fabricated in the same foundry using the same technology but on different substrates. FD devices (FB and BT) presented in the first part of the table are fabricated in the same fab as FD devices (nMOS and GCMOS) presented in the second part of the table but on a different run, the GCMOS and nMOS being on a more recent and advanced one.

The shortest GCMOS that could be fabricated on this run has a drawn channel length of 0.24 μm and is thus compared to the shortest available classical nMOS (for this technology) of a drawn channel length of 0.15 μm since they both should have the same effective channel length (since L_{eff} of a GCMOS is equal to $L/2$ for the case considered in this work).

The comparison between a GCMOS and a classical nMOS of the same drawn channel length is guaranteed through the PD SOI devices shown in the second part of the table and are fabricated in a different facility than the PD SOI devices shown in the first part of the table. Notice that, in chapter 6, for a better RF noise characterization, a different set of devices with larger channel widths are used for the PD GCMOS devices.

Temperature measurements are performed between 25^{o}C (room temperature) and 250^{o}C using a temperature controlled chuck except for the case of FD devices since they showed a high sensibility and fragility at 250^{o}C and thus were measured till 200^{o}C only.

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CHAPTER 3

WIDE BAND AND HIGH TEMPERATURE CHARACTERIZATION

The various MOSFET structures presented in chapter 2 are the subject of a wide-band measurement and characterization campaign in the current chapter. The objective is to provide a deep understanding of the behavior of each structure and how it differs from the other structures. Based on this understanding, the merits and advantages of each structure can be distinguished in order to prepare the stage for the final objective; optimized use of various MOSFET structures in RF circuits.

The characterization follows a classical approach, starting by standard dc figures of merit and moving to analog characterization. This is followed by a high frequency or RF characterization, based on measured S-parameters and the extraction of the parameters of a standard small-signal equivalent circuit. The conventional RF figures of merit are also extracted from measured data.

In order to provide a *real-life* practical information about the different device structures considered here, a high temperature characterization, based on measured data, is provided at each step of the characterization flow. The high temperature behavior of MOSFET structures is becoming a daily-basis problem. The increasing number of transistors per chip and the increasing speed of operation contribute to an increasing operation temperature for almost every available consumer application at the current time. This fact is true for bulk MOSFET devices, and is more pronounced in SOI MOSFET devices due to the

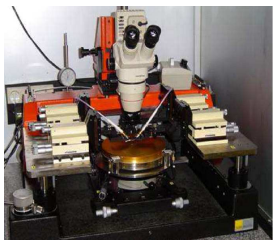
presence of the buried oxide with its poor thermal conductivity. In normal operation conditions, devices could operate at temperatures up to 80^oC. In addition, the high temperature applications is becoming a large value market. Automotive electronics, on-engine and on-transmission applications, wheel-mounted applications, aerospace and environmental monitoring (e.g. mining and well logging), ... are all examples of industrial sectors that have been difficult to serve up till now.

Silicon-on-Insulator (SOI) technology is emerging as the most mature solution for high temperature applications in MOS technology area. Indeed, SOI MOSFETs present lower leakage currents than bulk devices at high temperature, as well as a smaller variation of threshold voltage with temperature [1]. They are also immune to temperature-induced latchup. As a result, SOI circuits can operate at temperatures above 300^oC, while bulk CMOS is usually limited to 150^oC [2, 3]. In previous published work [1, 4], high temperature dc behavior has been considered, while RF high temperature behavior has rarely been discussed [5].

3.1 MEASUREMENT SETUP

All measurements presented in this chapter are acquired using on-wafer measurements. A Suss probe-station PM8® along with a temperature controlled chuck are employed (see Fig. 3.1a). A HP 4145® semiconductor parameter analyzer (see Fig. 3.1b) is used for dc bias and dc measurements. An Anritsu 37369A® Vector Network Analyzer (VNA) (see Fig. 3.1c) is used to acquire the small-signal S-parameters in a 40-MHz–40-GHz frequency range. All RF measurements are performed with a source power of -7 dBm.

Generally, characterization of semiconductor devices could be achieved through packaged chips or using On-wafer probing. In packaged chip measure-



(a) Suss Probe station PM8® with high temperature chuck

(b) HP 4145®

(c) Anritsu 37369A®

Fig. 3.1.: The measurement setup used for dc and RF characterization.

ments the test chip is inserted into a ZIF[1] socket on a PCB having external connectors. On the other hand, the On-wafer probing involves designing the test chip with separate pads near each device. On-wafer probing is much more difficult and requires very high level of care in order to avoid damaging the device or the probes. However, despite the difficulties of on-wafer measurements, characterization of deep sub-micron devices using packaged chips has become obsolete. This is because as the technology shrinks down, the parasitics (introduced by the package pins, wire bonds and interconnects) become much larger compared to that associated with the device itself. For this reasons, on-wafer probing is more suitable for the characterization of deep sub-micron devices, especially when RF measurements are concerned.

RF on-wafer probes must have special electrical characteristic like a wide bandwidth and a low contact resistance as well as special mechanical characteristics like consistent probe shape and durability. It must also be optimized for loss, impedance match, power and current handling capabilities, contact force, and tip visibility.

For on-wafer measurements, at room temperature, the Infinity probe® [8] is used whereas for high temperature measurements the |Z| probe® [9] is used (see Fig. 3.2). Both probes are used with a 100–μm pitch except for the case of PD GCMOS devices which required a 150–μm pitch probes.

A good grounding is essential to achieve reliable measurements. The probes used feature a Ground-Signal-Ground (GSG) configuration as shown in Fig. 3.3. Two grounds are used to provide a good shield for the signal and minimize the cross talk between the signal tip and other conductors. This also minimizes the ground inductance since they are in parallel. Another important feature is that the two halves of the DUT are exposed to the same conditions.

(a) Infinity probe®

(b)|Z| probe®

Fig. 3.2.: The probes used in dc and RF measurements at room and high temperatures (Courtesy of Cascade Microtech, Inc.® [7]).

[1]ZIF is an acronym for *zero insertion force*, a concept used in the design of IC sockets, invented to avoid problems caused by applying force upon insertion and extraction of the IC in the socket. A normal integrated circuit (IC) socket requires the IC to be pushed into sprung contacts which then grip by friction. For an IC with hundreds of pins, the total insertion force can be very large (tens of newtons), leading to a danger of damage to the device or the PCB. With a ZIF socket, before the IC is inserted, a lever or slider on the side of the socket is moved, pushing all the sprung contacts apart so that the IC can be inserted with very little force (generally the weight of the IC itself is sufficient with no external downward force required). The lever is then moved back, allowing the contacts to close and grip the pins of the IC [6].

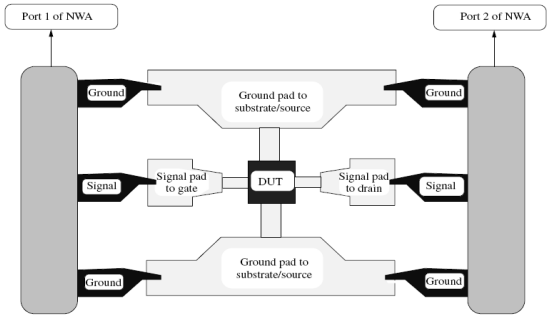


Fig. 3.3.: Illustration of the ground-signal-ground technique used in RF measurements of a two-port system.

3.1.1 Calibration

The perfect measurement instrument does not exist. Therefore, a calibration step is crucial. The different calibration techniques are intended to overcome the effect of errors that are repeatable and predictable over time and temperature, and hence can be removed. Other types of errors that cannot be removed also exist, they are neither repeatable nor predictable. Fortunately, these later errors do not alter the accuracy of measurements to a big extent. In general, three types of errors exist [10]:

- Systematic errors.
- Random errors.
- Drift errors.

Systematic errors, as defined by Agilent Technologies [10], are caused by imperfections in the test equipment and test setup. If these errors do not vary over time, they can be characterized through calibration and mathematically removed during the measurement process. Systematic errors encountered in network measurements are related to signal leakage, signal reflections, and frequency response. There are six types of systematic errors (see Fig. 3.4):

- Directivity and crosstalk errors related to signal leakage.
- Source and load impedance mismatches related to reflections.
- Frequency response errors caused by reflection and transmission tracking within the test receivers.

(The full two-port error model includes all six of these terms for the forward direction and the same six (with different data) in the reverse direction, for a total of twelve error terms. This is why two-port calibration is often referred to as twelve-term error correction.)

Random errors vary randomly as a function of time. Since they are not predictable, they cannot be removed by calibration. The main contributors to random errors are instrument noise (e.g. sampler noise and the IF noise floor), switch repeatability, and connector repeatability. When using network analyzers, noise errors can often be reduced by increasing the source power, narrowing the IF bandwidth, or by using trace averaging over multiple sweeps.

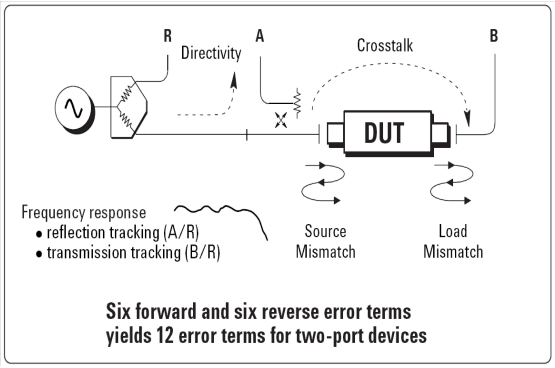
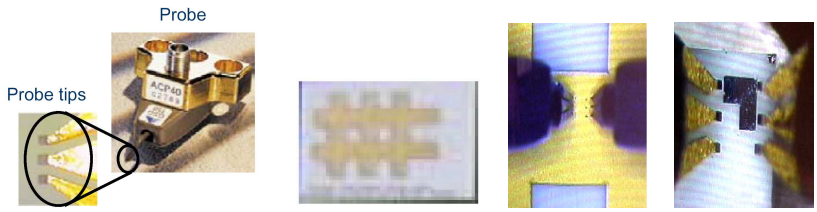


Fig. 3.4.: Systematic measurement errors (source: Agilent Technologies [10]).

Drift errors occur when a test system's performance changes after a calibration has been performed. They are primarily caused by temperature variation and can be removed by additional calibration. The rate of drift determines how frequently additional calibrations are needed. However, by constructing a test environment with stable ambient temperature, drift errors can usually be minimized. While a test equipment may be specified to operate over a temperature range of 0^oC to $+55^oC$, a more controlled temperature range such as $+25^oC$ $\pm 5^oC$ can improve measurement accuracy (and reduce or eliminate the need for periodic calibration) by minimizing drift errors.

Typically, before starting an on-wafer calibration procedure two steps should be performed, the planarity adjustment and the alignment. The first assures that the three tips of the probes (see Fig. 3.5a) are on the same horizontal plane and is achieved using a contact substrate (see Fig. 3.5b). If three identical scratches are produced by a simple contact, then the planarity is achieved (see Fig. 3.5c). The second is simpler and it consists of adjusting the two probes exactly face to face (see Fig. 3.5d).



(a) Illustration of the probe tips.

(b) A contact substrate.

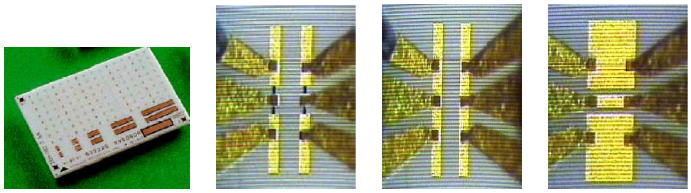
(c) Adjusting planarity.

(d) Aligning probes.

Fig. 3.5.: Pre-calibration steps: Probes planarity and alignment (source: Cascade Microtech, Inc.® [7]).

The system calibration for on-wafer measurements is achieved by using a so-called Impedance Standard Substrate (ISS) (see Fig. 3.6a) that can provide

high-accuracy and low-loss standards for two-port calibration procedures such as short-open-load-through (SOLT), through-reflect-line (TRL), or line-reflect-match (LRM). The later is the method used in this work. In a first step, the load (Match) is measured (see Fig. 3.6b). This also assures the position of the probes (x- and y-coordinates) which should not be changed throughout the rest of the calibration procedure (to avoid variations in cables bending, cross-talk between probes tips, etc). The short and open (Reflect) are then measured using the short on the ISS (see Fig. 3.6c) and an open air measurement. Finally, the through (Line) is measured (see Fig. 3.6d). The standards themselves are defined in a cal-kit definition file, which is stored in the Network Analyzer. After measuring the standard calibration structures, the Network Analyzer calculates and saves the 12 error correction terms which are used later in correcting the measurement readings. If the calibration is successful, an open air measurement on either of the two ports should result in a variation of the magnitude of S_{11} not more than ± 0.1 dBm around 0 dB. In this case, the reference planes could be assumed at the tips of the measurement probes taking into account any effects along the path from the VNA source to the DUT measurement pads and back to the VNA receiver (see Fig. 3.7). To move the reference planes to the edges of the DUT, a de-embedding procedure is needed.



(a) An Impedance Standard Substrate (ISS). (b) Load measurement. (c) Short measurement. (d) Thru measurement.

Fig. 3.6.: Calibration steps (source: Cascade Microtech, Inc.® [7]).

3.1.2 De-Embedding

The de-embedding procedure is used to remove the parasitics related to the test structure including the pads and the connection lines. Special test structures like open and short test structures should be deliberately designed and fabricated on the same chip as the DUT. The open structure should have exactly the same pad structure as the DUT but without the DUT included. The short structure is the same as the open structure but with the pads shorted together. The DUT characteristics can then be obtained by removing the parasitics of these two structures from the original (DUT) structure as illustrated schematically in Fig. 3.8. The exact procedure of the de-embedding using open and short structures is explained in Appendix A.

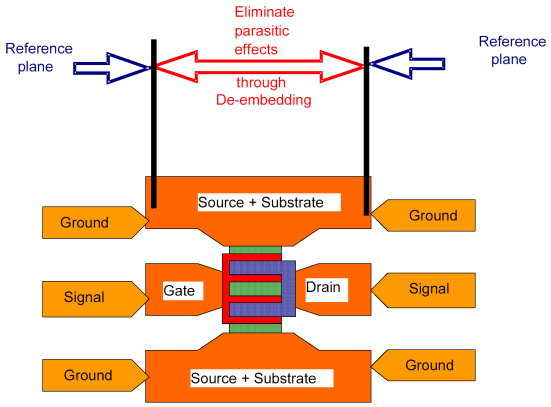


Fig. 3.7.: Reference planes after a successful calibration procedure (Source: Agilent Technologies [11]).

After de-embedding, the reference planes are located at the borders of the DUT, as shown in Fig. 3.9.

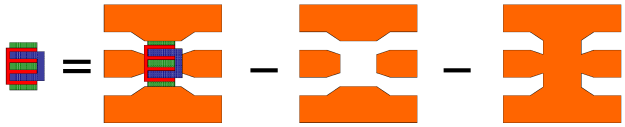


Fig. 3.8.: A schematic illustration of the de-embedding procedure.

3.2 DC CHARACTERIZATION

It is of significant importance to correctly characterize a device in dc before moving to higher frequency ranges. Key figures of merit like V_T, g_m/I_{DS}, $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, I_{Leakage}, g_D, and V_{EA} are presented in this section based on measured data at room and high temperatures.

3.2.1 Threshold Voltage

The definition and the extraction of the threshold voltage have been a subject of disagreement between authors in literature for a long time. It is indeed a challenging bias point, and it becomes more crucial as applications tend to operate near or even below this critical point.

One certain fact about the operation of the MOSFET transistor is the pinch-off condition. Below that point, the channel of the MOSFET operates as a linear

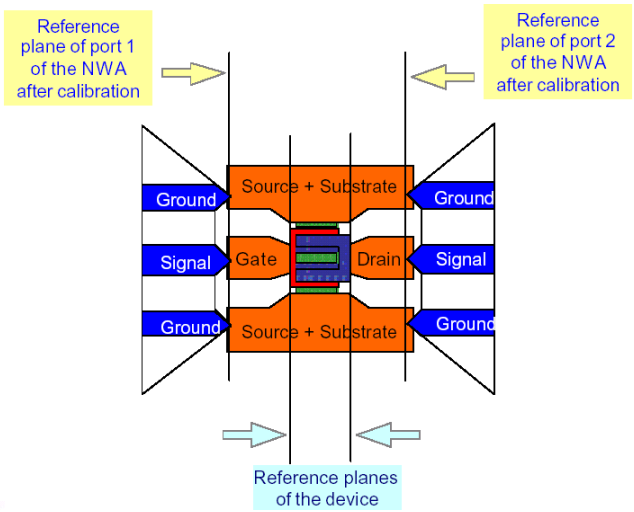


Fig. 3.9.: Reference planes after a successful calibration and de-embedding procedures (Source: Agilent Technologies [11]).

resistor where the current passing from source to drain I_{DS} is directly proportional to the drain bias V_{DS}. The resistance of the channel is modulated through the gate voltage V_{GS}. The interaction between the vertical and horizontal electric fields which result from V_{GS} and V_{DS}, respectively, result in a thinning of the channel near the drain side. At a certain V_{DS} value, for a fixed V_{GS} bias, the channel thickness vanishes, or goes to zero, at the drain side. This is the pinch-off point, or the saturation point, and is marked by $V_{DS,sat}$. As V_{DS} increases, this zero thickness channel point moves away from the drain diffusion region towards the source. Nevertheless, the potential of that point always remains $V_{DS,sat}$. Therefore, the amount of current stimulated by the potential difference $V_{DS,sat}$ is essentially constant. Electrons will then fly through the "*no-channel*" region like they do through the base of a BJT. The channel is no longer a linear resistor where the current is directly proportional to the drain voltage. Hence, two distinct modes of operation are defined for a MOSFET; the linear region and the saturation region, and the border between these two modes is the pinch-off point.

In fact, another border exists, and this one is more difficult to define. It is the border between the OFF and the ON (linear) states of the transistor. The threshold voltage should be the point at which the transistor starts to conduct current, or in other words, the point at which the channel is created, thus the name "threshold". The best way to correctly define this border is to go back to the physics of the MOS transistor.

The threshold voltage of an n-channel MOSFET is given by

$$V_T \cong \Phi_{\mathrm{MS}} + 2\psi_{\mathrm{F}} - \frac{Q_{\mathrm{ox}}}{C_{\mathrm{ox}}} - \frac{Q_{\mathrm{D}}}{C_{\mathrm{ox}}} \tag{3.1}$$

where Φ_{MS}, ψ_{F}, Q_{ox}, Q_{D}, and C_{ox} are the metal-semiconductor work function difference, the Fermi potential, the charge density in the gate oxide, the depletion charge controlled by the gate, and the gate oxide capacitance, respectively.

Equation (3.1) is valid for Partially-Depleted devices where

$$Q_{\mathrm{D}} = qN_A X_{\mathrm{Dmax}} \tag{3.2}$$

where X_{Dmax} is the maximum depletion width and is given by

$$X_{\mathrm{Dmax}} = \sqrt{\frac{4\varepsilon_{\mathrm{Si}}\psi_{\mathrm{F}}}{qN_A}} \tag{3.3}$$

where $\varepsilon_{\mathrm{Si}}$ is the permitivity of the silicon, N_A is the doping concentration, and q is the charge of electron.

If an N^+-polysilicon is assumed, the value of the work-function difference is given by

$$\Phi_{\mathrm{MS}} = -\frac{E_{\mathrm{g}}}{2} - \psi_{\mathrm{F}} \tag{3.4}$$

with

$$\psi_{\mathrm{F}} = \frac{kT}{q}\ln(N_A/n_{\mathrm{i}}) \tag{3.5}$$

where E_{g}, T, and n_{i} are the silicon energy band gap, the temperature, and the silicon intrinsic carrier concentration, respectively.

The temperature dependence of the intrinsic carrier concentration, n_{i}, is given by [12]

$$n_{\mathrm{i}} = 3.9 \times 10^{16} T^{3/2}\ e^{-E_{\mathrm{g}}/2kT} \tag{3.6}$$

The temperature dependence of the threshold voltage can be obtained from (3.1) and (3.5). Q_{ox} is assumed to have no temperature dependence over the temperature range under consideration (25–250^{o}C). The same applies to E_{g}, which varies by only 0.3% for this temperature range [13, p. 56]. Therefore, for bulk and thick-film SOI devices [14],

$$\frac{\mathrm{d}V_T}{\mathrm{d}T} = \frac{\mathrm{d}\psi_{\mathrm{F}}}{\mathrm{d}T}\left[1 + \frac{q}{C_{\mathrm{ox}}}\sqrt{\frac{\varepsilon_{\mathrm{Si}}N_A}{kT\ln(N_A/n_{\mathrm{i}})}}\right] \tag{3.7}$$

with

$$\frac{\mathrm{d}\psi_{\mathrm{F}}}{\mathrm{d}T} = 8.63 \times 10^{-5}\left[\ln(N_A) - 38.2 - \frac{3}{2}\left\{1 + \ln(T)\right\}\right] \tag{3.8}$$

In the case of thin-film Fully-Depleted (FD) devices, Q_{D} has a value which can range between $qN_A t_{\mathrm{Si}}$ and $qN_A t_{\mathrm{Si}}/n$, with t_{Si} the silicon film thickness,

which is independent of temperature, and the value of n ranges between 1 and 2, depending on the oxide charge and the back-gate bias conditions. If n is assumed independent of temperature, therefore Q_{D} is independent of temperature. And since Q_{ox} and E_{g} were assumed independent of temperature too, therefore, from (3.1)

$$\frac{\mathrm{d}V_T}{\mathrm{d}T} = \frac{\mathrm{d}\Phi}{\mathrm{d}T} \tag{3.9}$$

From (3.7) and (3.9), it can be seen that $\mathrm{d}V_T/\mathrm{d}T$ is larger in bulk and thick-film SOI devices than in thin-film SOI devices by a ratio given by the bracket term of (3.7) which typically ranges from 2 to 3, depending on the gate oxide thickness and the channel doping concentration. In other words, it depends on C_{D} and C_{ox}, depletion capacitance and oxide capacitance, per unit area, respectively. Typical values of $\mathrm{d}V_T/\mathrm{d}T$ range between -0.7 and -0.8 mV/^{o}C in thin-film SOI MOSFET's and between -2.4 and -3 mV/^{o}C in bulk and thick-film SOI MOSFET's (with N_A of $\sim 1.6 \times 10^{17}$ cm^{-3}) depending on oxide thickness and temperature range [14].

In this work, V_T is extracted from the I_{DS}-V_{GS} curves measured in the linear region ($V_{\mathrm{DS}} = 50$ mV) using the second derivative method. The second derivative of the drain current with respect to gate voltage is calculated ($\mathrm{d}^2 I_{\mathrm{DS}}/\mathrm{d}V_{\mathrm{GS}}^2 = \mathrm{d}g_m/\mathrm{d}V_{\mathrm{GS}}$). The maximum of the second derivative is then found and the corresponding V_{GS} is taken as V_T (see Fig. 3.10).

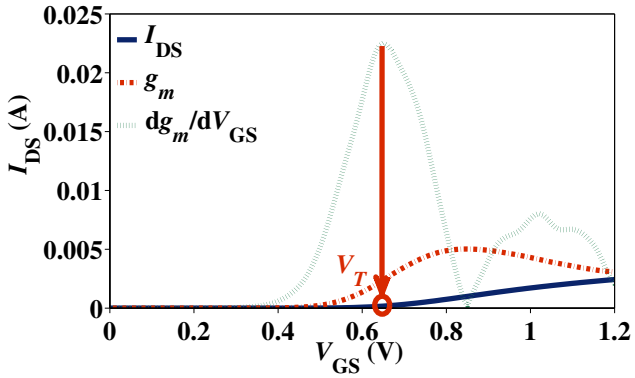
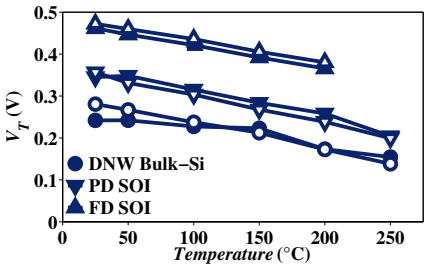
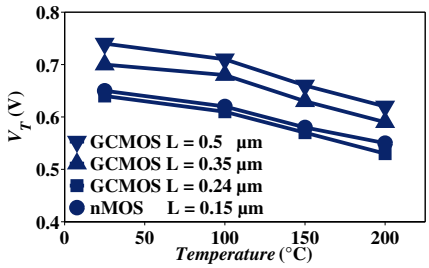


Fig. 3.10.: Illustration of the second derivative extraction method of V_T.

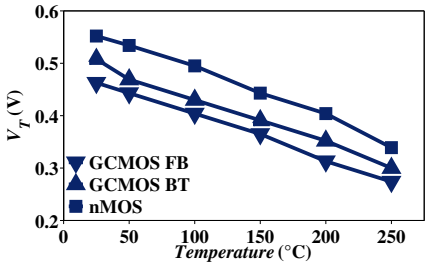
The extracted V_T as a function of temperature is shown in Fig. 3.11. The devices used in this work show different values of V_T at room temperature. This certainly affects the different characteristics of the device like the OFF current, which might result in an unfair comparison between the devices. Differences in V_T are taken into account throughout by comparing figures of merit at the same normalized drain current or for the same gate over drive voltage ($V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_T$). In this section, the temperature dependence of V_T is compared for all the devices.



(a) DNW bulk, PD and FD SOI in FB (solid symbols) and BT (empty symbols) structures.



(b) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(c) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.11.: Variation of V_T with temperature for different devices.

In Fig. 3.11a, the variation of V_T with temperature for the classical devices is presented. All device have relatively the same tendency with temperature. The only exception is noticed for the FB DNW bulk, which shows an interesting stability of V_T up to 150^{o}C before degradation takes place. This same behavior is also noticed for FB PD SOI but only up to 50^{o}C. A summary of the variation of V_T with temperature is presented in Table 3.1. FB DNW bulk device shows the lowest variation (calculated from a linear regression over the whole range of temperatures, in order to take into account the quasi-stable behavior below 150^{o}C). However, if both structures are to be considered, i.e. FB and BT structures, the FD SOI presents the lowest variation with temperature for both FB and BT structures. The better performance of FD SOI is expected [14], whereas the DNW bulk shows an interesting enhancement compared to classical bulk devices which ranges between -2.4 and -3 mV/^{o}C as mentioned earlier.

The V_T variation with temperature for FD GCMOS devices is shown in Fig. 3.11b. For comparison reasons, a classical FD nMOS fabricated on the same die is shown on the same figure. The presence of the lightly-doped region does not affect the V_T variation with temperature. Except for very high temperature (200^{o}C), GCMOS of 0.24 μm channel length shows very close variation of V_T with temperature as the classical nMOS of 0.15 μm channel length.

Based on the summary of Table 3.1, if one would choose a device for its stability in V_T with temperature, the choice would be a DNW bulk FB device followed by a DT device (either DNW bulk or PD SOI) and on the same footings the BT FD SOI device.

Table 3.1.: Threshold voltage V_T at room temperature and its variation with temperature expressed in mV/^{o}C. The variation is calculated from a linear regression taken over the whole range of temperature.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
V_T (V)	0.24	0.28	0.26	0.35	0.36	0.34	0.46	0.47
ΔV_T	−0.4	−0.63	−0.54	−0.63	−0.68	−0.54	−0.55	−0.53

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
V_T (V)	0.65	0.64	0.7	0.74	0.55	0.46	0.51
ΔV_T	−0.58	−0.63	−0.64	−0.7	−0.93	−0.85	−0.87

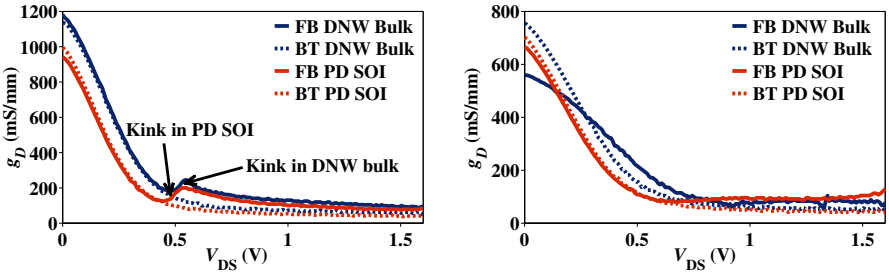
3.2.2 Current-Voltage Characteristics

The current-voltage I_{DS}-V_{GS} characteristics is an essential way to study a transistor since it is mainly a "transfer resistor". There are so many text books and articles published to describe and model the I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of a transistor, either in bulk, PD SOI, or FD SOI and many other variations of transistor structures. More details and references to other resources can be found in [2, 12, 13, 15, 16]. This section is then only devoted to describing the characteristics of the devices considered in this work.

3.2.2.1 DNW Bulk and PD SOI

It is very interesting to see that adding a deep n-well protection to a bulk device results in mimicking many of the SOI characteristics, be it advantages or disadvantages. The floating-body effects FBE including the kink effect are introduced to the DNW bulk devices which can be useful in some cases since it results in an increased drive current. As in PD SOI, the kink effect is suppressed from the DNW bulk device by using a body-tied structure and also by increasing the tem-

perature. This can be easily seen from Fig. 3.12, where the output conductance is presented for FB and BT DNW Bulk and PD SOI devices at room temperature (Fig. 3.12a) and at 250^{o}C (Fig. 3.12b).



(a) T = 25^{o}C (b) T = 250^{o}C

Fig. 3.12.: Output conductance g_D for FB and BT structures of DNW bulk and PD SOI devices at $V_{\mathrm{GS}} = 0.8$ V.

The suppression of the kink effect at high temperatures is better illustrated in Fig. 3.13. This feature promotes FB transistors to work at harsh environments without problems arising from floating body effects. Several factors can explain this improved performance for FB transistor. First, this can be due to the enhanced generation processes at high temperatures which leads to a more efficient extraction of the excess carrier from the floating body. Also due to the attenuation of the impact ionization up to total disappearance at high temperatures (due to the decrease of the carrier mean free path) which also leads to the increase of Early voltage at elevated temperatures [17]. It can also be related to the reduction of the excess minority carrier concentration in the device body through increased recombination. And also, the reduction of the body potential variations owing to an increase of the saturation current of the source junction [2].

It is worth noticing that these figures of g_D are calculated from dc measurements using

$$g_D = \left.\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{DS}}}\right|_{V_{\mathrm{GS}}} \tag{3.10}$$

3.2.2.2 PD SOI and FD SOI

As mentioned earlier (see section 2.3), FD SOI devices have the advantage of the suppression of FBE. Fig. 3.14 shows the suppression of the hump in the g_D characteristics of FB FD devices as compared to FB PD devices. In FD devices, there is practically no difference between FB and BT output conductance characteristics. For the PD device, except for the region where the kink effect is manifested, both FB and BT structures show close values of g_D. Overall, PD devices show higher values of g_D than FD devices.

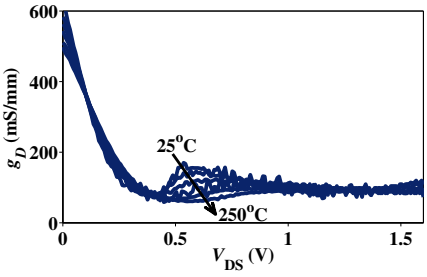
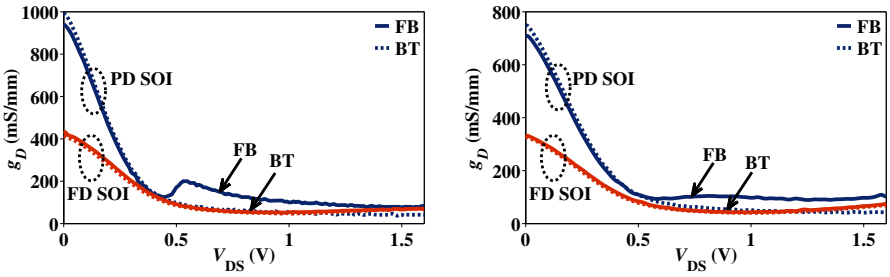


Fig. 3.13.: Illustration of the suppression of the kink effect at higher temperatures using a PD SOI FB device at $V_{GS} = 0.6$ V.



(a) T = 25^{o}C (b) T = 200^{o}C

Fig. 3.14.: Output conductance g_D for FB and BT structures of PD and FD SOI devices at $V_{GS} = 0.8$ V.

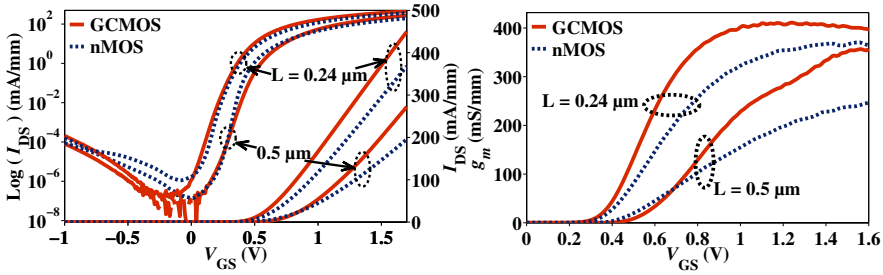
3.2.2.3 *GCMOS and classical nMOS*

The lightly doped region of the channel in the GCMOS device is naturally inverted at zero gate bias; hence it acts as an extension to the drain beneath the gate till the border of the highly doped region when the device is in saturation. This feature results in a shorter effective channel length than the drawn one, thus explaining the better dc and analog performances of the GCMOS device in comparison to the classical MOS device of the same drawn channel length. Fig. 3.15 shows the advantages[2] of FD GCMOS as compared to FD classical nMOS such as higher drive current, higher transconductance, and steeper subthreshold slope.

The same advantages are noticed for PD GCMOS devices (either in FB or in BT) structures as shown in Fig. 3.16 and Fig. 3.17. It is also quite interesting to notice how a 0.5 μm channel length GCMOS can compete with a 0.35 μm channel length classical nMOS, which is one node ahead as shown in Fig. 3.18. Under certain bias conditions, the 0.5 μm GCMOS can even compete with a 0.25

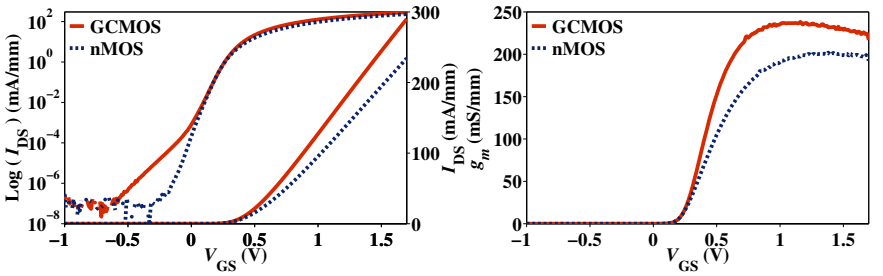
[2]The data for these devices are delivered by the fabricator. The devices themselves are not available for characterization. This is why they do not appear in high temperature or RF comparisons.

μm classical nMOS. This is in consistent with what was published for GCMOS of longer channel lengths, where the GCMOS of drawn channel length L cannot usually outperform a classical nMOS of channel length $L/2$ (provided that $L_{\mathrm{LD}}/L = 0.5$) [18].



(a) I_{DS}-V_{GS} (b) g_m-V_{GS}

Fig. 3.15.: Transfer characteristics and transconductance of FD GCMOS and FD classical nMOS of 0.5 and 0.24 μm channel lengths at $V_{\mathrm{DS}} = 1.7$ V.

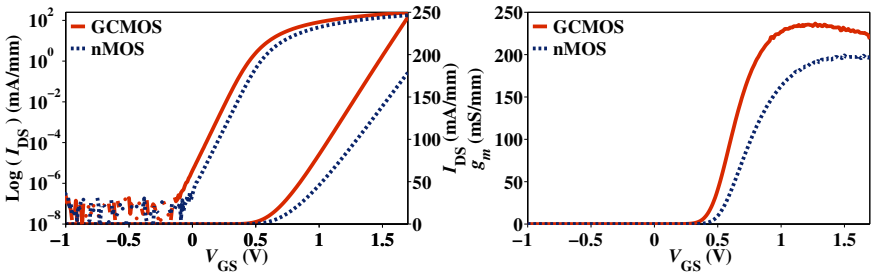


(a) I_{DS}-V_{GS} (b) g_m-V_{GS}

Fig. 3.16.: Transfer characteristics and transconductance of of FB PD GCMOS and PD classical nMOS of 0.5 μm channel lengths at $V_{\mathrm{DS}} = 1.7$ V.

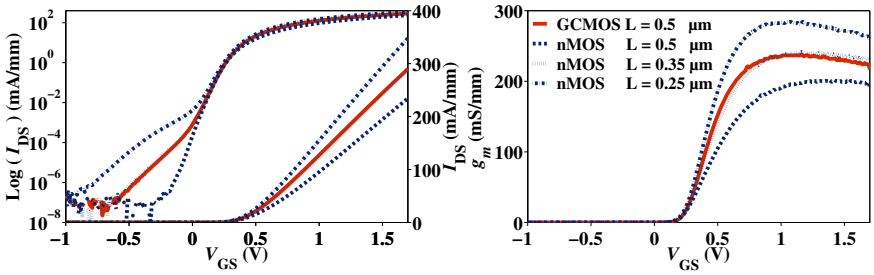
3.2.3 Maximum Transconductance

The maximum transconductance of a transistor is an indication of how fast the transistor can perform. Even though extracted from dc measurements, which suffers from some self-heating effects, it is a good measure to predict the behavior of the current gain cutoff frequency. Later in this chapter, the maximum of transconductance based on RF measurements is presented, and at that point, it is of interest to compare the two behaviors (from dc and from RF measurements) and evaluate how much a device suffer from self-heating effects. The behavior of maximum transconductance with temperature is also of great interest because it has its direct impact on the temperature behavior of cutoff frequencies.



(a) I_{DS}-V_{GS} (b) g_m-V_{GS}

Fig. 3.17.: Transfer characteristics and transconductance of BT PD GCMOS and PD classical nMOS of 0.5 μm channel lengths at $V_{DS} = 1.7$ V.

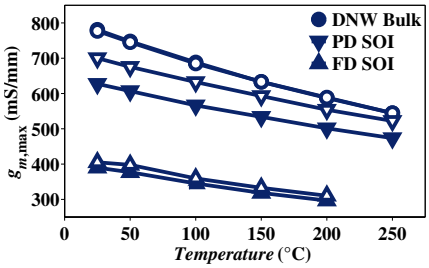


(a) I_{DS}-V_{GS} (b) g_m-V_{GS}

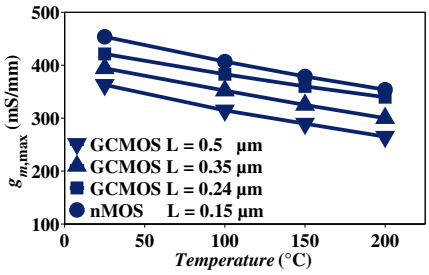
Fig. 3.18.: Transfer characteristics and transconductance of BT PD GCMOS of 0.5 μm and PD classical nMOS of 0.5, 0.35 and 0.25 μm channel lengths at $V_{DS} = 1.7$ V (Legend in (b) is also valid for (a)).

The maximum g_m behavior with temperature of the devices of this work in saturation condition ($V_{DS} = V_{DD}$) is shown in Fig. 3.19 and the values and the variation with temperature are summarized in Table 3.2. In general, a BT structure shows a better $g_{m,max}$ than a FB structure but a lower stability with temperature. This is true for all devices except for the DNW bulk devices where both structures show nearly the same behavior and the PD GCMOS where the FB shows much better behavior than the BT structure but less stability with temperature.

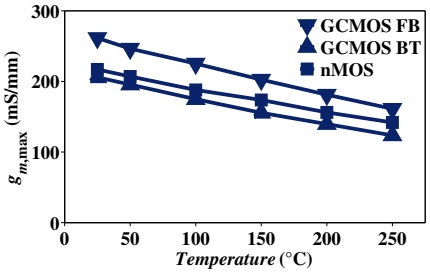
Although the FD GCMOS of 0.24 μm channel length has double the value of the drawn channel length of the classical nMOS of 0.15 μm, it can still compete with it as far as the absolute values of $g_{m,max}$ are considered. When considering the stability with temperature, the GCMOS device outperforms the classical nMOS device. The contrary is true when considering the PD GCMOS structure, GCMOS device has higher absolute value of $g_{m,max}$ while having less stability with temperature when compared to the classical nMOS.



(a) DNW bulk, PD, and FD SOI in FB (solid symbols) and BT (empty symbols) structures.



(b) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(c) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.19.: Variation of $g_{m,\max}$ with temperature for different devices.

3.2.4 Subthreshold Slope

In digital circuits, the speed of switching from ON state to OFF state and vice versa is a critical figure of merit. In order to quantify this figure of merit, it is sufficient to look at the drain current in the sub-threshold region. If the subthreshold current is plotted against the gate voltage on a logarithmic scale, it will appear like a straight line going from the ON current value to the OFF current plateau. The speed (by definition) of this transition is calculated by taking the slope of this straight line. It is more significant for a digital circuit designer to represent this speed in terms of how many volts (or milli-volts) of gate bias it takes to switch the transistor OFF or turn it ON. Hence, instead of taking the differential $\mathrm{d}I_{\mathrm{DS}}/\mathrm{d}V_{\mathrm{GS}}$, we take $\mathrm{d}V_{\mathrm{GS}}/\mathrm{d}I_{\mathrm{DS}}$ or since we are working in a logarithmic scale environment, it is $\mathrm{d}V_{\mathrm{GS}}/\mathrm{d}\log(I_{\mathrm{DS}})$. Hence, the name "inverse subthreshold slope" or "subthreshold swing". For simplicity, it is refered to as "subthreshold slope", and given by:

$$S = \frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}\log(I_{\mathrm{DS}})} \tag{3.11}$$

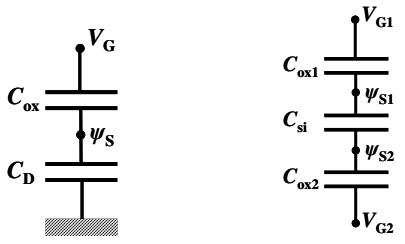
Table 3.2.: Maximum transconductance $g_{m,\max}$ (at room temperature) and its variation with temperature expressed in mS/mm/^{o}C. The variation is calculated from a linear regression taken over the whole range of temperature.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
$g_{m,\max}$ (mS/mm)	780.8	777.1	—	627.3	700.2	—	390	405.1
$\Delta g_{m,\max}$	−1.05	−1.03	—	−0.68	−0.79	—	−0.54	−0.57

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
$g_{m,\max}$ (mS/mm)	453.8	421.3	394.2	362.9	217	261.6	205.8
$\Delta g_{m,\max}$	−0.57	−0.47	−0.54	−0.56	−0.33	−0.44	−0.37

A detailed derivation of the subthreshold slope expression is presented in [2] for the case of bulk, PD SOI, and FD SOI. In essence, after a simple approximation, S is generally expressed by:

$$S = \frac{kT}{q} \ln(10) \frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}\psi_{\mathrm{S}}} \tag{3.12}$$



(a) Bulk and PD SOI (b) FD SOI

Fig. 3.20.: Equivalent capacitance network [2].

Normally, for bulk and PD SOI transistors (if the interface traps are neglected and thus the associated capacitance $C_{\mathrm{it}} = 0$), the variation of the surface potential with the applied gate bias is controlled by the simple capacitance network

shown in Fig. 3.20a. Therefore the subthreshold slope is given by [19, 20]:

$$S = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{\mathrm{D}}}{C_{\mathrm{ox}}}\right) \tag{3.13}$$

$$C_{\mathrm{D}} = \frac{\mathrm{d}Q_{\mathrm{D}}}{\mathrm{d}\psi_{\mathrm{S}}} \tag{3.14}$$

$$Q_{\mathrm{D}} = qN_A X_{\mathrm{Dmax}} \tag{3.15}$$

where ψ_{S} is the surface potential at the $\mathrm{Si}-\mathrm{SiO}_2$ interface.

In a FD SOI, the capacitance network is more complicated as the back-gate capacitance should be taken into account (see Fig. 3.20b). Nevertheless, this results in a much simplified expression of $\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}\psi_{\mathrm{S}}}$:

$$\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}\psi_{\mathrm{S}}} = 1 + \frac{1}{C_{\mathrm{ox1}}}\left(\frac{C_{\mathrm{si}}C_{\mathrm{ox2}}}{C_{\mathrm{si}} + C_{\mathrm{ox2}}}\right) \tag{3.16}$$

And since in FD SOI, $C_{\mathrm{ox2}} << C_{\mathrm{ox1}}$ and $C_{\mathrm{ox2}} << C_{\mathrm{si}}$, $\mathrm{d}V_{\mathrm{GS}}/\mathrm{d}\psi_{\mathrm{S}}$ tends to unity, and therefore

$$S = \frac{kT}{q}\ln(10) \tag{3.17}$$

This is the theoretical minimum limit of S, i.e. 60 mV/dec. FD SOI devices are usually very close to this limit (slightly higher). If a device features a $S = 60$ mV/dec it means that it only needs 60 mV variation in V_{GS} to decrease the drain current by one decade (or 10 times). It also indicates a perfect coupling between the gate bias V_{GS} and the surface potential ψ_{S} [2, p. 196]. It is important to notice that, as explained in section 2.5, FB devices could feature some anomalous subthreshold behavior forcing S to be lower than the theoretical minimum limit.

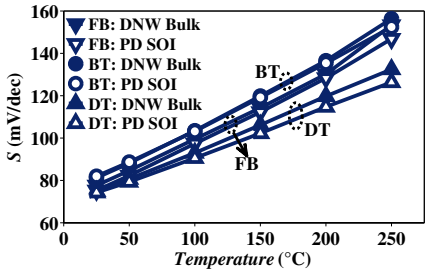
From (3.14) and (3.15), as X_{Dmax} varies with temperature, C_{D} depends on temperature as well and so does the subthreshold slope. This variation was traditionally considered nonlinear for bulk and thick film SOI devices and linear for thin film SOI devices based on the depletion approximation and a charge-sheet model. However, Rudenko *et al.* showed in 2000 that the increase of free carriers charge densities with temperature results in an increased substrate effective capacitance and hence proposed a corrected model in which the variation of subthreshold slope is basically nonlinear for thin-film SOI devices with temperature [19]. Rudenko introduced a correction factor n that takes into account the effect of the lowering of the surface electric field with temperature and he replaced C_{D} by C_{stot}; the total surface differential capacitance, which includes the contribution from the free carriers and is higher than the depletion capacitance C_{D}. Rudenko *et al.* suggested that the classical model should be valid up to 150^{o}C before it fails and that the thin film device should follow a nonlinear behavior according to:

$$S = \frac{nkT}{q}\ln(10)\left(1 + \frac{C_{\mathrm{stot}}}{C_{\mathrm{ox}}}\right) \tag{3.18}$$

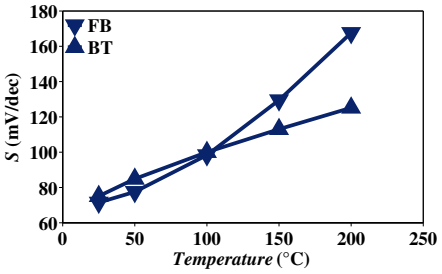
However, the experimental results presented in Fig. 3.21 shows a clear linear behavior for all the devices except the FB FD Device up to 250^{o}C. Fig. 3.21a shows that (as expected from theory) the DNW bulk devices and the PD SOI devices show identical variation with temperature and quite close values of S (with the exception of the DT structure for which the PD SOI device is slightly better than the DNW bulk device). DT structure shows the best values of S followed by the FB structure. The same applies to the variation with temperature, where DT structures show the lowest variation of S with temperature.

From Fig. 3.21b, it is clear that the FB structure of the FD SOI device starts to show the nonlinear behavior at 100^{o}C, even earlier than expected by Rudenko. However, this effect is eliminated when the body is tied to the source as shown for the BT structure.

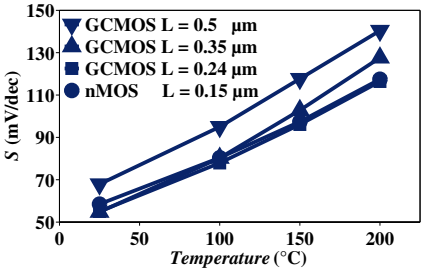
Fig. 3.21c shows that GCMOS devices suffer (although it is beneficial) from the anomalous subthreshold characteristics giving rise to values of S at room temperature less than the theoretical minimum limit. It can also be seen that they do not offer an advantageous stability of S with temperature compared to other devices as summarized in Table 3.3. The GCMOS device of 0.24 μm channel length shows very similar behavior of S as the classical nMOS of $L = 0.15$ μm.



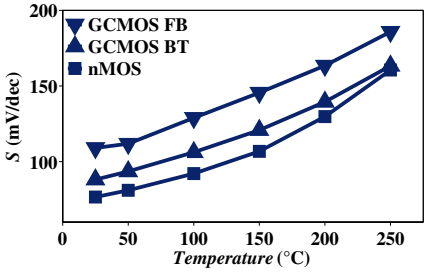
(a) DNW bulk and PD SOI in FB, BT, and DT structures.



(b) FD SOI in FB and BT structures.



(c) FD GCMOS with 48 fingers and FD classical nMOS with 32 fingers of 2.5 μm width each and different channel lengths.



(d) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.21.: Variation of subthreshold slope S with temperature for different devices.

Table 3.3.: Subthreshold slope S at room temperature (in saturation region; $V_{DS} = V_{DD}$) and its variation with temperature expressed in % per ^{o}C. The variation is calculated from a linear regression taken over the whole range of temperature.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
S (mV/dec)	77.6	81.2	75	75.3	82	74.3	71.5	75.1
ΔS	0.33	0.33	0.26	0.32	0.31	0.23	0.55	0.28

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
S (mV/dec)	58.5	55	54.8	67.9	76.58	109	88.11
ΔS	0.33	0.35	0.42	0.42	0.36	0.34	0.33

3.2.5 I_{ON}-to-I_{OFF} Ratio

This figure of merit is very important for digital circuit designers. It is well known that SOI devices provide much higher I_{ON}-to-I_{OFF} ratio than bulk devices, and this is related to the much smaller area of source and drain junctions in SOI compared to bulk (by a factor of 15 to 100, depending on the design rules) [2], and more important, the largest of all junctions, the well junctions, are totally absent from SOI CMOS. This contributes to a drastic reduction in the overall standby current consumption of SOI circuits compared to bulk ones.

In highly-doped devices, the evaluation of the I_{ON}-to-I_{OFF} ratio with temperature is determined by the variations with temperature of threshold voltage, subthreshold slope, and OFF current. On the other hand, in lightly-doped devices, it is dependent on threshold voltage and subthreshold variations only. Usually, we can expect to have stronger temperature dependence of the I_{ON}-to-I_{OFF} ratio in devices with higher threshold voltages.

The measured I_{ON}-to-I_{OFF} ratio and I_{OFF} are shown in Fig. 3.22. Measurements of I_{OFF} are taken at $V_{GS} = 0$ V and of I_{ON} at $V_{GS} = V_{DD}$ with $V_{DS} = V_{DD}$ in both cases. As expected, BT structures show better I_{ON}-to-I_{OFF} ratio, due to its lower OFF current. It should also be noticed that the I_{ON}-to-I_{OFF} ratio of BT structures degrades faster with temperature. This is related to a higher degradation scheme of the OFF current for BT structures. The relatively large difference

between OFF currents for FB and BT structures at room temperature (about one decade) tends to diminish at 250^{o}C, which explains the tendency to have close values of I_{ON}-to-I_{OFF} ratios for FB and BT structures at 250^{o}C. Values and variations with temperature are summarized in Table 3.4

3.2.6 Leakage Current

The increase of junction leakage current is one of the main causes of failure in circuits operating at high temperature. The junction leakage current is proportional to the area of the junction. The strongest leakage component found in bulk CMOS operating at high temperatures originates from the "huge" well junctions. This causes loss of functionality in bulk CMOS circuits at temperature above 180^{o}C while the same SOI CMOS circuits can operate up to 300^{o}C [2].

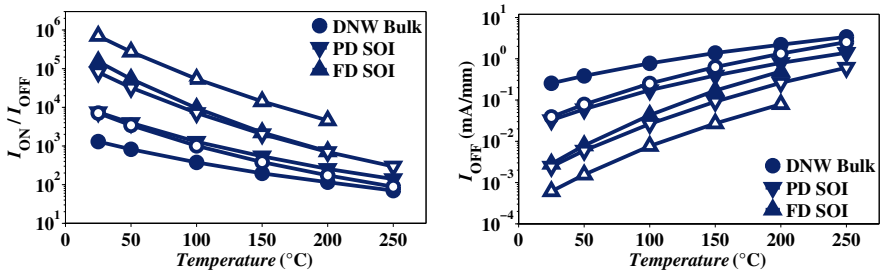
The leakage current in SOI MOSFET transistors is basically composed of two parts, a generation component and a diffusion component, both related to the N^+-P junction (body-drain junction). The sum of these two components describes the leakage current as follows [2]

$$I_{\text{Leakage}} = qA\left(\frac{D_{\text{n}}}{\tau_{\text{n}}}\right)^{1/2}\frac{n_{\text{i}}^2}{N_A} + qA\frac{n_{\text{i}}X_{\text{D}}}{\tau_{\text{e}}} \tag{3.19}$$

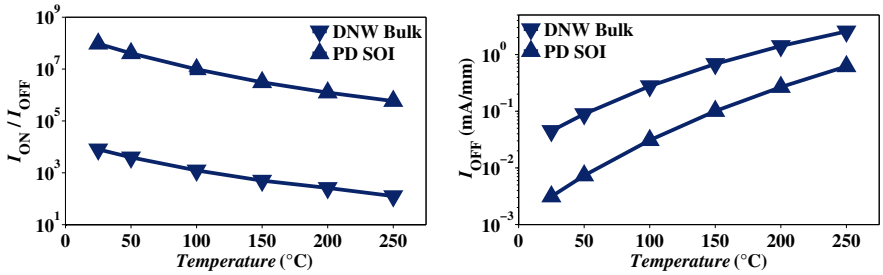
where A is the junction area, D_{n} is the electron diffusion coefficient, τ_{n} is the electron lifetime in p-type neutral silicon, X_{D} is the depletion width, and $\tau_{\text{e}} = (\tau_{\text{n}} + \tau_{\text{p}})/2$ is the effective lifetime related to the thermal generation process in the depletion region. The temperature dependence of the leakage current is based on the temperature dependence of n_{i} which is given in (3.6).

The first term in (3.19) (the diffusion component) is proportional to n_{i}^2, and the second term (the generation component) is proportional to n_{i}. It has been experimentally observed [21] that the leakage current of SOI MOSFETs and reverse-biased diodes varies as n_{i} below a temperature of 100–150^{o}C and varies as n_{i}^2 above those temperatures, which implies that the diffusion component is more effective at higher temperatures while at lower temperatures it is the generation component which is more effective. It is also worth noticing that A, the area of the junction, and $A \cdot W$, the volume of the space-charge region associated with the diode, are both much smaller in SOI transistors than in bulk devices. Therefore, extremely low leakage current can be obtained in SOI devices.

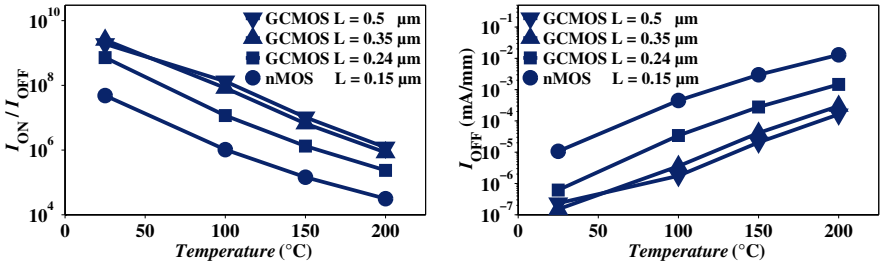
In FB transistors, this diffusion component becomes more important due to the presence of the floating charge reservoir in the body. And as the temperature increases, this reservoir becomes more and more important with charges thermally generated and accumulated inside it, hence the diffusion component is highly magnified. On the other hand, in BT transistors, the connection between the body and the source limits the diffusion component as no accumulation of charges takes place in the body.



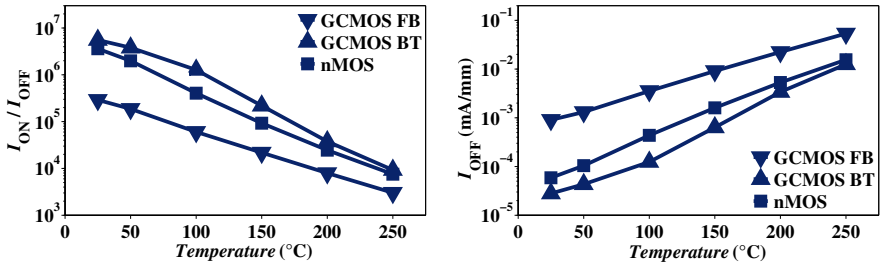
(a) DNW bulk, PD, and FD SOI in FB (solid) and BT (empty) structures.



(b) DNW bulk and PD SOI in DT structure.



(c) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(d) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.22.: Variation of I_{ON}-to-I_{OFF} ratio and I_{OFF} with temperature for different devices.

Table 3.4.: I_{ON}-to-I_{OFF} ratio and I_{OFF} at room temperature and their variation with temperature expressed in decade per ^{o}C. The variation is calculated from a linear regression taken over the whole range of temperature.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
I_{ON}/I_{OFF} ($\times 10^{6}$)	0.0013	0.0071	0.08	0.0075	0.081	95	0.15	0.7
I_{OFF} (mA/mm) ($\times 10^{-6}$)	250000	39000	45000	33000	2400	3100	2800	610
Δ I_{ON}/I_{OFF} ($\times 10^{-3}$)	-5.6	-8.5	-8	-7.7	-10.8	-9.8	-13.3	-12.5
Δ I_{OFF} ($\times 10^{-3}$)	5	8.1	7.8	7.3	10.7	10.2	12.8	12.1

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
I_{ON}-to-I_{OFF} ($\times 10^{6}$)	48	720	2500	1900	3.6	0.292	5.56
I_{OFF} (mA/mm) ($\times 10^{-6}$)	11	0.62	0.15	0.23	58.8	910	28
Δ I_{ON}-to-I_{OFF} ($\times 10^{-3}$)	-18.2	-19.9	-19.9	-18.3	-11.9	-8.82	-12.3
Δ I_{OFF} ($\times 10^{-3}$)	17.6	19.3	18.9	16.2	10.77	7.87	11.78

Leakage current is measured when the transistor is in deep depletion region, which in this case is taken for small negative values of V_{GS} and for $V_{DS} = V_{DD}$. Under this biasing condition, the drain current is characterized by a plateau, and as V_{GS} becomes more negative the transistor turns into accumulation regime and the channel current starts to increase again (see Fig. 3.23). Therefore, the current at the plateau region is due only to junction leakage current. This represents the importance of the $I_{Leakage}$ figure of merit, since it overcomes the variation of V_T between devices, and a fair comparison between different devices can be held.

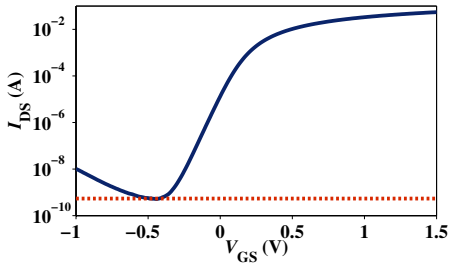


Fig. 3.23.: Illustration of the calculation method of $I_{Leakage}$.

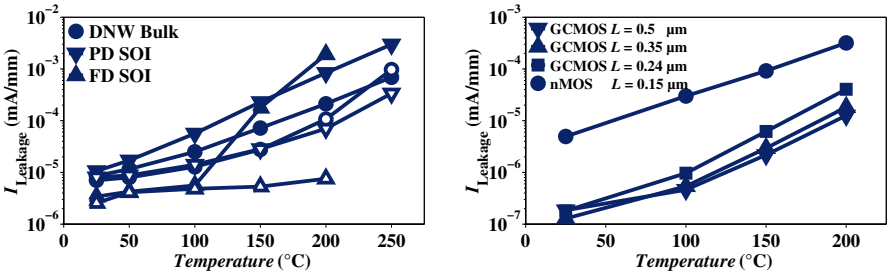
Fig. 3.24 shows the experimental results of $I_{Leakage}$ for the devices considered in this work. Starting by the PD SOI devices (Fig. 3.24a), the theoretical discussion presented earlier is clearly put in evidence. The FB structure are showing much higher leakage current than the BT structure, although they both show the same $I_{Leakage}$ at room temperature. The difference starts to be more manifested as the temperature increases, showing the important effect of the diffusion component and the floating-body reservoir. If DNW bulk devices are introduced into the comparison, an interesting behavior is worth noticing. The BT structure of the DNW bulk device shows quite the same values of $I_{Leakage}$ as the BT structure of the PD SOI device, with the exception of very high temperature situation. The FB structure of the DNW bulk device, on the other hand, shows an interesting reduction of $I_{Leakage}$ compared to the FB structure of PD SOI device as the temperature increases, knowing that both devices present close values of $I_{Leakage}$ at room temperature. Despite the larger junction areas, the DNW bulk device shows better control of the $I_{Leakage}$ taking into consideration that both devices are fabricated using the same technology in the same foundry. The bigger reservoir in the case of the DNW bulk device relaxes the diffusion component, as the carriers generated can easier be recombined rather than bypassing the energy barrier at the junction. It is worth noticing also that in the case shown in Fig. 3.24a, the DNW N^+ protection ring is connected to V_{DD}. This ensures a reverse biased *p*-*n* junction at all time. In a different measurement setup [22], the DNW N^+ was connected to the ground. Although in the later setup a more elevated diffusion current could pass through the bulk-N^+ (of the DNW protection) junction, especially at high temperatures, the comparison of the measured $I_{Leakage}$ does not show a big difference. The later case shows

slightly higher I_{Leakage} than the case of V_{DD} connection for the FB structure, and exactly the same I_{Leakage} for the BT structure[3].

The leakage current of the FD devices shown in Fig. 3.24a features very low values compared to the other devices. This is expected since the junction areas are significantly reduced compared to either the bulk or the PD devices. However, the degradation of I_{Leakage} of the FB structure with increasing the temperature is unexpected. This results from the fact that these devices are on the limit of being fully depleted, and as temperature increases, the depletion width decreases and a neutral region is created in the silicon film of the FB FD device. The increased temperature stimulates a high generation rate of electron-hole pairs and the diffusion component increases significantly giving rise to a highly degraded I_{Leakage} as shown. The FD devices are also highly doped compared to the other devices which makes the effect of the diffusion component more significant compared to the other devices.

In Fig. 3.24b, the leakage current of FD GCMOS devices of different channel lengths is compared to a FD classical nMOS device of a channel length approximately equal to the effective channel length of the shortest GCMOS device. All devices are FB. GCMOS shows impressive reduction of leakage current basically due to the significant reduction of impact ionization. The lightly doped region also reduces the overall doping level of the channel which reduces the number of electron-hole pairs generated at high temperatures.

Notice that, the FD FB device shown in Fig. 3.24b is a recent version of the same technology as that shown in Fig. 3.24a. The improved leakage current in the recent device is due to an improved FD process, although the values of I_{Leakage} are more or less the same, but with a linear increase with temperature.



(a) DNW bulk, PD, and FD SOI in FB (solid symbols) and BT (empty symbols) structures.

(b) FD GCMOS with 48 fingers and nMOS with 32 fingers of 2.5 μm width each and different channel lengths.

Fig. 3.24.: Variation of the leakage current I_{Leakage} with temperature.

[3]The current flowing in the N^+ protection ring is measured in both cases and it shows a very weak current in the order of pA.

Table 3.5.: I_{Leakage} at room temperature and its variation with temperature expressed in decade per ^{o}C. The variation is calculated from a linear regression taken over the whole range of temperature. A multiplication factor of 10^{-6} is taken for I_{Leakage} and 10^{-3} for $\Delta\ I_{\text{Leakage}}$.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
I_{Leakage} (mA/mm)	8.6	7.1	6.4	11	2.6	8.1	3.4	2.6
$\Delta\ I_{\text{Leakage}}$	8.5	9.5	5.4	10.9	7.2	5.3	15.7	2.7

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
I_{Leakage} (mA/mm)	4.95	0.18	0.13	0.19	—	—	—
$\Delta\ I_{\text{Leakage}}$	10.3	13.4	12.3	10.5	—	—	—

3.2.7 Zero Temperature Coefficient

The so called Zero Temperature Coefficient (ZTC) point has been identified for bulk CMOS by Shoucair [23] and Prijic *et al.* [24] in both the linear and the saturation regions for temperatures between 27 and 200^{o}C. According to Shoucair, the ZTC of drain current is usually well defined up to approximately $200^{o}C$, whereas at higher temperatures, drain-to-body leakage currents typically cause the characteristics to shift upwards on a linear scale of micro-Amperes. Later, Groeseneken *et al.* [14] and Jeon *et al.* [25] demonstrated the existence of the ZTC point experimentally for thin and thick-film SOI MOSFETs, respectively. The analytical formulation for ZTC in SOI devices has been introduced by Osman *et al.* [26]. ZTC point is device-geometry-independent for a given process [23] but it depends on the bias of the body for body-contacted SOI devices [27].

Basically, there are two ZTC points for a transistor, one for the drain current and the other for the transconductance, and in general they have different values in linear and in saturation regions. These ZTC points are defined as the points at which the drain current or the transconductance remains constant as temperature varies, i.e. $\partial I_{\text{DS}}(T)/\partial T \approx 0$ or $\partial g_m(T)/\partial T \approx 0$, respectively. This can be explained as follows. The ZTC points are values of V_{GS} at which the reduction of the threshold voltage due to increasing temperature is counter-balanced by the reduction of the mobility, and as a result, the value of the drain current or

the value of the transconductance remains constant as the temperature varies. For gate voltages lower than ZTC, the decrease of the threshold voltage is dominant and so the drain current increases with temperature, while for gate voltages higher than ZTC, the mobility degradation predominates and the drain current decreases with temperature. The ZTC is a very important bias point for analog designers as it corresponds to a gate voltage at which the device dc performance remains constant with temperature [28, 29].

Fig. 3.25 to 3.32 present the normalized I_{DS}–V_{GS} characteristics of the different devices considered in this work in both linear and saturation regimes of operation, respectively, in addition to the normalized transconductance g_m calculated from dc measurements using

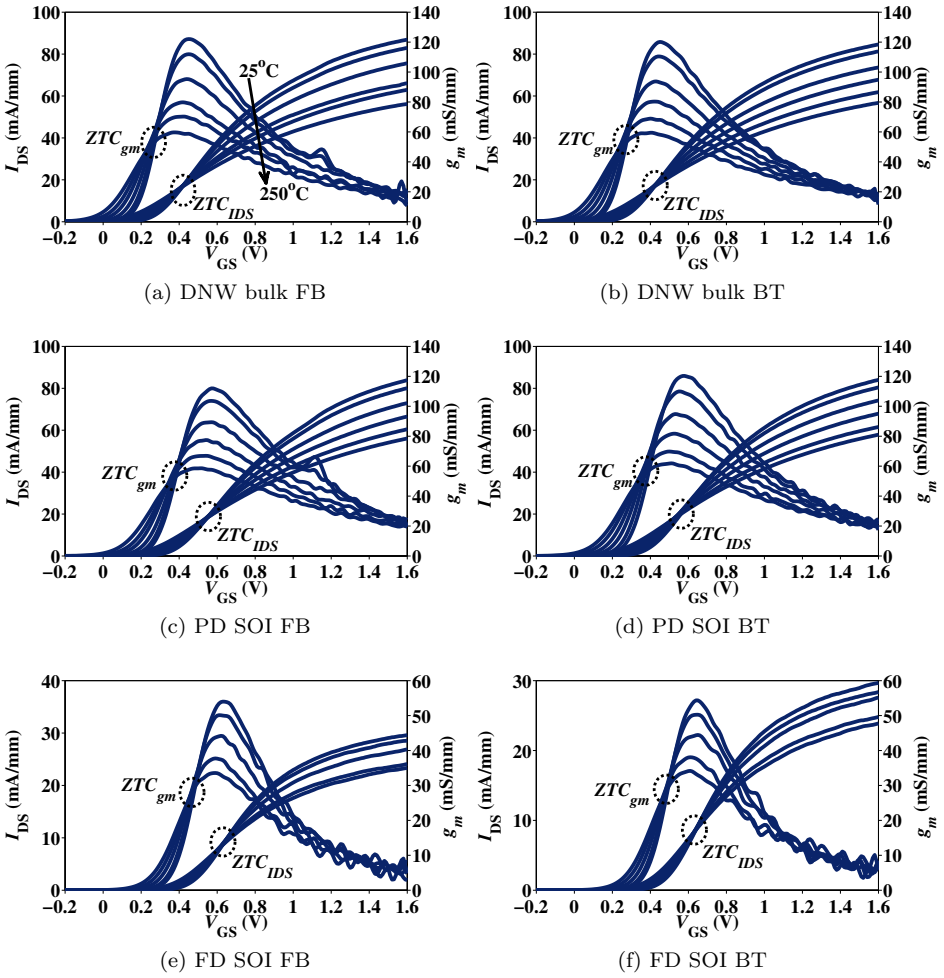
$$g_m = \left.\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}}\right|_{V_{\mathrm{DS}}} \tag{3.20}$$

All devices are measured in a temperature range of 25 to 250^{o}C except for the FD devices which were measured till 200^{o}C only as mentioned in section 2.8.

For an easier reference and comparison, Table 3.6 provides a summary of all ZTC points as well as V_T values in both linear and saturation regions. It is of importance to identify whether the ZTC point lies below or above V_T. A device designed to deliver high drive current should operate above V_T whereas it might be of interest to look at the subthreshold characteristics of a device designed to be used in a low voltage low power (LVLP) application (the later is discussed in more detail in chapter 4).

Starting by the DNW bulk devices, the first interesting point is that the DNW protection extended the validity of ZTC points to 250^{o}C in contrary to what Shoucair noticed for Bulk transistors [23]. However, this is not true for DT devices. For the DT DNW bulk device in linear region, Fig. 3.26a, the ZTC_{gm} is only defined up to 200^{o}C (as Shoucair noticed) and in saturation region, Fig. 3.30a, ZTC_{IDS} is only defined up to 200^{o}C (the same is noticed at lower values of $V_{\mathrm{DS}} = 0.6$ V). The second point is the identical ZTC_{IDS} for both FB and BT devices in linear region. The same applies for ZTC_{gm}. However, the points differ significantly in the saturation region. In all cases, ZTC_{gm} is in the order of or below V_T (for FB and DT, it is slightly higher than V_T in linear region and for DT in saturation region). This is a drawback for high drive current applications, since it will not be possible to have constant transconductance (and hence cutoff frequencies as will be seen in section 3.4) while providing high drain current. On the other hand, it is well suited for LVLP applications (in contrary to a situation where ZTC_{gm} is higher than V_T, since the LVLP applications are interested in operating the device at or below V_T).

PD devices feature quite close characteristics as the DNW bulk devices from the ZTC point of view (see Fig. 3.25 and Fig. 3.26 for the linear region and Fig. 3.29 and Fig. 3.30 for the saturation region). Both ZTC points are well defined up to 250^{o}C with the exception of the DT device where the ZTC_{IDS} is only defined up to 200^{o}C. Regarding the relation between the ZTC points and V_T, the behavior is nearly identical to that observed for DNW bulk devices.



(a) DNW bulk FB (b) DNW bulk BT

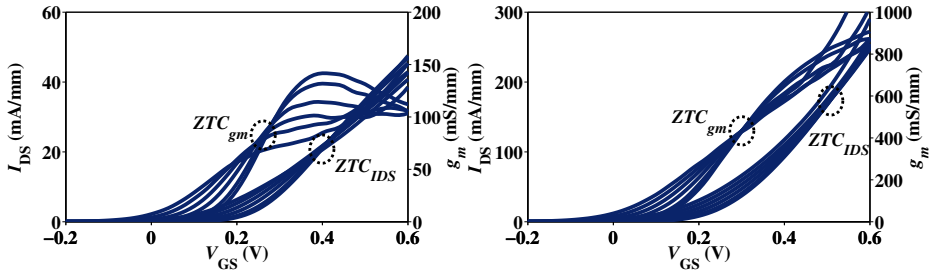
(c) PD SOI FB (d) PD SOI BT

(e) FD SOI FB (f) FD SOI BT

Fig. 3.25.: ZTC points in linear region for DNW bulk, PD, and FD SOI in FB and BT structures for a temperature range of 25 to 250^{o}C (200^{o}C for the FD devices).

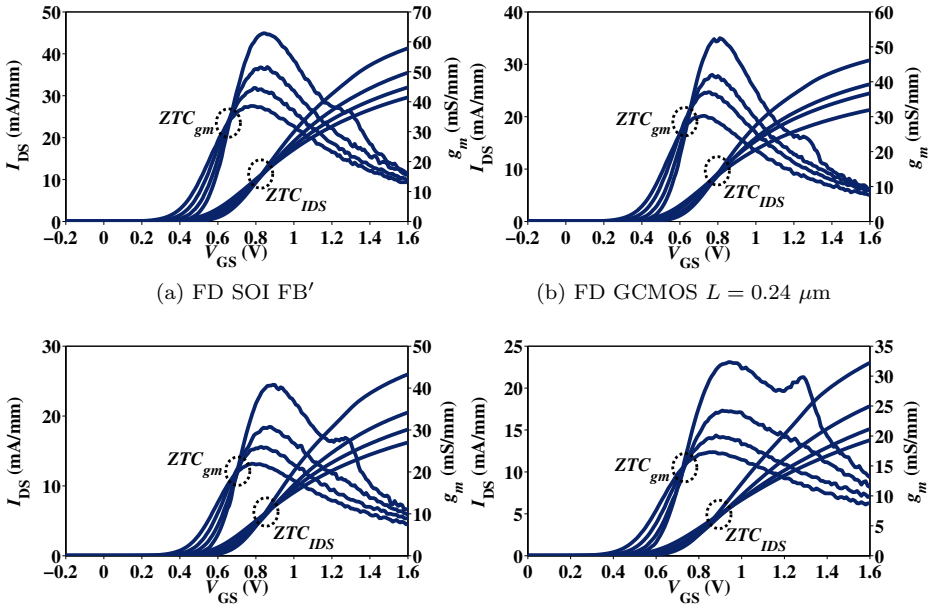
FD devices are characterized by very well defined ZTC points, both for I_{DS} and g_m, even in linear region of operation (see Fig. 3.25e and Fig. 3.25f for linear region and Fig. 3.29e and Fig. 3.29f for saturation region), knowing that the validity of the ZTC points at 250^{o}C is not verified.

The ZTC points in GCMOS devices were first presented in [30]. Fig. 3.27 and Fig. 3.31 show the ZTC_{IDS} and the ZTC_{gm} points for three FD GCMOS devices in linear and saturation regions (a classical nMOS device is also shown from the same technology for comparison). They are well defined and follow the scaling



(a) DNW bulk DT (b) PD SOI DT

Fig. 3.26.: *ZTC* points in linear region for DNW bulk and PD SOI in DT structure for a temperature range of 25 to 250^{o}C.



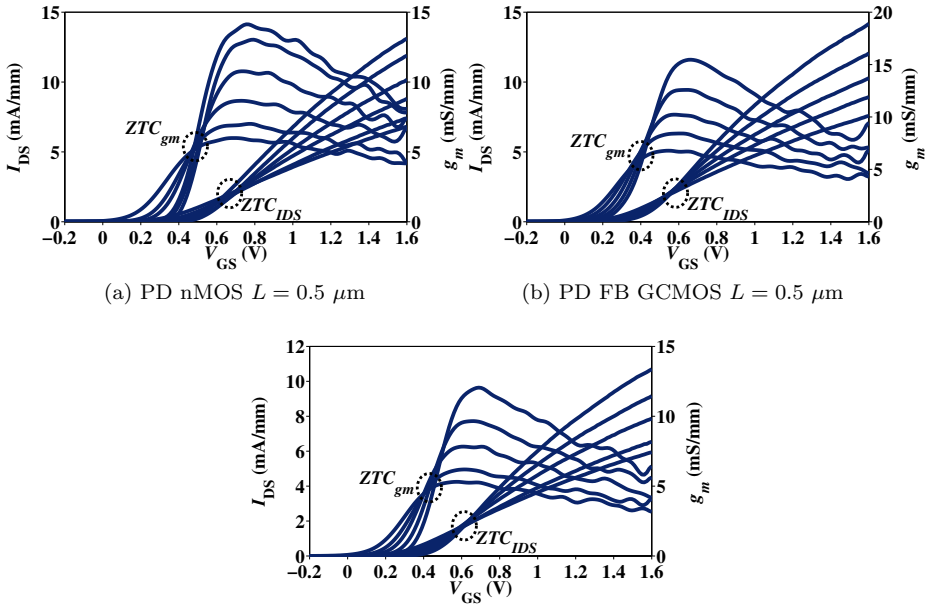
(a) FD SOI FB′ (b) FD GCMOS $L = 0.24$ μm

(c) FD GCMOS $L = 0.35$ μm (d) FD GCMOS $L = 0.5$ μm

Fig. 3.27.: *ZTC* points in linear region for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths for a temperature range of 25 to 200^{o}C.

trend of classical FD SOI [31]. Furthermore, GCMOS shows the advantage of a lower difference between ZTC_{gm} and ZTC_{IDS}. This reduces the uncertainty of designing a circuit working at a stable I_{DS} or a stable g_m with temperature.

This feature, the difference between ZTC_{gm} and ZTC_{IDS}, as well as the difference between *ZTC* points and V_T for both linear and saturation regimes



(a) PD nMOS $L = 0.5$ μm

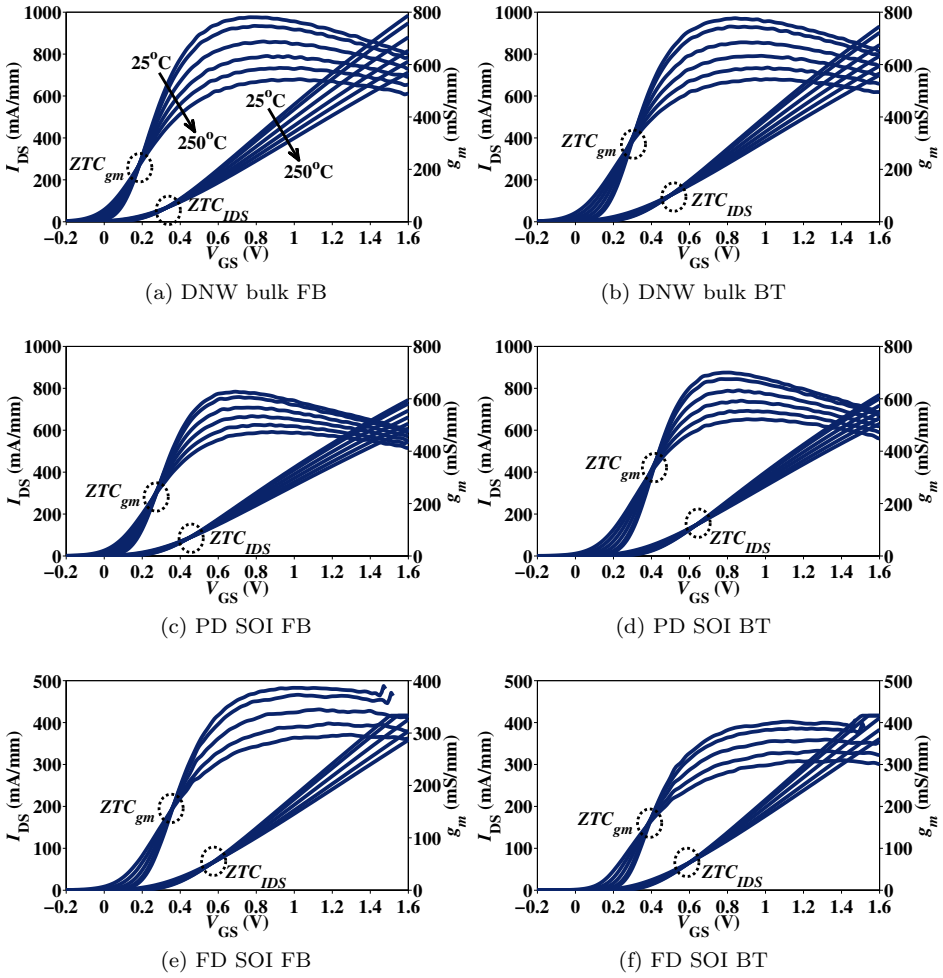
(b) PD FB GCMOS $L = 0.5$ μm

(c) PD BT GCMOS $L = 0.5$ μm

Fig. 3.28.: ZTC points in linear region for PD GCMOS and classical nMOS of 0.5 μm channel lengths for a temperature range of 25 to 250^{o}C.

of operation are summarized in Table 3.6 for all the devices. It is clear from this table that a choice for a LVLP application would be a GCMOS device where both the ZTC points lie at or below V_T (especially in saturation region), and where the difference between the two ZTC points is minimum.

A very interesting advantage of the PD SOI BT transistor over the FB transistor is shown in Fig. 3.29d and Fig. 3.29c where the ZTC points are noticed at higher V_{GS} for BT transistor for both drain current and transconductance measured at $V_{\mathrm{DS}} = 1.2$ V. For BT transistor, ZTC_{IDS} and ZTC_{gm} take place at $V_{\mathrm{GS}} = 0.6$ and 0.4 V, respectively, whereas for the FB transistor they take place at $V_{\mathrm{GS}} = 0.43$ and 0.25 V, respectively. This ensures, for BT transistor rather than FB transistor, an operation in ON mode at the ZTC point, giving higher drive current and higher overdrive voltage which is quite important for analog circuit designers working at varying temperature environments. It can also be noticed that the ZTC point for both PD SOI FB and BT transistors are well defined even up to 250^{o}C (and up to 300^{o}C for the work of Osman *et al.* [26]) thanks to the suppression of leakage currents by the insulating layer between the body and substrate; i.e. the Buried Oxide (BOX).



(a) DNW bulk FB (b) DNW bulk BT

(c) PD SOI FB (d) PD SOI BT

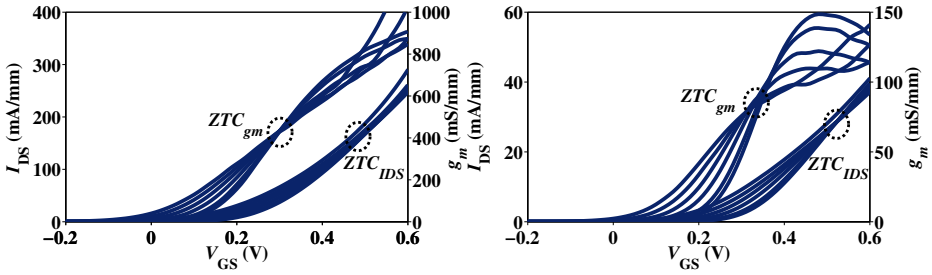
(e) FD SOI FB (f) FD SOI BT

Fig. 3.29.: ZTC points in saturation region for DNW bulk, PD, and FD SOI in FB and BT structures for a temperature range of 25 to 250^{o}C (200^{o}C for the FD devices).

3.3 ANALOG CHARACTERIZATION

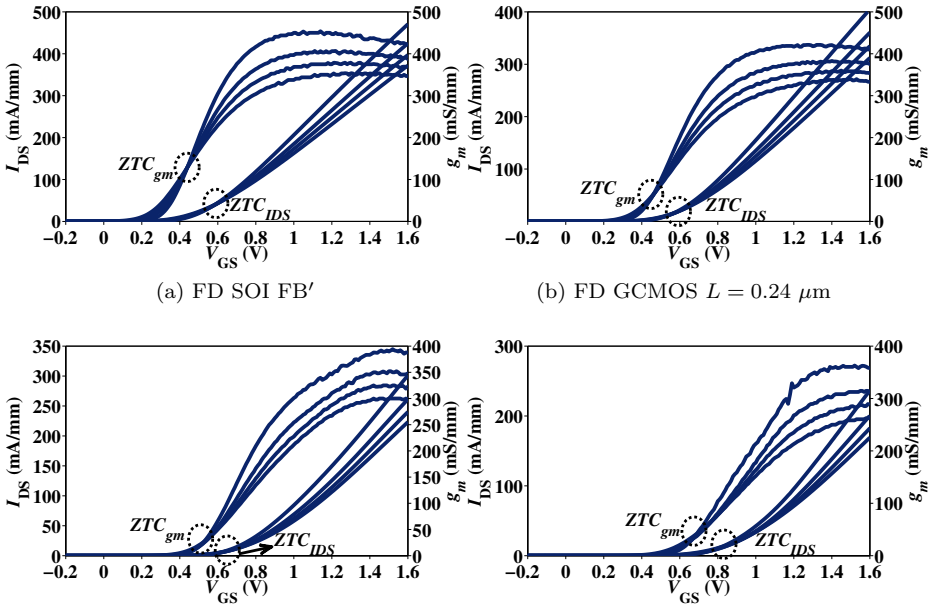
An analog designer is mostly concerned by three parameters: the ratio of transconductance to the drain current, the early voltage, and the intrinsic gain. Basically, these three parameters constitute the three vertices of the same triangle, since they are related by the low-frequency open-loop gain A_{v0} [32]:

$$A_{v0} = \frac{g_m}{g_D} = \frac{g_m}{I_{\mathrm{DS}}} V_{\mathrm{EA}} \tag{3.21}$$



(a) DNW bulk DT (b) PD SOI DT

Fig. 3.30.: *ZTC* points in saturation region for DNW bulk and PD SOI in DT structure for a temperature range of 25 to 250^{o}C.

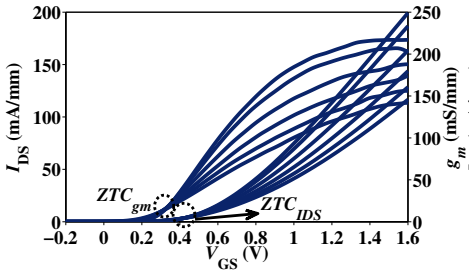


(a) FD SOI FB′ (b) FD GCMOS $L = 0.24$ μm

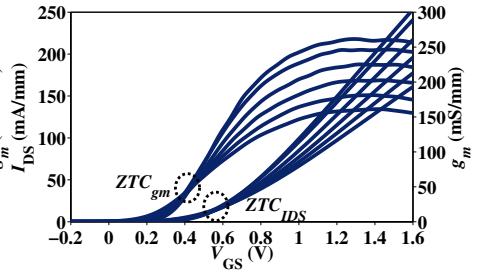
(c) FD GCMOS $L = 0.35$ μm (d) FD GCMOS $L = 0.5$ μm

Fig. 3.31.: *ZTC* points in saturation region for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths for a temperature range of 25 to 200^{o}C.

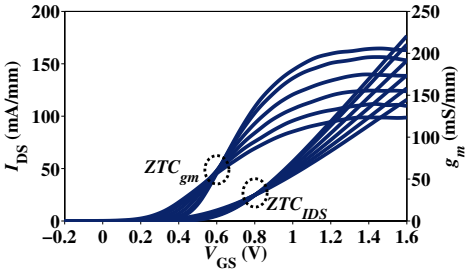
For analog applications, a transistor is always operated in saturation, hence, the extraction of these figures of merit are presented hereafter in saturation region. Another two factors which are very important for analog circuit design: the intrinsic gate capacitance and the noise performance of the transistor [33].



(a) PD nMOS $L = 0.5$ μm



(b) PD FB GCMOS $L = 0.5$ μm



(c) PD BT GCMOS $L = 0.5$ μm

Fig. 3.32.: ZTC points in saturation region for PD GCMOS and classical nMOS of 0.5 μm channel lengths for a temperature range of 25 to 250^{o}C.

The intrinsic gate capacitance is presented in section 3.4 whereas the noise performance is presented in chapter 6 for some selected devices.

3.3.1 Transconductance to Drain Current Ratio g_m/I_{DS}

It is well known that the maximum analog performance of a MOSFET device is obtained at the condition of maximum g_m/I_{DS} [33]. This condition is known to occur in weak inversion for MOSFETs [34]. In weak inversion, the g_m/I_{DS} can be calculated from [33]:

$$\frac{g_m}{I_{DS}} = \frac{dI_{DS}}{I_{DS}dV_{GS}} = \frac{\ln(10)}{S} = \frac{q}{nkT} \tag{3.22}$$

whereas in strong inversion, the g_m/I_{DS} is calculated from [33]:

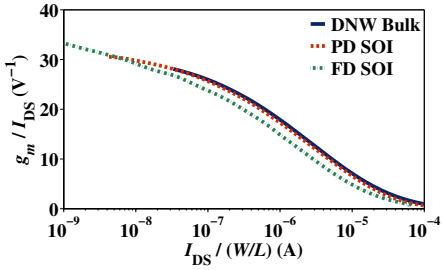
$$\frac{g_m}{I_{DS}} = \sqrt{\frac{2\mu C_{ox} W/L}{nI_{DS}}} \tag{3.23}$$

Theoretically, the low body-effect coefficient n of SOI devices results in a near ideal behavior of g_m/I_{DS} (maximum physically achievable values at room temperature). This is strongly related to the subthreshold swing S which also depends on n.

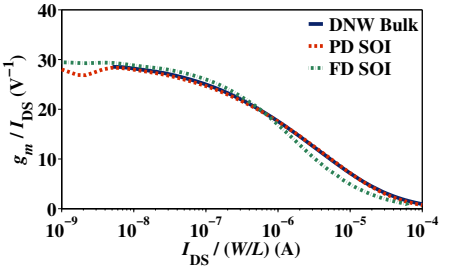
Table 3.6.: ZTC points for different devices in linear (Lin.) and saturation (Sat.) regimes. Threshold voltage values (in linear and saturation) are appended to easily identify the position of the ZTC point with respect to V_T. The three important figures of merit: $ZTC_{diff} = ZTC_{IDS} - ZTC_{gm}$, $A = ZTC_{IDS} - V_T$, and $B = ZTC_{gm} - V_T$ for different devices in linear and saturation regions are also calculated. All values are in volts with a multiplication factor of 10^{-2}.

	DNW Bulk			PD SOI			FD SOI		FD				PD		
	FB	BT	DT	FB	BT	DT	FB	BT	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2	2	2	2	2	2	5	5	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	30	30	30	30	30	30	48	48	32	48	48	48	12	12	12
Lin.															
ZTC_{IDS}	43	43	40	55	55	52	63	64	83	80	89	93	70	56	61
ZTC_{gm}	27	27	28	40	41	30	48	49	66	65	71	73	50	43	44
V_T	24	28	26	35	36	34	46	47	65	64	70	74	55	46	51
ZTC_{diff}	16	16	12	15	14	22	15	15	17	18	18	20	21	13	17
A	19	15	14	20	19	18	17	17	18	19	18	19	15	10	10
B	3	−1	2	5	5	−4	2	2	1	1	1	−1	−5.5	−3	−7
Sat.															
ZTC_{IDS}	32	51	51	45	63	52	56	60	59	56	58	77	42	55	79
ZTC_{gm}	19	30	30	27	42	35	36	39	44	46	56	68	33	42	59
V_T	22	30	26	29	40	36	35	36	47	55	69	85	48	53	63
ZTC_{diff}	13	21	21	18	21	17	20	21	15	10	2	9	9	13	20
A	10	21	25	16	23	16	21	24	12	1	−11	−8	−6	2	16
B	−3	0	4	−2	2	−1	1	3	−3	−9	−13	−17	−15	−11	−4

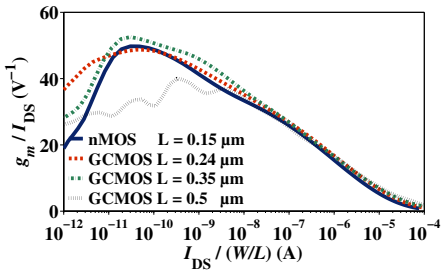
In the ideal case, an S of 60 mV/dec corresponds to a g_m/I_{DS} of 38 V^{-1} [35]. In bulk devices, a typical value of g_m/I_{DS} is 25 V^{-1}. As already mentioned, n in FD devices is lower than PD devices, hence, FD devices have better values of g_m/I_{DS} than PD devices.



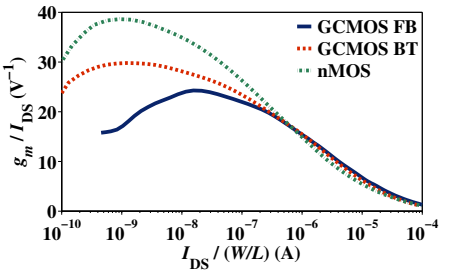
(a) DNW bulk, PD, and FD SOI in FB structures.



(b) DNW bulk, PD, and FD SOI in BT structures.



(c) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(d) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.33.: Comparison of g_m/I_{DS} for different devices.

The comparison of g_m/I_{DS} presented hereafter adopts the approach used by V. Kilchytska *et al.* [35] of comparing g_m/I_{DS} as a function of normalized drain current $I'_{DS} = I_{DS}/(W/L)$. This approach is ideal for comparing different devices, like the ones studied in this work, since it eliminates the dependence on the threshold voltage and the channel length. The later is guaranteed to the first order until the short channel effects become dominant in weak inversion or until the velocity saturation dominates in strong inversion.

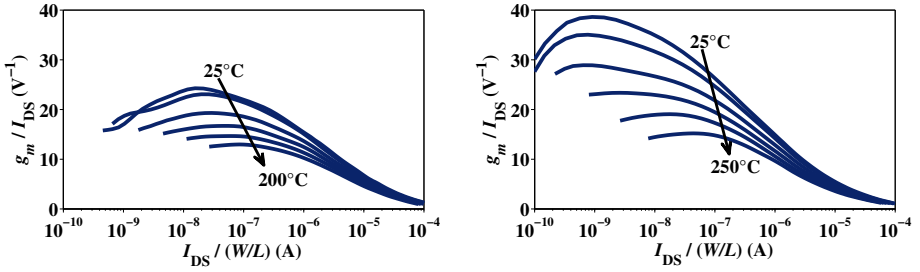
It was shown by V. Kilchytska *et al.* [35] that in saturation, g_m/I_{DS} keeps a constant maximum in weak inversion and starts to quadratically decrease with normalized current I'_{DS} through the influence of the body effect and the mobility.

The g_m/I_{DS} for the different devices considered in this work is shown in Fig. 3.33 for the saturation condition where $V_{DS} = V_{DD}$. The DNW bulk devices, either in FB or BT structures, are shown to deliver the same performance as the PD SOI devices. On the other hand, the FD device shows lower performance for

the entire range of operation for the FB structure whereas for the BT structure, it outperforms the DNW bulk and the PD SOI devices in weak inversion only.

In general, GCMOS devices, either in PD or FD technologies, are not able to outperform the classical nMOS devices except for strong inversion region of operation.

Increasing the temperature has a double effect on the g_m/I_{DS} behavior. The peak value of g_m/I_{DS} is reduced along with an increase of the normalized I_{DS} at which the peak occurs, as shown in Fig. 3.34 where the FB structure of a PD GCMOS and a PD classical nMOS devices are taken as an example. All the other devices show the same behavior.



(a) PD GCMOS of 0.5 μm channel lengths.

(b) PD classical nMOS of 0.5 μm channel lengths.

Fig. 3.34.: The double effect of increasing the temperature on the behavior of g_m/I_{DS}.

3.3.2 Early Voltage V_{EA}

The Early effect was originally defined in 1952 by J. M. Early for junction transistors (like BJTs) to account for a lack of saturation in the common-emitter output characteristics [16, 36]. In MOSFETs, the Early effect is also present where the drain current does not saturate at high values of drain voltage giving rise to some undesired effects. At higher values of drain voltage, the junction depletion width X_{D} (of the drain-body junction) increases, which reduces the effective electrical channel length. This means that the parasitic bipolar effective base width also decreases. As a result, the parasitic bipolar gain increases and the device can suffer from several drawbacks, one of which being a higher vulnerability to the Soft Error Rate (SER)[4][37].

The Early voltage V_{EA} is a measure of the Early effect, and is calculated from the intersection with the x-axis of the extrapolated line of the drain current drawn as a function of the drain voltage. The higher the absolute value of V_{EA}

[4]Soft Error Rate is the fail rate of an array due to alpha and cosmic radiation, commonly measured in fails per thousand hours per thousand bits.

(since it is by definition of negative value for n-type MOSFETs), the better the performance of the device for analog applications.

According to [33, 38], V_{EA} is highly dependent on bias conditions and technological parameters. Hence, it can be used as an indicator of several physical phenomena. A V_{EA} increasing from week inversion to strong inversion indicates an enhanced vertical gate coupling and in the same time a lower lateral drain influence on the drain current. Also, the increase of V_{EA} (in FD SOI as compared to bulk devices) shows a reduced penetration of the drain depletion region into the channel.

In literature, V_{EA} is either calculated from the extrapolation of the drain current till it intersects with the negative side of the drain voltage axis, or by dividing the drain current I_{DS} by the output conductance g_D at a certain $V_{GS} = V_{DS}$ condition. The first method is used in this work despite the difficulties to achieve a good extrapolation especially with the presence of the kink effect in FB devices. A careful choice of the range of drain current points should be found in order to avoid the knee around the saturation value of V_{DS}, or $V_{DS,sat}$, and the knee due to the kink effect. Fig. 3.35 shows an illustration of how this extrapolation is performed. The dashed line (the extrapolation line) is extrapolated from the extrapolation range (marked by x symbols) and is extended till it intersects the negative V_{DS} axis at the $-V_{EA}$ value [5].

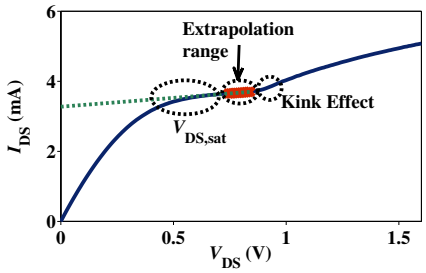


Fig. 3.35.: An illustration of the extrapolation to extract the Early voltage V_{EA}.

Results of V_{EA} extraction are shown in Fig. 3.36 for the different devices and structures. Fig. 3.36a shows that theory is conserved for most of the cases. If FB structures are considered, the DNW bulk device presents the lowest values of V_{EA} (see Table 3.7 for the values at room temperature and the variation of V_{EA} with temperature), whereas the FD device shows the highest values of V_{EA} as

[5] Different methods for the extraction of V_{EA} exist in literature. Besides the classical method employed in this chapter, another method is to calculate $V_{EA} = I_{DS}/g_D$ at a certain $V_{GS} = V_{DS}$ fixed for all devices. The author of this thesis found difficulties in applying the later method due to the strong variation of the position of the kink among the various structures studied in this work. Although the number of bias points along which the extrapolation is taken in the method presented above is small, it reflects the specific V_{EA} characteristics of each device since it avoids the saturation knee and the kink effect. This approach is thus believed to constitute a fair comparison between the different technologies and the various structures presented in this work.

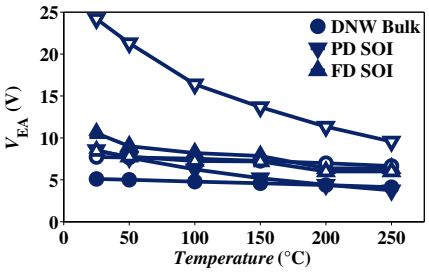
expected. The PD device shows a high degradation of V_{EA} till it coincides with the DNW bulk device at 250^{o}C, which is also expected due to the increased generation recombination rates with temperature which in turn increases the body factor. The depletion width of the drain junction also reduces with temperature. As a result, the PD SOI device tend to behave as the DNW bulk device at very high temperature, since these two effects are more pronounced in a PD SOI than in a bulk device where the later is already at its lowest values of V_{EA} due to the large value of body effect and the large drain junction depletion area.

BT structures, on the other hand, show an amazing behavior of V_{EA}. The PD SOI device shows the highest values of V_{EA} due to a well gate coupling resulting from the body-tie and the lack of the floating-body effects. As expected, this effect is more pronounced in PD SOI than in DNW bulk which has a much thicker t_{Si}. An exception is shown for the FD Device, where the BT structure shows lower values of V_{EA} than the FB structure.

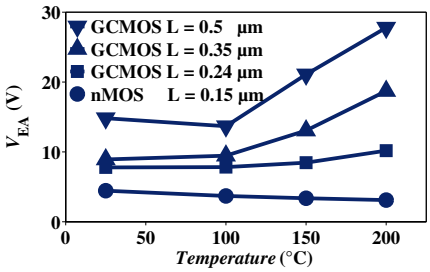
GCMOS devices, either on FD (Fig. 3.36b) or PD (Fig. 3.36c) technologies, merit a highly reduced impact ionization which results in a higher V_{EA} compared to the corresponding classical nMOS device. A BT GCMOS structure can even provide a better V_{EA} as shown in Fig. 3.36c. Depending on which factor is more dominant, the lowering of the impact ionization or the reduction of the depletion width of the drain junction, V_{EA} might show an increase with temperature as seen for the FD GCMOS devices. Another factor is how much the kink effect is affecting the region where the extrapolation is taken, since the increase of temperature eliminates the kink, thus reduces g_D, and V_{EA} can then increase since $V_{\mathrm{EA}} = I_{\mathrm{DS}}/g_D$. This effect is shown on the g_D curves as presented in Fig. 3.37, Fig. 3.38, and Fig. 3.39

3.4 RF CHARACTERIZATION

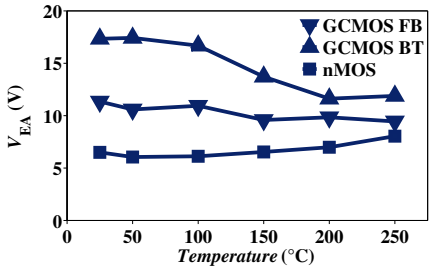
The high-temperature RF behavior of SOI MOSFETs has not received the same attention in the literature as the high-temperature dc behavior. In the following subsections, the high-temperature RF behavior is studied in detail based on measured data. An Anritsu 37369A two-port Vector Network Analyzer VNA operating up to 40 GHz and a 100 μm-pitch Ground-Signal-Ground (GSG) high-frequency high-temperature Z-probes are used for RF signal measurements while dc biasing is achieved using a HP 4145B device parameter analyzer. A temperature controlled 200 mm chuck is used to obtain measurements from room temperature up to 250^{o}C. An OPEN dummy structure is measured to perform a one-step de-embedding and hence removing the effects of the pad capacitances on the gate and the drain sides, C_{pg} and C_{pd}, respectively. The effect of the access inductances L_{g}, L_{d}, and L_{s} are found to be negligible due to the short access lines and the relatively low frequencies at which the extraction is performed (between 1 and 4 GHz). Therefore, the reference plan could be put at the dashed box in the small-signal equivalent circuit shown in Fig. 3.40. This is the physical borders of the transistor or the device under test DUT. However, these physical



(a) DNW bulk, PD, and FD SOI in FB (solid symbols) and BT (empty symbols) structures.



(b) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(c) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.36.: Variation of V_{EA} with temperature for different devices.

borders include two types of elements, the ones outside the dotted box, called the extrinsic elements and the ones inside the dotted box called the intrinsic elements. The distinction between "extrinsic" and "intrinsic" elements depends on their properties rather than their position in space, or in other words, elements are classified according to their specific behavior with respect to bias rather than on their location with respect to the underlying physical layout inside or outside a certain conceptual boundary [39]. An "extrinsic" element depends on the geometry of the device and is independent of the biasing conditions of the transistor. On the other hand, an "intrinsic" element is dependent on the bias conditions and on the size of the active zone.

In a first step, the two main figures of merit for RF characterization, f_T and $f_{\max}$, are extracted from measured data after the de-embedding step, without trying to distinguish between extrinsic and intrinsic effects. In a second step, these extrinsic and intrinsic elements are studied in detail.

3.4.1 Cutoff Frequencies

The RF behavior of a transistor is usually characterized by three cutoff frequencies: current gain cutoff frequency f_T, unilateral gain cutoff frequency $f_{\max}$, and

Table 3.7.: Early voltage V_{EA} in V at room temperature and its variation with temperature in mV/°C.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
V_{EA}	5.1	7.72	—	8.55	24.2	—	10.56	8.44
ΔV_{EA}	−4.3	−4.8	—	−21.1	−64.2	—	−17.6	−10.7

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
V_{EA}	4.45	7.78	8.92	14.8	6.5	11.34	17.34
ΔV_{EA}	−7.7	12.9	54.7	76	7.1	−7.9	−29.6

maximum available gain cutoff frequency f_{MAG}. The cutoff frequency is the frequency point where the corresponding gain is equal to unity [33]. The first two cutoff frequencies are considered and extracted in this section for all the devices. Their behavior with temperature is also studied and presented.

3.4.1.1 Current Gain Cutoff Frequency f_T

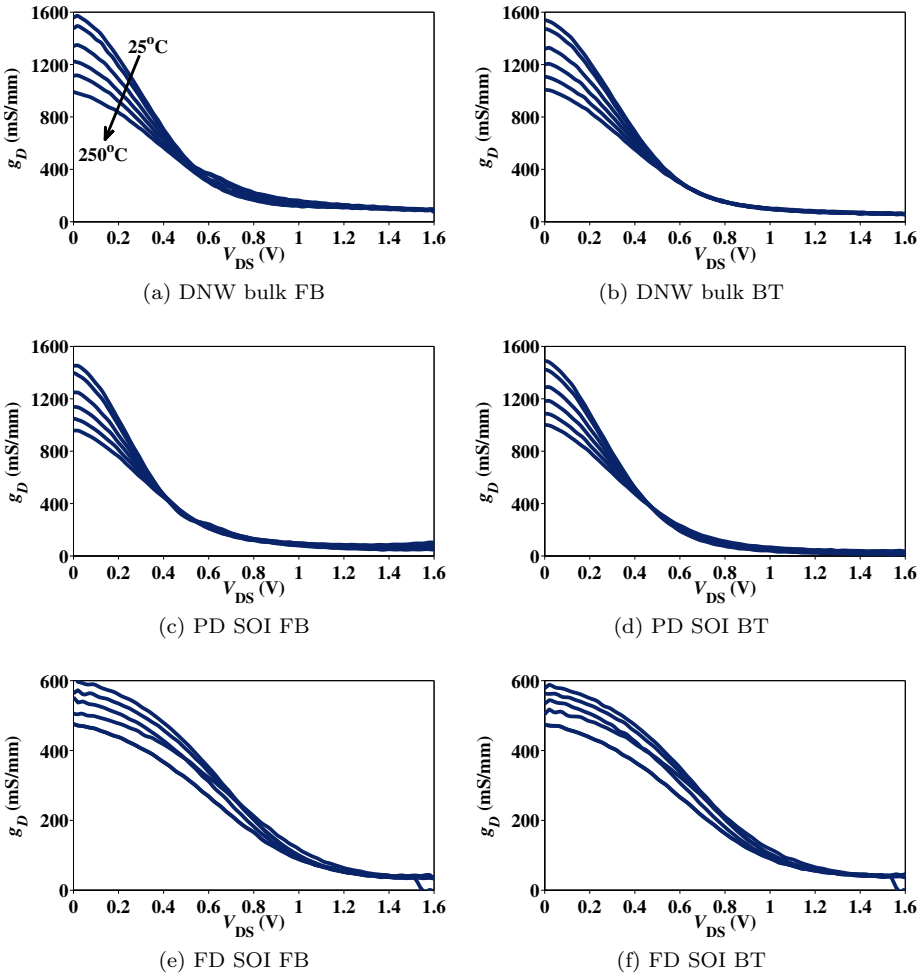
The current gain cutoff frequency f_T of a transistor (also known as the transition frequency) characterizes the point at which the current gain of the transistor vanishes. Hence, f_T characterizes the high frequency behavior of a transistor. It is extracted from the x-axis intersection of an extrapolated −20 dB/dec line on the curve of the current gain $|H_{21}|$ versus frequency (see Fig. 3.41). The current gain can also be calculated from the measured S parameters using:

$$|H_{21}| = \left| \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \right| \tag{3.24}$$

Based on the small-signal equivalent circuit, the current gain cutoff frequency f_T can be obtained analytically from:

$$f_T = \frac{\Re(Y_{21})}{2\,\pi\,\Im(Y_{11})/\omega} \tag{3.25}$$

where $\Re(Y_{21})$ is mainly a function of the gate transconductance and $\Im(Y_{11})/\omega$ is directly related to the total gate capacitance. In a simplified form, f_T could be



(a) DNW bulk FB (b) DNW bulk BT

(c) PD SOI FB (d) PD SOI BT

(e) FD SOI FB (f) FD SOI BT

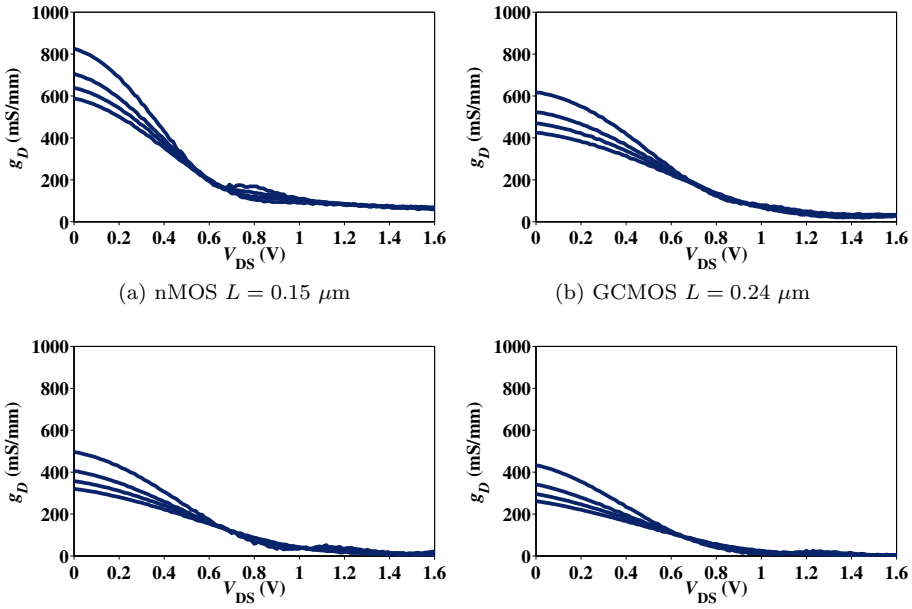
Fig. 3.37.: Output conductance g_D in saturation region ($V_{\mathrm{DS}} = V_{\mathrm{DD}}$) for DNW bulk, PD, and FD SOI in FB and BT structures for a temperature range of 25 to 250^{o}C (200^{o}C for the FD devices).

given by

$$f_T = \frac{g_m}{2\pi C_{\mathrm{gg}}} \tag{3.26}$$

where C_{gg} is the total gate capacitance ($C_{\mathrm{gg}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$).

It is worth noticing that the theoretical slope of -20 dB/dec is easily found for all the devices considered in this work at different bias points. The values of f_T extracted from the graphical representation of $|H_{21}|$ and the -20 dB/dec slope were also verified using the small-signal equivalent circuit as follows: the elements (intrinsic and extrinsic) of the small-signal equivalent circuit are ex-



(a) nMOS $L = 0.15$ μm

(b) GCMOS $L = 0.24$ μm

(c) GCMOS $L = 0.35$ μm

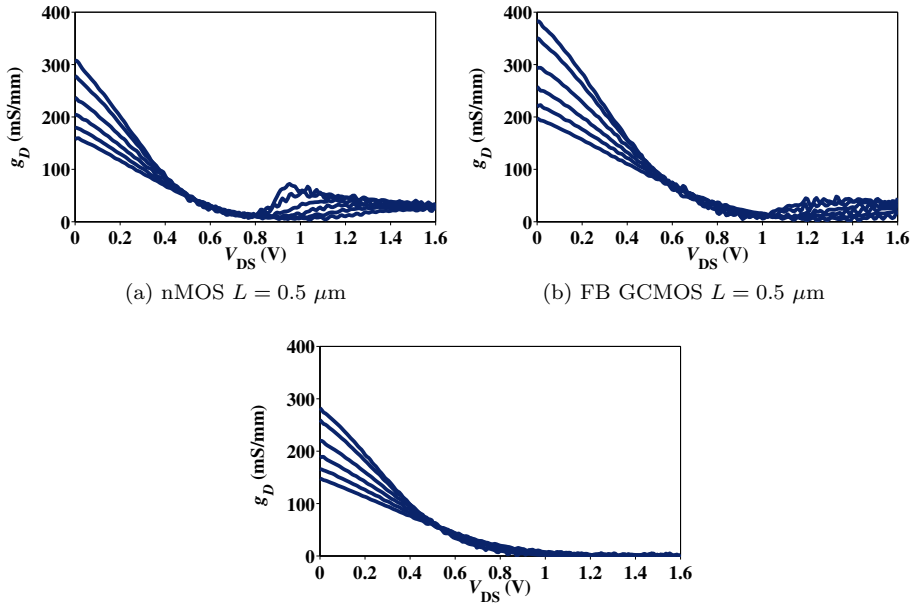
(d) GCMOS $L = 0.5$ μm

Fig. 3.38.: Output conductance g_D in saturation region ($V_{\mathrm{DS}} = V_{\mathrm{DD}}$) for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths for a temperature range of 25 to 200^{o}C.

tracted then used to generate a new set of S-parameters. $|H_{21}|$ is then calculated and f_T is extracted once again using the -20 dB/dec extrapolation. Eq. (3.25) and (3.26) were also used to calculate f_T. In all the cases, the values of f_T are very close with a negligible margin of error.

The relation between f_T and the bias conditions is tied to the relation between the transconductance and the bias conditions. However, this relation should be treated with caution since the transconductance extracted from dc measurements could suffer from self-heating giving some inaccurate behavior. A transconductance extracted from RF measurements is more efficient in studying the relation between f_T and the bias conditions. Fig. 3.42 shows how f_T and g_m vary as V_{GS} and V_{DS} vary. It is clear that the maximum of f_T occurs at the same bias conditions as the maximum of g_m. In general, this maximum occurs at the maximum of V_{DS} knowing that at a certain point, the increase of f_T saturates with the increase of V_{DS} where the device reaches its maximum limit of RF performance.

It has been already shown that GCMOS devices exhibit higher transconductance than the corresponding classical nMOS devices. As a direct consequence, GCMOS devices also benefit from higher cutoff frequency than classical nMOS devices, assuming that the capacitance is comparable between the two structures. This relation was found to be true for PD as well as for FD GCMOS devices. A



(a) nMOS $L = 0.5$ μm

(b) FB GCMOS $L = 0.5$ μm

(c) BT GCMOS $L = 0.5$ μm

Fig. 3.39.: Output conductance g_D in saturation region ($V_{\mathrm{DS}} = V_{\mathrm{DD}}$) for PD GCMOS and classical nMOS of 0.5 μm channel lengths for a temperature range of 25 to 250^{o}C.

comparison of f_T is shown in Fig. 3.43a for PD devices of 0.5 μm channel length. In Fig. 3.43b, it is shown that the 0.5 μm GCMOS is not capable to compete with the 0.35 μm classical nMOS which would be predicted from the behavior of the dc transconductance shown in section 3.2.2.3. An explanation could be given based on the behavior of the device capacitance (see (3.26)) as will be shown in section 3.4.3.2.

To study of the effect of temperature on the current gain cutoff frequency, the variation of the maximum of f_T is considered as a function of temperature. This is shown in Fig. 3.44 for the different devices.

It is clear that as the temperature increases, the cutoff frequency f_T decreases with different slopes. From (3.25), this degradation of f_T can be related to either a degradation with temperature in the behavior of $\Re(Y_{21})$, thus the transconductance, or $\Im(Y_{11})/\omega$, thus the total gate capacitance, or both. This can be further studied when looking at the intrinsic parameters presented in section 3.4.3. Table 3.8 summarizes the behavior of f_T for the different devices.

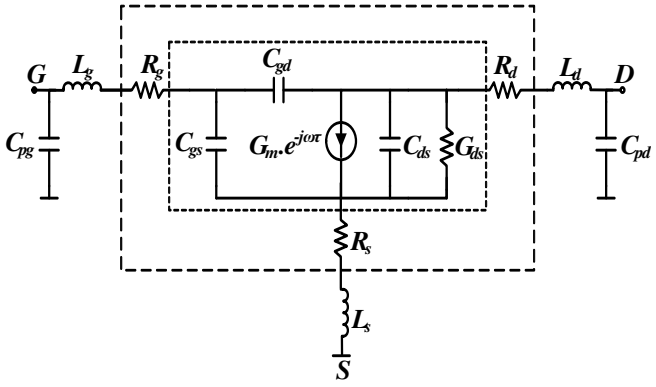


Fig. 3.40.: Small-signal equivalent circuit of a MOSFET including the effects of measurement pads.

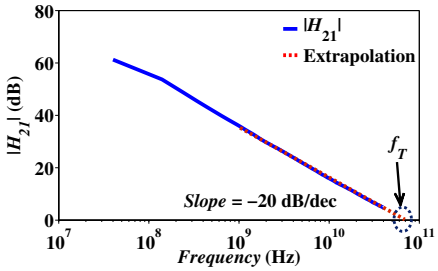


Fig. 3.41.: An illustration of the extraction of f_T from measured S-parameters after calculating the current gain $|H_{21}|$.

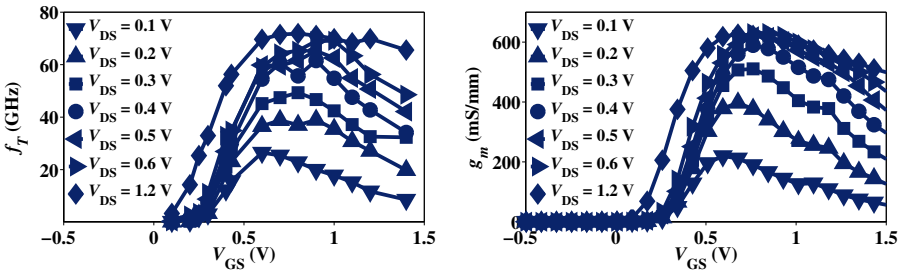
3.4.1.2 Maximum Oscillation Frequency $f_{\max}$

The maximum oscillation frequency is a very important figure of merit for the RF circuit designers. It is defined as the cutoff frequency of the unilateral gain ULG and can be expressed in terms of f_T as follows [16]:

$$f_{\max} = \frac{f_T}{2\sqrt{2\pi f_T R_{\mathrm{g}} C_{\mathrm{gd}} + G_{\mathrm{dsi}}\left(R_{\mathrm{g}} + R_{\mathrm{s}} + R_{\mathrm{gsi}}\right)}} \tag{3.27}$$

Hence, if f_T is independent of extrinsic resistances, $f_{\max}$ on the contrary is highly dependent on these resistances. Layout optimization techniques could highly enhance the performance of $f_{\max}$.

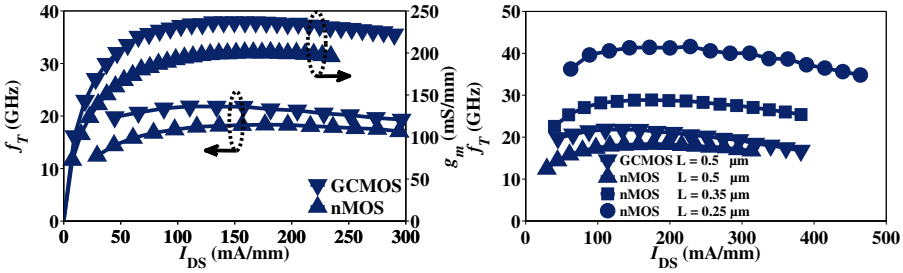
$f_{\max}$ is extracted using an extrapolation of ULG plotted as a function of frequency (the same idea as in the case of f_T). However, a slope of -20 dB/dec could not be easily found for the devices considered in this work, due to the high values of $f_{\max}$ and the limited frequency band of the measurement equipment (40 GHz). Therefore, for a fair comparison, the same slope of -30 dB/dec was fixed for the extraction of $f_{\max}$ for all devices. The extraction of $f_{\max}$ is shown



(a) Current gain cutoff frequency f_T as a function of V_{GS} and V_{DS}.

(b) DC transconductance g_m as a function of V_{GS} and V_{DS}.

Fig. 3.42.: Bias dependence of the current gain cutoff frequency f_T and the transconductance g_m for a FB DNW bulk device at room temperature.



(a) GCMOS and classical nMOS of 0.5 μm channel length.

(b) f_T for GCMOS and classical nMOS of different channel lengths.

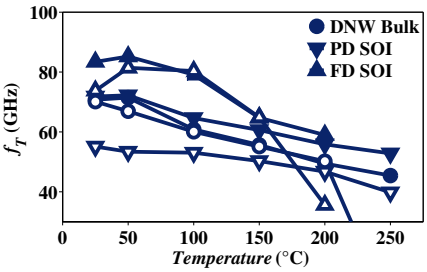
Fig. 3.43.: Current gain cutoff frequency for PD GCMOS and PD classical nMOS at $V_{DS} = 1.7$ V.

in Fig. 3.45 for the different devices considered in this work. A summary of the values of f_{max} as well as its variation with temperature is presented in Table 3.8.

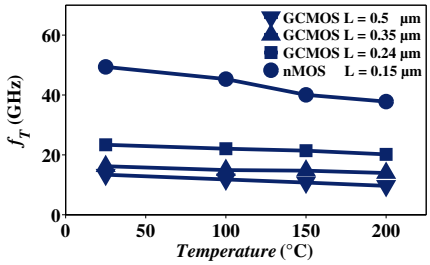
3.4.1.3 *Comments on Cutoff Frequencies*

The careful reading of Table 3.8 shows that:

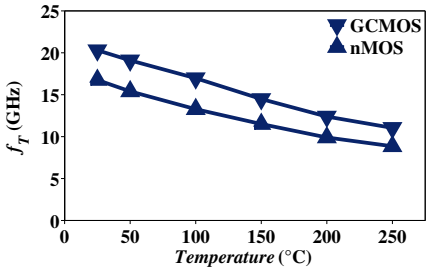
- The ratio f_{max}/f_T is almost 3 for FB devices and almost 2 for BT structures (except for FD SOI devices).
- DT structure in DNW bulk device shows a very reduced f_T value compared to DT structure of PD SOI device. This should be related to the gate capacitance and hence to the layout used. An optimization of the layout can help to enhance f_T of DT DNW bulk device.
- BT devices are mostly less sensitive to the variations in temperature, either for f_T or f_{max}. However, the absolute values of f_T and f_{max} for BT devices are lower than for FB devices. Nevertheless, the temperature stability helps



(a) FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



(b) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(c) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

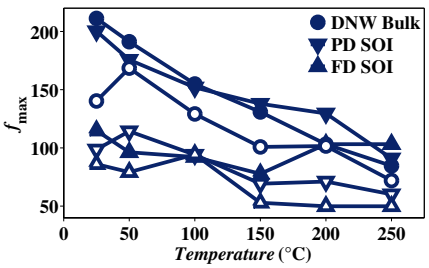
Fig. 3.44.: Variation of the maximum of f_T with temperature for the different devices studied in this work.

to keep the functionality of RF circuits using these devices up to high temperatures of operation.

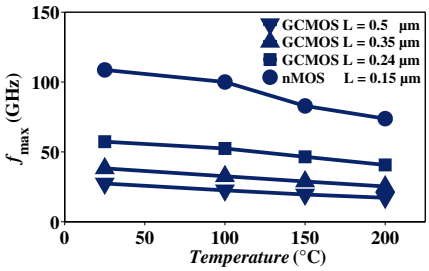
– Although GCMOS structure enhances the absolute values of f_T and $f_{\max}$ compared to the same drawn channel length of classical nMOS, it does not help to keep the thermal stability of these cutoff frequencies. GCMOS structures show higher sensitivity of f_T and $f_{\max}$ to temperature variation.

3.4.2 Extrinsic Resistances

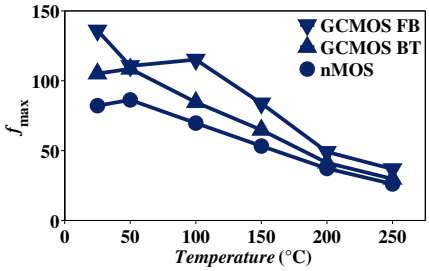
In Fig. 3.40, the dotted box differentiates between the intrinsic (inside) and extrinsic (outside) elements of a typical equivalent circuit for a MOSFET. The extraction of intrinsic elements from the measured S-parameters is very sensitive to the values of the extracted extrinsic resistances $R_{\rm g}$, $R_{\rm d}$, and $R_{\rm s}$. The extraction of these extrinsic resistances is achieved using the cold FET method proposed by Bracale *et al.* [40] and applying the $\omega^2\Re(Z_{\rm ij})$ versus ω^2 method proposed by G. Crupi *et al.* in [41] to minimize the frequency dependence of $\Re(Z_{\rm ij})$ associated to an incomplete capacitance de-embedding and/or intrinsic capacitive effects.



(a) FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



(b) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(c) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.45.: Variation of the maximum of $f_{\max}$ with temperature for the different devices studied in this work.

Fig. 3.46 to 3.48 show the results of the extraction. R_{d} and R_{s} are quite similar for FB and BT structures. However, the difference in the values between R_{d} and R_{s} is related to a slight asymmetry between the two sides of the transistor. Resistivity of doped silicon is calculated from [12]:

$$\rho(T) = \frac{1}{qN_A\mu_p(T)} \tag{3.28}$$

where $\mu_p(T)$ is the hole mobility as a function of temperature which can be calculated using Arora's mobility model [42]. For highly doped silicon (as in the case of source and drain regions), only a 25% increase in resistivity is obtained for the considered temperature range. In our case, the classical Bracale method, used to extract the extrinsic resistances, does not consider the mobility degradation. This produces an overestimation of R_{d} and R_{s} [43], giving the high percentages of increase shown in Fig. 3.46 to 3.48.

Table 3.9 presents a summary of the extracted values of R_{g}, R_{d}, and R_{s} at room temperature and its variation with temperature for the different devices.

Table 3.8.: Current gain cutoff frequency f_T and maximum oscillation frequency $f_{\max}$ in GHz of the different transistors at room temperature and their variation with temperature in GHz/^{o}C.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
f_T	70.8	70.1	24.9	71.8	55.1	62.2	83.4	73.8
$f_{\max}$	211.2	140.3	77.8	200.2	98.6	103.8	114.8	86
$f_{\max}/f_T$	2.98	2	3.12	2.79	1.79	1.67	1.37	1.17
Δf_T	−0.12	−0.11	−0.08	−0.092	−0.062	−0.09	−0.16	−0.08
$\Delta f_{\max}$	−0.56	−0.36	0.7	−0.42	−0.22	0.003	−0.02	−0.19

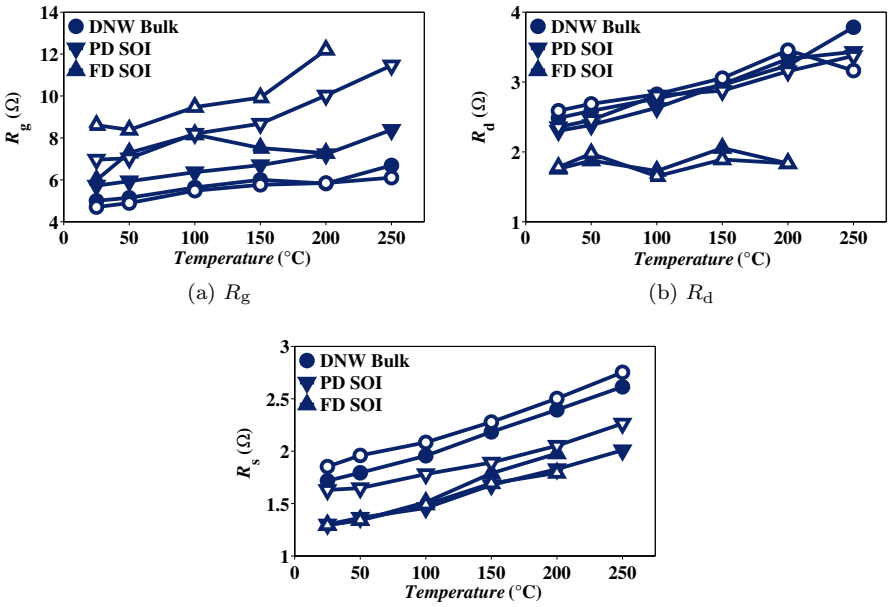
	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
f_T	49.4	23.4	16.2	13.4	16.8	20.3	17.3
$f_{\max}$	108.7	57.3	38.2	27.4	50.2	65.8	50.6
$f_{\max}/f_T$	2.2	2.45	2.36	2.04	2.99	3.2	2.92
Δf_T	−0.069	−0.018	−0.012	−0.02	−0.035	−0.042	−0.037
$\Delta f_{\max}$	−0.21	−0.096	−0.07	−0.06	−0.11	−0.14	−0.02

3.4.3 Intrinsic Elements

The values of extrinsic resistances extracted in the previous section are subtracted from the measured Z-parameters (Z_{ext}) to get the intrinsic Z-parameters (Z_{int}) using the following relation:

$$[Z_{\text{int}}] = [Z_{\text{ext}}] - \begin{bmatrix} R_{\text{g}} + R_{\text{s}} & R_{\text{s}} \\ R_{\text{s}} & R_{\text{d}} + R_{\text{s}} \end{bmatrix} \tag{3.29}$$

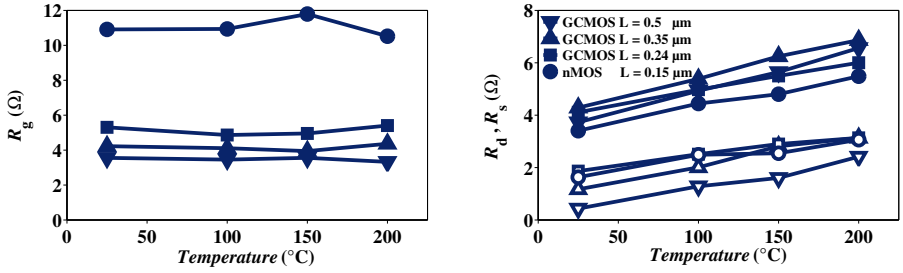
At this point, the reference plan is moved to the dotted box in Fig. 3.40. This represents the intrinsic part of the small-signal equivalent circuit of the MOSFET transistor. Besides the transconductance and the output conductance (presented in the next section), the intrinsic part contains three capacitances; C_{gs}, C_{gd}, and C_{ds}. It is of interest to extract these capacitances when the transistor is operated in the ON (inversion) and the OFF (depletion) states. This will give more insight for circuit designers.



(a) R_g (b) R_d

(c) R_s

Fig. 3.46.: Variation of the extrinsic resistances R_g, R_d, and R_s with temperature for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.

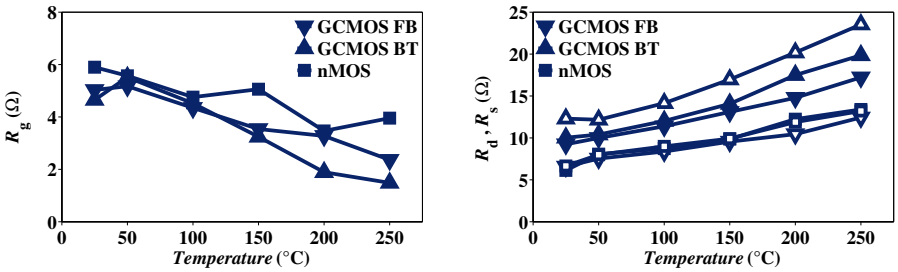


(a) R_g (b) R_d (solid) and R_s (empty)

Fig. 3.47.: Variation of the extrinsic resistances R_g, R_d, and R_s with temperature for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.

3.4.3.1 Capacitances in OFF State

To extract the capacitances in the OFF state, transistors are biased in deep depletion mode, i.e. negative values of V_{GS} and zero V_{DS}. The direct extraction method introduced by Raskin *et al.* in [44] is then applied. V_{GS} is set to -0.5



(a) R_g (b) R_d (solid) and R_s (empty)

Fig. 3.48.: Variation of the extrinsic resistances R_g, R_d, and R_s with temperature for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

V where the capacitances showed a minimum when traced as a function of V_{GS}. The results of the extraction are shown in Fig. 3.52 and Fig. 3.53. C_{gs} and C_{gd} in the OFF state contain the contribution of three capacitances, as shown in Fig. Fig. 3.49; the fringing capacitances, the overlap capacitances, and the body depletion capacitances. The later has a high sensitivity to temperature variation as it depends on the intrinsic carrier density n_i, which is sensitive to temperature changes as shown earlier in (3.6). This explains the variation of the capacitances in deep depletion with temperature as summarized in Table 3.10.

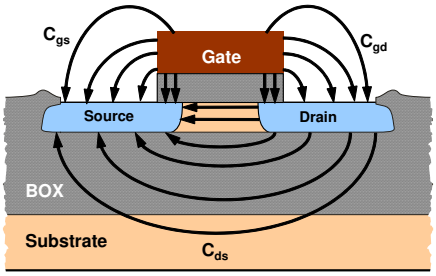


Fig. 3.49.: Capacitances in the OFF state.

Theoretically, C_{ds} in BT should be double that in FB, due to the absence of one of the two series capacitances because of the connection between the body and the source, as shown in Fig. 3.50. Fig. 3.53a shows that this is rather correct especially for PD SOI devices, as BT structures show nearly double the value of C_{ds} compared to the FB structures. On the other hand, FB structures show double the variation of C_{ds} with temperature compared to BT structures, as shown in Table 3.10, for the same reason; in a FB structure, two capacitors in series vary with temperature, while in a BT structure one of these series capacitances is removed.

Table 3.9.: Extrinsic resistances R_g, R_d, and R_s in Ω of different transistors at room temperature and their variation with temperature in mΩ/^{o}C.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
R_g	5	4.7	–	5.72	6.96	–	5.99	8.61
R_d	2.5	2.6	–	2.3	2.35	–	1.76	1.78
R_s	1.72	1.85	–	1.3	1.63	–	1.3	1.29
ΔR_g	7	6	—	1.1	20	—	5	20
ΔR_d	5	3	—	5	4	—	0.7	0.04
ΔR_s	4	4	—	3	3	—	4	3

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
R_g	10.9	5.31	4.23	3.56	5.9	5.03	4.65
R_d	3.41	4.11	4.29	3.73	6.1	9.2	10.03
R_s	1.63	1.87	1.17	0.43	6.65	6.6	12.3
ΔR_g	−0.3	0.3	0.2	−10	−10	−12	−18
ΔR_d	12	11	15	16	30	35	45
ΔR_s	7.7	7.4	12	11	28	24	52

This connection between the body and the source also affects the gate-source capacitance C_{gs}, where again it is higher in the case of BT structures as shown in Fig. 3.52, due to the metal connections which adds to C_{gs} and varies according to the layout implemented. Fig. 3.51 shows an illustration of the layout used in the case of the BT PD SOI device. Therefore, a good layout optimization technique can highly reduce this capacitance. It is worth mentioning here that the capacitance related to the body node in BT transistors is very small compared to capacitances related to metal layers connections. Values for extracted body node capacitances for the same technology used in this work (for the PD SOI case) were published by D. Lederer *et al.* in [45]. The layout variations also affect the amount of difference between C_{gs} and C_{gd} in the OFF state for the same transistor, whether FB or BT, thus affecting the theoretical symmetry of the transistor assumed at zero V_{DS}. Fig. 3.52 shows a small difference between C_{gs} and C_{gd} in the case of FB (nearly symmetric) whereas a large difference

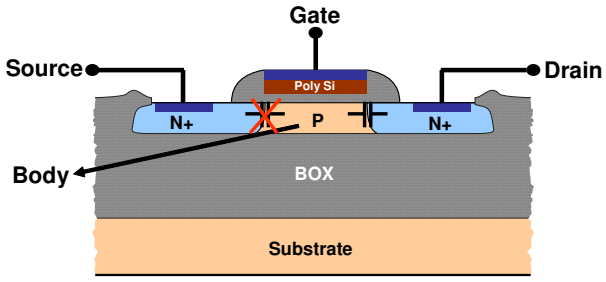


Fig. 3.50.: The difference in C_{ds} between FB and BT structures.

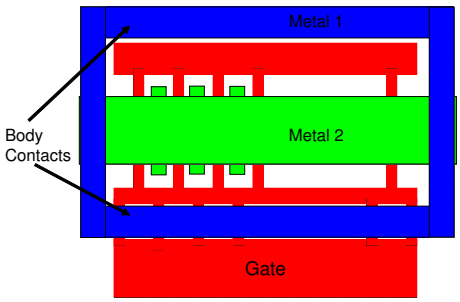


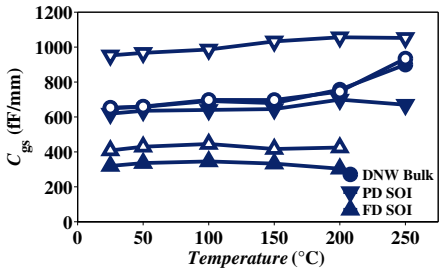
Fig. 3.51.: An illustration of the layout of the BT PD SOI showing the metal connections between the body and the source.

(nearly the double) is noticed in the case of BT PD SOI transistor. The layout was enhanced in the case of DNW bulk and FD SOI devices, and the result is a lower difference between C_{gs} and C_{gd} in the case of the BT structure as seen from Fig. 3.52 and Table 3.10.

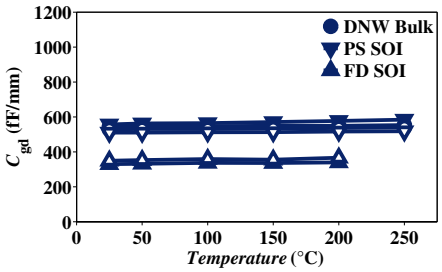
3.4.3.2 *Intrinsic Elements in ON State*

As in the case of the extraction of the capacitances in deep depletion, the extraction of the intrinsic elements in the ON state is performed using the intrinsic Z-parameters (Z_{int}) (obtained from (3.29)) and the direct extraction method [44] under saturation and strong inversion bias conditions; i.e. $V_{DS} = V_{GS} = V_{DD}$. The results of the extraction are shown in Fig. 3.54, Fig. 3.55, and Fig. 3.56. Variation of the intrinsic elements with temperature is given in Table 3.11.

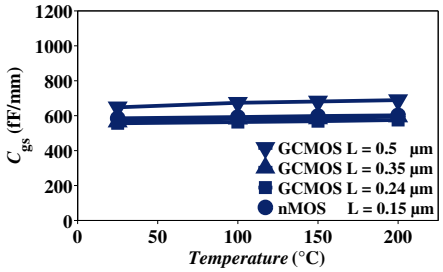
C_{gs} in the ON state shows higher values for BT structures compared to FB structures, for the same reason of metal connections explained in the previous section. Also a higher difference (compared to the OFF state case) between C_{gs} and C_{gd} for the same transistor due to the presence of the inversion layer in the saturation region, i.e. the transistor is no more symmetric. C_{gs} and C_{gd} show relatively stable behavior with temperature, as can be seen from Table 3.11, whereas C_{ds} shows higher degradation (increase) with temperature. This degra-



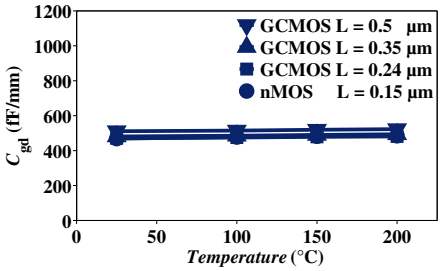
(a) OFF state C_{gs} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



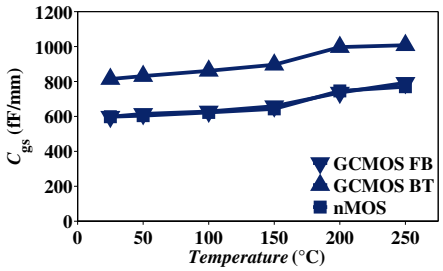
(b) OFF state C_{gd} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



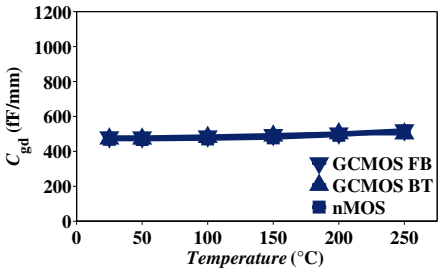
(c) OFF state C_{gs} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(d) OFF state C_{gd} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(e) OFF state C_{gs} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

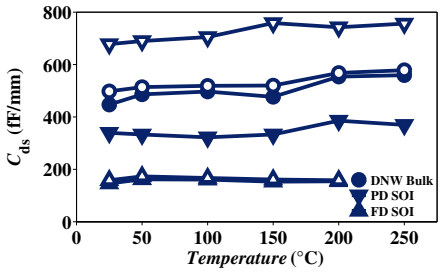


(f) OFF state C_{gd} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

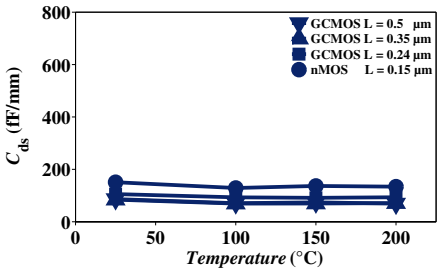
Fig. 3.52.: Variation of the OFF state capacitances C_{gs} and C_{gd} with temperature for the different devices studied in this work.

dation in C_{ds} is related to the increase in generation and recombination rates in the channel with temperature.

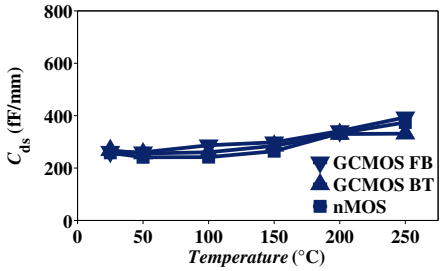
Intrinsic output conductance G_{dsi}, shows a relatively stable behavior with temperature, where BT structures show a higher increase than FB structures due to the suppression of the kink effect as explained in section 3.2.2. As a result,



(a) OFF state C_{ds} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



(b) OFF state C_{ds} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(c) OFF state C_{ds} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.53.: Variation of the OFF state capacitance C_{ds} with temperature for the different devices studied in this work.

both structures show stable output performance at high temperatures, hence the matching with next stages is not affected by the increase in temperature.

Intrinsic transconductance G_{mi}, on the other hand, shows some degradation with temperature. This is explained by the degradation of the surface mobility with temperature, an effect that has been measured and modeled by Reichert *et al.* [46]. The intrinsic transconductance G_{mi} is extracted from the intrinsic Z-parameters (Z_{int}) in the saturation region, thus away from the ZTC point of g_m and also from the maximum value of g_m. Therefore, this degradation will directly affect the intrinsic gain of the transistor at elevated temperatures.

3.5 CONCLUSION

An extensive characterization has been presented in this chapter. The devices considered in this work have been characterized in dc, ac, and RF both at room temperature and at high temperatures. At each step, a detailed comparison has been held between the different technologies and the different device structures. These comparisons are to be used in the next chapters to help explain certain

Table 3.10.: OFF state capacitances C_{gs}, C_{gd}, and C_{ds} in fF/mm of the different transistors at room temperature and their variation with temperature in fF/mm/^{o}C.

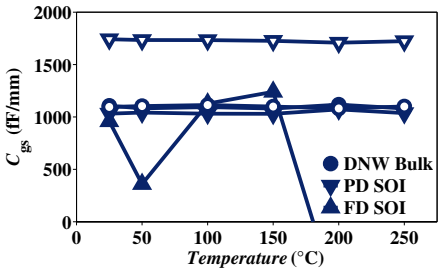
	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
C_{gs}	649.7	653.3	–	618.9	952.3	–	319.4	408.3
C_{gd}	543.6	529.2	–	557	510.3	–	329.6	349.4
C_{ds}	447	497.9	–	339.5	677.9	–	146	158.5
ΔC_{gs}	0.96	1.04	–	0.28	0.5	–	−0.09	0.03
ΔC_{gd}	0.03	0.045	–	0.11	0.036	–	0.054	0.08
ΔC_{ds}	0.45	0.35	–	0.21	0.37	–	0.008	−0.036

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
C_{gs}	584.8	556.4	566.1	647.8	598.2	598.2	813.9
C_{gd}	568.6	470.2	481	510.9	468.7	481.4	472.1
C_{ds}	150.9	105.6	84.26	86.34	258.1	262.4	268.1
ΔC_{gs}	0.1	0.11	0.16	0.23	0.81	0.85	0.93
ΔC_{gd}	0.09	0.064	0.073	0.07	0.2	0.17	0.18
ΔC_{ds}	−0.08	−0.07	−0.07	−0.09	0.56	0.57	0.36

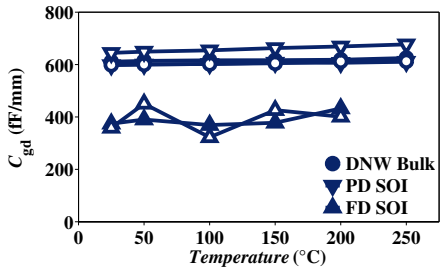
phenomena and to provide the basis for new approaches in dealing with these devices under different conditions.

A highlight of the most important results obtained throughout this chapter is given hereafter:

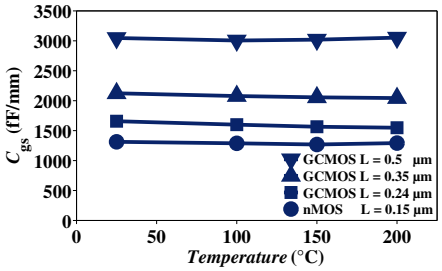
- Due to the variety of technologies and structures used in this work, a difference is noticed in threshold voltages of the different devices. This difference is taken into account in all representations of figures of merit by tracing them as a function of normalized drain current or gate overdrive voltage.
- The behavior of the threshold voltage with increasing temperature varies significantly from technology to technology and from structure to structure. The FB DNW bulk device shows the lowest variation in threshold voltage



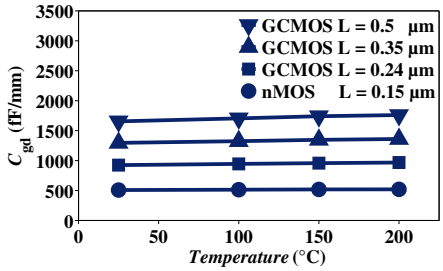
(a) ON state C_{gs} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



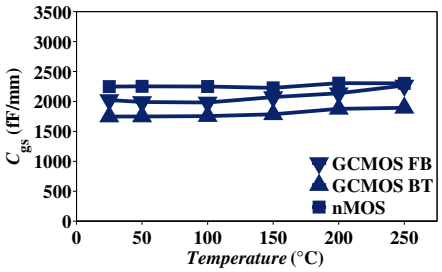
(b) ON state C_{gd} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



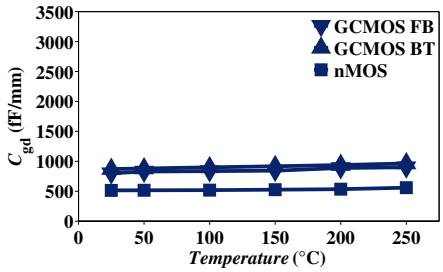
(c) ON state C_{gs} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(d) ON state C_{gd} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(e) ON state C_{gs} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

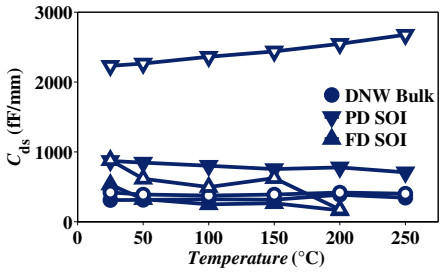


(f) ON state C_{gd} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

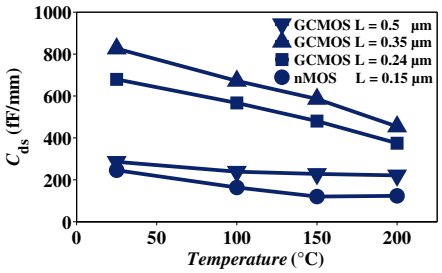
Fig. 3.54.: Variation of the ON state capacitances C_{gs} and C_{gd} with temperature for the different devices studied in this work.

with temperature. PD GCMOS shows a lower variation in V_T than the corresponding classical nMOS. In general, FB structures show less variation in V_T than BT structures.

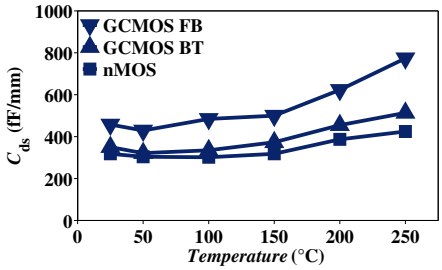
– DNW bulk devices are shown to be a good mimic of SOI devices. The DNW gives the possibility to fabricate FB and BT structures on a bulk



(a) ON state C_{ds} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



(b) ON state C_{ds} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



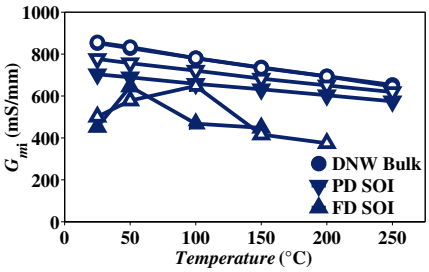
(c) ON state C_{ds} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.55.: Variation of the ON state capacitance C_{ds} with temperature for the different devices studied in this work.

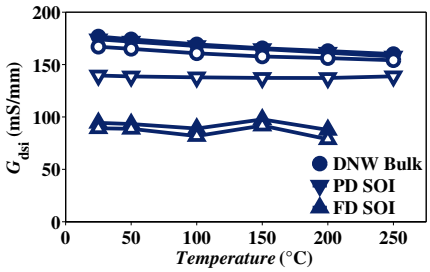
technology. They even feature floating-body effects represented by the kink effect shown on the output conductance.

– The variation of the subthreshold slope with temperature is shown to be very similar between the different devices, except for the DT devices which show a significant stability with temperature.
– The ratio of ON to OFF current I_{ON}-to-I_{OFF} cannot be used in a direct comparison between devices due to the difference in threshold voltage, but as an indication of the capabilities of different technologies and structures. Another measure is introduced which is the leakage current I_{Leakage} calculated at the lowest current that can be delivered by the transistor. The DNW bulk devices show an impressive performance that is even better than the PD SOI devices, especially for the FB structure. Nevertheless, the FD devices present the lowest leakage current with the BT structure showing good stability with temperature.

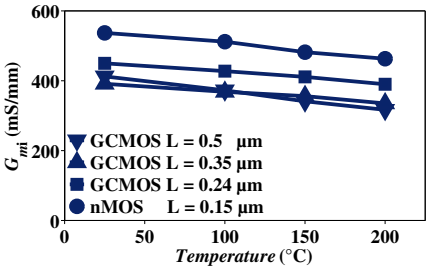
– Using the DNW technique, it is possible to define a ZTC point till 250^{o}C for bulk devices. As for the PD SOI devices, the BT structure shows an advantage with respect to the FB structure by featuring higher ZTC points



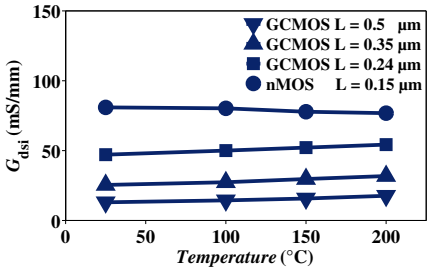
(a) Intrinsic G_{mi} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



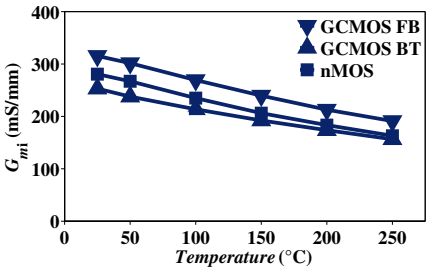
(b) Intrinsic G_{dsi} for FB (solid symbols) and BT (empty symbols) structures of DNW bulk, PD SOI, and FD SOI devices.



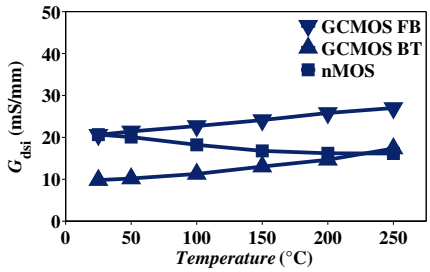
(c) Intrinsic G_{mi} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(d) Intrinsic G_{dsi} for FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.



(e) Intrinsic G_{mi} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.



(f) Intrinsic G_{dsi} for PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 3.56.: Variation of the intrinsic G_{mi} and G_{dsi} with temperature for the different devices studied in this work.

which makes it easier to benefit from a higher drive current and transconductance when operating the device at ZTC points. However, this same advantage could turn to be a disadvantage if low voltage low power operation is considered.

Table 3.11.: ON state intrinsic capacitances $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ in fF/mm and the intrinsic transconductance $G_{m\rm i}$ and the intrinsic output conductance $G_{\rm dsi}$ in mS/mm of the different transistors at room temperature and their variation with temperature in fF/mm/^{o}C and mS/mm/^{o}C, respectively.

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
$N_{\rm finger}$	30	30	30	30	30	30	48	48
$C_{\rm gs}$	1107	1096	–	1032	1742	–	958.9	–
$C_{\rm gd}$	610.9	598.9	–	597.8	644.4	–	374.4	358.6
$C_{\rm ds}$	310.2	419.2	–	870.6	2232	–	532.5	880.9
$G_{m\rm i}$	852.3	855.9	–	703.7	776.8	–	452.1	500.8
$G_{\rm dsi}$	176.8	167	–	174	139.6	–	94.36	89.2
$\Delta C_{\rm gs}$	−0.015	−0.04	–	0.07	−0.12	–	−5.9	–
$\Delta C_{\rm gd}$	0.05	0.066	–	0.055	0.14	–	0.24	0.11
$\Delta C_{\rm ds}$	0.24	0.02	–	−0.65	1.95	–	−1.67	−3
$\Delta G_{m\rm i}$	−0.89	−0.93	–	−0.57	−0.7	–	−0.65	−1
$\Delta G_{\rm dsi}$	−0.07	−0.057	–	−0.07	−0.005	–	−0.02	−0.04

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
$N_{\rm finger}$	32	48	48	48	12	12	12
$C_{\rm gs}$	1313	1658	2124	3047	2248	2023	1748
$C_{\rm gd}$	507.6	924.5	1295	1655	514.7	800.5	871.2
$C_{\rm ds}$	245.8	679.3	826.2	285.8	318.1	457.7	350.2
$G_{m\rm i}$	537	449.9	391.3	412.4	280.6	315.4	253.1
$G_{\rm dsi}$	80.92	47.09	25.42	12.99	20.65	20.61	9.807
$\Delta C_{\rm gs}$	−0.16	−0.64	−0.47	0.023	0.26	1.1	0.7
$\Delta C_{\rm gd}$	0.072	0.25	0.38	0.62	0.18	0.42	0.4
$\Delta C_{\rm ds}$	−0.74	−1.73	−2.08	−0.369	0.51	1.37	0.8
$\Delta G_{m\rm i}$	−0.43	−0.34	−0.31	−0.55	−0.53	−0.56	−0.43
$\Delta G_{\rm dsi}$	−0.025	0.04	0.037	0.026	−0.02	0.029	0.033

– For ac operation, the transconductance to drain current ratio $g_m/I_{\rm DS}$ of the DNW bulk devices is quite comparable to that of the PD SOI devices. The GCMOS devices, on the other hand, are not capable to compete with the classical nMOS except for the strong inversion regime of operation.

Temperature has a double effect on g_m/I_{DS} since it reduces the peak value and pushes its place on the I_{DS} axis further. This double effect could be undesirable for the correct operation of analog circuits.

- The BT structure of the PD SOI shows interesting high values of Early voltage outperforming all other devices. Yet, it shows the highest degradation with temperature.
- The two main figures of merit for RF performance, f_T and $f_{\max}$, are presented and also their variation with temperature. BT structures show more stable behavior than FB structure, but FB structures show higher values of f_T and $f_{\max}$. GCMOS devices outperform classical nMOS devices but they loose when stability with temperature is considered.
- The extraction of the small-signal equivalent circuit is helpful to understand the behavior of the different devices in RF. Extrinsic resistances are extracted at different temperatures then the intrinsic elements values are extracted in different operation regimes and at different temperatures. These values serve to explain the behavior of f_T and $f_{\max}$. They will also serve in understanding phenomena to be presented in the next chapters.

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CHAPTER 4

LOW VOLTAGE LOW POWER CHARACTERIZATION

The debate on the future of the semiconductor market continues between the supporters of the Bulk-Si technology and the Silicon-on-Insulator (SOI) technology. With a history of more than 30 years in both technology and circuit design, Bulk-Si is believed to continue as the mainstream of the semiconductor market. Currently, only 4–5% of all the wafers produced worldwide are SOI, or more specifically, 8% of the 300 mm logic wafer market is SOI [1]. However, as the technology continues to scale down beyond 45 nm, it is believed that the variability and complexity would be a difficult barrier for Bulk-Si technology [2]. On the other hand, SOI provides less process complexity and variability, lower power (30–40% lower power or higher performance), higher reliability (10x soft error rate reduction with no latch up) [2]. Moreover, the high cost, which is the main obstacle for SOI, is believed to go down while the cost of Bulk-Si goes up (due to complexity issues) until the crossover is believed to take place at 32 or 22 nm technology nodes [2].

SOI merits many advantages over Bulk-Si such as higher I_{ON}-to-I_{OFF} ratio, lower leakage current, lower parasitic capacitances, radiation hardness, and higher immunity to latch-up problems (due to the presence of the buried oxide layer BOX). These advantages put the SOI ahead for high speed applications and also for Low-Voltage Low-Power (LVLP) applications [3]. LVLP electronics is gaining more grounds due to the fast growing market of wireless communi-

cation devices which require portability and reliability and above all extended battery lifetime [4].

As for high temperature performance, SOI can function correctly up to 300°C while bulk devices fail beyond 180°C due to leakage current [5]. On the other hand, the presence of the BOX leads to less thermal conductivity (due to poor thermal coefficient of SiO_2), hence higher temperatures inside the channel leading to self-heating effects. Other effects also limit the performance of SOI devices like the floating body effect [5].

Although the high temperature characteristics of SOI devices operating in RF regime is very important for modern wireless communication applications as mentioned above, especially when combined with Low-Voltage Low-Power operation, this type of study is rarely addressed in literature [6–8]. On the other hand, the dc LVLP characteristics is well covered in literature, however, in order to cover the high temperature RF LVLP regime of operation, a dc study is indispensable.

LVLP applications could be divided into two main categories, the first concerns the applications where a relatively high drive current is required whereas the second is strictly concerned by extremely low power consumption criteria. In both cases, the best possible performance of the device is required. As far as the RF applications are concerned, the switching speed is on top of the priorities list of high performance. In order to fulfill the requirement of high drive current in the first category, operation above threshold voltage is needed. On the other hand, the second category is most fitted in near- or sub-threshold operation style. In the next two sections the two categories are addressed in detail.

4.1 ABOVE THRESHOLD OPERATION

In this operation mode, a device is operated at the threshold voltage or slightly above it. The idea is to limit the consumed power to its minimum while generating a relatively high drive current. In a first step, a room temperature characterization is performed (although a real device is rarely operated at room temperature due to the presence of other circuits and devices in the proximity which result in an elevated temperature environment). Afterwards, based on a good understanding of LVLP operation, a high temperature characterization is presented.

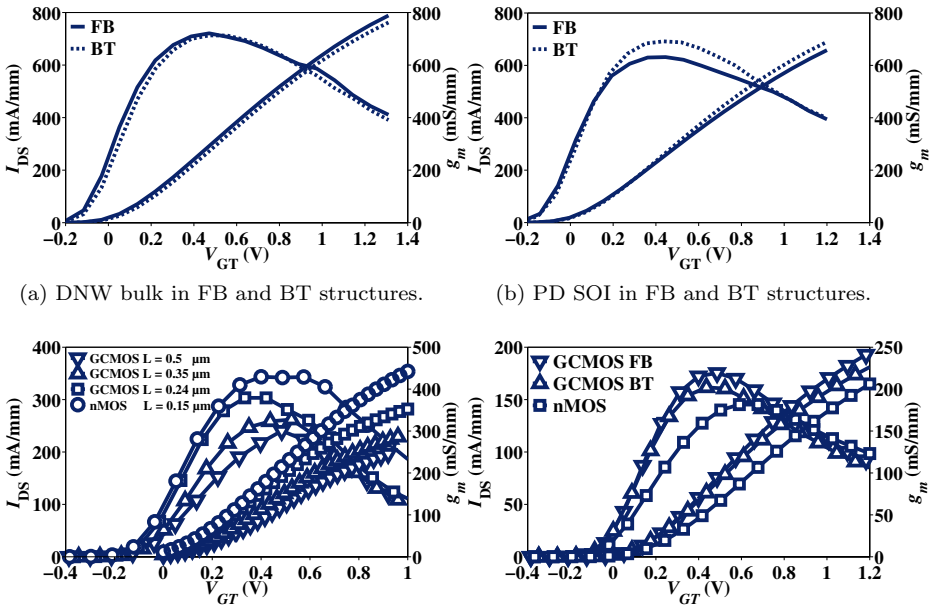
4.1.1 At Room Temperature

The devices considered in this work have been presented in chapter 3 in saturation region, i.e. when $V_{DS} = V_{DD}$. This behavior is significantly changed when operating the device at or near V_T.

A key parameter in the performance of the device in LVLP above V_T is the behavior of its g_m, all along while tracking its drive current and power consumption. Fig. 4.1 shows the behavior of the drive current and the dc transconductance of the DNW bulk devices and the PD SOI devices as a function of the gate volt-

age overdrive $V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_T$. The interesting characteristic to notice in this figure is the position of the maximum transconductance $g_{m,\max}$ with respect to V_{GT} (see Table 4.1). The lower the value of V_{GT} at which $g_{m,\max}$ occurs, the more adequate this device to a LVLP operation. A low value of V_{GT} means a better performance at a lower bias point, hence a lower dc power consumption (see Table 4.1). In general, GCMOS devices, whether in PD or FD technologies, show a better behavior compared to their corresponding classical nMOS devices. They feature their maximum transconductance at lower V_{GT} with lower dc power consumption.

It should be noticed that a trade-off between performance and dc power consumption is unavoidable. Operating the device at its maximum performance results in high power consumption whereas operating the device at an acceptable performance but with significantly reduced power consumption is still doable as can be seen from the plot of the maximum g_m and the dc power consumption P_{dc} as a function of the drain bias V_{DS} in Fig. 4.2. The choice of the appropriate drain bias V_{DS} for a certain design or application depends on the required performance and the constraints on the power consumption.



(a) DNW bulk in FB and BT structures.

(b) PD SOI in FB and BT structures.

(c) FD GCMOS with 48 fingers and nMOS of 32 fingers, of 2.5 μm width each and different channel lengths.

(d) PD GCMOS and classical nMOS of 0.5 μm channel lengths.

Fig. 4.1.: Transfer characteristics I_{DS}-V_{GS} and dc transconductance g_m as a function of gate voltage overdrive V_{GT} at room temperature and $V_{\mathrm{DS}} = 0.6$ V.

Table 4.1.: The value of the maximum g_m (mS/mm) at room temperature (at $V_{\mathrm{DS}} = 0.6$ V) and its position on the V_{GT} (V) axis along with the corresponding dc power consumption P_{dc} (mW/mm).

	DNW Bulk			PD SOI			FD SOI	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
$g_{m,\max}$	720.8	712.8	—	691.7	631.6	—	350	350
V_{GT}	0.47	0.47	—	0.44	0.45	—	0.5	0.5
P_{dc}	175	163.1	—	152.6	161.4	—	97.7	98.2

	FD				PD		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
$g_{m,\max}$	429.4	379.2	327.4	300.5	181.6	219.3	202.1
V_{GT}	0.4	0.33	0.52	0.48	0.68	0.49	0.44
P_{dc}	81.1	57.3	77.3	56.8	51.2	45.2	36.7

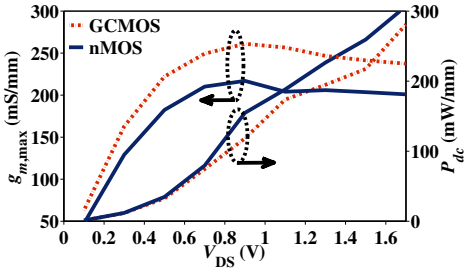
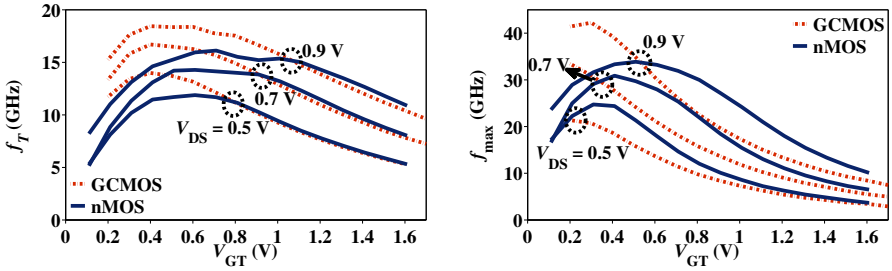


Fig. 4.2.: The maximum of dc transconductance $g_{m,\max}$ and the corresponding dc power consumption P_{dc} as a function of the drain bias V_{DS} for PD GCMOS and classical nMOS of $L = 0.5$ μm.

A case study is taken to show how a different choice of V_{DS} can importantly affect the performance of a device, especially in RF. In this case study, the PD GCMOS and the PD classical nMOS (both of 0.5 μm drawn channel length and both are in FB structure) are compared [9].

As shown earlier, in Fig. 4.1d and Table 4.1, the maximum of dc transconductance $g_{m,\max}$ of the GCMOS device occurs at a V_{GT} value of approximately 190 mV lower than the case of the classical nMOS device. Hence, a better dc

and RF[1] performance at a lower gate bias and a lower dc power consumption. The higher g_m occurring at a lower V_{GT} is directly translated into optimized current gain cutoff frequency f_T which is shown to present its maximum at a lower V_{GT} for the GCMOS device compared to the classical nMOS device (Fig. 4.3a) at $V_{DS} = 0.5$ V. On the other hand, the maximum oscillation frequency f_{max} is shown to be lower for GCMOS compared to classical nMOS at $V_{DS} = 0.5$ V as shown in Fig. 4.3b. Nevertheless, the maximum of f_{max} occurs at a lower V_{GT} for GCMOS compared to classical nMOS, which favours again the LVLP performance of the GCMOS.



(a) Current gain cutoff frequency at room temperature and $V_{DS} = 0.5$, 0.7, and 0.9 V.

(b) Maximum oscillation frequency at room temperature and $V_{DS} = 0.5$, 0.7, and 0.9 V.

Fig. 4.3.: PD GCMOS and classical nMOS of 0.5 μm channel lengths and FB structures.

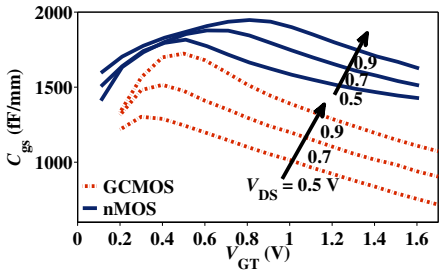
The explanation of the behavior of f_T and f_{max} is achieved through the extraction of the parameters of a small-signal equivalent circuit using [10, 11] for the extrinsic resistances and using [12] for the intrinsic elements. GCMOS presents a lower C_{gs} (Fig. 4.4a) and a higher C_{gd} (Fig. 4.4b) compared to nMOS. These two capacitances nearly compensate to give a comparable total gate capacitance C_{gg} (Fig. 4.4c), while the intrinsic transconductance G_{mi} is in favor of GCMOS (Fig. 4.4d). As a result GCMOS outperforms nMOS in f_T behavior since $f_T = \dfrac{G_{mi}}{2\pi C_{gg}}$ (see section 3.4.1.1).

The higher C_{gd} of GCMOS is explained by the fact that the lightly doped region near the drain is in strong inversion but not yet in pinch-off at this low V_{DS} value [13]. The non pinched-off channel also results in higher G_{dsi} for GCMOS compared to nMOS (Fig. 4.4e). Therefore, the higher f_{max} of GCMOS can be explained using (3.27) (see section 3.4.1.2).

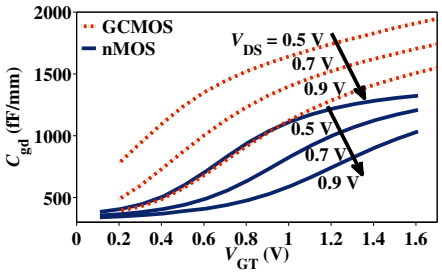
As V_{DS} increases, the pinch-off region is created near the drain in the GCMOS. As a result, C_{gd} decreases to reach a value near that of nMOS (Fig. 4.4b). The same applies for G_{dsi} where the difference between GCMOS and nMOS is clearly decreased (Fig. 4.4e). This transition starts to happen at $V_{DS} = 0.7$ V and is

[1]Notice that the current gain cutoff frequency is related to g_m through: $f_T = \dfrac{g_m}{2\pi(C_{gs} + C_{gd})}$

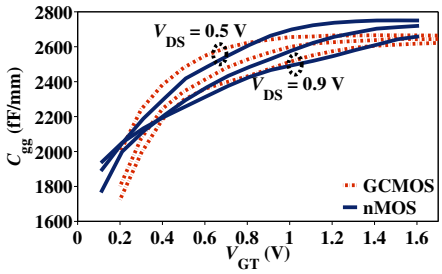
highly manifested at higher values of V_{DS} as can be seen from the intersection point in f_T and $f_{\max}$ curves (Fig. 4.3) which goes to higher V_{GT} as V_{DS} increases.



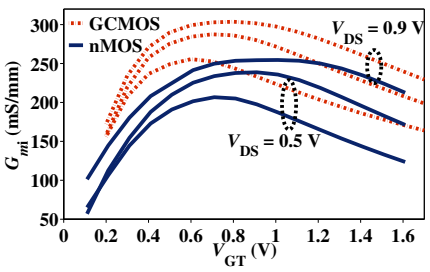
(a) Gate-to-source capaciatnce C_{gs}.



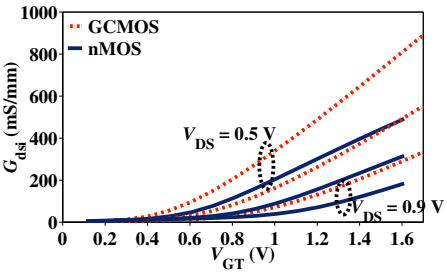
(b) Gate-to-drain capaciatnce C_{gd}.



(c) Total gate capaciatnce $C_{\mathrm{gg}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$.



(d) Intrinsic transconductance G_{mi}.



(e) Intrinsic output conductance G_{dsi}.

Fig. 4.4.: Intrinsic elements of a PD GCMOS and a classical nMOS of 0.5 μm channel lengths and FB structures at room temperature and $V_{\mathrm{DS}} = 0.5, 0.7,$ and 0.9 V.

4.1.2 At High Temperatures

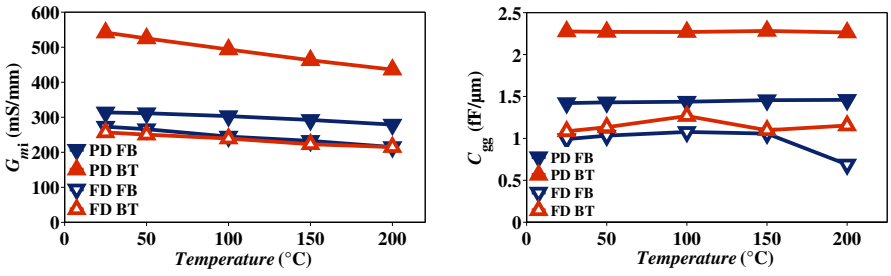
For applications operating at a bias near or slightly above V_T (for the sake of relatively high drive current), a very interesting bias point is the ZTC_{IDS} presented in section 3.2.7. It has been shown in Table 3.6 that the ZTC_{IDS} always lies above V_T with a slight difference ranging between 0.1 and 0.25 V

(with some exceptions where ZTC_{IDS} lies just below V_T). Operating the device at ZTC_{IDS} is very beneficial for above threshold LVLP applications since it guarantees a constant drive current and constant dc power consumption with increasing temperature. At the same time, a slight variation in transconductance g_m, and hence in f_T, is assured since the ZTC_{IDS} point is not far from the ZTC_{gm} point where g_m is constant with temperature. All these characteristics should be clarified using a case study in which the SOI devices (both in PD and FD technologies and in FB and BT structures) are considered.

In Table 4.2, the values of ZTC_{IDS} points at $V_{\rm DS} = 0.6$ V and the values of V_T in saturation are listed. The values of ZTC_{IDS} at $V_{\rm DS} = 0.6$ V differ from the values presented in section 3.2.7 where $V_{\rm DS}$ is taken at $V_{\rm DD}$. In this case study, $V_{\rm DS}$ is chosen to be 0.6 V to assure an operation in saturation region while keeping a LVLP scheme. A parameter extraction of the small-signal equivalent circuit is performed. The extracted intrinsic transconductance $G_{m\rm i}$ and the intrinsic total gate capacitance $C_{\rm gg}$ as they vary with temperature are shown in Fig. 4.5. Very stable behavior for $C_{\rm gg}$ can be noticed, while $G_{m\rm i}$ shows a variation with temperature since the devices are not biased at ZTC_{gm}.

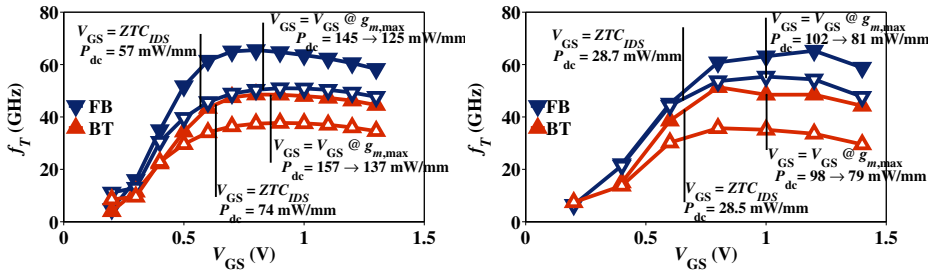
Fig. 4.6 shows the variation of f_T with $V_{\rm GS}$ at 25^{o}C and 200^{o}C. Two bias points are marked up, ZTC_{IDS} and $g_{m,\rm max}$ points. DC power consumption P_{dc} at each point is given, knowing that P_{dc} varies with temperature when $I_{\rm DS}$ varies with temperature. Therefore, only one value of P_{dc} is given in Fig. 4.6 at ZTC_{IDS} point where $I_{\rm DS}$ is constant with temperature.

It can be seen from Fig. 4.6 and Table 4.2, that operating a device at $V_{\rm GS} = ZTC_{IDS}$ ensures a LVLP operation scheme (57 and 74 mW/mm for FB and BT PD devices and 28.7 and 28.5 mW/mm for FB and BT FD devices, respectively) while keeping the variation in f_T very small as shown in Table 4.2. On the other hand, operating the device at $g_{m,\rm max}$ condition, in order to achieve maximum f_T, results in higher dc power consumption and higher variation in f_T with temperature (conf. values given in Fig. 4.6 and Table 4.2: Higher P_{dc} values



(a) Intrinsic transconductance $G_{m\rm i}$. (b) Total gate capaciatnce $C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$.

Fig. 4.5.: Intrinsic transconductance and total gate capacitance of PD and FD SOI devices in FB and BT structures as they vary with temperature at $V_{\rm DS} = 0.6$ V and $V_{\rm GS} = ZTC_{IDS}$.



(a) PD (b) FD

Fig. 4.6.: f_T variation with V_{GS} at 25^{o}C (solid symbols) and 200^{o}C (empty symbols) for PD and FD devices in FB and BT structures and the difference between ZTC_{IDS} and $g_{m,\max}$ bias points.

are at 25^{o}C and lower P_{dc} values are at 200^{o}C). FD devices show very low P_{dc} at ZTC_{IDS} compared to corresponding values of PD devices. Also the ratio between P_{dc} at $g_{m,\max}$ condition and that at ZTC_{IDS} condition is nearly 2 in PD devices whereas it is nearly 3 in FD devices, showing the advantage of FD devices at ZTC_{IDS} bias point.

A similar study could be held for the other devices studied in this work. Table 4.2 presents the details needed for such a study. For example, DNW bulk devices are seen to consume more power than PD SOI devices at the $g_{m,\max}$ condition (knowing that they are both fabricated using the same technology but different wafers). Nevertheless, DNW bulk devices show an interesting lower power consumption at the ZTC_{IDS} condition while keeping a lower f_T variation with temperature. This promotes them as a better choice than the PD SOI devices for LVLP high drive current applications.

The PD SOI GCMOS devices (which are fabricated on a different technology than the one presented above) consume more power at ZTC_{IDS} than classical nMOS devices since they are characterized by delivering more current.

4.2 SUB-THRESHOLD OPERATION

In the previous section, the advantage of operating the transistors at the ZTC_{IDS} point was demonstrated. However, for applications that need a precise frequency of operation, especially as temperature increases, an operation at the ZTC_{gm} point is more interesting. This scheme of operation is significantly interesting for the following reasons:

- The transconductance g_m is constant, hence f_T is also constant with increasing the temperature.
- ZTC_{gm} point usually lies below V_T which is more adequate for LVLP subthreshold applications.

Table 4.2.: LVLP RF behavior of different transistors at $V_{\mathrm{DS}} = 0.6$ V and the variation of f_T between room temperature and 200^{o}C in GHz/^{o}C. P_{dc} is also shown at 25 and 200^{o}C in mW/mm.

	DNW Bulk		PD SOI		FD SOI		PD		
	FB	BT	FB	BT	FB	BT	nMOS	FB GC	BT GC
L (μm)	0.13	0.13	0.13	0.13	0.15	0.15	0.5	0.5	0.5
W (μm)	2	2	2	2	5	5	3.3	3.3	3.3
N_{finger}	30	30	30	30	48	48	12	12	12
ZTC_{IDS} (V)	0.46	0.52	0.58	0.64	0.65	0.66	0.72	0.69	0.79
V_T (V)	0.22	0.3	0.29	0.4	0.35	0.36	0.48	0.53	0.63
$ZTC_{IDS} - V_T$	0.24	0.22	0.29	0.24	0.3	0.3	0.24	0.16	0.16
V_{GS} @ $g_{m,\mathrm{max}}$ (V)	0.76	0.79	0.83	0.85	1	1	1.4	1.1	1.1
Δf_T @ ZTC_{IDS}	−0.066	−0.09	−0.082	−0.073	−0.075	−0.04	−0.011	−0.031	−0.02
P_{dc} @ ZTC_{IDS}	52.79	65.76	57.14	73.98	28.7	28.5	8.86	15.1	13.96
Δf_T @ $g_{m,\mathrm{max}}$	−0.12	−0.11	−0.092	−0.08	−0.11	−0.12	−0.03	−0.038	−0.03
P_{dc} @ $g_{m,\mathrm{max}}$ (25^{o}C)	174.4	175.4	148.9	157.3	102.1	98.2	77.1	66.4	43.6
P_{dc} @ $g_{m,\mathrm{max}}$ (200^{o}C)	138.1	144.8	125	136.8	81.4	79	50.2	45.9	31.7

– Since ZTC_{IDS} lies above ZTC_{gm}, operating the transistor at ZTC_{gm} has an extra advantage, the driving current increases with increasing temperature. Although this increase is very small, since ZTC_{IDS} point is very close, it guarantees that the amount of the required drive current (imposed by the designer at room temperature) is always available even at higher temperatures.

This last advantage point could be extended to an even better mode of operation, where the disadvantages of high temperature environment could be turned into an advantage. This could be achieved by operating the transistor at a gate bias below the ZTC_{gm} point. Under this condition, the transconductance, and hence the cutoff frequency, as well as the drive current, all increase as temperature increases. In other words, the increase of temperature enhances the performance of the transistor in contrary to what is traditionally known of the undesired effects of high temperatures [14].

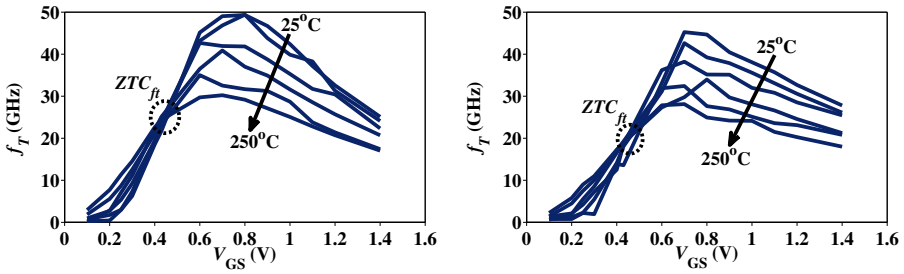
4.2.1 Operation below ZTC_{gm}

The choice of the bias point for a successful design of a sub-ZTC_{gm} operation scheme is crucial. V_{GS} should be correctly chosen to put the device in a region where it is functioning and at the same time well below ZTC_{gm} to benefit from the increasing feature of g_m and I_{DS} with temperature. This will also ensure an increasing behavior of f_T with temperature. On the other hand, a careful choice of V_{DS} should be made in order to meet the specifications of the design for the amount of consumed power and the minimum cutoff frequency needed for the operation of the circuit.

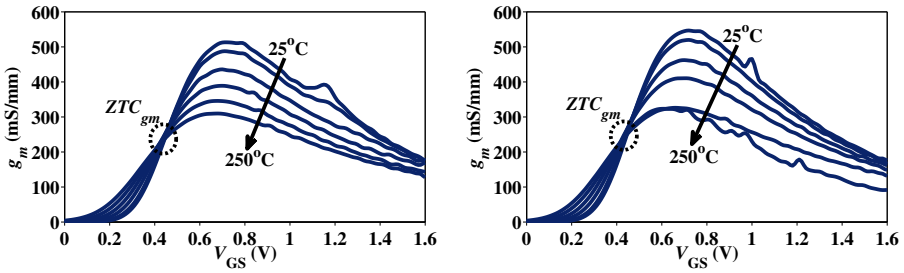
For the choice of V_{GS}, Fig. 4.7 shows that a ZTC point also exists for the current gain cutoff frequency f_T (to be referred to as ZTC_{ft}) which coincides approximately with the ZTC_{gm} point. The choice of V_{GS} could be made based on this graph (Fig. 4.7). A simple rule of thumb is to fix V_{GS} at a value less than ZTC_{gm} by $\cong 100$ mV. In the case study to be considered here (PD SOI devices in both FB and BT structures), V_{GS} is fixed at 0.3 V.

As for V_{DS}, Fig. 4.8 shows the effect of increasing V_{DS} on the value of f_T and the amount of power consumed. In this case study, V_{DS} is taken to be 0.3 V, knowing that this choice limits the cutoff frequency of the circuit but it drastically reduces the amount of power consumed by at least two orders of magnitude compared to the case where V_{DS} and V_{GS} are set to V_{DD} as shown in Fig. 4.9d.

Fig. 4.9a shows the two cutoff frequencies f_T and $f_{\max}$ as they vary with temperature at this temperature favored bias scheme, $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.3$ V, whereas Fig. 4.9b shows it at $V_{\mathrm{DS}} = 0.6$ V for comparison. The traditional "degradation" behavior with temperature (see Fig. 4.9c) is replaced by an "enhancement" behavior as temperature increases. This enhancement is mainly due to a significant enhancement in the intrinsic transconductance G_{mi} as shown in Fig. 4.10. The enhancement in G_{mi} is high enough to overcome the increase in the intrinsic



(a) f_T of FB. (b) f_T of BT.



(c) g_m of FB. (d) g_m of BT.

Fig. 4.7.: A demonstration of the ZTC_{ft} point and its correspondence to the ZTC_{gm} point for both FB and BT structures of the PD SOI technology at $V_{\mathrm{DS}} = 0.3$ V.

total gate capacitance C_{gg} which would normally cause a degradation in f_T. On the other hand, this increase in C_{gg} helps to make the enhancement in $f_{\max}$ even more pronounced than in f_T. The values and the variation of all parameters are presented in Table 4.3 and Table 4.4. It is worth noticing that, ZTC_{gm} varies with V_{DS}, it has a lower value at a higher V_{DS} which means a closer value of V_T and also a lower variation of g_m and f_T if V_{GS} is fixed and V_{DS} is varied.

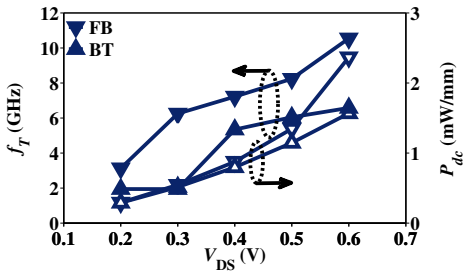
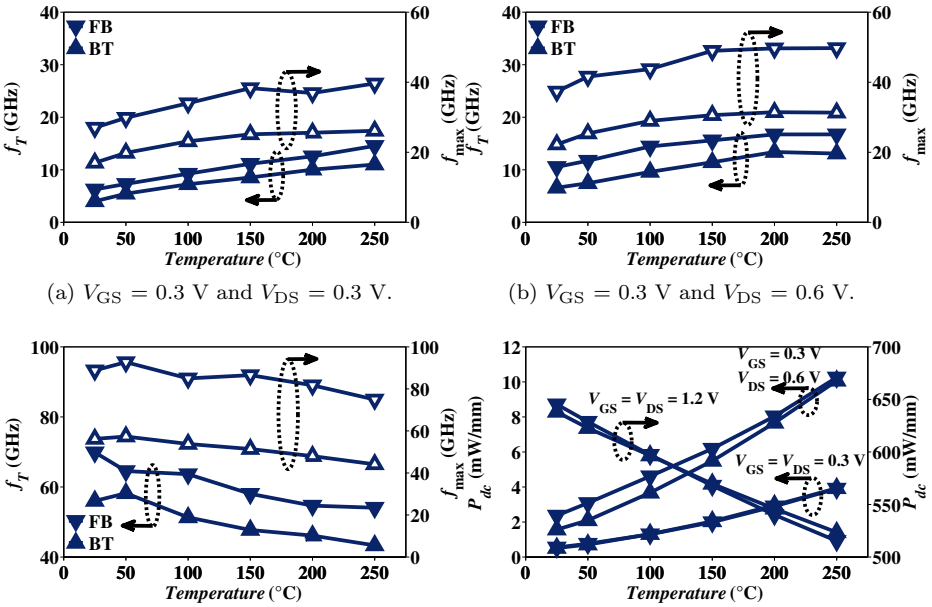


Fig. 4.8.: Variation of f_T and P_{dc} with the increase of V_{DS} for both FB and BT structures of the PD SOI device at room temperature and $V_{\mathrm{GS}} = 0.3$ V.



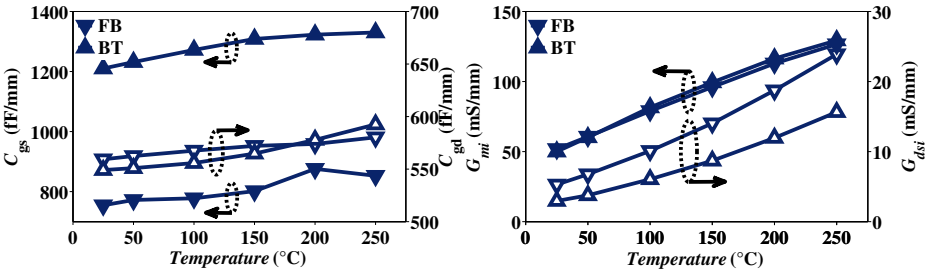
(a) $V_{\mathrm{GS}} = 0.3$ V and $V_{\mathrm{DS}} = 0.3$ V.

(b) $V_{\mathrm{GS}} = 0.3$ V and $V_{\mathrm{DS}} = 0.6$ V.

(c) $V_{\mathrm{GS}} = 1.2$ V and $V_{\mathrm{DS}} = 1.2$ V.

(d) P_{dc} at the different biases.

Fig. 4.9.: Variation of f_T, $f_{\max}$, and P_{dc} with temperature at different V_{GS} and V_{DS} biasing .



(a) C_{gs} and C_{gd}.

(b) $G_{m\mathrm{i}}$ and G_{dsi}.

Fig. 4.10.: Variation of intrinsic elements with temperature of PD SOI devices at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.3$ V.

However, this approach has some drawbacks:

– DC power consumption increases with temperature instead of decreasing. However, huge reduction of P_{dc} is achieved by operating the device at this sub-ZTC_{gm} regime compared to V_{DD} operation scheme as shown in Fig. 4.9d.

Table 4.3.: PD SOI devices characteristics at sub-ZTC_{gm} regime with $V_{\mathrm{DS}} = 0.3$ V and V_{GS} depending on the ZTC_{gm} of each device.

	PD SOI		
	FB	BT	DT
L (μm)	0.13	0.13	0.13
W (μm)	2	2	2
N_{finger}	30	30	30
ZTC_{gm} (V)	0.45	0.45	0.43
V_T (V)	0.29	0.4	0.36
$ZTC_{gm} - V_T$	0.16	0.05	0.07
ZTC_{ft} (V)	0.45	0.45	0.44
V_{GS} (V)	0.3	0.3	0.3
f_T @ 25^{o}C (GHz)	6.25	4	7.18
f_{max} @ 25^{o}C (GHz)	27.01	17	14.04
P_{dc} @ 25^{o}C (mW/mm)	0.55	0.51	1.42
Δf_T (GHz/^{o}C)	0.036	0.028	0.03
Δf_{max} (GHz/^{o}C)	0.053	0.039	0.066
ΔP_{dc} (mW/mm/^{o}C)	0.015	0.015	0.027

– Absolute values of f_T and f_{max} are highly reduced when compared to their values at V_{DD} operation scheme (see Fig. 4.9)
– Intrinsic output conductance increases with increasing temperature (Fig. 4.10b), which might add a constraint on the design of cascaded devices.
– In the case where ZTC_{gm} is lower than V_T, the RF operation is very limited, and could even be very difficult to extract a valid f_T or f_{max}. The best case is when ZTC_{gm} is slightly above V_T so that the operation is around V_T or slightly below.

In conclusion, this approach could be very interesting for LVLP applications where the stability of the RF performance is of crucial importance while keeping the dc power consumption at its minimum.

4.3 CONCLUSION

In this chapter the Low Voltage Low Power (LVLP) operation scheme is presented. Two categories of LVLP are considered; the one that requires high drive current and the one that demand an extremely low power consumption.

In the first category, two case studies were presented. The first case study focused on room temperature operation. It was shown that a key parameter in choosing a device for high drive current LVLP operation (especially for RF applications) is to check the location of the maximum transconductance $g_{m,\mathrm{max}}$

with respect to the gate bias. A device which presents $g_{m,\max}$ at a lower V_{GT} will deliver better performance when operated in LVLP scheme. GCMOS devices were shown to have this advantage over classical MOS devices. The second case study presented the high temperature operation. For an application demanding relatively high drive current, an operation at ZTC_{IDS} is suggested in order to fix the drain current as temperature increases (which will also fix the consumed dc power) while keeping the variation in f_T as minimum as possible. FD devices were shown to outperform PD devices in this operation scheme with lower dc power consumption P_{dc}. Not only lower *absolute* values of P_{dc}, but also FD devices present a significant reduction (higher than PD devices) in P_{dc} when operated at ZTC_{IDS} compared to operation at $g_{m,\max}$ condition. Nevertheless, PD devices deliver slightly higher f_T at ZTC_{IDS} than FD devices.

In the second category, where significant low power consumption is required and also stable dc and RF behavior with temperature, a new approach is proposed. Instead of loosing dc and RF performance as temperature increases, the device could be biased at a gate voltage slightly below the ZTC_{gm} point (which is usually below the ZTC_{IDS} point) in order to benefit from the increasing behavior (with temperature) of I_{DS} and g_m at this bias condition. The result is also an increasing behavior of f_T at very low dc power consumption levels. Some drawbacks could be attributed to this approach but the proper choice of the bias point could maximize benefits and minimize drawbacks.

Table 4.4.: Devices characteristics at sub-ZTC_{gm} regime with $V_{\mathrm{DS}} = 0.6$ V and V_{GS} depending on the ZTC_{gm} of each device.

	DNW Bulk			PD SOI			FD SOI		PD		
	FB	BT	DT	FB	BT	DT	FB	BT	nMOS	FB GC	BT GC
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15	0.5	0.5	0.5
W (μm)	2	2	2	2	2	2	5	5	3.3	3.3	3.3
N_{finger}	30	30	30	30	30	30	48	48	12	12	12
ZTC_{gm} (V)	0.29	0.33	0.33	0.39	0.44	0.44	0.42	0.43	0.5	0.43	0.51
V_T (V)	0.22	0.3	0.26	0.29	0.4	0.36	0.35	0.36	0.48	0.53	0.63
$ZTC_{gm} - V_T$	0.07	0.03	0.07	0.10	0.04	0.08	0.07	0.07	0.02	−0.1	−0.12
ZTC_{ft} (V)	0.28	0.33	0.3	0.4	0.42	0.46	0.46	0.485	0.56	0.47	0.56
V_{GS} (V)	0.2	0.2	0.2	0.3	0.3	0.3	0.3	0.3	—	0.2	0.3
f_T @ 25^{o}C (GHz)	9.2	7.07	3.73	10.54	6.58	9.53	10.91	11.6	—	0.24	0.03
f_{max} @ 25^{o}C (GHz)	35	24.66	10.75	37.33	22.24	20.25	17.1	12.48	—	19.94	—
P_{dc} @ 25^{o}C (mW/mm)	11.81	1.71	2.83	2.367	1.567	3.97	0.862	0.668	—	0.019	0.007
Δf_T (GHz/^{o}C)	0.041	0.05	0.034	0.029	0.032	0.038	0.027	0.017	—	0.006	0.006
Δf_{max} (GHz/^{o}C)	0.044	0.09	0.05	0.055	0.039	0.11	0.013	0.024	—	0.2	—
ΔP_{dc} (mW/mm/^{o}C)	0.045	0.035	0.045	0.034	0.038	0.063	0.008	0.0073	—	0.001	0.002

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CHAPTER 5

NONLINEAR CHARACTERIZATION

MOSFET devices are continuously climbing the ladder of high frequency performance. They are increasingly employed in RF circuit design including Low Noise Amplifiers (LNA), Voltage Controlled Oscillators (VCO), RF antenna switches, etc. Therefore, no wonder that the linearity response of MOSFET devices is becoming a frequently visited subject in the literature. This work is not an exception, a nonlinear study of the devices characterized for RF applications constitutes a basic brick in the wall. Linearity or nonlinearity is a crucial requirement in the analog and RF circuit design. A fail to correctly design the linearity aspect of a communication system is equivalent to a fail in its operation. There exist some parameters or figures of merit that describe the linear characteristics of a device or a system as to be introduced in this chapter.

5.1 INTRODUCTION

A linear system (or device) is a system whose output follows its input in a linear fashion. Mathematics is able to give a more comprehensive definition of a linear system. A system is said to be linear if its transfer function follows a straight line function such as

$$Output = Gain \times Input \tag{5.1}$$

which is represented graphically in Fig. 5.1. The gain constitutes the slope of the straight line. The system is linear since the output always follows the input with a certain gain. If mathematics should be a little relaxed, a dc offset could be added to (5.1)

$$Output = Offset + Gain \times Input \tag{5.2}$$

This is ideal mathematics. In reality, there exists no system or device that could follow this linear model. Yet, the linearity study is concerned by the capacity of a certain system to sustain such a linear model. In other words, the linearity study or characterization tries to answer the question: What is the maximum limit of a system or a device after which it will fail to follow the linear model of (5.2)? That is why it is usually called a nonlinear study or characterization since it starts at the ceiling of linear behavior and continues to check the nonlinear behavior of the system or the device as far as the design is concerned.

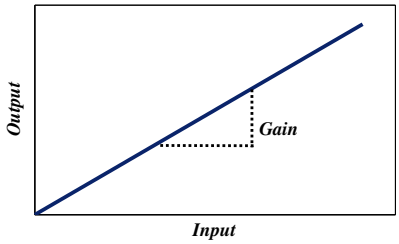


Fig. 5.1.: The ideal mathematical definition of a *linear* behavior.

5.2 NONLINEARITY

A real (non-ideal) device or system behaves linearly according to (5.2) till a certain point or condition (which could be external) where it fails to follow the simple model of (5.2). Starting from this point and beyond, a more complicated model should be utilized. Generally, the Taylor series is adequate for describing the behavior of the system at relatively low frequencies. For very high frequencies, a Volterra series analysis could be necessary. Despite its better accuracy, Volterra series increases the complexity of the analysis significantly.

Assuming a memoryless time-invariant system, for simplicity, a nonlinear system excited by an input $x(t)$ to give an output $y(t)$ can be described using [1]

$$y(t) = f(x(t)) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots + \alpha_n x^n(t) \tag{5.3}$$

If the right-hand side of (5.3) converges to $f(x(t))$, the coefficients α_n are calculated using the coefficients of a Taylor series of $f(t)$

$$\alpha_n = \frac{1}{n!}\frac{\mathrm{d}^n f}{\mathrm{d}x^n} \tag{5.4}$$

This model is frequently used in literature to define and quantify several nonlinear characteristics of the system. Harmonic distortion, gain compression, cross modulation, inter modulation, and desensitization are among these characteristics.

5.2.1 Harmonic Distortion

Consider the case where the input signal to a system or a device contains only one frequency component and its amplitude is small enough so that the system or the device is able to behave according to its linear characteristics. In this case, the output signal also contains one frequency component which is the frequency component of the input signal. No other frequency components or *harmonics* are generated by the system. The output frequency is thus called the *fundamental frequency* or the *first harmonic*. The amplitude of the output signal is the amplitude of the input signal amplified by the value of the gain of the system according to (5.1). Mathematically, this behavior could be simply represented as follows. If the input signal is a simple sinusoidal signal represented by

$$x(t) = X_{\text{in}} \cos(\omega t) \tag{5.5}$$

where X_{in} is the input signal amplitude and ω is its frequency. And if the system is characterized by

$$y(t) = f(x(t)) = Ax(t) \tag{5.6}$$

where A is the gain of the system. Therefore, the output signal $y(t)$ takes the form

$$y(t) = AX_{\text{in}} \cos(\omega t) \tag{5.7}$$

Usually a dc offset exists as described in (5.2).

Although the real system will not show that ideal behavior, due to the existence of some noise and parasitics, this behavior could be found in reality if a small enough signal is applied to a system which has a high enough ceiling of linearity.

At the moment that the input signal amplitude attains the linearity ceiling of the system, (5.7) is no more valid. An analysis using the power series representation given in (5.3) should be employed. Consequently, the output signal takes the form [1]

$$y(t) = \beta_0 + \beta_1 \cos(\omega t) + \beta_2 \cos(2\omega t) + \beta_3 \cos(3\omega t) + \ldots + \beta_n \cos(n\omega t) \tag{5.8}$$

where the term β_n is given by:

$$\beta_0 = \alpha_0 + \frac{\alpha_2}{2} X_{\text{in}}^2 + \dots \tag{5.9a}$$

$$\beta_1 = \alpha_1 X_{\text{in}} + \frac{3}{4}\alpha_3 X_{\text{in}}^3 + \dots \tag{5.9b}$$

$$\beta_2 = \frac{\alpha_2}{2} X_{\text{in}}^2 + \dots \tag{5.9c}$$

$$\beta_3 = \frac{\alpha_3}{4} X_{\text{in}}^3 + \dots \tag{5.9d}$$

The nonlinear response of a system, as can be seen from (5.8), results in additional frequency components. The *fundamental* frequency component, in addition to several multiples of it, are found in the output signal. These multiples, also called harmonics, are mostly undesired for the correct function, thus the name *Harmonic Distortion*[1]. The more the *Harmonic Distortion* components are minimized, the more the desired output signal, here the *fundamental* component, is clear.

Harmonic Distortion HD components can be quantified. A *Harmonic Distortion* of order n, HD_n, is defined as the ratio of the n^{th} harmonic β_n to the fundamental output component β_1 [3]

$$HD_n = \frac{|\beta_n|}{|\beta_1|} \tag{5.10}$$

hence, from (5.9), the second and third harmonic distortion factors can be defined as a function of the input or the output magnitude (X_{in} or X_{out}) by [1]

$$HD2 = \frac{|\beta_2|}{|\beta_1|} \cong \frac{1}{2}\frac{\alpha_2}{\alpha_1} X_{\text{in}} \cong \frac{1}{2}\frac{\alpha_2}{\alpha_1^2} X_{\text{out}} \tag{5.11a}$$

$$HD3 = \frac{|\beta_3|}{|\beta_1|} \cong \frac{1}{4}\frac{\alpha_3}{\alpha_1} X_{\text{in}}^2 \cong \frac{1}{4}\frac{\alpha_3}{\alpha_1^3} X_{\text{out}}^2 \tag{5.11b}$$

Generally, the amplitude of the n^{th} harmonic consists of a term proportional to X_{in}^n in addition to other terms proportional to higher powers of X_{in}, as in (5.9b) for example. For small values of X_{in}, the higher powers terms can be neglected and the n^{th} harmonic can be correctly assumed to grow proportionally to X_{in}^n [4]. This is clearly seen in (5.11a), where it is assumed that $\alpha_1 X_{\text{in}} \gg \frac{3}{4}\alpha_3 X_{\text{in}}^3$ in (5.9b).

[1] A distortion is the alteration of the original shape (or other characteristic) of an object, image, sound, waveform or other form of information or representation. Distortion is usually unwanted, and often many methods are employed to minimize it in practice. In some fields, however, distortion is actually desirable; such is the case with electric guitar (where distortion is often induced purposely with the amplifier or an electronic effect to achieve an aggressive sound where desired), or censoring words. The slight distortion of analog tapes and vacuum tubes is considered pleasing in certain music listening situations [2].

The second and third harmonic distortion factors are presented in (5.11), yet higher harmonic distortion factors can also exist. Harmonic factors resulting from α_j with j an even number are called even harmonics and those resulting when j is an odd number are called odd harmonics. In practice, even harmonics vanish when the system has odd symmetry, i.e. when it is fully differential [4]. However, mismatches existing in the system (and in devices) disturb the symmetry yielding finite even harmonics. However, usually a certain harmonic distortion is more dominant, as will be seen later for the case of MOSFET devices. It is also worth noticing that even order harmonics give rise to a component at zero frequency, as shown in (5.9a), causing a dc shift. This phenomenon is called *self-biasing* since the bias level of the nonlinear circuit might change as a function of the input signal amplitude.

The advantage of the power series (or Taylor series) representation is the possibility to quantify mathematically the total harmonic distortion present in the system and defined as [3]

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} \left|\beta_n^2\right|}{\left|\beta_1^2\right|}} \tag{5.12}$$

5.2.2 Gain Compression

The small-signal gain of a circuit is always obtained with the assumption that the harmonics are negligible [4]. As long as the signal is small enough to keep the circuit or the device within its linear limits, the gain is simply represented as shown in Fig. 5.1. As the amplitude of the input signal increases, the gain begins to vary. Usually, this is used as an alternative definition of nonlinearity being the variation of the small-signal gain with the input level [4]. Mostly, this variation takes the form of *compression* or *saturation* of the gain. In other words, the gain approaches zero as the input signal attains a sufficiently high amplitude. Mathematically, the gain could be represented as $\alpha_1 + \frac{3}{4}\alpha_3 X_{\text{in}}^2$ (from (5.9b)). If α_3 is negative, the gain is a decreasing function of the input signal amplitude X_{in}. The figure of merit utilized to quantify this phenomenon is called the "1-dB compression point", defined as the input signal level that causes the small-signal gain to drop by 1 dB. This definition is illustrated in Fig. 5.2. In the literature, it is alternatively used for the input signal amplitude (voltage) or the input signal power. For the former case, it is denoted $X_{\text{in,1-dB}}$ whereas in the later case it is denoted $P_{\text{1-dB}}$.

Using (5.9b), the calculation of the 1-dB compression point is straightforward [4]

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 X_{\text{in,1-dB}}^2\right| = 20\log|\alpha_1| - 1\,\text{dB} \tag{5.13}$$

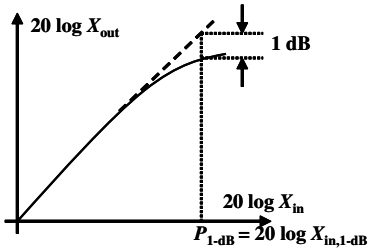


Fig. 5.2.: An illustration of the definition of the 1-dB compression point $P_{1\text{-dB}}$.

from which

$$X_{\text{in,1-dB}} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|} \tag{5.14}$$

Typically, for a front-end RF amplifier, $X_{\text{in,1-dB}}$ ranges between -20 and -25 dBm (63.2 and 35.6 mV_{pp} in a 50-Ω system) [4].

5.2.3 Desensitization and Blocking

The gain compression phenomenon is sometimes coupled with another inconvenience called *desensitization* [4]. A weak desired signal arriving at the input of the system accompanied by a strong interferer would suffer from a significantly small gain, since the strong signal would have already caused the gain of the system to compress. As a result the desired weak signal is blocked.

Consider (5.3) and an input signal of $x(t) = X_{\text{in},1} \cos \omega_1 t + X_{\text{in},2} \cos \omega_2 t$, the output signal could be expressed as

$$y(t) = \left(\alpha_1 X_{\text{in},1} + \frac{3}{4} \alpha_3 X_{\text{in},1}^3 + \frac{3}{2} \alpha_3 X_{\text{in},1} X_{\text{in},2}^2 \right) \cos \omega_1 t + \dots \tag{5.15}$$

If $X_{\text{in},1} \ll X_{\text{in},2}$, the output reduces to

$$y(t) = \left(\alpha_1 + \frac{3}{2} \alpha_3 X_{\text{in},2}^2 \right) X_{\text{in},1} \cos \omega_1 t + \dots \tag{5.16}$$

This means that the gain for the desired signal is equal to $\left(\alpha_1 + \frac{3}{2} \alpha_3 X_{\text{in},2}^2 \right)$ which is a decreasing function of $X_{\text{in},2}$ if α_3 is negative. If $X_{\text{in},2}$ is large enough, this gain drops to zero and the desired signal is *blocked*. In RF design, the term *blocking signal* usually refers to an interferer that desensitizes a circuit even if the gain does not completely drop to zero. A good design of a RF receiver should withstand blocking signals 60 to 70 dB larger than the desired signal.

5.2.4 Cross Modulation

Besides gain compression and blocking, the presence of a strong interferer at the input with a weak desired signal could also result in a phenomenon known

as *cross modulation*. Amplitude modulation of the strong signal (or sometimes noise) passes to the amplitude of the weak signal [4].

Assuming that the amplitude of the interferer is modulated by a sinusoidal signal of frequency ω_m and modulation index m (where $m < 1$) such that the interferer is represented by $X_{\text{in},2}\,(1 + m\cos\omega_m t)\cos\omega_2 t$, then from (5.16)

$$\begin{aligned} y(t) = \Bigg[& \alpha_1 X_{\text{in},1} + \frac{3}{2}\alpha_3 X_{\text{in},1} X_{\text{in},2}^2 \\ & \times \left(1 + \frac{m^2}{2} + \frac{m^2}{2}\cos 2\omega_m t + 2m\cos\omega_m t\right)\Bigg] \cos\omega_1 t + \ldots \end{aligned} \tag{5.17}$$

Therefore, an amplitude modulation at the frequencies ω_m and $2\omega_m$ is superimposed on the desired signal at the output of the system.

5.2.5 Intermodulation

All previous phenomena are related to the nonlinear behavior of a system subject to an input signal of single tone for which these figures of merit are sufficient to describe the nonlinearities of the system. Yet, some systems are designed to overcome these phenomena (as is the case of the low-pass filter with harmonics) but they still suffer from other nonlinearities that need to be characterized. Mostly, communication systems would be subject to a *two-tone* signal at their input. In that case, the nonlinear behavior is different from the single-tone case. At the output, new components are found which are not the harmonics of the input signal. These components result from the *mixing* (multiplication) of the two frequency components of the input signal when their sum is raised to a power greater than unity. This phenomena is called *intermodulation* (IM).

Assume an input signal of the form $x(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$. Using (5.3), the output takes the form

$$\begin{aligned} y(t) = & \alpha_1\left[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)\right] + \alpha_2\left[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)\right]^2 \\ & + \alpha_3\left[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)\right]^3 \end{aligned} \tag{5.18}$$

The expansion of this output shows the presence of three intermodulation products $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$, and $\omega_1 \pm 2\omega_2$ and two fundamental components ω_1 and ω_2 with the following amplitudes [4]:

$$\omega_1 \pm \omega_2 : \quad \alpha_2 A_1 A_2\cos(\omega_1 + \omega_2)t \quad + \alpha_2 A_1 A_2\cos(\omega_1 - \omega_2)t \tag{5.19a}$$

$$2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \tag{5.19b}$$

$$\omega_1 \pm 2\omega_1 : \frac{3\alpha_3 A_1 A_2^2}{4}\cos(\omega_1 + 2\omega_2)t + \frac{3\alpha_3 A_1 A_2^2}{4}\cos(\omega_1 - 2\omega_2)t \tag{5.19c}$$

and the fundamental components

$$\begin{aligned}\omega_1,\omega_2: \quad & \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos(\omega_1 t) \\ & + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_1^2 A_2\right)\cos(\omega_2 t)\end{aligned} \tag{5.20}$$

Practically, only two components of (5.19) are important whereas the others are mostly ignored by designers either because they are too high in frequency or too low, so that they are naturally filtered by the RF filters already implemented in the circuit. The important components are the third order IM products at $2\omega_1 - \omega_2$ and $\omega_1 - 2\omega_2$ since they could lie in the vicinity of the useful signals if the difference between ω_1 and ω_2 is small (see Fig. 5.3). The result is a nonlinear behavior even in the presence of good filters. Typically, it is assumed that $A_1 = A_2 = A$, and the ratio between the amplitude of the third order IM and the amplitude of the fundamental component is the ratio between $\frac{3}{4}\alpha_3 A^3$ and $\alpha_1 A$ (using (5.19b),(5.19c), and (5.20)).

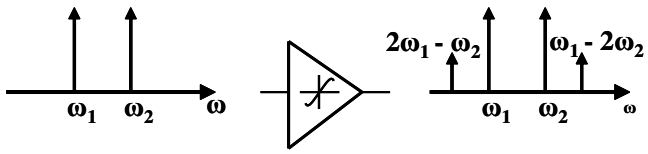


Fig. 5.3.: Intermodulation due to the third order IM products.

Intermodulation could also affect a single-tone desired input signal if it is weak enough and accompanied by two strong interferers whose frequencies are close enough. A third order IM of the two interferers would lie in the band of interest and the distortion (nonlinearity) occurs (see illustration in Fig. 5.4). Although the desired signal is a single tone, this behavior of nonlinearity could not be described by harmonic distortion. A different metric is used, instead, to account for this phenomenon, known as the *third intercept point* IP_3.

To measure IP_3, a two-tone test is adapted in which the amplitude is small enough to ensure that high-order nonlinear terms are negligible and that the gain is kept equal to α_1. From (5.19b),(5.19c), and (5.20), as A increases, the fundamental components increase proportional to A, whereas the third-order IM components increase proportional to A^3 (see Fig. 5.5). If a log-log scale is used (Fig. 5.5), it can be noted that the magnitude of the third-order IM components grows at three times the rate of the fundamental components, so that they both intersect at a certain point, defined as the third-order intercept point IP_3. If referred to the input signal, IP_3 is called the input IP_3 or IIP_3 whereas if referred to the output signal it is called the output IP_3 or OIP_3.

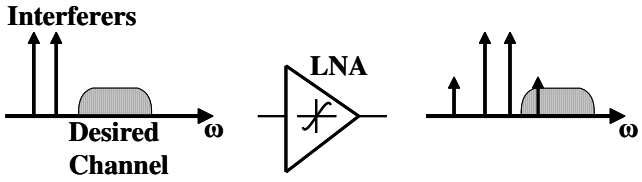


Fig. 5.4.: Effect of intermodulation between two strong interferers on a desired channel.

Introducing a two-tone signal of the form $x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$ in (5.3), the output takes the form:

$$\begin{aligned} y(t) = &\left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos(\omega_1 t) + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos(\omega_2 t) \\ &+ \frac{3}{4}\alpha_3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 A^3 \cos(\omega_1 - 2\omega_2)t + \ldots \end{aligned} \tag{5.21}$$

Assuming $\alpha_1 \gg \frac{9}{4}\alpha_3 A^2$, the input signal amplitude at which the fundamental components (ω_1 and ω_2) have the same amplitude as the third-order IM components ($2\omega_1 - \omega_2$ and $\omega_1 - 2\omega_2$) is simply calculated from

$$|\alpha_1|\, A_{IP3} = \frac{3}{4}\,|\alpha_3|\, A_{IP3}^3 \tag{5.22}$$

Therefore, the input IP_3 is

$$A_{IP3,\text{in}} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{5.23}$$

and the output IP_3 is

$$A_{IP3,\text{out}} = \alpha_1 A_{IP3,\text{in}} \tag{5.24}$$

Note that IP_3 quantifies only the third-order IM component. The assumption $\alpha_1 \gg \frac{9}{4}\alpha_3 A^2$ is valid for small input levels. If the input level is increased to reach the intercept point, the assumption is no longer valid, the gain compresses and higher orders of IM become significant. Usually, the level of IP_3 is higher than the allowable input range and the supply voltage of the circuit. Therefore, in practice, extrapolation is required to find the intercept point on Fig. 5.5.

The IP_3 figure of merit can be calculated as follows. Assuming the input amplitude of the two tones to be A_{in}, the amplitude of the output fundamental components A_{fund} and the amplitude of the third-order IM components (at the

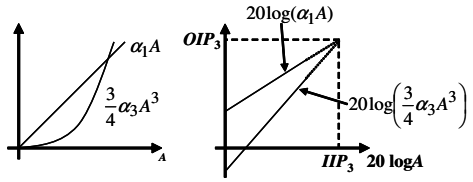


Fig. 5.5.: Determination of the third intercept point IP_3 using extrapolation.

output) to be A_{IM3}, therefore using (5.21)

$$\frac{A_{\text{fund}}}{A_{IM3}} \approx \frac{|\alpha_1|\, A_{\text{in}}}{\frac{3}{4}\,|\alpha_3|\, A_{\text{in}}^3} \tag{5.25a}$$

$$= \frac{4\,|\alpha_1|}{3\,|\alpha_3|}\,\frac{1}{A_{\text{in}}^2} \tag{5.25b}$$

using (5.23)

$$\frac{A_{\text{fund}}}{A_{IM3}} = \frac{A_{IP3,\text{in}}^2}{A_{\text{in}}^2} \tag{5.26}$$

and expressing all signal in dBm

$$20\log A_{\text{fund}} - 20\log A_{IM3} = 20\log A_{IP3,\text{in}}^2 - 20\log A_{\text{in}}^2 \tag{5.27}$$

therefore

$$20\log A_{IP3,\text{in}} = \frac{1}{2}\,(20\log A_{\text{fund}} - 20\log A_{IM3}) + 20\log A_{\text{in}} \tag{5.28}$$

or simply

$$IIP_3|_{\text{dBm}} = \frac{\Delta P|_{\text{dB}}}{2} + P_{\text{in}}|_{\text{dBm}} \tag{5.29}$$

as presented graphically in Fig. 5.6. Thus, using this method, the IP_3 can be measured with only one input level, without the need of extrapolation. This is the method employed to measure IP_3 of the devices considered in this work.

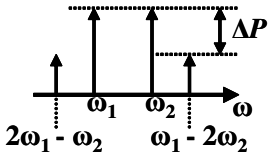


Fig. 5.6.: Determination of the third intercept point IP_3 without extrapolation.

5.3 INTEGRAL FUNCTION METHOD

The measurement of nonlinear behavior (either single- or two-tone) requires special equipment and special precautions. Fortunately, these measurements can be replaced by mathematical analysis based on simple dc measurements. Several analysis methods exist such as Taylor series, Volterra series, and describing functions [3]. Taylor series and Volterra series analysis have some limitations when considering the case of studying the nonlinear behavior of MOSFET devices. They require the calculation of high-order derivatives of $I_{DS}(V_{DS})$ and $I_{DS}(V_{GS})$ characteristics using Fourier methods (Fourier coefficients for periodical functions and Fourier integrals for non-periodical functions) which increases the sensitivity to the noise imposed by measurement equipments. The describing function, on the other hand, depends on the signal amplitude. A new method was introduced which also depend on the signal amplitude and does not require high-order derivatives. This method, called the Integral Function Method IFM, was first proposed by A. Cerdeira *et al.* in 2002 [5–7]. Although the IFM works on dc measurements to predict the nonlinear behavior, it was proven to be valid for high frequencies [3].

5.3.1 Mathematical Basis

The mathematical basis of this new method, IFM, was presented in [8]. The method is quite simple. It only requires the knowledge of the transfer (input-output) characteristics of the transistor (or circuit) to be analyzed, which can be measured, simulated, or calculated. For a MOSFET transistor, this would be the $I_{DS}(V_{GS})$ or the $I_{DS}(V_{DS})$ characteristics. In general, the output is designated as $Y(X)$ where X is the input. As shown in Fig. 5.7, the range of the transfer characteristics to be analyzed is chosen through the definition of the input small-signal constant bias X_0 and amplitude A. The small signal takes the form

$$X = X_0 + A\sin(\omega t) \tag{5.30}$$

The output signal is a function of this small-signal input signal

$$Y = f(X) \tag{5.31}$$

where, in general, $f(X)$ is a nonlinear function, and X and Y can be voltages or currents depending on the type of device or circuit being analyzed.

The first step is to normalize both magnitudes (of input and output) to an interval [0,1]. The following formulas can be applied where x and y are the normalized forms of X and Y

$$x = \frac{X - (X_0 - A)}{(X_0 + A) - (X_0 - A)} = \frac{X - (X_0 - A)}{2A} \tag{5.32}$$

$$y = \frac{Y(X) - Y(X_0 - A)}{Y(X_0 + A) - Y(X_0 - A)} \tag{5.33}$$

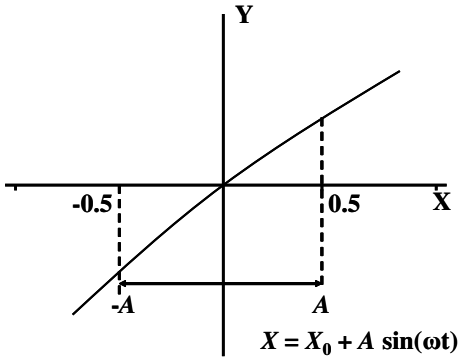


Fig. 5.7.: Input-output characteristic $y = f(x)$ where the input has a dc bias $X_0 = 0$ and a sinusoidal input signal of amplitude A and frequency ω.

From (5.32), X can be written as

$$X = X_0 + A(2x - 1) \tag{5.34}$$

therefore, substituting (5.34) in (5.33), the normalized output is obtained as a function of the operating point and the input signal amplitude

$$y(x) = \frac{Y(X_0 + A(2x-1)) - Y(X_0 - A)}{Y(X_0 + A) - Y(X_0 - A)} \tag{5.35}$$

The normalized input-output characteristic is shown in Fig. 5.8. The area of the box including the normalized characteristics is equal to 1. The normalized characteristic curve divides this box into two areas: AREA1 and AREA2. If the characteristic is perfectly linear, i.e. $y(x) = x$, AREA1 and AREA2 would be completely equal. On the other hand, in a nonlinear case, the gray area in Fig. 5.8 represent the nonlinearity of the system, which summarizes the main idea of the IFM. The nonlinear distortion is related to the difference between the area above the function $y(x)$ and the area below it, or simply AREA1 − AREA2. This basic idea is used to calculate the harmonic distortion figures of merit.

An integral function D is defined as:

$$\begin{aligned} D &= \int_0^1 y(x)\,\mathrm{d}x - \int_0^1 x(y)\,\mathrm{d}y \\ &= 2\int_0^1 y(x)\,\mathrm{d}x - 1 \end{aligned} \tag{5.36}$$

If $y(x)$ is linear, both areas are equal and D reduces to zero. The function D is directly related to the total harmonic distortion THD including the dc offset defined as THD_0 (note that THD defined in (5.12) does not include the dc

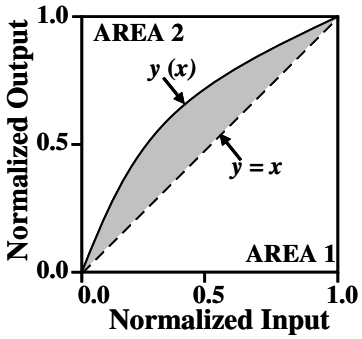


Fig. 5.8.: Normalized input-output characteristic $y = f(x)$ showing the two areas of the square of unity area. The gray part is a measure of the nonlinearity of the system.

offset)

$$THD_0 = \sqrt{\frac{\sum_{n=2}^{\infty} \left|\beta_n^2\right|}{\left|\beta_1^2\right|} + \frac{\left|\beta_0^2\right|}{\left|\beta_1^2\right|}} \tag{5.37}$$

It was shown in [5] that $THD_0 \approx 1.06\, D$.

In the case of balanced or fully differential circuits, the even order harmonics are eliminated. Therefore, to correctly characterize these circuits, the output signal based on the dc measurements of the device is then defined as:

$$Y_r(X) = Y(X_0 + A\sin(\omega t)) - Y(X_0 - A\sin(\omega t)) \tag{5.38}$$

which can be normalized using

$$y_r(x) = \frac{Y_r(X_0 + A(2x-1)) - Y_r(X_0 - A)}{Y_r(X_0 + A) - Y_r(X_0 - A)} \tag{5.39}$$

If $y_r(x)$ is plotted against x, the curve would look perfectly linear, since the values of the odd harmonics (especially the third-order harmonic) are very small compared to the even harmonics. Since, the even harmonics will be eliminated in the fully balanced circuit, $y_r(x) - x$ can be plotted against x, which eliminates the effect of even harmonics. However, the result is a function which cuts the diagonal line in several points including the mid-point at $x = 0.5$. The application of the function D will give zero due to the symmetry around the diagonal line. A function $D_r(x)$ is then defined, which applies the integration only till the mid-point and then multiplies by two:

$$D_r = 2 \times \left| 2 \int_0^{0.5} y_r(x)\, \mathrm{d}x - 0.5^2 \right| \tag{5.40}$$

D_r is also directly proportional to THD_0 without even harmonic distortions.

Another difficulty may occur and disturb the calculation of harmonic distortions using IFM. This happens when the function $y(x)$ is not completely above or below the diagonal line of the unity area square containing the normalized transfer characteristics. This is solved simply by displacing the characteristics to lie completely above the diagonal line using the function $y_s(x)$ defined as

$$y_s(x) = |y(x) - x| + x \tag{5.41}$$

and in this case, the differential function is defined as

$$D_s = 2\int_0^1 y_s(x)\,\mathrm{d}x - 1 \tag{5.42}$$

Notice that, D_s reduces to D if $y(x)$ lies completely below or above the diagonal line. D_s is still proportional to THD_0.

The same approach can be used in the case of fully differential circuits where a function y_{rs} is defined from which a differential D_{rs} is calculated as follows:

$$y_{rs}(x) = |y_r(x) - x| + x \tag{5.43}$$

$$D_{rs} = 2\int_0^1 y_{rs}(x)\,\mathrm{d}x - 1 \tag{5.44}$$

where, again, if y_r has only one inflection point around the diagonal line at the mid-point, y_{rs} reduces to y_r. The relation between D_{rs} and THD_0 is still valid.

5.3.2 Harmonic Distortions

The differential functions introduced so far are then used to calculate the different nonlinear figures of merit. THD_0 is calculated using D or D_s depending on the form of the transfer function, whereas $HD3$ is calculated using D_r. On the other hand, THD is calculated using D_s and D_{rs} [6].

$$THD_0 = 1.06D_s \tag{5.45}$$

$$THD = \sqrt{\frac{(1.06D_s)^2}{2} + \frac{D_{rs}^2}{2}} \tag{5.46}$$

$$HD2 = \sqrt{\frac{(1.06D_s)^2}{2} - \frac{D_{rs}^2}{2}} \tag{5.47}$$

$$HD3 = D_r \tag{5.48}$$

5.3.3 Intermodulation Distortions

The IFM also calculates the intermodulation distortion IMD based on the definitions given by [9] and the well-known fixed relation between the IMD of order

n and the harmonic distortion of the same order, for a very wide range of input signal amplitudes. These definitions consider two input signals of frequency ω_1 and ω_2 and amplitudes A_1 and A_2. The IMD of second order and frequencies $\omega_1 \pm \omega_2$ is calculated from

$$IMD_2 = 2 \times HD2 = 2 \times \sqrt{\frac{(1.06D_s)^2}{2} - \frac{D_{rs}^2}{2}} \tag{5.49}$$

The IMD of order 3, used for broadband amplifiers, considering that A_1 and A_2 are small and equal to A, for frequencies $2\omega_1 \pm \omega_2$ and $\omega_1 \pm 2\omega_2$ is calculated from

$$IMD_3 = 3 \times HD3 = 3 \times D_r \tag{5.50}$$

5.3.4 Voltage Intercept Points

The voltage intercept points VIP can be calculated using the magnitude of the harmonics [10]. This method, however, is only valid for very low amplitudes of the input signal, since only the first term in the harmonic expression is used, neglecting the higher terms. Using the IFM, also for very low signal amplitude, VIP can also be calculated as follows:

$$VIP_2 = \frac{A}{\sqrt{\frac{(1.06D_s)^2}{2} - \frac{D_{rs}^2}{2}}} \tag{5.51}$$

$$VIP_3 = \frac{A}{\sqrt{D_r}} \tag{5.52}$$

5.3.5 Extension to Higher Frequencies

B. Parvais introduced an extension of the IFM method to high frequencies [3, 11]. According to Parvais, the transfer function at high frequency is subject to memory effects and hysteresis due to the charging and discharging capacitors. The result of a time-domain simulation ($X(t)$ and $Y(t)$) imposed on the dc transfer function ($Y(X)$) after removing the time variable shows a kind of envelope with an upper limit above and a lower limit below the transfer function of dc characteristics for each analyzed fundamental frequency. A new differential function is then introduced as

$$D = \left[\int_0^1 y(x)\,\mathrm{d}x\right]_{\mathrm{up}} + \left[\int_0^1 y(x)\,\mathrm{d}x\right]_{\mathrm{down}} - 1 \tag{5.53}$$

where the subscripts "up" and "down" refer to the upper and lower limits of the envelope. Using this differential function with the IFM, the harmonic distortions can be calculated for high frequency large signal cases.

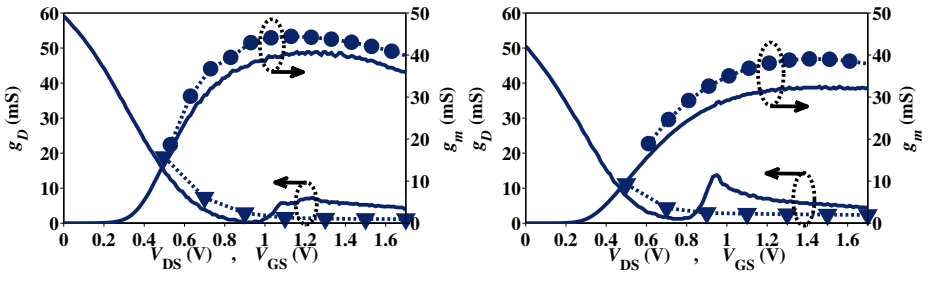
5.4 NONLINEARITIES IN MOSFETS

The IFM is employed to characterize the nonlinear behavior of the devices considered in this work. The IFM is applied on the dc measurements of the considered devices. A Mathcad code written by A. Cerdeira (and adapted for Matlab by Rodrigo Doria from Centro Universitário da FEI in Brazil) is employed for this characterization. This code allows to directly extract the nonlinear figures of merit based on the IFM method, with good validity in high frequency ranges, without the need to apply (5.53).

5.4.1 GMOS and Classical nMOS

The nonlinear behavior of Partially-Depleted (PD) SOI GCMOS and classical nMOS are studied and compared. The two devices selected for this comparison feature a drawn channel length of 0.5 μm with 12 parallel gate fingers of 13.2 μm width each.

In order to fairly compare the GCMOS and the classical nMOS devices considered in this study, the total harmonic distortion (THD) and the third-order harmonic distortion ($HD3$) in the saturation region are presented after normalization with respect to the intrinsic gain (A_{v0}) [12]. A_{v0} is calculated from RF measurements to avoid the impact of self-heating where it results in overestimated A_{v0} when extracted from dc measurements as can be seen from Fig. 5.9 and Fig. 5.10 [13]. Fig. 5.9 shows the effect of self-heating on g_m and g_D which are then used to calculate A_{v0} shown in Fig. 5.10.



(a) GCMOS (b) nMOS

Fig. 5.9.: Transconductance g_m and output conductance g_D for GCMOS extracted from dc (lines) and RF (symbols) measurements at $V_{GT} = 0.7$ V.

5.4.1.1 *Saturation Region*

In the saturation regime of operation, the harmonic distortion figures of merit are extracted using the I_{DS}-V_{GS} measurements at $V_{DS} = 0.5$ V in order to avoid the kink effect region. A sinusoidal ac signal is applied to the gate such that $V_{GS} = V_0 + V_a \sin(x)$, where V_0 is fixed at zero and V_a is varied from 0.1 to 1.5 V and $0 < x < \pi$.

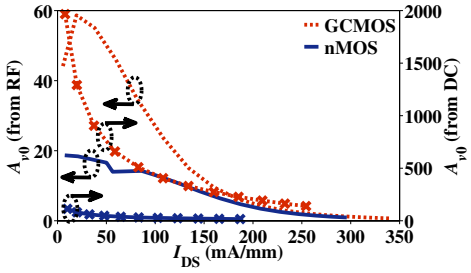


Fig. 5.10.: Intrinsic gain A_{v0} calculated from G_{mi}/G_{dsi} extracted from RF measurements at $V_{DS} = 1$ V (lines) and A_{v0} calculated from dc measurements ($A_{v0} = g_m/I_{DS} \times V_{EA}$) at $V_{DS} = 1$ V (lines with x symbols).

Fig. 5.11a shows a better THD/A_{v0} for GCMOS compared to nMOS device operated in the strong inversion regime ($G_{mi}/I_{DS} < 10$ V^{-1}). An improvement of more than 5 dB is clearly noticed over approximately the complete range.

The second harmonic distortion, and hence the total harmonic distortion, are related to the device physical parameters through this equation [11]:

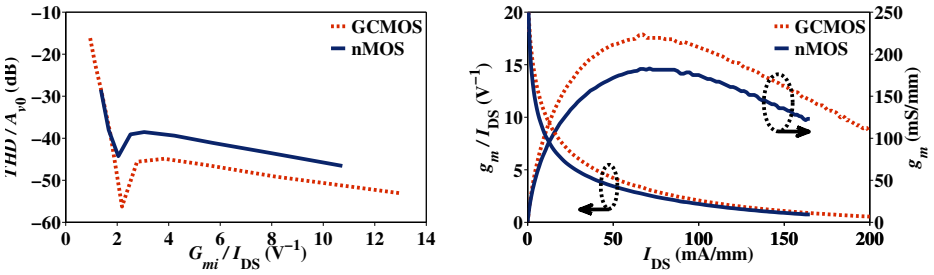
$$HD2 \propto \left| \frac{g_{m2}}{g_{m1}} - A_{v0} \frac{g_{D2}}{(Y_L + g_{D1})} \right| \tag{5.54}$$

where g_{m1} and g_{D1} are the transconductance and the output conductance whereas g_{m2} and g_{D2} are their derivatives and Y_L is the load admittance. Therefore, the minimum of THD/A_{v0} in Fig. 5.11a could be related to the maximum point of g_m with respect to the drain current (Fig. 5.11b). This equation also shows the sensitivity of the linearity figures of merit to the device parameters, especially for high intrinsic gain and small values of load. Therefore, the better dc and RF behavior of the GCMOS device reflect as better linearity figures of merit in comparison to classical nMOS device.

5.4.1.2 Linear Region

In the linear regime of operation, the I_{DS}-V_{DS} measurements for V_{DS} varying from -0.5 V to 0.5 V at $V_{GT} = V_{GS} - V_T = 1.3$ V (Fig. 5.12a) for both devices are used. A sinusoidal ac signal is applied to the drain such that $V_{DS} = V_0 + V_a \sin(x)$, where V_a is fixed at 50 mV, V_0 is varied from -0.5 to 0.5 V and $0 < x < \pi$.

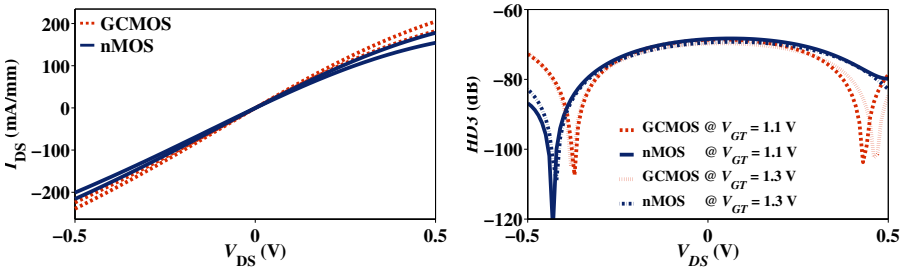
A slight difference is observed between both devices when comparing the third harmonic distortion (Fig. 5.12b), and this slight difference is always in favour of the GCMOS device. Thus, GCMOS can offer similar linearity but smaller on-resistance (R_{ON}), i. e. allows for higher I_{DS} at the same bias, which is of interest for switches. If a certain R_{ON} is targeted, as in the case of MOSFETs acting as tunable resistors in filters, the application of GCMOS allows for the reduction of V_{GT} from 1.3 to 1.1 V without any penalty in linearity, which privileges low voltage circuits.



(a) Total harmonic distortion THD normalized by the intrinsic gain A_{v0} calculated from RF measurements as a function of G_{mi}/I_{DS} where G_{mi} is the intrinsic transconductance calculated from RF.

(b) Transconductance to current ratio g_m/I_{DS} and transconductance g_m both calculated from dc measurements.

Fig. 5.11.: THD/A_{v0}, g_m, and g_m/I_{DS} for both GCMOS and classical nMOS ($L = 0.5$ μm for both devices) at $V_{DS} = 0.5$ V and V_{GT} varying from 0.1 to 1 V.



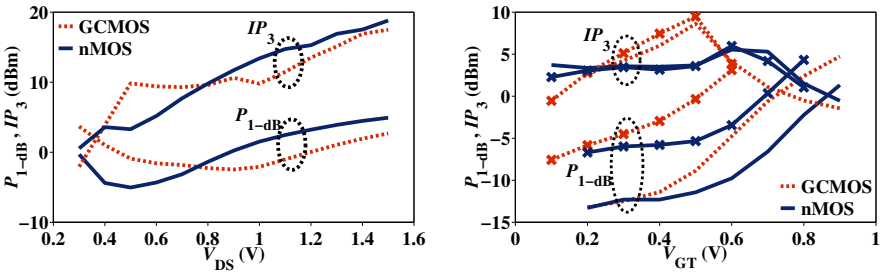
(a) I_{DS}-V_{DS} measurements.

(b) Third harmonic distortion $HD3$.

Fig. 5.12.: I_{DS}-V_{DS} and $HD3$ of GCMOS and classical nMOS devices operated in linear region with V_{DS} varying from -0.5 to 0.5 V and $V_{GT} = 1.1$ and 1.3 V.

5.4.1.3 Compression and Intercept Points

In the design of low noise amplifiers (LNA) it is crucial to accurately consider two figures of merit, the 1-dB compression point $P_{1\text{-dB}}$ and the third intercept point $IP3$ of the device. Fig. 5.13a shows these two figures of merit measured at 6 GHz for the GCMOS and the classical nMOS device. It is clear that the GCMOS and the classical nMOS have close values of $IP3$, while for $P_{1\text{-dB}}$, the classical nMOS outperforms the GCMOS device for values of V_{DS} higher than 0.8 V. This could be explained by the higher gain of the GCMOS in comparison to the classical nMOS device. Based on these results, the GCMOS device could be very interesting for low voltage low power applications. This is confirmed by the values of $P_{1\text{-dB}}$ and $IP3$ shown in Fig. 5.13b where the GCMOS device outperforms the classical nMOS device at $V_{DS} = 0.5$ V over the whole range of V_{GT} at different frequencies (3 and 6 GHz).



(a) $P_{1\text{-dB}}$ and IP_3 at $V_{GT} = 0.5$ V and frequency = 6 GHz.

(b) $P_{1\text{-dB}}$ and IP_3 at $V_{DS} = 0.5$ V and frequency = 3 GHz (lines) and 6 GHz (lines with x symbols).

Fig. 5.13.: 1-dB compression point $P_{1\text{-dB}}$ and third intercept point IP_3 for GCMOS and classical nMOS.

5.4.2 High Temperature

After showing the advantage of GCMOS over classical nMOS for the nonlinear behavior, it is of interest to study the effect of temperature on the nonlinear behavior of both structures [14]. For this study, Fully-Depleted (FD) SOI GCMOS and classical nMOS are used. The GCMOS device features 48 parallel fingers of 2.5 μm width each and a channel length of 0.24 μm. The classical nMOS device features 32 parallel fingers of 2.5 μm width each and a channel length of 0.15 μm. These devices have been characterized in dc, ac and RF in chapter 3 (including high temperature effect) [15] and RF noise behavior is studied in chapter 6 [16]. Nevertheless, it is necessary to give a very brief introduction hereafter before presenting the nonlinear behavior.

The lightly doped region in the GCMOS is naturally inverted at very low gate bias values giving rise to a shorter channel length which corresponds to $L_{\text{eff}} = L - L_{\text{LD}}$. In the GCMOS considered in this study, the designed $L_{\text{LD}}/L = 0.5$. Hence, the effective channel length is about 0.12 μm for the GCMOS with a physical gate length (L) of 0.24 μm. Usually, the performance of such a GCMOS, in terms of dc (I_{DS}, g_m, V_{EA}, etc.) and RF (f_T, $f_{\max}$, etc), is lower than a classical nMOS of a channel length equals to L_{eff}, but it is higher than a classical nMOS of a channel length equals to L [16–18].

Both devices considered in this study; GCMOS of 0.24 μm and classical nMOS of 0.15 μm, show very close threshold voltage V_T values at room temperature; 0.64 and 0.63 V, respectively. The trend of V_T with temperature is also very similar for both devices, as shown in Fig. 5.14. The transfer characteristics and the transconductance of both devices are shown in Fig. 5.15a at room temperature and at 200^{o}C in saturation region ($V_{\text{DS}} = 1.5$ V). It is clear that the classical nMOS of 0.15 μm drawn channel length exhibits a better dc performance compared to the GCMOS of 0.24 μm drawn channel length, as explained above. This could also be related to a slight shift in the L_{LD}/L ratio due to a lateral

diffusion of dopants from the heavily doped part of the channel as well as due to a slight misalignment of masks during fabrication. However, when considering the ac properties, GCMOS device outperforms the classical nMOS device as shown by the two figures of merit g_m/I_{DS} and A_{v0} (intrinsic voltage gain) in Fig. 5.15b, especially for moderate and high values of gate voltage overdrive $V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_T$.

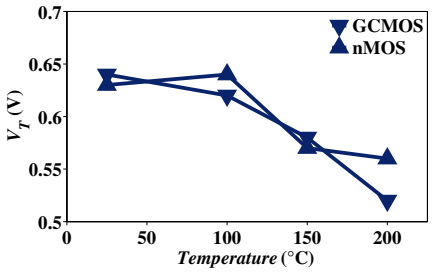
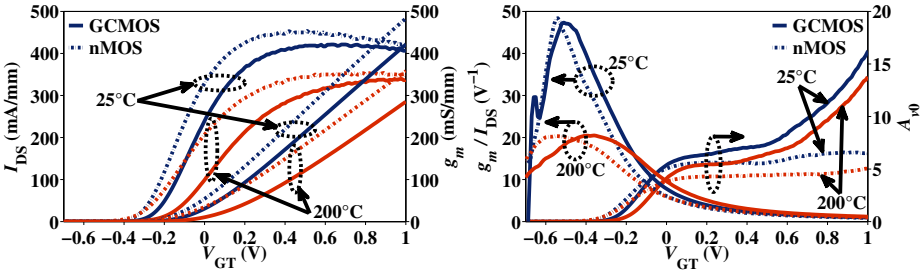


Fig. 5.14.: Threshold voltage V_T variation with temperature for both FD GCMOS and FD classical nMOS devices extracted using the second derivative method at $V_{\mathrm{DS}} = 50$ mV.



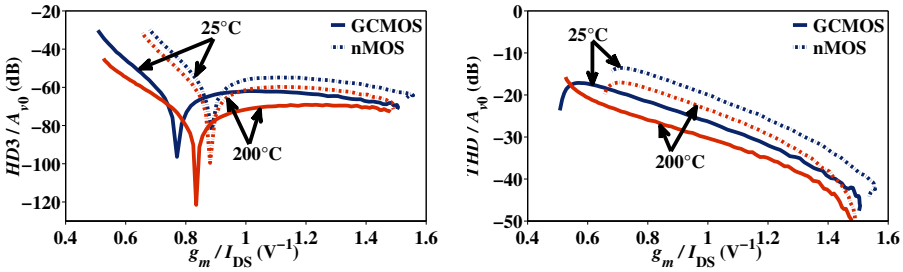
(a) Normalized drain current I_{DS} and normalized dc transconductance g_m.

(b) Transconductance to drain current ratio g_m/I_{DS} and intrinsic gain A_{v0}.

Fig. 5.15.: DC and ac characteristics of FD GCMOS and FD classical nMOS at room temperature and 200°C as a function of gate voltage overdrive $V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_T$ and $V_{\mathrm{DS}} = 1.5$ V.

The Integral Function Method (IFM) is used to calculate the harmonic distortion. Although both devices have close values of V_T, the difference in A_{v0} and in g_m/I_{DS} could affect the comparison of the harmonic distortion figures of merit such as the Total Harmonic Distortion THD and the Third Harmonic Distortion $HD3$. Therefore, these figures of merit will be normalized by the intrinsic voltage gain A_{v0} and presented as a function of g_m/I_{DS} [12]. THD and $HD3$ for both devices in the linear and the saturation regions of operation are extracted.

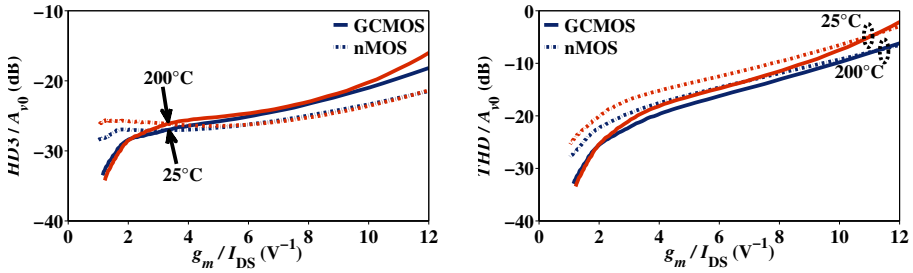
In the linear region, the I_{DS}-V_{DS} characteristics at $V_{GT} = 0.7$ V are used for the calculations of the IFM method. The signal applied is equal to $V_0 + V_a \sin(x)$, where V_a is fixed at 50 mV and V_0 is varied from 0 to 1.5 V with $0 < x < \pi$. Normalized $HD3$ and THD are shown in Fig. 5.16. It is clear that GCMOS shows lower harmonics in the linear region at ambient as well as at high temperatures.



(a) $HD3$ (b) THD

Fig. 5.16.: Third harmonic distortion $HD3$ and total harmonic distortion THD normalized by intrinsic gain and presented as a function of g_m/I_{DS} for FD GCMOS and FD classical nMOS in linear region at $V_{DS} = V_a = 50$ mV and $V_{GT} = 0.7$ V.

In the saturation region, the I_{DS}-V_{GS} characteristics at $V_{DS} = 1.5$ V are used. A sinusoidal ac signal is applied to the gate such that $V_{GS} = V_0 + V_a \sin(x)$, where V_0 is fixed at 0 V and V_a is varied from 0.1 to 1.5 V with $0 < x < \pi$. As shown in Fig. 5.17, the GCMOS device shows lower THD over the whole considered range. However, nMOS device shows lower $HD3$ values except at low g_m/I_{DS} (i.e. in strong inversion). Both devices show a stable $HD3$ with temperature.



(a) $HD3$ (b) THD

Fig. 5.17.: Third harmonic distortion $HD3$ and total harmonic distortion THD normalized by intrinsic gain and presented as a function of g_m/I_{DS} for FD GCMOS and FD classical nMOS in saturation region at $V_{DS} = 1.5$ V and V_{GT} varying from 0 to 0.9 V.

5.5 CONCLUSION

In addition to the favoured behavior of GCMOS over classical nMOS in dc, ac, and RF as shown in chapter 3, this chapter presents another aspect where the GCMOS device outperforms the classical nMOS device; the nonlinear behavior. On-wafer measurements, accurate characterization and robust extraction methodologies were employed to show the better linearity of GCMOS especially for low voltage low power applications. A study of harmonic distortion, 1-dB compression point and third intercept point for devices operating at low bias conditions shows the capability of GCMOS to manipulate signals of higher power amplitudes with better linear behavior.

The better nonlinear performance is also confirmed for deep sub-micron fully-depleted GCMOS devices compared to classical nMOS devices over a wide range of operation, in linear and in saturation regimes of operation. In addition, this better performance is shown, experimentally, to be valid at temperatures as high as 200^{o}C.

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CHAPTER 6

THERMAL NOISE CHARACTERIZATION

THE word *noise* is frequently used in the common spoken language. It is difficult to trace the origin of this word, however, it is commonly referred to in etymology references to date to the 13th century (Middle English), from the Anglo-French "disturbance" [1]. In the early 13th century, the word *noise* was used with the meaning of "loud outcry, clamor, shouting." In Old French[1], *noise* was used to mean "uproar, brawl" (in modern French[2] it is only used in the phrase "chercher noise" which means "to pick a quarrel"). Apparently, it also has roots from the classical Latin[3] "nausea" meaning "disgust, annoyance, discomfort," or literally "seasickness". Another theory traces the Old French word to classical Latin "noxia" which means "hurting, injury, damage." Oxford English Dictionary considers that "the sense of the word is against both suggestions," but "nausea" could have developed a sense in Vulgar Latin[4] of "unpleasant situ-

[1]Old French: the French language as written and spoken between 900-1400. More than 90 percent of it was from Vulgar Latin, with a smattering of Celtic and Germanic, plus some Medieval Latin learned terms (Medieval Latin: Latin as written and spoken approximately in the period 700-1500).
[2]Modern French: Romance language spoken chiefly in France.
[3]Classical Latin: the Italic language of ancient Rome until about the 4th century.
[4]Vulgar Latin: the everyday speech of the Roman people, as opposed to literary Latin.

ation, noise, quarrel". It is also related to the Old Provençal[5] "nauza" meaning "noise, quarrel" [2].

It is also difficult to trace the word *noise* in the scientific literature. The word *noise* started to be extensively used within the scientific community in the second half of the nineteenth century. Noise represented a problem to scientists while conducting the "Reaction experiment with Hipp chronoscope" which is one of the classical experiments in modern psychology (1860–1890), where the problem of noise was explicitly reported in 1890 by Hugo Münsterberg (1863–1916) and other psychologists complaining that environmental noise filtered into their laboratories and disrupted work [3]. The noise pollution was a main concern in the period of 1870-1914, and received an intensive attention in medical and environmental periodicals, especially by Neurologists and ear specialists [4]. As from 1914, the word *noise* started to appear in electrical and mechanical engineering literature [5–8]. From 1923, it entered the literature of telecommunications [9–11].

The first appearance of the word *noise* in the literature of electronics could be attributed to W. Schottky in 1918 when he first discussed the shot noise in different electrical conductors [12][6,7]. During the following decade, this was the only type of noise being studied and many publications appeared to describe this phenomenon and to characterize and measure it [16–30][8]. In 1928, S. Ballantine introduced the first study of high-frequency shot noise [27].

Thermal noise did not appear until January 1927, when J. B. Johnson published a short note in *Nature* that described the phenomenon and characterized it [32][9]. In 1928, both J. B. Johnson and H. Nyquist published at the same time other studies that put for the first time the formula which is still used till now and known as Nyquist formula [33, 34]. They showed that the limiting factor for the performance of receiver circuits was not the tubes, but the resistances, due to the thermal noise produced by them.

In 1930, F. B. Llewellyn presented "a study of noise in vacuum tubes and attached circuits" where he considered three types of noise: shot noise, thermal noise and generation-recombination noise; theoretically and experimentally [35][10]. At around the same time, S. Ballantine studied the fluctuation noise (RF noise) in the receiver circuits [37]. He also introduced a new method for measur-

[5]Old Provençal: Romance language of the troubadors, spoken in southern France before approximately 1500.

[6]J. A. Gubner reported in [13] that the most basic shot-noise statistics, namely the mean and variance, were reported by Campbell in 1909 [14, 15]

[7]The definition of the different types of noise, like shot noise, will be presented in the following sections.

[8]This bibliography ([12, 16–30]) is based on the bibliography introduced by N. P. Case [31].

[9]In [33], J. B. Johnson cites another short note published in Phys. Rev. vol. 29 p. 367, Feb. 1927, and another short note published by H. Nyquist in Phys. Rev. vol. 29 p. 614, 1927, however the author could not retrieve neither of them.

[10]In 1928, H. T. Friis proved experimentally that thermal-agitation noise (Johnson noise) determined the absolute sensitivity of short-wave radio receivers in an unpublished report according to [36].

ing the merit of a receiving system with regard to its signal-to-noise ratio, where this later term was introduced for the first time[11]. The term "Signal-to-Noise ratio" was then emphasized later by F. B. Llewellyn in 1931 who introduced a rapid method for the calculation of the Signal-to-Noise ratio for high gain receivers [38].

Few months later, the concept of reducing the noise in receivers (to be known later as Low Noise Amplifier - LNA) was introduced by N. P. Case in 1931 [31]. However, the first LNA was not published until 1949 by H. S. Sommers *et al.* [39].

In 1933, S. Ballantine studied the fluctuation noise in electronic amplifier tubes [40]. In 1946, Kompfner *et al.* introduced the first noise source based on a transmission-line diode working at centimeter wavelengths [41].

It was not until 1944 that H. T. Friis from Bell Telephone Laboratories in New York introduced the concept of "Noise Figure" [36]. However, according to H. T. Friis himself, his work was based on a "Noise Factor" introduced by D. O. North two years earlier [42]. In an interesting discussion published one year later, D. O. North and H. T. Friis were not able to agree on which term to use, "Noise Factor" or "Noise Figure" [43]! D. K. C. MacDonald also published a comment on these two definitions later in [44]. However, according to M. J. O. Strutt [45], some similar definitions to that of H. T. Friis had already been introduced between 1939 and 1943 by K. Fraenz [46, 47], W. Kleen [48], H. Rothe [49], M. J. O. Strutt, A. van der Ziel [50, 51], E. W. Herold and L. Malter [52]. Nevertheless, M. J. O. Strutt continued to use the definition introduced by H. T. Friis [36, 45] and it has kept being used till now!

6.1 WHAT IS NOISE?

This work is concerned by the noise in the electronic components like transistors, and more precisely the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). In this section, some definitions will be given as cited by several publications over the years. This is naturally followed by the introduction of the different types of noise that exist in MOSFETs.

6.1.1 Definition

Generally, noise could be defined as:

- Any unwanted sound. And in analog and digital electronics, noise is an unwanted perturbation to a wanted signal (Wikipedia) [53].

- A sound, especially one that is loud, unpleasant, or disturbing / continuous or repeated loud, confused sounds / technical: irregular fluctuations

[11] F. B. Llewellyn spoke about "the ratio of signal to noise" in [35], but not in an explicit way as did S. Ballantine in [37].

accompanying and tending to obscure an electrical signal (Oxford English Dictionary) [54].

– Any bad change in a signal, especially in a signal produced by an electronic device (Cambridge Dictionary) [55].

– Loud, confused, or senseless shouting or outcry / any sound that is undesired or interferes with one's hearing of something / an unwanted signal or a disturbance (as static or a variation of voltage) in an electronic device or instrument (as radio or television) / a disturbance interfering with the operation of a usually mechanical device or system / electromagnetic radiation (as light or radio waves) that is composed of several frequencies and that involves random changes in frequency or amplitude / irrelevant or meaningless data or output occurring along with desired information (Merriam-Webster Dictionary) [1].

These definitions are not far from what A. van der Ziel presented [56]. Van der Ziel referred to the spontaneous fluctuations in current, voltage, and temperature of a system under test as being noise. Van der Ziel gave a simple explanation. If the fluctuating voltage or current generated in an electronic device or circuit component is amplified by a low-frequency amplifier and the amplified signal is fed into a loudspeaker, the loudspeaker produces a hissing sound; that is why it is called *noise*. This applies to any fluctuating voltage or current, even if no audible sound is heard, as in the case of a "snowy" picture on a television screen, or the lower limit of a measurement instrument.

6.1.2 Types of Noise

There are four main types of noise sources related to MOSFET devices, which are basically the same for most of the other electronic components. These are thermal, shot, generation-recombination, and flicker noise sources.

The thermal noise is related to the fluctuations (or random motion) of carriers velocity occurring in a resistor like material. This fluctuation is translated into a fluctuating electromagnetic force (emf) across the terminals of the device. More details about the thermal noise in MOSFETs are given in the next section.

Shot noise is originally defined by Schottky as the fluctuation of current in a tube carrying voltage-saturated thermionic current as a consequence of the random emission (and flow) of electrons [12, 37]. It could also be regarded as being produced by irregularities in the stream of electrons from the filament to the plate of the vacuum tube. In the absence of space charge this noise has been termed by Schottky the "schroteffekt," or "small shot effect," from the analogy which the flight of electrons from the filament to the plate of a vacuum tube bears to the spattering of small shot fired from a shot gun [35]. In modern devices, the shot noise occurs when carriers cross barriers independently and at random, as, for example, in Schottky-barrier diodes, in p-n junctions, and in bipolar transistors [56].

The generation-recombination noise occurs in a semiconductor involving donors, traps, and recombination centers. The number of carriers, and hence the resistance, fluctuates, giving rise to a fluctuating current through the device, thus a fluctuating emf across its terminals.

The fourth type of noise is the flicker noise. The first characteristic of this type of noise is its spectrum density which is inversely proportional to the frequency, hence the name $1/f$ noise. Literature shows two theories on the origin of flicker noise [57]. The first theory, the carrier number fluctuation theory [58–63], also called McWhorter's model since it was originally introduced by A. L. McWhorter in 1957 [64], attributes the flicker noise to the random trapping and releasing processes of charges in the oxide traps near the $Si-SiO_2$ interface. The charge fluctuation results in a fluctuation of the surface potential, which in turn modulates the channel carrier density. It is assumed that the channel can exchange charges with the oxide traps through tunneling. The second theory, the mobility fluctuation theory [65–67], attributes the flicker noise to the fluctuation in the mobility of carriers in the bulk of the device based on an empirical formula introduced by Hooge in 1969 [68–70], hence the theory is also known as Hooge's model. In MOSFETs, it is assumed that this fluctuation of mobility is induced by phonon fluctuations induced by phonon scattering. The number fluctuation theory presumes an independent input noise power of the gate bias while being inversely proportional to the gate capacitance. On the other hand, the mobility fluctuation theory assumes an input noise power proportional to the gate bias and inversely proportional to the gate oxide capacitance. Since in the case of MOSFET, the measured noise power has a more complicated dependence on the gate bias and the gate oxide capacitance, some would use a theory based on combining both the number and the mobility fluctuation theories [57, 71, 72].

6.2 THERMAL NOISE IN MOSFETS

Thermal noise is usually the predominant source of noise in a well designed amplifier [33]. This has been true for amplifiers built using tubes and is also true for amplifiers built using field effect transistors [73, 74]. The rest of this chapter will deal with thermal noise in MOSFETs.

6.2.1 Introduction

> "The electric charges in a conductor are found to be in a state of thermal agitation, in thermodynamic equilibrium with the heat motion of the atoms of the conductor. The manifestation of the phenomenon is a fluctuation of potential difference between the terminals of the conductor which can be measured by suitable instruments."

These were the words by which J. B. Johnson described the thermal noise phenomenon [33, 35]. This phenomenon was discovered by Johnson in 1927 [32], and he called it "Thermal Noise". It was then also known after him as Johnson's

noise. In 1928, Nyquist introduced an analytical formula that quantifies this noise based completely on a theoretical analysis [34] (as opposed to the experimental study of Johnson), thus it is also sometimes known as Nyquist's noise. Nyquist based his reasoning on the principles of thermodynamics and statistical mechanics (especially the second law of thermodynamics), which was shown to agree with the experimental results published earlier by Johnson [33]. Nyquist was able to prove that his formula is valid for any frequency range, stating that the electromotive force due to thermal agitation in conductors is a universal function of frequency, resistance, and temperature and of these variables only. This is summarized in the well known Nyquist relation which describes the thermal electromotive force in a conductor of pure resistance R and of temperature T:

$$E^2 \, \mathrm{d}\nu = 4RkT \, \mathrm{d}\nu \tag{6.1}$$

where $E^2 \, \mathrm{d}\nu$ is the square of the voltage within the frequency interval $\mathrm{d}\nu$, and k is the Boltzmann constant. In another formulation, the available thermal noise power in a frequency interval $\mathrm{d}\nu$ is represented by:

$$P_{\mathrm{av}} = kT \, \mathrm{d}\nu \tag{6.2}$$

Despite the proof that he provided for Nyquist's formula of P_{av} as a universal function of the temperature T, van der Ziel was convinced that a quantum correction is needed if hf is comparable to kT, with h being Planck's constant [75],[56, Ch. 5]. For high frequencies and low temperatures, van der Ziel's formula is written as:

$$P_{\mathrm{av}} = \left[\frac{1}{2} hf + \frac{hf}{e^{hf/kT} - 1} \right] \Delta f \tag{6.3}$$

This formula reduces to Nyquist's formula (6.2) for $hf/kT \ll 1$

During the 50's, van der Ziel, as well as a group of other scientists, focused on the thermal and the shot noises in junction diodes and junction transistors [76–82]. Then starting from the early 60's, van der Ziel turned his attention to Field-Effect Transistors (FETs) or more specifically, Junction-FETs (JFETs) [73, 74, 83–85]. Being a modulated conductance, the thermal noise in the channel of a MOSFET was shown to be the dominant noise mechanism. Van der Ziel introduced equations representing the channel noise current, the gate noise current and the correlation between them as being a capacitive coupling through the gate. His work was the basis for several works introduced later and the ranges of the values of the constants in his equations are still applicable in modern devices, as will be shown later [83].

6.2.2 Different Representations

As the noise in electronic devices and circuits started to gain more attention, a need was raised to correctly represent and account for noise in devices and circuits. The traditional theory of four-poles only represents the electrical characteristics of the network under consideration through voltage and current equations

based on the internal sinusoidal currents or voltages of the network. However, the information about the noise behavior of the network was still missing. In 1956, Rothe and Dahlke first introduced the theory of noisy four-poles [86]. This theory was later standardized by the *IRE*[12] in the tutorial paper by H. A. Haus *et al.* in 1960 [87].

The idea is to separate the classical noiseless network from the noise sources of the network. Assume that the network in Fig. 6.1 is a noisy network. Classically, this network would be electrically characterized by the following equations:

$$\begin{aligned} I_1 &= Y_{11}V_1 + Y_{12}V_2 \\ I_2 &= Y_{21}V_1 + Y_{22}V_2 \end{aligned} \tag{6.4}$$

or by:

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \end{aligned} \tag{6.5}$$

depending on which representation is chosen (admittance representation (6.4) or impedance representation (6.5)).

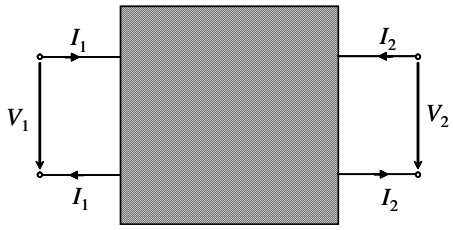
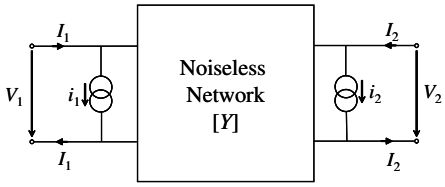


Fig. 6.1.: A noisy two-port (four-pole) network.

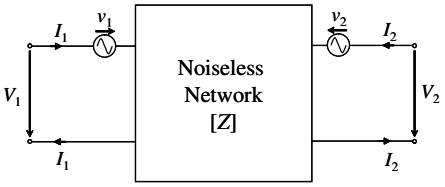
The noise of this two-port network is observed as fluctuations of voltage (or current) at the terminals of the network. This results from the internal noise sources of the network. A simple way to characterize these noise sources is to characterize the observed fluctuations at the terminals only. This can simply be achieved by considering a noiseless network corresponding to the same network but without any noise sources, and adding two noise sources outside the network. This could be two noise current sources (one at the input and one at the output of the noiseless network), two noise voltage sources (one at the input and one at the output of the noiseless network), or one noise current source and one noise voltage source (both at the input of the noiseless network), as shown in Fig. 6.2.

The current-current representation shown in Fig. 6.2a is used in conjunction with a noiseless network represented by its admittance matrix. The voltage-voltage representation shown in Fig. 6.2b is used with an impedance matrix

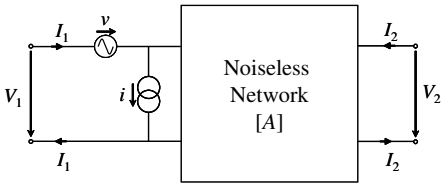
[12] A new industry arose beginning with Guglielmo Marconi's wireless telegraphy experiments at the turn of the century. What was originally called "wireless" became "radio" with the electrical amplification possibilities inherent in the vacuum tubes which evolved from John Fleming's diode and Lee de Forest's triode. With the new industry came a new society in 1912, the Institute of Radio Engineers (*IRE*). More information on: http://www.ieee.org/about/ieee_history.html



(a) Current-current representation.



(b) Voltage-voltage representation.



(c) Current-voltage representation.

Fig. 6.2.: Different representations of a noisy two-port (four-pole) network.

of the noiseless network. Whereas the current-voltage representation shown in Fig. 6.2c is employed in order to have all internal noise sources represented at the input of the noiseless network. The later is believed to be the most convenient method for noise characterization. In this later case, the noiseless network is represented using its chain matrix:

$$\begin{aligned} I_1 &= AV_2 + BI_2 \\ V_2 &= CV_2 + DI_2 \end{aligned} \tag{6.6}$$

Equations (6.4)-(6.6) can then be modified in order to include the noise sources and can be written as follows:

For current-current representation:

$$\begin{aligned} I_1 &= Y_{11}V_1 + Y_{12}V_2 + i_1 \\ I_2 &= Y_{21}V_1 + Y_{22}V_2 + i_2 \end{aligned} \tag{6.7}$$

For voltage-voltage representation:

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 + e_1 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 + e_2 \end{aligned} \tag{6.8}$$

For current-voltage representation:

$$\begin{aligned} I_1 &= AV_2 + BI_2 + i \\ V_2 &= CV_2 + DI_2 + e \end{aligned} \tag{6.9}$$

There are three basic principles for dealing with these representations:

– Since the noise phenomenon is a random process, the noise sources are usually characterized by their spectral and cross spectral densities rather than by their absolute values (voltage or current) i.e. $\overline{e^2}$, $\overline{i^2}$ and $\overline{ei^*}$.
– The second principle is to consider a correlation factor between the two noise sources employed in the two-port network. It could also be useful to consider the noise source as composed of two parts; one which has no correlation with the other noise source and the other which is correlated by a correlation factor (usually complex, in the form of $Y_{\rm cor} = G_{\rm cor} + jB_{\rm cor}$) to the other source.
– A noiseless network connected to the terminals of a noisy network does not change the signal-to-noise ratio (or the noise factor) calculated at these terminals, thus the noise factor of the over-all network is equal to that of the noisy network[13].

The spot noise factor (figure) of a network at a specific frequency is defined by the ratio of the output noise power per unit bandwidth available at the output port to the portion of that output noise power engendered by the input termination at the standard temperature T_0 (290 K) [36, 88].

Therefore, if the current-voltage representation is considered, the noise factor at the output terminals should be the same as the noise factor at the input terminals of the noiseless network. Thus, if a current source is connected to the input terminals, it is sufficient to consider the network shown in Fig. 6.3 to calculate the over-all noise factor of the entire network of Fig. 6.2c.

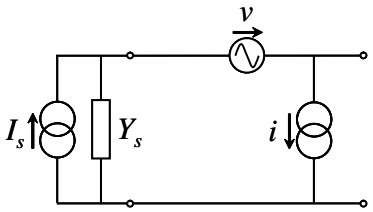


Fig. 6.3.: Current-voltage representation in cascade with a current source of internal admittance $Y_{\rm s}$.

The noise factor is then calculated to be [87]

$$NF = NF_{\rm min} + \frac{R_n}{G_{\rm s}}\left[(G_{\rm s} + G_{\rm opt})^2 + (B_{\rm s} - B_{\rm opt})^2\right] \tag{6.10}$$

where NF is the noise factor, $NF_{\rm min}$ is the minimum noise factor that is achieved when the source admittance $Y_{\rm s} = G_{\rm s} + jB_{\rm s}$ attains its optimum value of $Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt}$, and R_n is the equivalent noise resistance which is defined by

[13]This is only true under the condition of equal impedances at the terminals, otherwise, the noise factor (or the noise figure) is changed but the minimum noise figure stays the same.

Nyquist's formula

$$R_n = \frac{\overline{e^2}}{4kT_0\Delta f} \tag{6.11}$$

knowing that R_n is not the resistance of a physical resistor in the network in which e is a physical noise voltage and therefore does not appear as a resistance in the equivalent circuit of the network. It rather helps to have a direct comparison between the noise due to internal sources and the noise of resistances generally presented in the circuit. R_n also characterizes the rapidity with which NF increases above $NF_{\min}$ as Y_s deviates from Y_{opt} (the mismatch between Y_s and Y_{opt}).

From (6.10), the knowledge of only four parameters can fully characterize the noise behavior of a two-port network, namely $NF_{\min}$, R_n, and Y_{opt} ($Y_{opt} = G_{opt} + jB_{opt}$). These four parameters are readily obtained from standard noise measurements. The use of this representation (Fig. 6.3) also has the advantage that it does not require the knowledge of the physical origin of all the internal noise sources of the network.

In 1976, Hillbrand and Russer introduced the correlation matrix concept [89][14] which can deal with two-port networks that include partially correlated noise sources, as is the case of MOSFETs. The correlation matrix concept is based on the circuit theory of linear noisy networks, where the noise in linear circuits is described in terms of correlation matrices instead of voltages and currents. The philosophy behind this method is simple. The two-port is considered as an interconnection of basic two-ports whose noise behavior is known. The analysis then proceeds by interconnecting simpler two-ports to more complicated two-ports until finally the noise performance of the original two-port is obtained. The noiseless part of the two-port network is described by the conventional electrical matrices (Y, Z, or A), whereas the noisy part of the two-port network is described by its correlation matrix. In the noisy part, the noise sources are usually represented by their mean square fluctuations in a bandwidth Δf centered around a frequency f. For two noise sources s_1 and s_2, these mean square fluctuations are directly related to the power spectral densities by

$$\left\langle s_i s_j^* \right\rangle = 2\Delta f C_{s_i s_j^*} \qquad i,j = 1,2 \tag{6.12}$$

where the factor 2 denotes a frequency range from $-\inf$ to $+\inf$. The correlation matrix C corresponding to the noise sources s_1 and s_2 is given by

$$C = \frac{1}{2\Delta f}\begin{bmatrix} \langle s_1 s_1^* \rangle & \langle s_1 s_2^* \rangle \\ \langle s_2 s_1^* \rangle & \langle s_2 s_2^* \rangle \end{bmatrix} \tag{6.13}$$

In the case of passive elements, the correlation matrix is written as

$$C = 2kT\begin{bmatrix} Z_{11} + Z_{11}^* & Z_{12} + Z_{12}^* \\ Z_{21} + Z_{21}^* & Z_{22} + Z_{22}^* \end{bmatrix} \tag{6.14}$$

[14]The rest of this sub-section is mostly based on this reference ([89]).

which can be simplified using the symmetric reciprocity proposed by R. Q. Twiss [90, 91], i.e. $Z_{12} = Z_{21}$, so that the noise correlation matrix can simply be given in terms of its impedance or admittance electrical matrices as follows

$$\begin{aligned} C_Z &= 2kT\Re\{Z\} \\ C_Y &= 2kT\Re\{Y\} \end{aligned} \tag{6.15}$$

In the case of active devices, the noise correlation matrix can be defined using the noise equivalent circuit. For example, in the case of a MOSFET, the noise correlation matrix can be given for the current-current representation as:

$$C = \frac{1}{2\Delta f}\begin{bmatrix} \langle i_g i_g^* \rangle & \langle i_g i_d^* \rangle \\ \langle i_d i_g^* \rangle & \langle i_d i_d^* \rangle \end{bmatrix} = \frac{1}{2\Delta f}\begin{bmatrix} \langle i_g^2 \rangle & \langle i_g i_d^* \rangle \\ \langle i_d i_g^* \rangle & \langle i_d^2 \rangle \end{bmatrix} \tag{6.16}$$

It can also be given for the current-voltage representation and based on direct measurements giving the four noise parameters defined earlier ($NF_{\min}$, R_n, and Y_{opt}) as follows:

$$\left[C_A\right] = \begin{bmatrix} \overline{e^2} & \overline{ei^*} \\ \overline{e^* i} & \overline{i^2} \end{bmatrix} = 4kT_0\Delta f \begin{bmatrix} R_n & \dfrac{NF_{\min}-1}{2} - R_n Y_{\text{opt}}^* \\ \dfrac{NF_{\min}-1}{2} - R_n Y_{\text{opt}} & R_n \left|Y_{\text{opt}}\right|^2 \end{bmatrix} \tag{6.17}$$

The noise figure is then simply calculated using

$$NF = 1 + \frac{z^+ C_A z}{2kT\Re\{Z_{\text{s}}\}} \tag{6.18}$$

where

$$z = \begin{bmatrix} 1 \\ Z_{\text{s}}^* \end{bmatrix} \tag{6.19}$$

and Z_{s} is the source impedance whereas the '+' sign indicates the Hermitian conjugation (i.e. transposed conjugate)

Next, for interconnecting the different simple two-port networks to reconstruct the original two-port network, the correlation matrices are simply manipulated using:

$$C_Y = C_{Y1} + C_{Y2} \quad \text{(parallel)} \tag{6.20}$$

$$C_Z = C_{Z1} + C_{Z2} \quad \text{(series)} \tag{6.21}$$

$$C_A = A_1 C_{A2} A_1^+ + C_{A1} \quad \text{(cascade)} \tag{6.22}$$

where A is the electrical chain matrix. The need may arise to pass from one representation to another. This is simplified through the use of Appendix C and Appendix D.

Therefore, the correlation matrix concept makes the noise analysis of any two-port network as simple as the combination of three operations: change of representation, interconnection, and noise figure calculation. As a result, this concept is extensively used in literature for noise analysis. Equation (6.22) is usually used in de-embedding procedures especially for on-wafer measurements.

6.3 MODELS OF THERMAL NOISE

The modeling of thermal noise has always been a challenge. Any model should be based on a deep understanding of the phenomenon and a correct representation of it. Since the introduction of the thermal noise term in the literature of electronics by Johnson and Nyquist [32–34], many publications tried to build a thorough understanding. The effort to understand shot noise served as a good base. Also the pioneering work of Rothe and Dahlke [86] in representing the noisy four-pole networks and later the standardization of these representations by the *IRE* led by Haus *et al.* [87] were all a necessary start.

In 1962 and 1963, van der Ziel first introduced an understanding and a modeling of the thermal noise in Field-Effect Transistors (FETs) [73, 74, 83, 84]. His work was concentrating on Junction Field-Effect Transistors JFETs and was based on the treatment of the small-signal parameters published later by van der Ziel and Ero in 1964 [85]. Van der Ziel and Ero adopted the theory of Shockley that assumed a constant mobility throughout the channel, even in saturation (pinched off) region, and they considered the region under the gate as an active nonuniform transmission line. They then solved the resulting nonlinear wave equation using a power series in frequency. The result was an accurate quantitative expression for the intrinsic two-port small-signal parameters applicable to moderately high frequencies. Van der Ziel identified the thermal noise in the channel as the main source of noise in FETs. He then derived expressions for the drain current and induced gate current noise and the correlation between them using a Green's function solution for the thermal voltage fluctuation distribution along the channel. Van der Ziel stated that the correlation between the two current noise sources should be pure imaginary.

Later, in 1966, M. Shoji presented the first work on MOSFETs [92] to be an extension of the work of van der Ziel on JFETs and of the work of A. G. Jordan and N. A. Jordan on shot and flicker noises in MOSFETs [93]. Around the same time, C. T. Sah *et al.* also studied the thermal noise in MOSFETs [94].

A year later, F. M. Klaassen and J. Prins introduced their well known model of thermal noise in MOSFETs [95]. They showed in a series of publications an extension of the model of van der Ziel to higher frequencies [95–99]. However, they showed a complex correlation between the two current noise sources (the drain current noise source and the gate induced current noise source) due to the influence of the high frequency gate-channel coupling on the noise of the drain current. This effect was earlier neglected by van der Ziel. It was shown later that this effect is important only beyond the useful frequency range of operation of FETs [100]. Also in 1967, J. Mavor presented a theory about a lower noise behavior of MOSFETs operated in a common-gate configuration [101]. It seems that all this attention given to MOSFETs encouraged A. van der Ziel to turn his attention to MOSFETs. In 1968, in a joint work with H. E. Hallady [102], they introduced a modification of the equations of Klaassen-Prins and in 1969, A. van der Ziel classified the theories of J. Mavor as an incorrect hypothesis [103]. A. van der Ziel then continued to introduce a series

of pioneering work on the modeling of thermal noise in MOSFETs [104–109] taking into account the different representations of noisy two-port networks and the calculation of the noise figure and the minimum noise figure for MOSFETs. Based on this pioneering work more models were introduced later on. In 1971-1972, W. Baechtold was the first to consider the velocity saturation effects on the noise performance of microwave FETs [110, 111]. He combined the effort of A. van der Ziel in thermal noise and the Turner-Wilson model [112] (the first to introduce the concept of velocity saturation in FETs) to derive the noise coefficients as a function of velocity saturation. Although W. Baechtold included a field-dependent noise temperature to account for the "hot" electrons, his model suffered from the same limitations of Turner-Wilson model, which presumes that the critical field for velocity saturation is always located (pinned) at the drain side of the channel. Hence, the model of W. Baechtold neglects any noise that may be generated by carriers traveling at their limiting velocities.

6.3.1 Three-parameter model

In 1974, R. A. Pucel *et al.* introduced the model to be known later by the three-parameter model or the PRC model [100, 113, 114]. In his model, R. A. Pucel abandoned the Turner-Wilson model. Instead, he adopted the two-section model of Grebene-Ghandhi [115]. In his model, he considered the dc, small-signal, and the noise characteristics of the GaAs FET. Below velocity saturation, R. A. Pucel based his model on A. van der Ziel's model with suitable modifications to account for the variable boundary position between the two regions. He also adopted the modifications of W. Baechtold to account for the electron temperature. He then introduced a new model for the velocity saturation region (saturation or depletion region). He showed that the noise in that later region can be very important and that the noise in the unsaturated region becomes negligible. P. Lauritzen and O. Leistiko Jr. observed the same phenomenon in 1962 through noise measurements and related it to the high electric field in the pinch-off region [116]. R. A. Pucel also showed that a strong correlation exists between the drain and the gate which results in a strong noise cancellation and hence an attractively low minimum noise figure.

This noise model considers the current-current representation of the FET device, with a gate noise current source i_g (induced gate noise) at the input and a drain noise current source i_d at the output, whose spectral densities are proportional to noise dimensionless coefficients R and P, respectively. These two noise sources are correlated, with a pure imaginary complex correlation coefficient $Cor = j.C$, explained by the capacitive coupling existing between the channel and the gate (C is referred to as the correlation coefficient). For a recent technology node (gate length $\geqslant$ 65 nm) of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), either in bulk or in Silicon-on-Insulator (SOI) technologies, the value of C is relatively weak (lower than 0.4) [117–119], in contrast to those usually observed in the case of III-V FETs or HEMTs (between 0.8 and 0.95) [114].

6.3.2 Two-parameter model

In 1989, M. W. Pospieszalski proposed a two-parameter noise model [120, 121]. In this model, two uncorrelated noise sources are considered; a gate noise voltage source at the input and a drain noise current source at the output. The spectral densities of these two noise sources are proportional to the equivalent noise temperatures T_g (for the input - the gate) and T_d (for the output - the drain), respectively. The extraction of the equivalent noise temperature T_g is relatively difficult. This is because its accuracy depends strongly on the accuracy of the extraction of the intrinsic resistance R_{i} of the small signal equivalent circuit of the transistor [122]. Measurement uncertainties and errors in extracting the extrinsic resistances could highly affect the accuracy of extracting R_{i}. To overcome this problem, F. Danneville and G. Dambrine introduced the following definitions of T_{in}(instead of T_g) and T_{out}(instead of T_d):

$$T_{\mathrm{in}} = \frac{\overline{e_g^2}}{4k\Re(H_{11})\Delta f} = \frac{\overline{e_g^2}}{4k\Re\left(\dfrac{1}{Y_{11}}\right)\Delta f} \tag{6.23}$$

$$T_{\mathrm{out}} = \frac{\overline{i_d^2}}{4k\Re(H_{22})\Delta f} = \frac{\overline{i_d^2}}{4k\Re\left(\dfrac{1}{Z_{22}}\right)\Delta f} \tag{6.24}$$

Equation (6.24) can also be expressed in terms of the elements of the small signal equivalent circuit as:

$$T_{\mathrm{out}} \approx \frac{\overline{i_d^2}}{4kg_D\left[1+\dfrac{g_m}{g_D}\dfrac{C_{\mathrm{gd}}}{C_{\mathrm{gd}}+C_{\mathrm{gs}}}\right]\Delta f} \tag{6.25}$$

Based on (6.25), F. Danneville and G. Dambrine concluded that T_{out} is lower (by a factor of 2 to 3) than T_d defined by M. W. Pospieszalski. Hence, for $V_{\mathrm{DS}} = 0$ V, the transconductance g_m becomes equal to zero and as a result it is found that $T_{\mathrm{out}} = T_d = T_{\mathrm{a}}$. This leads to the one-parameter model discussed in the next sub-section.

6.3.3 One-parameter model

In 1991, B. Hughes proposed the "temperature noise model for extrinsic FETs", or simply a one-parameter model [123]. He used the assumption proposed earlier by M. Gupta and P. T. Greiling [124] and set the input (gate) temperature T_g in Pospieszalski's model to the ambient temperature T_{a}. B. Hughes was able to show that this simple model can predict accurately the frequency dependence of the minimum noise figure NF_{min} and the associated gain G_{ass}. It is also possible to predict the maximum oscillation frequency f_{max} based on the noise measurements and B. Hughes showed that this prediction is also accurate enough. This was shown to be true for a wide variety of FET devices [123].

6.3.4 Summary

Despite the differences between the models introduced earlier, it is of interest to highlight some common features of all thermal noise models [125]:

- The power spectral density of the drain noise current source $\overline{i_d^2}$ is frequency independent. This is explained by the fact that the drain noise current source is generated by diffusion noise in the channel, which has a white spectrum as shown experimentally by W. C. Bruncke *et al.* [126] and analytically by A. van der Ziel [83].
- The gate noise current source i_g results from the channel noise, and because of the capacitive coupling existing between the channel and the gate, it varies as a function of $j\omega$ (where ω is the radial frequency and equals $2\pi f$). The power spectral density $\overline{i_g^2}$ is therefore a function of the frequency squared [116, 126].
- Based on this capacitive coupling, the correlation between the two noise sources is mainly imaginary (the real part is negligible) [73]. In addition, the correlation being represented as $\overline{i_g^* i_d}$ varies as $j\omega$, or in other words, it increases linearly with frequency.

6.4 THERMAL NOISE MEASUREMENTS

The process of thermal noise measurement in FETs in general is difficult and complicated. Over the years, several methods and approaches were introduced in literature to overcome the difficulties and to provide more accurate results. As early as 1953 and later in 1959, the committee of the *IRE* introduced a standardization of noise measurement methods [127, 128]. Later, several authors introduced variations on these standard methods as well as entirely new methods. In this section, the two most used methods are to be introduced, namely the Tuner method and the F50 method.

6.4.1 Concept

Thermal noise is classified as a Gaussian noise. A Gaussian noise has steady or stationary characteristics and is composed of a linear superposition of a large number of small independent events. For any Gaussian noise, a measurement in terms of power is usually comprehensive and adequate [128]. It is particularly important to highlight the assumption of linearity for such type of measurements. The noise event usually occurs at a point of the system where the useful signal is weak; hence the principle of superposition can be correctly applied. In practical terms, currents and voltages produced by signals and noise can be added together without taking into consideration the harmonics and inter-modulation effects that occur in nonlinear systems.

The noise measured at the output of any linear two-port is the summation of two noise sources; the noise coming from the source (i.e. the noise at the input of the two-port) and the noise source internal to the two-port. If the two-port is

noiseless, the noise signal at its input terminal (coming from the source) should travel to its output terminal without suffering from any change. Based on this concept, the idea of measuring the noise performance of any linear two-port resides in measuring the noise power at the output terminal of the two-port and the noise power at the output terminal of its noiseless equivalent, which is an imaginary case in which the two-port keeps all its characteristics except that it has no internal noise sources. This concept is simply formulated by what is known as the Noise Figure, defined as [128]: The ratio of: (a) the noise power per unit bandwidth available at the output port when the noise temperature of the input termination is standard (290K) to (b) the portion of (a) engendered at the input frequency by the input termination.

Based on this definition, the noise figure is a function of two factors: the internal structure of the two-port and its input termination. On the other hand, it is independent of the output termination. Therefore, the noise performance of a two-port is only obtained if the input termination is correctly specified.

The standard formula of the noise figure NF is given by (6.10) and can simply be written as [129]:

$$NF = NF_{\min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2 \tag{6.26}$$

with

$$NF_{\min} = 1 + 2R_n (G_{opt} + G_{cor}) \tag{6.27}$$

where G_{cor} is the real part of the correlation admittance Y_{cor}.

This simple equation sets the base for all noise measurement methods. The target is to be able to calculate or measure the four parameters of (6.26) that fully characterize the noise performance of any FET; $NF_{\min}$, R_n, and Y_{opt}.

6.4.2 Tuner Method

This method is also known in literature as the multi-impedance method or the traditional method. The later name being given since this was the measurement method used for so many years and standardized by the *IRE* committee [128].

The basic idea of this method is to use a variable impedance source in front of the Device-under-Test (DUT) and to measure the corresponding noise figure (or noise power) at the output. These data are then used to search for the minimum noise figure $NF_{\min}$ and the corresponding source admittance Y_{opt}, and then use (6.26) to find the equivalent noise resistance R_n. In modern systems, an automatic variable admittance generator is used in conjunction with an automatic noise figure meter, thus making the measurement procedure simpler. However, this method has its limitations and difficulties especially for the calibration step.

In its original form, the measurement is achieved in three main steps [128]:

- The source conductance G_s is kept constant while the source susceptance B_s is varied and the noise figure NF is measured for each value of B_s. The optimum source susceptance B_{opt} is then determined as being the value corresponding to the minimum obtained NF.

- Similarly, the optimum source conductance G_{opt} is obtained by fixing the source susceptance B_{s} at its optimum value B_{opt} and measuring the noise figure NF for different values of the source conductance G_{s}.
- Equation (6.26) is then used to obtain R_n and $NF_{\min}$ by plotting NF as a function of $x = |Y_{\text{s}} - Y_{\text{opt}}|^2 / G_{\text{s}}$. The result is a straight line ($NF = NF_{\min} + R_n x$) whose slope is R_n and its intersection on the NF axis at $x = 0$ gives $NF_{\min}$.

Two techniques exist for the Tuner measurement method; the standard technique [130] and the cold source technique [131, 132]. In the first technique, a noise source is connected to the input of the DUT. This noise source is first used in its cold state (equivalent temperature T_{C}) then in its hot state (equivalent temperature T_{H}). The corresponding noise powers are measured and used to calculate the Noise Figure of the DUT. Whilst in the second technique, the noise source is only necessary during the calibration phase in order to determine the kBG coefficient (Gain-Bandwidth product) of the noise receiver. A Tuner is connected to the input of the DUT to generate different impedances during the phase of the NF measurements. The thermal noise of the Tuner (proportional to the ambient temperature and the resistive or real part of the generated impedance) amplified by the DUT and the additional noise power generated by the DUT are measured by the receiver. The NF of the DUT is then calculated knowing the generated impedance at its input, the S-parameters of the DUT and the reflection coefficient at the input of the noise receiver. This later method is adopted in the Tuner measurements shown in this work.

Mostly, modern Tuner measurement systems perform the measurement steps and the associated calculations automatically. However, this method suffers from the following limitations [124, 125]:

- The mounting of the measurement system is not simple.
- The system requires complicated calibration steps.
- The choice of the source admittance values is very critical.
- Accuracy of associated numerical analysis is not guaranteed.
- Elevated cost of measurement equipments.

These limitations motivated many research groups to search for an alternative method to measure high frequency noise, such as the F50 method, presented hereafter.

6.4.3 F50 Method

The Tuner method is still used both on the academic and the industrial levels. Commercial equipments are still being enhanced to give better accuracy for noise measurements using the Tuner method. Nevertheless, many publications tried, as early as 1969, to overcome the limitations and complications of this traditional method [124, 133].

In this context, G. Dambrine *et al.* introduced the F50 method in 1993 [125]. It was first introduced for MESFETs and HEMTs, but was proved later to be

applicable on MOSFETs. This method is based on the fact that the number of noise parameters can be reduced if simple theoretical considerations are taken into account.

Based on the work by H. Hillbrand and P. H. Russer [89], G. Dambrine *et al.* presented the relation between the voltage-current representation of noise sources and the current-current representation as follows:

$$\overline{e^2} = \frac{\overline{i_d^2}}{|Y_{21}|^2} + 4kT_0\left(R_\mathrm{s} + R_\mathrm{g}\right)\Delta f \tag{6.28}$$

$$\overline{i^2} = \overline{i_g^2} + \frac{|Y_{11}|^2\,\overline{i_d^2}}{|Y_{21}|^2} - 2\Re\left(\frac{Y_{11}\overline{i_g^* i_d}}{Y_{21}}\right) \tag{6.29}$$

$$\overline{e^* i} = \frac{Y_{11}\overline{i_d^2}}{|Y_{21}|^2} - \frac{\overline{i_g i_d^*}}{Y_{21}^*} \tag{6.30}$$

Note that, these are basically the equations that constitute the chain matrix in (6.17).

From (6.28)-(6.30), the equivalent noise resistance R_n and the correlation admittance Y_cor could be defined as:

$$R_n = \frac{\overline{e^2}}{4kT_0\Delta f} = \left(R_\mathrm{g} + R_\mathrm{s}\right) + \frac{\overline{i_d^2}}{4kT_0\,|Y_{21}|^2\,\Delta f} \tag{6.31}$$

$$Y_\mathrm{cor} = \frac{\overline{e^* i}}{\overline{e^2}} = \frac{\left(Y_{11}\overline{i_d^2} - Y_{21}\overline{i_g i_d^*}\right)}{4kT_0 R_n\,|Y_{21}|^2\,\Delta f} \tag{6.32}$$

Using (6.29), Y_cor can be approximated by:

$$Y_\mathrm{cor} \approx Y_{11} - \frac{\overline{i_g i_d^*}}{4kT_0 R_n Y_{21}^* \Delta f} \tag{6.33}$$

For operating frequencies lower than the intrinsic cutoff frequency f_T of the device, where

$$f_T = \frac{g_m}{2\pi C_\mathrm{gs}} \tag{6.34}$$

the magnitude of Y_{21} is nearly equal to the transconductance g_m. Therefore, the equivalent noise resistance R_n is frequency-independent.

As for the correlation admittance $Y_\mathrm{cor} = G_\mathrm{cor} + jB_\mathrm{cor}$, from (6.33):

- B_cor is much larger than G_cor [134] due to the fact that the imaginary part B_{11} is larger than the real part G_{11} while $\overline{i_g i_d^*}$ is mainly imaginary and Y_{21} is mainly real. It can also be seen from (6.33) that B_cor increases linearly with frequency.
- G_cor can be approximated by G_{11} because the second term of (6.33) is mainly imaginary. Hence, G_cor is a function of ω^2.

G. Dambrine *et al.* also showed through simulations that G_{opt} is much larger than G_{cor}, and knowing that

$$G_{\text{opt}} = \sqrt{G_{\text{cor}}^2 + \frac{G_n}{R_n}} \tag{6.35}$$

where G_n is the equivalent noise conductance [135], it is clear that G_n/R_n is much larger than G_{cor}^2.

The above theoretical reasoning puts the basis for the F50 method. It can be summarized as follows:

- R_n is frequency independent.
- $G_{\text{cor}} \ll B_{\text{cor}}$ and $G_{\text{cor}} \ll G_{\text{opt}}$.
- $G_{\text{cor}}^2 \ll G_n/R_n$.
- B_{cor} varies as ω and G_{cor} varies as ω^2.

It should also be noticed that these results are valid for any FET device, since they are mainly based on the capacitive coupling between the gate and the channel.

The idea of the method is to introduce a source (generator) of 50 Ω impedance ($Y_{\text{s}} = G_{\text{s}} = 20$ mS). In this case, (6.26) becomes:

$$F_{50} = 1 + R_n G_{\text{s}} + \frac{R_n}{G_{\text{s}}}\left(2G_{\text{s}}G_{\text{cor}} + |Y_{\text{opt}}|^2\right) \tag{6.36}$$

Equation (6.36) has two particular features:

- Since R_n is frequency independent while G_{cor} and $|Y_{\text{opt}}|^2$ vary as ω^2, the plot of F_{50} versus ω^2 is linear and the value of F_{50} at $\omega = 0$ is $(1 + R_n G_{\text{s}})$. Thus, R_n can be easily deduced.
- Since G_{cor} can be approximated by G_{11}, the slope of F_{50} versus ω^2 provides the magnitude of Y_{opt}.

Therefore, one measurement at 50 Ω of source impedance provides two important noise parameters (R_n and $|Y_{\text{opt}}|$) (or in terms of noise sources $\overline{e^2}$ and $\overline{i^2}$[129]).

The advantages of this method can be summarized as:

- The measurement is very simple, no tuner is needed.
- The results are highly accurate since no analytical calculations are needed.
- The accurate determination of R_n is assured which represents a special importance since R_n is directly related to the drain noise current source $\overline{i_d^2}$. Thus the measurement of R_n can be considered as a direct measurement of $\overline{i_d^2}$ which allows a direct comparison of the noise behavior of different devices.
- Since G_{cor} can be approximated by G_{11}, only three noise parameters R_n, G_{opt}, and B_{opt} are needed to describe the FET noise performance. R_n and $|Y_{\text{opt}}|$ are acquired through the F50 measurement and using the 2-parameter model [120], the assumption of uncorrelated noise sources is used to get NF_{min}:

$$C = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \approx j\frac{|Y_{21}|}{|Y_{11}|}\sqrt{\frac{\overline{i_g^2}}{\overline{i_d^2}}} \tag{6.37}$$

Therefore, to determine the four noise parameters ($NF_{\min}$, R_n, and Y_{opt}), five simple steps are needed:

i. S-parameters measurements to extract the small-signal equivalent circuit.
ii. F_{50} is measured versus frequency which gives R_n and $|Y_{\text{opt}}|$ (or simply, $\overline{e^2}$ and $\overline{i^2}$).
iii. $\overline{i_d^2}$ is deduced from $\overline{e^2}$ by using (6.28).
iv. Substituting (6.37) in (6.29), $\overline{i_g^2}$ can be determined.
v. Substituting (6.37) in (6.30), $\overline{e^* i}$ and Y_{cor} can be found.

6.5 THERMAL NOISE IN GCMOS

6.5.1 Introduction[15]

The idea of a Graded-Channel device was first introduced by T. A. DeMassa, G. G. Goddard, and G. T. Catalano in 1971 [136] and 1973 [137]. In 1975, T. A. DeMassa and S. R. Iyer proposed a closed form solution for a Graded-Channel Junction Field Effect Transistor (JFET) [138] and they also introduced a study of the thermal noise in the same device [139]. Later, in 1978, R. E. Williams and D. W. Shaw presented improved linearity and noise figure using a Graded-Channel FET [140]. The RF favoured performance of Graded-Channel devices over classical uniform doping devices was highlighted in 1980 by S. D. S. Malhi and C. A. T. Salama, where they reported a higher cutoff frequency for Graded-Channel FET [141].

The Metal-Oxide-Semiconductor MOS version of the Graded-Channel devices was introduced for the first time in 2000 by M. A. Pavanello *et al.* [142], and since then, it has received an increasing attention. In these academic devices, the implantation used to adjust the threshold voltage V_T is masked near the drain over a distance L_{LD} (Lightly-Doped) (see Fig. 6.4a), yielding a high V_T region near the source in series with a low V_T part adjacent to the drain.

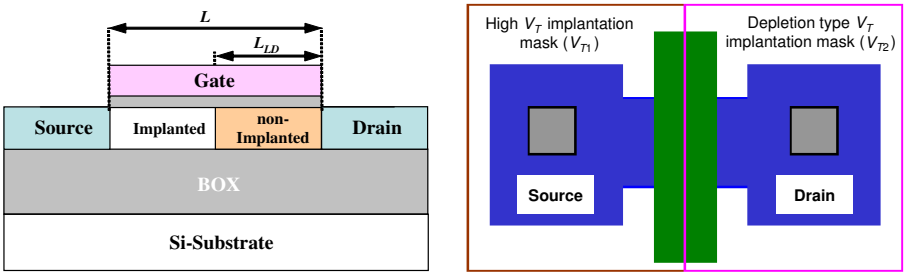
Nevertheless, in order to align the fabrication of GCMOS within the framework of an industrial standard CMOS process, a different procedure is used. The channel is shared between two different doping schemes introduced through two perfectly aligned masks, one for a high V_T (near the source) giving rise to V_{T1} and the other for a depletion mode MOSFET (near the drain) giving rise to V_{T2}(see Fig. 6.4b). The target is to introduce the maximum possible $V_T = V_{T1} - V_{T2}$. As a result, a lightly doped region is created near the drain over a length of L_{LD}.

[15]The Graded Channel MOS (GCMOS) was defined and introduced in section 2.7. However, this introduction is included here for the completeness of the chapter of thermal noise characterization.

The high difference in V_T results in a naturally inverted region near the drain side (over L_{LD}) at approximately zero gate bias which emulates an extended drain area beneath the gate. Hence, the effective channel length is reduced from L (the drawn channel length) to $L_{\mathrm{eff}} = L - L_{\mathrm{LD}}$. The ratio L_{LD}/L defines the characteristics of the device [142].

The highly doped part of the channel at the source end improves the threshold voltage roll-off and the drain induced barrier lowering (DIBL), whereas the light doping near the drain ensures high mobility, reduced peak electric field, and lowered impact ionization [142–144]. It also results in higher Early and breakdown voltages [145]. As a result a better analog performance is achieved with a better intrinsic gain due to a higher dc transconductance (g_m) and a lower output conductance (g_D). In addition, the analog and RF characteristics of the GCMOS are highly improved with a higher cut-off frequency (f_T) compared to classical MOSFET transistors [143–148].

The low frequency ($1/f$ noise) performance of Graded-Channel MOS (GCMOS) have also been analyzed in order to investigate the ability of this device to integrate in the recent low-power low-noise applications [149]. In addition, using TCAD simulations, T. C. Lim *et al.* [150] showed that the minimum noise figure of the laterally asymmetric channel MOS should outperform the classical nMOS device for both bulk and partially-depleted SOI due to a higher correlation factor C in the Pucel's model [100, 113, 114]. On the other hand, Roy *et al.* described the noise sources distribution along the channel [151, 152] and showed a higher correlation factor in the case of GCMOS transistor compared to classical nMOS [153]. Finally, our work provides the experimental evidence of the better RF noise performance of GCMOS as compared to classical MOSFET for both partially-depleted and fully-depleted SOI technologies (for both academic and industrial processes) [154, 155].



(a) Cross-section of a PD GCMOS structure.

(b) Top view mask layout of the FD GCMOS structure.

Fig. 6.4.: PD and FD GCMOS structures.

6.5.2 TCAD Simulations

T. C. Lim *et al.* provided the first TCAD simulations of high frequency noise performance in GCMOS and compared it to classical nMOS devices [150]. T. C. Lim started by theoretically proving that the reason for which GaAs-pHEMT (the most used device for low noise applications) provides lower $NF_{\min}$ than the classical MOSFET devices, although having much lower cutoff frequency f_T, is mainly the parameter C. C is the imaginary part of the correlation factor which, as mentioned earlier, is mainly imaginary due to the capacitive coupling between the channel noise source and the gate noise source. C is also the third parameter of Pucel's three parameter noise model [100, 113, 114]. In GaAs-pHEMT like devices, C is much higher than in classical MOSFET devices, ~ 0.9 and ~ 0.3, respectively [150]. T. C. Lim explained this very low C in classical MOSFET as follows: in classical MOSFETs, the threshold voltage is uniform all along the channel, and so is the distribution of the drain noise current due to local channel current fluctuations (based on [119, Fig. 9]). On the other hand, the distribution of the induced gate noise current is highly different from the drain noise current, leading to a very low correlation between the two noise sources. On the contrary, this is not the case for III-V devices, where the correlation is very high between the two noise sources [156]. T. C. Lim showed by TCAD simulations that a much higher C can be obtained through channel engineering in MOSFET devices. A laterally asymmetric device (or simply a GCMOS) can give a value of C as high as 0.9 when biased in the saturation region. Interesting observations were obtained through TCAD simulations:

- The better RF performance for GCMOS over classical nMOS is confirmed through a higher f_T.
- Similar values of P are obtained for both GCMOS and classical nMOS whereas R has a slightly higher value for GCMOS indicating a higher coupling between the channel current fluctuations and the gate.
- C is much higher in GCMOS as compared to classical nMOS which results in a significant reduction in $NF_{\min}$.
- The low value of $NF_{\min}$ in GCMOS is relatively stable over a wide range of gate bias ($V_{GS} > V_T$) as opposed to the classical nMOS which is highly dependent on f_T (lower $NF_{\min}$ is obtained at higher f_T). Although this fact is perturbed as the devices are scaled down (from 2 μm to 130 nm) due to short channel effects, GCMOS is still able to give very low values of $NF_{\min}$ (making it comparable to those of pHEMT), which cannot be achieved using classical nMOS devices, even by aggressively scaling the device (to increase its f_T).
- $NF_{\min}$ is improved for GCMOS as compared to classical nMOS. A fact that holds true for, a priori, the entire frequency range.

6.5.3 Analytical Explanation

The pioneering work of A. S. Roy *et al.* in modeling the thermal noise in laterally asymmetric channel MOSFETs [151, 152, 157] preceded the TCAD simulations provided by T. C. Lim *et al.* and helped to, later, provide a solid analytical explanation for the reasons of the higher C in GCMOS devices [153].

A. S. Roy showed that for a GCMOS, the traditional Klaassen-Prins noise model [97] is not valid. Based on his reasoning, A. S. Roy showed that the contribution to the terminal drain noise from any point along the channel is determined by the product of two terms; the impedance field IF of the drain, ΔA_{d} ([151, Fig. 3, eq. (12)]), which represents the noise propagation [157, 158], and the local noise source, whose power spectral density is proportional to the inversion charge ([151, Fig. 3, eq. (14)]). For a classical MOSFET, IF is independent of position and is equal to the inverse of the channel length. But the lateral asymmetry causes ΔA_{d} to highly peak near the source end and this effect is much more prominent at low gate voltages ([151, Fig. 4a]). As the source end is highly doped compared to the drain end, the inversion charge towards the drain end is much higher. This is where the Klaassen-Prins model fails since it assigns the same weight to both the strongly inverted region near the drain and the lightly inverted region near the source. On the contrary, A. S. Roy shows that the lightly inverted region near the source dominates the noise behavior especially at lower gate voltages. At higher gate voltages, the peak of ΔA_{d} is lower and the constant model of Klaassen-Prins can be less erroneous.

In order to physically explain this behavior, A. S. Roy used a two-series-connected-transistors approach, with the transistor near the source side being highly doped and the one near the drain being lightly doped. At low gate voltages, the transistor near the source end will be weakly inverted while the transistor near the drain end will be strongly inverted. As the weakly inverted transistor will have a much higher resistance, and hence a much higher noise voltage, the overall noise behavior of the channel will be dominated by the region near the source side. A. S. Roy also explained this behavior mathematically through the equations provided in [151, Fig. 3].

The peak of ΔA_{d} near the source side can be regarded as a localized source of noise. Or as described physically, the noise behavior of the channel is mainly dominated by the source end of the channel. This happens at lower gate bias values, which means when the channel is in saturation condition. As the drain bias is increased, going deeply in saturation condition, the localization of the noise source is even increased and the portion of the channel responsible for the noise performance gets more shrunk. As a result, the current fluctuations in the channel near the drain are negligible; resulting in negligible induced gate noise sources near the drain end, and hence, the induced gate noise source is also localized near the source end. These results are clearly seen in the peaking behavior of ΔA_{d} and ΔA_{g} in [153, Fig. 2 and 4]. These similar characteristics of ΔA_{d} and ΔA_{g} is directly translated into a high correlation between $\overline{i_d^2}$ and $\overline{i_g^2}$ (or high values of C). The two noise sources are simply approaching the ideal

case of having a single channel noise source near the source end which generates a single induced gate noise source, and thus they are approaching a perfectly correlated situation.

6.5.4 Measurements

In order to correctly characterize the RF noise performance of the devices, it is necessary to ensure a correct dc and RF characterization. Standard dc and ac characteristics are measured, at room temperature, using an HP4142B semiconductor parameter analyzer and an HP8510C vector network analyzer (VNA) controlled by ICCAP 2006B software. Noise parameters are then measured using the two different techniques mentioned earlier; the F50 and the Tuner techniques.

6.5.4.1 Difficulties with the F50 method

In a first run, devices considered in this work were measured using the F50 method. As mentioned earlier, the F50 method is highly accurate and much easier to apply. However, a serious difficulty was noticed for the case of GCMOS. Two parameters are readily extracted from the measured F50 data: R_n and $|Y_{\text{opt}}|^2$. In order to extract the rest of the noise parameters, either a special test structure has to be used where the access line to the gate is varied or a theoretical assumption has to be made [125]. The first option cannot be realized since the devices and the test structures are already fabricated. The second option, the theoretical assumption, is based on the Pospieszalski's Two-parameter model which assumes two uncorrelated noise sources [120]. This assumption is in clear contradiction with the results obtained from TCAD simulations and mathematical analysis presented earlier. In addition, this was clearly noticed from the results of the extraction performed on the F50 measurements when non-physical values of C were obtained ($C > 1$ and $C < 0$). Therefore, the results obtained using the F50 method were discarded, and the Tuner method was adopted for further characterization of the RF noise performance of GCMOS. However, it should be mentioned that, the calculation of F_{50} can be easily achieved based on the Tuner measurements and the extracted PRC parameters (Pucel's model) using a simple equation (see derivation in Appendix F):

$$F_{50} = 1 + \left(R_{\text{g}} + R_{\text{s}} + \frac{P}{g_m}\right) G_0 + \frac{\omega^2 C_{\text{tot}}}{G_0 g_m}\left(P + R - 2C\sqrt{PR}\right) + \frac{P}{g_m} G_{\text{cor}} \quad (6.38)$$

where $G_0 = 20$ mS (the inverse of 50 Ω) and C_{tot} is the total gate capacitance ($C_{\text{tot}} = C_{\text{gs}} + C_{\text{ds}}$). In (6.38), the effect of the pads capacitances are not included. However, in this work, the noise characterization is performed using on-wafer measurements, and thus the effect of the pad capacitance C_{p} is important. A more exact equation is thus needed to account for C_{p} (see Appendix F for deriva-

tion for the derivation):

$$F_{50} = 1 + \left(R_g + R_s + \frac{P}{g_m}\right) G_0 + \frac{\omega^2}{G_0 g_m} \left\{ C_{tot}^2 \left(P + R - 2C\sqrt{PR}\right) + C_p^2 \left[P + (R_g + R_s)\, g_m\right] - 2C_p C_{tot} \left(C\sqrt{PR} - P\right) \right\} \quad (6.39)$$

6.5.4.2 Mechanical Tuner Method

The tuner measurement technique is typically recommended to go up to a maximum frequency equals to half of the cutoff frequency f_T of the DUT. For the GCMOS transistors studied in this work, its low f_T (around 19 GHz) made it necessary to measure the noise performance at relatively low frequencies. Measurements were achieved using a mechanical tuner system from Maury Microwaves in the 1-8-GHz frequency range. This frequency range is particularly difficult to measure and the calibration process needs extra prudence. Therefore, in order to reach robust and repeatable results, extractions and analysis shown hereafter are all done at 6 GHz so as to avoid the uncertainties at lower frequencies. The calibration procedure for the measurement setup is summarized in Appendix G.

6.5.4.3 Devices under Test

The devices measured in this section are fabricated on a Partially-Depleted (PD) Silicon-on-Insulator (SOI) 0.25 μm academic technology and on a Fully-Depleted (FD) SOI 0.15 μm industrial technology.

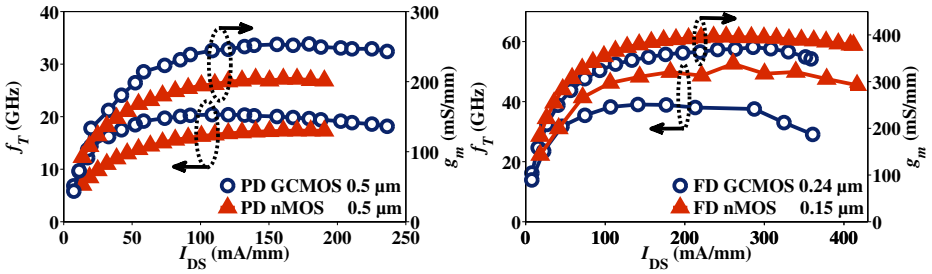
For the PD devices, results presented in this work are for classical nMOS devices of 0.25 and 0.5 μm and for a GCMOS device of 0.5 μm channel lengths. All of the three devices are n-type and feature gates with 12 parallel fingers each of which has a 13.2 μm width. The silicon film, the buried oxide (BOX) and the gate polysilicon thicknesses are 100, 400, and 200 nm, respectively. The ratio of the low-doped channel length to the total channel length (L_{LD}/L) is approximately 0.5 [145]. The threshold voltage is 0.4 V in the case of $L = 0.5$ μm (for both GCMOS and classical nMOS) and 0.5 V in the case of $L = 0.25$ μm classical nMOS device. All noise measurements are performed while keeping the transistor in saturation ($V_{DS} = 1.2$ V) and varying V_{GS} from 0.5 to 1.5 V.

Fig. 6.5a shows the measured current gain cutoff frequency f_T and the dc transconductance g_m for the PD GCMOS and classical nMOS transistors. A better performance for both f_T and g_m is clearly noticed for the case of GCMOS. This is in agreement with already reported better performance of GCMOS compared to classical nMOS [143–148] and is very critical for the better RF noise performance as will be shown hereafter.

For the FD technology, two devices are considered in this work. A classical n-type MOSFET device (nMOS) with a drawn channel length equals to 0.15 μm and 96 parallel fingers of 2.5 μm width each. The second device is a GCMOS (n-type) with a drawn channel length equals to 0.24 μm and 48 parallel fingers of 5 μm width each. The designed ratio L_{LD}/L is 0.5. Both devices are fabricated on the same wafer through the same industrial process [155, 159–162]. A slight

difference is noticed for the threshold voltage V_T for GCMOS and classical nMOS with values equal to 0.62 V and 0.65 V, respectively. This slight difference is compensated by presenting all figures of merit in this section as a function of the normalized drain current density I_{DS}, i.e. normalzied with respect to the total gate width.

Fig. 6.5b shows the current gain cutoff frequency f_T and the dc transconductance g_m for the FD GCMOS and classical nMOS transistors. The superior performance of the classical nMOS in dc and RF could be related to a slight shift in the L_{LD}/L ratio due to a lateral diffusion of dopants from the heavily doped part. In practice, the dc and RF performances of a GCMOS of a drawn channel length L are usually higher than the dc and RF performances of a classical MOSFET of a channel length L but slightly lower than that of a channel length L_{eff} [145, 154].



(a) PD GCMOS and classical nMOS of $L = 0.5$ μm.

(b) FD GCMOS ($L = 0.24$ μm) and classical nMOS ($L = 0.15$ μm).

Fig. 6.5.: Measured current gain cutoff frequency f_T and dc transconductance g_m as a function of the drain current density I_{DS} for GCMOS and classical nMOS in PD and FD technologies.

6.5.5 Intrinsic Noise Performance

The intrinsic experimental noise performance is first presented in this section in order to provide a basic understanding of the advantage of using GCMOS devices over classical nMOS devices.

Tuner measurements give the four noise parameters (NF_{min}, R_n, and $Y_{\mathrm{opt}} = G_{\mathrm{opt}} + jB_{\mathrm{opt}}$) for each device and at each selected frequency point.

First, a 1-step (Open) de-embedding procedure is applied to withdraw the pad parasitics network influence on noise parameters using the correlation matrix technique as explained in Appendix B. Next, the procedure using [89] is used to remove the effect of the Nyquist noise in the extrinsic resistances (R_{g}, R_{d}, and R_{s}), and thus obtain what is referred to as the intrinsic noise parameters (see Appendix B). Extrinsic resistances are extracted from measured S-parameters using the Cold-FET method [163]. The results for both PD and FD devices are shown in Table 6.1 (Note that the values shown for PD devices are for channel

length $L = 0.5\ \mu$m). In a first step, the measured intrinsic noise parameters are presented, and then the extraction of the three-parameter noise model is shown.

Table 6.1.: Extrinsic resistances of both GCMOS and classical nMOS devices extracted using the Cold-FET method.

		R_g (Ω)	R_s (Ω)	R_d (Ω)
PD	GCMOS	3.8	3.3	
	nMOS	3.8	3.3	
FD	GCMOS	3	1.7	3.7
	nMOS	2.95	1	2.4

6.5.5.1 Intrinsic Noise Parameters

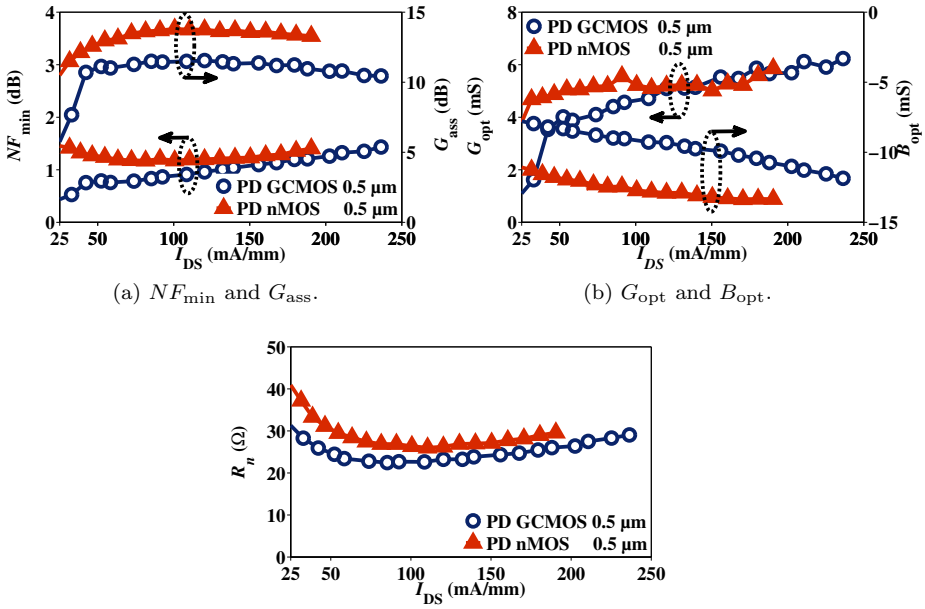
Fig. 6.6 shows the intrinsic noise parameters as a function of drain current density I_{DS} for PD devices. The intrinsic minimum noise figure NF_{min} (Fig. 6.6a) of the GCMOS device shows an interesting reduction compared to the intrinsic NF_{min} of the classical nMOS device where both of which have the same geometry. This better noise performance is more pronounced in the low current region, which is interesting for low-voltage low-power applications. However, the intrinsic associated gain G_{ass} (Fig. 6.6a) of the GCMOS shows relatively lower performance compared to the classical nMOS.

In the low-voltage low-power regime of operation, a slightly lower G_{opt} and $|B_{opt}|$ are observed in the case of GCMOS (Fig. 6.6b), which is indicative of a slightly greater difficulty in satisfying noise matching. However, R_n (Fig. 6.6c) is lower for GCMOS, yielding a lower sensitivity of noise figure mismatch from optimum source impedance.

These intrinsic results are in complete accordance and provide experimental evidence of trends described in [150] where the authors used TCAD simulations for bulk and PD SOI devices.

As for the FD devices, the comparison is more aggressive, since a 0.24 μm channel length GCMOS is being compared to a 0.15 μm channel length classical nMOS. Nevertheless, as seen from Fig. 6.7a, the GCMOS device shows a comparable intrinsic NF_{min} behavior over a wide range of operation, especially at low current densities. The intrinsic associated gain G_{ass} follows the same trend noticed for PD devices with a relatively higher difference between the two devices compared to the PD case.

The intrinsic optimum noise impedance Y_{opt} shown in Fig. 6.7b in its real and imaginary parts does not show a big difference between the two FD devices. As a result, a comparable noise matching characteristics can be achieved. The same applies for the intrinsic equivalent noise resistance R_n shown in Fig. 6.7c.



(a) $NF_{\min}$ and G_{ass}.

(b) G_{opt} and B_{opt}.

(c) R_n.

Fig. 6.6.: Intrinsic measured four noise parameters and associated gain as a function of normalized drain current I_{DS} for the PD GCMOS and classical nMOS at $V_{\text{DS}} = 1.2$ V and frequency = 6 GHz.

6.5.5.2 *Three-parameter PRC Noise Model*

In addition to the four intrinsic noise parameters presented in section 6.5.5.1 for the different devices, the extraction of Pucel's 3-parameter (P, R, and C) noise model [100, 113, 114] is of interest and should provide more insight in understanding this favoured noise performance of GCMOS over classical nMOS device.

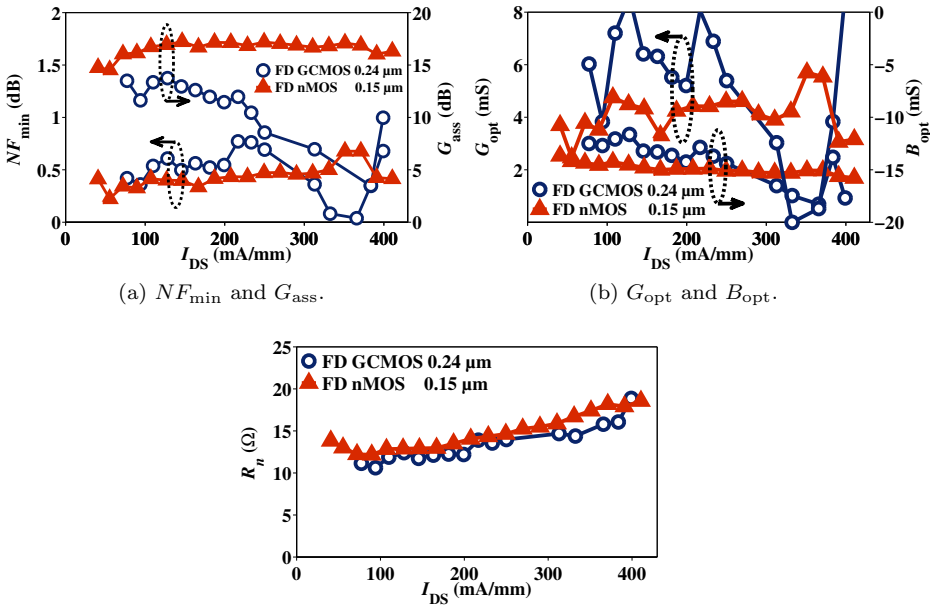
PRC noise parameters can simply be obtained from induced gate noise current $\overline{i_g^2}$, drain noise current $\overline{i_d^2}$, their cross-correlation $\overline{i_g i_d^*}$ [164], and the intrinsic admittance parameters (Y_{11} and Y_{21}):

$$\overline{i_g^2} = 4kT_{\text{a}} \frac{|Y_{11}|^2}{|Y_{21}|} R\Delta f \tag{6.40}$$

$$\overline{i_d^2} = 4kT_{\text{a}} |Y_{21}| P\Delta f \tag{6.41}$$

$$\overline{i_g i_d^*} = jC\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \tag{6.42}$$

where T_{a} is the ambient temperature. Throughout, it is assumed that T_{a} is equivalent to the standard noise temperature T_0, thus $T_{\text{a}} = T_0 = 290$ K.



(a) $NF_{\min}$ and G_{ass}.

(b) G_{opt} and B_{opt}.

(c) R_n.

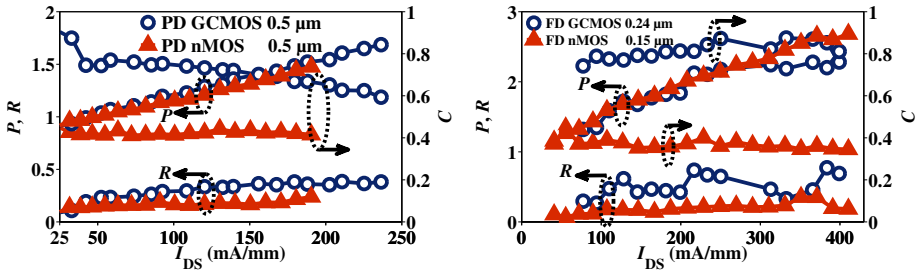
Fig. 6.7.: Intrinsic measured four noise parameters and associated gain as a function of normalized drain current I_{DS} for the FD GCMOS and classical nMOS at $V_{\text{DS}} = 1.5$ V and frequency = 6 GHz.

As mentioned earlier, P, R, and C are dimensionless and they depend on the physical properties of the device. They are bias dependent and frequency independent.

Fig. 6.8a shows the PRC noise parameters as a function of drain current density for PD devices. The value of P is more or less similar for both devices whereas the value of R is higher for GCMOS, indicating a higher capacitive coupling between diffusion channel noise and the gate (note that this same result was obtained using TCAD simulations [150]). Higher values of C for GCMOS are clearly observed (nearly double the values of C for the classical nMOS), which is the main reason as why the $NF_{\min}$ of GCMOS outperforms the $NF_{\min}$ of classical nMOS. This fact is discussed in detail in section 6.5.5.3 when analytical expressions are considered.

For the FD devices, Fig. 6.8b shows the extracted values of P, R, and C. The values of P and R are quite comparable for both devices and they follow the theoretical expectations; R has a value around 0.2 for nMOS and around 0.4 for GCMOS whereas P varies linearly with increasing I_{DS} [164]. For the classical nMOS, a value of the correlation factor C around 0.4 is found, which is typical in the case of classical MOSFETs [83]. On the other hand, for GCMOS, the value of C is nearly twice its value for classical nMOS, starting from 0.8 and slightly

increasing with the increase of I_{DS}. Again, this double value of C is shown later (section 6.5.5.3) as the direct explanation of the better $NF_{\min}$ for the case of GCMOS.



(a) PD. (b) FD.

Fig. 6.8.: PRC parameters as a function of normalized drain current I_{DS} for PD and FD GCMOS and classical nMOS in saturation region at frequency = 6 GHz.

6.5.5.3 *Analytical Expressions*

$NF_{\min}$. The analysis of the previously shown intrinsic results is based on the following analytical formula [113]:

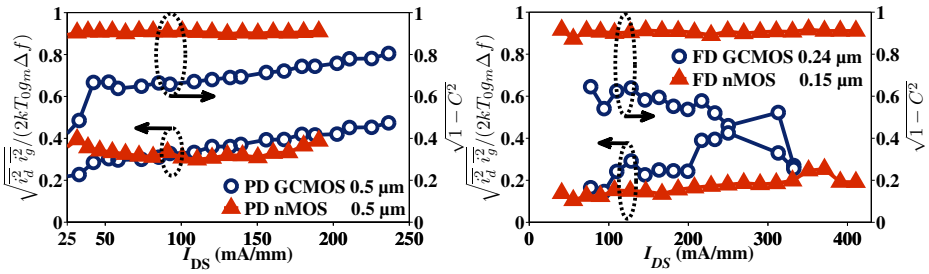
$$NF_{\min} = 1 + \frac{\sqrt{\overline{i_g^2}\ \overline{i_d^2}}}{2kT_0G_{mi}\Delta f}\sqrt{1-C^2} \tag{6.43}$$

where G_{mi} is the intrinsic transconductance calculated from the real part of the intrinsic admittance parameter Y_{21}.

The second term of (6.43) can be regarded as the product of two parts, i.e. $\frac{\sqrt{\overline{i_g^2}\ \overline{i_d^2}}}{2kT_0G_{mi}\Delta f}$ and $\sqrt{1-C^2}$. By plotting both parts as a function of the drain current density (Fig. 6.9), it is clear that $\frac{\sqrt{\overline{i_g^2}\ \overline{i_d^2}}}{2kT_0G_{mi}\Delta f}$ (left axis) is quite similar for both devices while $\sqrt{1-C^2}$ (right axis) shows an obvious difference between GCMOS and classical nMOS. This constitutes an experimental evidence of the role of the correlation coefficient. The origin of the better $NF_{\min}$ performance for GCMOS compared to classical nMOS is clearly related to the higher correlation coefficient C in the case of GCMOS.

6.5.6 Extrinsic Noise Performance

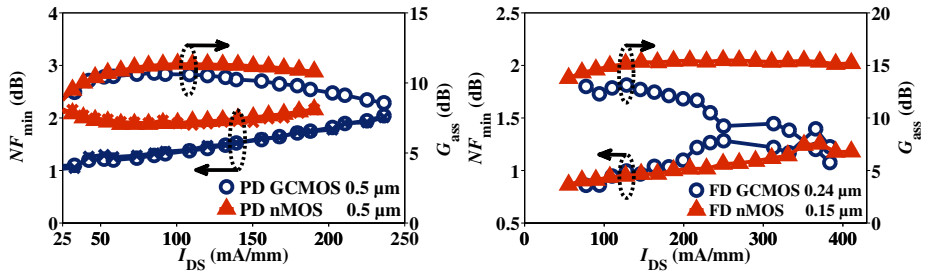
The previous section showed a favourable noise performance of GCMOS over classical nMOS in its intrinsic form. This trend should be confirmed looking at the extrinsic noise parameters, based on raw measurements without removing



(a) PD. (b) FD.

Fig. 6.9.: Verification of the effect of the correlation coefficient C in both PD and FD GCMOS and classical nMOS in saturation region at frequency = 6 GHz.

the effect of extrinsic resistances. They are obtained directly from Tuner measurements (after Open de-embedding). Minimum noise figure $NF_{\min}$ as well as associated gain G_{ass} are shown in Fig. 6.10a for PD devices and in Fig. 6.10b for FD devices. For PD devices, the difference between $NF_{\min}$ of GCMOS and classical nMOS in Fig. 6.10a is found to be bigger compared to its intrinsic case shown in Fig. 6.6a. It can also be seen that associated gain G_{ass} is reduced more in classical nMOS relative to GCMOS when comparing extrinsic to intrinsic cases. The same observations apply for the FD devices when comparing intrinsic values of $NF_{\min}$ and G_{ass} in Fig. 6.7a and the extrinsic case in Fig. 6.10b.



(a) PD ($NF_{\min}$ calculated from (6.44) is shown in X shapes). (b) FD.

Fig. 6.10.: Extrinsic minimum noise figure $NF_{\min}$ and extrinsic associated gain G_{ass} as a function of drain current density I_{DS} for both PD and FD GCMOS and classical nMOS in saturation region at frequency = 6 GHz.

The difference in the sensitivity of $NF_{\min}$ to the thermal noise of the extrinsic resistances between GCMOS and classical nMOS can be explained using the formula [114]:

$$NF_{\min} = 1 + \frac{2f}{f_T}\sqrt{PR\,(1-C^2) + \left(P + R - 2C\sqrt{PR}\right)(R_{\text{g}} + R_{\text{s}})\,g_m} \qquad (6.44)$$

In order to check its accuracy, a comparison of (6.44) with experimental data is given in Fig. 6.10a for PD devices. The impact of extrinsic resistances is quantified by the term $\left(P + R - 2C\sqrt{PR}\right)(R_{\mathrm{g}} + R_{\mathrm{s}})\, g_m$. Given the higher correlation factor C in the case of GCMOS compared to classical nMOS, the lower impact of thermal noise featured by extrinsic resistances (R_{g} and R_{s}) on the $NF_{\min}$ of GCMOS is obvious.

This important result shows that the benefit of higher C for $NF_{\min}$ is not limited to the intrinsic noise contribution [i.e. $PR\left(1 - C^2\right)$ in (6.44)] but it also affects the sensitivity of $NF_{\min}$ to the thermal noise of the extrinsic resistances.

To have a complete picture, a comparison between all noise parameters in their extrinsic and intrinsic forms as well as the percentage of change in each parameter (relative to the intrinsic case) for the PD devices are summarized in Table 6.2 where values are given at a frequency of 6 GHz and $I_{\mathrm{DS}} = 50$ mA/mm.

Table 6.2.: Sensitivity of noise parameters to extrinsic resistances in both PD GCMOS and PD classical nMOS of 0.5 μm channel length ($NF_{\min}$ is presented in linear not in dB).

		$NF_{\min}$	G_{ass}	G_{opt}	$\lvert B_{\mathrm{opt}}\rvert$	R_n
GCMOS	Intrinsic	1.197	11.03	3.91	8.29	24.77
	Extrinsic	1.322	10.37	4.66	6.69	31.75
	$\Delta\%$	10.4	−5.98	19.2	−19.3	28.2
nMOS	Intrinsic	1.336	12.76	4.95	11.85	30.42
	Extrinsic	1.565	10.53	6.24	9.7	37.78
	$\Delta\%$	17.1	−17.5	26.1	−18.14	24.2

6.5.7 Validity of the Two-parameter Model

It has been shown through TCAD simulations, physical analysis and experimental results that GCMOS devices are characterized by a very high correlation between the drain current noise source and the induced gate noise source. This was also proven through the extraction of the three-parameter noise model of Pucel. It is therefore of increased interest to check the validity of the two-parameter noise model of Pospieszalski since, as shown earlier, it presumes two independent noise sources using voltage-current representation [165]. In other words, the two-parameter noise model presumes a zero correlation coefficient between the input gate noise voltage source and the output drain noise current source.

The fact that the noise sources in the two-parameter noise model are uncorrelated is equivalent to having the following relation between C, R, and P when considering the current-current representation:

$$C = \sqrt{\frac{R}{P}} \tag{6.45}$$

This relation reduces, *de facto*, Pucel's noise model to two parameters. In order to study the validity of (6.45), Danneville *et al.* [156] introduced a complete analytical study of noise models of III-V FETs using a uniform active line theory as well as a more realistic set of results obtained by using the software HELENA [166].

The two-parameter noise model of Pospieszalski has been widely used within the III-V research community as well as within the Si MOSFET research community [167–170]. Nevertheless, a clear study justifying the use of this noise model for MOSFETs has not been reported yet. The importance of such a study inherits from the fast growing trend to use the mainstream CMOS technology in high frequency (HF) applications. Recently, as a result of aggressive scaling, mainstream CMOS technology can provide higher cutoff frequencies than HEMTs [171] while offering more flexibility in terms of technological parameters (e.g. equivalent barrier thickness [171]), device architecture (e.g. gate structure), or even design methodologies. These advantages put the MOSFET ahead compared to other alternatives, such as HEMTs, as a preferred choice for HF applications.

Therefore, it is not only interesting to check the two-parameter noise model for GCMOS, but it is also quite important to introduce an experimental verification of this model for the current mainstream CMOS technology.

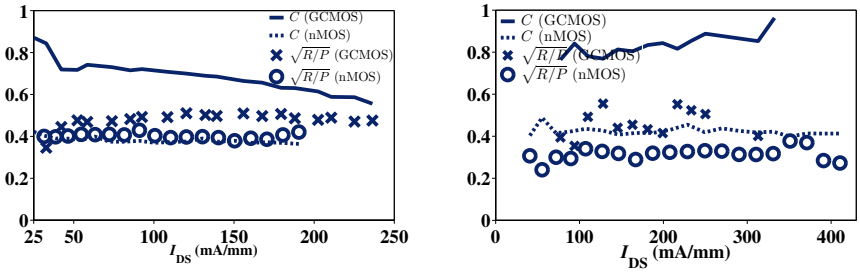
6.5.7.1 Mainstream CMOS Technology

In the mainstream CMOS technology, the channel is uniformly doped in the lateral direction, i.e. from source to drain, which is the case referred to in this chapter as classical MOSFET or classical nMOS.

In order to verify (6.45) in the case of classical MOSFETs, the value of the correlation coefficient C as well as $\sqrt{R/P}$ as a function of normalized drain current I_{DS} are shown in Fig. 6.11 for PD and FD devices. The value of the correlation coefficient C for nMOS is approximately 0.4, which is in complete agreement with the value predicted by van der Ziel [83], as mentioned before. It is also obvious that $\sqrt{R/P}$ is almost equal to C over the whole range of operation for the classical MOSFET both for PD and FD devices, i.e. from weak to strong inversion. It is worth to notice that the same results are obtained when using PRC values of bulk MOSFET calculated using TCAD simulations [150].

To further check the validity of (6.45), it is of interest to show the intrinsic noise parameters (after removing the effect of extrinsic resistance R_{g} and R_{s}). The expressions of NF_{min}, R_n, and Y_{opt} given in [150] and based on the analysis introduced in [114, 164] are employed to verify their dependency on C. NF_{min} is given by (6.44) in its general form, including the effect of the extrinsic resistances. For simplicity, it is repeated here along with the formulas of G_{opt}, B_{opt}, and R_n [164]:

$$NF_{\mathrm{min}} = 1 + \frac{2f}{f_T}\sqrt{PR\left(1-C^2\right) + \left(P + R - 2C\sqrt{PR}\right)\left(R_{\mathrm{g}} + R_{\mathrm{s}}\right) g_m} \quad (6.46)$$



(a) PD. (b) FD.

Fig. 6.11.: Correlation coefficient C and $\sqrt{R/P}$ extracted at 6 GHz as a function of normalized drain current I_{DS} for PD and FD GCMOS and classical nMOS devices.

$$G_{\mathrm{opt}} = \frac{\omega C_{\mathrm{tot}}}{[P + (R_{\mathrm{g}} + R_{\mathrm{s}})\, g_m]} \times \sqrt{PR\,(1 - C^2) + \left(P + R - 2C\sqrt{PR}\right)(R_{\mathrm{g}} + R_{\mathrm{s}})\, g_m} \tag{6.47}$$

$$B_{\mathrm{opt}} = \frac{\omega C_{\mathrm{tot}}}{[P + (R_{\mathrm{g}} + R_{\mathrm{s}})\, g_m]} \left(C\sqrt{PR} - P\right) \tag{6.48}$$

$$R_n = R_{\mathrm{g}} + R_{\mathrm{s}} + \frac{P}{g_m} \tag{6.49}$$

After removing the effect of extrinsic resistances (i.e. putting $R_{\mathrm{g}} = R_{\mathrm{s}} = 0$), the four noise parameters can simply be expressed as [150]:

$$NF_{\mathrm{min}} = 1 + \frac{2f}{f_T}\sqrt{PR\,(1 - C^2)} \tag{6.50}$$

$$G_{\mathrm{opt}} = \omega C_{\mathrm{tot}}\sqrt{\frac{R}{P}\,(1 - C^2)} \tag{6.51}$$

$$B_{\mathrm{opt}} = \omega C_{\mathrm{tot}}\left(C\sqrt{\frac{R}{P}} - 1\right) \tag{6.52}$$

$$R_n = \frac{P}{g_m} \tag{6.53}$$

From (6.50)–(6.53), it is clear that, in contrary to NF_{min} and Y_{opt}, R_n does not depend on C. On the other hand, instead of reporting Y_{opt}, it is preferred, from the circuit design point of view, to present Γ_{opt}(the optimum input reflection coefficient) in a Smith chart representation where:

$$\Gamma_{\mathrm{opt}} = \frac{1 - 50 \times Y_{\mathrm{opt}}}{1 + 50 \times Y_{\mathrm{opt}}} \tag{6.54}$$

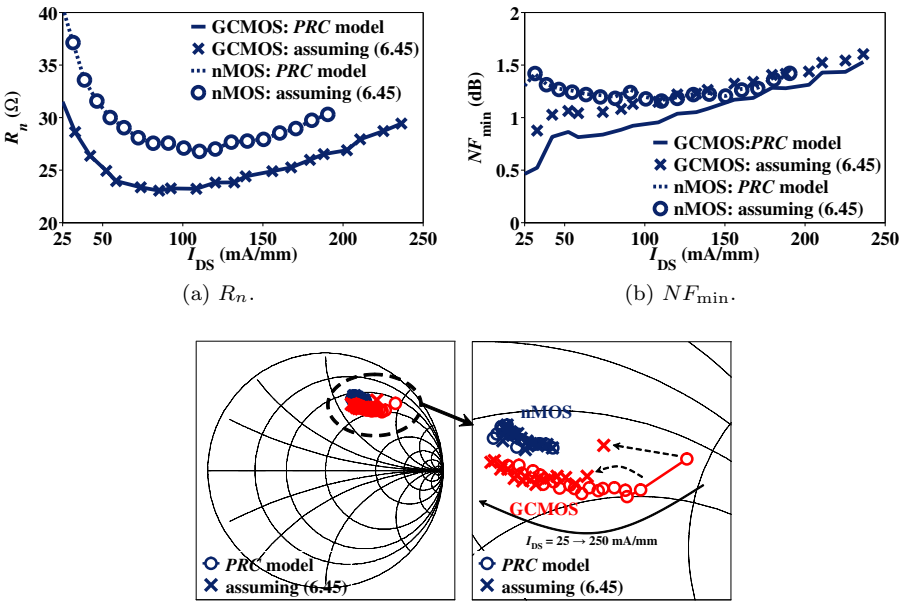
$NF_{\min}$, R_n, and Γ_{opt} are calculated using:

- Pucel's PRC noise model using (6.50)–(6.53) which was shown to give good agreement with measured data (see Fig. 6.10a);
- Equation (6.45) to define C (and then substitute in (6.50)–(6.53)).

The results are then shown in Fig. 6.12 for the PD GCMOS and classical nMOS.

A perfect match is noticed between the values of $NF_{\min}$ and Γ_{opt} obtained from Pucel's PRC noise model and the values calculated when using (6.45) as an assumption. The independence of R_n on C is confirmed in Fig. 6.12a where lines and symbols are seen to completely coincide.

These results clearly show that "two" noise parameters are sufficient to fully model/extract the four noise parameters ($NF_{\min}$, R_n, and Y_{opt}) featured by a classical MOSFET, independently on the chosen noise model (i.e. the extraction of P and R using Pucel's noise model or the extraction of T_g and T_d using Pospieszalski's noise model). It justifies as well why a simple noise figure measurement (as a function of frequency), using the F50 method, is sufficient to extract the four noise parameters [167–169, 172, 173].



(a) R_n. (b) $NF_{\min}$.

(c) Γ_{opt}.

Fig. 6.12.: An illustration of the validity of the two-parameter model by representing R_n, $NF_{\min}$, and Γ_{opt} calculated once using PRC model and then using (6.45) for PD GCMOS and classical nMOS at 6 GHz in saturation region.

6.5.7.2 GCMOS

In a GCMOS, unlike classical MOSFET, Fig. 6.11 shows that C is not equal but higher than $\sqrt{R/P}$ over the whole range of operation (again, the same result is obtained using PRC values of bulk MOSFET calculated from TCAD simulations [150]).

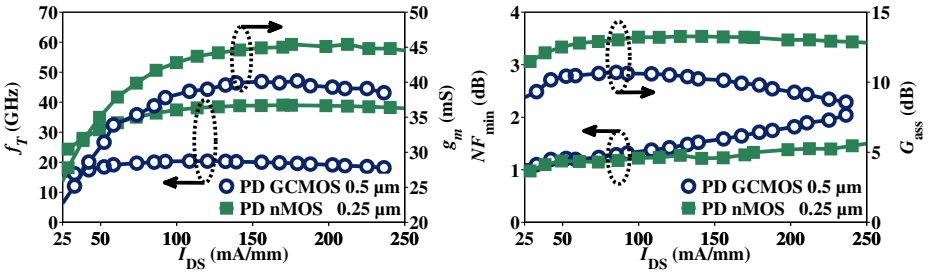
It is also of interest to evaluate the potential impact of employing the assumption of (6.45) in the case of GCMOS. In the case of $NF_{\min}$ (Fig. 6.12b), it turns out that an error as high as 0.2 dB (at I_{DS} = 50 mA/mm and frequency = 6 GHz) is observed when comparing the values extracted using Pucel's PRC noise model and the values calculated assuming (6.45). Moreover, the values of Γ_{opt} extracted using Pucel's PRC noise model are quite different from those calculated assuming (6.45) (Fig. 6.12c). This means that if (6.45) is used for a GCMOS, an important noise mismatch would occur when designing a low noise amplifier (LNA), leading to an important degradation of the LNA noise figure. From this study, it turns out that the use of Pucel's 3-parameter noise model (PRC) is required when studying the HF noise performance of a GCMOS. This result is not limited to novel devices like GCMOS, but also for state-of-the-art technologies, whenever a perfect uniformly doped channel is difficult to achieve.

It is worth noticing that Γ_{opt} for GCMOS is closer to the 50 Ω circle on the Smith chart than the Γ_{opt} of the calssical nMOS. This gives an indication of better matching with other stages in the circuit. The reason could be attributed to the shorter effective channel length of the GCMOS, hence a less inductive channel at lower values of current density (better for LVLP applications). At higher values of current density, both devices show relatively the same behavior.

6.5.8 Scaling

As can be seen from Fig. 6.13a, the 0.5 μm length PD GCMOS shows lower f_T and g_m than the 0.25 μm length PD nMOS devices. Nevertheless, the minimum noise figure $NF_{\min}$ (extrinsic) of 0.5 μm GCMOS competes with the 0.25 μm nMOS as shown in Fig. 6.13b (especially for I_{DS} lower than 100 mA/mm). At I_{DS} = 50 mA/mm, the 0.25 μm classical nMOS features f_T of 31 GHz, nearly double that of the GCMOS (18 GHz), whereas both values of $NF_{\min}$ are almost the same i.e. 1.17 dB and 1.21 dB, respectively, at 6 GHz. This interesting scaling trend is explained by the lower sensitivity of GCMOS to extrinsic thermal noise effects described earlier.

One may argue that these similar values of $NF_{\min}$ are due to the fact that the value of R_g for the 0.25 μm classical nMOS is twice that of the 0.5 μm GCMOS i.e. 7.6 and 3.8 Ω, respectively. However, it should also be noted that the value of f_T of the classical nMOS is almost twice that of the GCMOS. Therefore, it is expected that the downscaling would have a greater impact on the increase of f_T while keeping very low values of $NF_{\min}$ in the case of GCMOS by comparison with the classical nMOS device.



(a) Scaling in current gain cutoff frequency f_T and dc transconductance g_m.

(b) Scaling in extrinsic (measured) $NF_{\min}$ and G_{ass}.

Fig. 6.13.: Scaling effects on PD GCMOS and classical nMOS presented for the saturation region ($V_{\text{DS}} = 1.2$ V and frequency = 6 GHz).

6.6 CONCLUSION

Channel engineering, as presented in this chapter using the GCMOS concept, proves to be very useful in enhancing RF noise performance. The experimental extraction of the PRC noise parameters has confirmed that this interesting behavior is related to the increased correlation coefficient C in GCMOS devices, which then leads to a reduction in the minimum noise figure $NF_{\min}$. Although a slight reduction in the associated gain G_{ass} is noticed for GCMOS devices, this will not affect low power applications, as it starts to become critical only at higher currents. It has also been shown that this higher correlation coefficient C means that $NF_{\min}$ is less sensitive to the thermal noise in the case of GCMOS by comparison with the case of the classical nMOS device. The superior RF noise performance of GCMOS compared to classical MOSFETs is also confirmed for the 0.15 μm fully-depleted industrial technology.

The concept of a "two-parameter noise model" has clearly been validated for a classical MOSFET (mainstream CMOS), a device widely used in the HF domain, provided that the channel uniformity is ensured. Nevertheless, in the case of an asymmetric channel MOSFET (such as a GCMOS), whose noise physics is very different from the classical MOSFET, it has been shown that a three-parameter noise model is more appropriate.

Finally, the scaling advantage of GCMOS has been clearly highlighted, thus enabling the design of low-noise circuits at lower costs using currently well understood and stable technologies.

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CHAPTER 7

RF ANTENNA SWITCH

The RF antenna switch has the function of regulating the pass of the signal from/to the antenna to/from the low-noise amplifier (LNA) and the power amplifier (PA) in a RF wireless communication system. The ideal RF antenna switch would completely pass the signal in one path while completely isolating the signal from the other path. However, this performance is practically difficult to achieve. An optimization should be achieved between a semi-complete delivery of the signal with a certain Insertion Loss, while semi-complete isolation of the signal on the other path. Another important specification of the RF antenna switch is its nonlinear behavior described by its IP_3 and $P_{\text{1-dB}}$.

7.1 INTRODUCTION

Wireless communications started in the year 1880 when Alexander Graham Bell and Charles Sumner Tainter invented and patented their photophone, a device that facilitates audio conversations using wireless modulated light beams. However, the wireless communication experienced a boom during the few last decades due to the commercialization of consumer products with the cellular/mobile phone as the most famous example. As the wireless communication market grows with big steps, especially for consumer applications, portability is becoming an insisting need. Size and power consumption are meant to be drastically reduced.

Putting the whole wireless communication system on a single integrated chip is not anymore an option, rather a pushing requirement. In its most simple description, the wireless system is composed of three main blocks: an antenna, a receiving circuitry, and a transmitting circuitry. The RF antenna switch plays the role of the coordinator between these three blocks. It allows for a single antenna to function as a receiving and a transmitting pole at the same time through a time division duplexing TDD. It is also referred to as a single pole double through (SPDT) switch to differentiate it from a single pole multiple through SPMT which allows the use of multiple antennas.

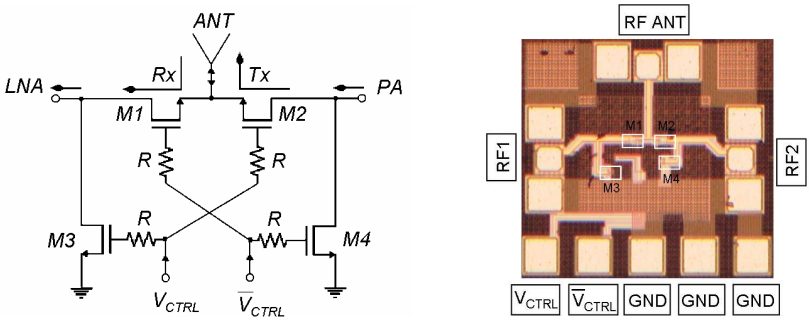
However, the introduction of the RF antenna switch concept encountered several problems which were reported in the literature. In fact, this concept has been an active research subject since the second half of the 20^{th} century. With the progress achieved in the field of high power semiconductor technology, designers started to think about replacing the mechanical relays in the RF transceivers with what was called a RF activated switch. The RF activated switch is basically a black-box with three external terminals, one for the transmitter, one for the receiver and one for the antenna. The same antenna had to be used for both transmission and reception. This black-box is composed of power diodes connected in forward and reverse bias in a way to achieve the switching function between transmission and reception. Nevertheless, and since that time, RF switches suffered from the same problems as those from which they still suffer today: loss of transmission power and power handling of huge transmitted signals. At that time, using the diodes with a threshold voltage of 0.7 V and a relatively low breakdown voltage created a problem, since they break down earlier than desired due to the large signal transmitted by the power amplifier. In 1966, K. W. Angel proposed a switch that operates using the principle of avalanche operation [1]. His circuit was successfully operating even at high temperatures like 60°C. Recently, Fanucci *et al.* reported the problems that face RF antenna switches in the 21^{th} century: the loss of transmission power due to the non-ideal isolation of the receiver stage and the loss of sensitivity due to the use of external switches which introduce a non-negligible loss and nonlinearities [2].

The RF antenna switch is characterized by its very simple circuit design and simple figures of merit that describe its performance as should be presented later. Therefore, it serves here as a demonstrator that concludes the comparative study introduced in the earlier chapters for different MOSFET technologies and device structures.

7.2 CIRCUIT DESIGN

The three vertices of the triangle of performance of a RF antenna switch are the “Insertion Loss”, ”Isolation”, and “Power Handling”. As in other design problems, a trade-off is always necessary between these different figures of merit, since it is impossible to maximize all of them in the same time. This trade-off becomes more difficult in bulk and low resistivity substrate SOI devices. The

low resistivity substrate results in an increased insertion loss and a decreased isolation [3]. The design adopted for the RF Antenna switch is very simple. It consists of only four transistors and four resistors as shown in Fig. 7.1. The same design has been used for RF antenna switches since it was first introduced by Huang and O in 2001 [4]. The series transistors M1 and M2 ensure the passage of the signal from the antenna to the Low Noise Amplifier (LNA) and from the Power Amplifier (PA) to the antenna. The shunt transistors M3 and M4 are used to tie the LNA or the PA to the ground when it is turned off, hence improving the isolation. The gate resistors R help improving the linearity of the system.



(a) A schematic of the design of the RF antenna switch considered in this work.

(b) A photo of the layout of the switch fabricated on a high resistivity substrate SOI wafer.

Fig. 7.1.: The RF antenna switch adopted in this work.

7.2.1 Insertion Loss and Isolation

The wireless system is in one of two states; transmission or reception. When in the transmission mode, a signal is leaving the PA and heading towards the RF antenna switch. The switch is then meant to guarantee a secured passage for the signal to the antenna. By secured passage we mean the maximum of the signal should reach the antenna (lowest possible insertion loss) and in the same time the LNA should be kept completely isolated from that signal (maximum isolation) or it would burn due to the high power transmitted by the PA. During reception, the same operation is repeated in a reverse way. The signal arriving at the antenna is needed to arrive at the LNA with minimum loss while being completely isolated from the PA.

The trade-off comes from the fact that the same transistor (either M1 or M2) is meant to provide maximum transmission in one case and a maximum isolation in the other case. If the previous paragraph is translated into device physics language, the secured passage is achieved through a transistor in the ON state (or in a strong inversion mode) of a common gate configuration , which means that the signal should pass from drain to source or the inverse. In other words, we need the ON resistance R_{ON} of the channel to be minimum to achieve minimum

loss of the signal or maximum passage of it. At the same time, the other series transistor (M2 or M1) is switched off (in deep subthreshold regime) and the two junctions source-body and drain-body are both reverse biased representing the off capacitance of the transistor C_{OFF}. For a perfect isolation, C_{OFF} should be minimum (giving a maximum impedance).

Therefore, to reduce insertion losses, R_{ON} needs to be minimum. This could simply be realized by increasing the transistor width. However, increasing the transistor width means more capacitive coupling with the substrate, which means more losses. It also affects the isolation, since more coupling will occur between the drain and the source through fringing capacitances. Hence, a trade-off should be found for an optimal value of the channel width. It is worth noticing here the advantage that an SOI device could present based on its highly reduced coupling capacitance (between the body and the substrate and between the drain/source and the substrate) due to the presence of the buried oxide. A SOI device with a high resistivity substrate is even a better choice since it highly reduces the losses through the substrate [5].

For a small-signal operation, the insertion loss (IL) could be calculated from R_{ON} using [4, 6]

$$IL = -20\mathrm{Log}_{10}\left(\frac{2R_0}{2R_0 + R_{\mathrm{ON}}}\right) \tag{7.1}$$

where R_0 is the sum of the source and the load resistances.

The second part of the task of providing a secured passage for the signal is achieved using the shunt transistors M3 and M4. Turning M3 or M4 ON provides a low impedance bridge between the corresponding port and the ground. This ensures a good protection of that port from the signal going through the switch. The level of protection depends on the value of the ON resistance of M3 or M4 which is controlled by the channel width. Again, the channel width should not be so much increased, otherwise, the desired signal is lost through capacitive coupling when M3 or M4 is turned OFF.

Another way to control the insertion losses (and reduce it) is to bias the gates of the series transistors M1 and M2 through a resistor of appropriate value R. In the absence of R, the voltage on the gates of M1 and M2, V_{GS}, fluctuates as a function of the applied RF signal at the drain. If a strong signal arrives at the drain, the channel resistance is highly increased resulting in an increase of the insertion losses. Therefore, the presence of R ensures a constant gate-to-channel voltage through the control of C_{gs} and C_{gd}, and hence, a stable channel resistance and an improvement of the linearity of the signal [3, 4].

7.2.2 Power Handling

The RF antenna switch is the first block of the circuit to meet the signal coming or leaving the transceiver which makes it subject to large signals either arriving at the antenna or leaving the power amplifier. The response of the switch to these large signals is very crucial, especially for the receiver circuitry which is dependent on the signal delivered to it by the switch. It is of utmost importance

that the signal passes through the switch without suffering from any compression or in other words that the switch operates in a perfect linear behavior. Therefore, the linear behavior constitutes the third figure of merit that characterizes the RF antenna switch. The best method to measure this behavior is the 1-dB input compression point $P_{\text{1-dB}}$. It is defined as the input power which results in a 1 dB reduction in the gain of the device under test. In the case of the RF antenna switch, $P_{\text{1-dB}}$ measures the 1-dB drop in the loss rather than in the gain. Huang and O [4] reported on the linearity problems provoked by the drain/source junctions in the bulk devices when used in building the RF antenna switch. For a zero biased gate and drain of the transistors M1 and M2, the RF signal arriving at the drain of any side of the switch could forward bias the drain/source to body junctions, resulting in a sudden drop in the insertion losses, thus clipping the RF signal and causing the output power to compress. Huang proposed a dc biasing to the drains of the transistors M1 and M2, otherwise the $P_{\text{1-dB}}$ of switches built using bulk devices is fixed at 6 dB [3]. The advantage of using a SOI device is evident to overcome this problem since the presence of the buried oxide (BOX) eliminates the junction between drain/source and bulk.

The sudden drop in insertion loss (the compression) of the RF antenna switch can also be caused by an undesired turning ON of a transistor which should be turned OFF. This could occur due to the arrival of a large RF signal at the drain of a transistor. It is difficult to completely eliminate this risk or to design a perfect switch against this phenomenon, yet, the voltage at which it occurs could be pushed to higher values. This is achieved by employing relatively high resistances at the gates of the transistors. A 10 kΩ is proposed as an adequate value for these gate resistances R [3, 4]. This value of resistance is high enough to favor a voltage dividing between the C_{gs} and C_{gd} of the OFF transistor, hence, a voltage proportional to the ratio $C_{\text{gs}}/(C_{\text{gs}}+C_{\text{gd}})$ should appear at the gate of the OFF transistor. This transistor is then guaranteed to work in the OFF for a signal of an amplitude as high as a value calculated using (see Fig. 7.2) [3]:

$$|V_{\text{GS}} - V_{\text{in}}| = \left| \frac{C_{\text{gs}}}{C_{\text{gs}} + C_{\text{gd}}} \times V_{\text{in}} \right| = V_T \tag{7.2}$$

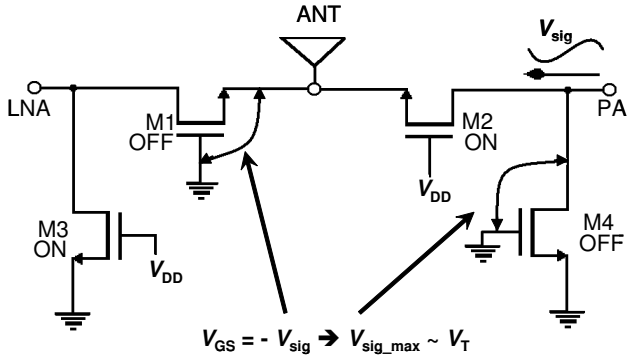
$$|V_{\text{in}}| = \frac{C_{\text{gs}} + C_{\text{gd}}}{C_{\text{gs}}} \times V_T \tag{7.3}$$

Therefore, the compression can be calculated (in dBm) from:

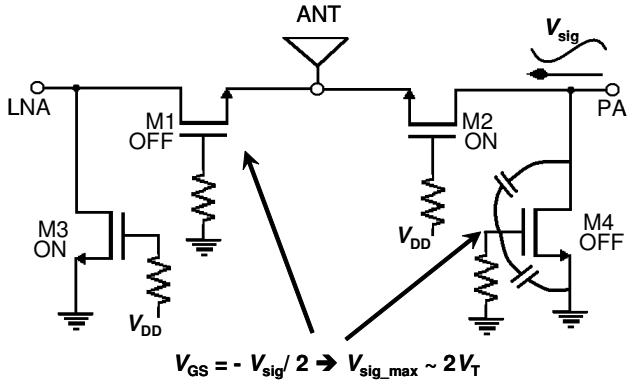
$$P_{\text{1-dB}} = 10\text{Log}_{10}\left(\frac{C_{\text{gs}} + C_{\text{gd}}}{C_{\text{gs}}} \frac{V_T^2}{50} \right) + 30 \tag{7.4}$$

7.3 LAYOUT

The fabricated layout of the RF antenna switch on the 130 nm high resistivity SOI technology is presented in Fig. 7.1b.



(a) Without R



(b) With R

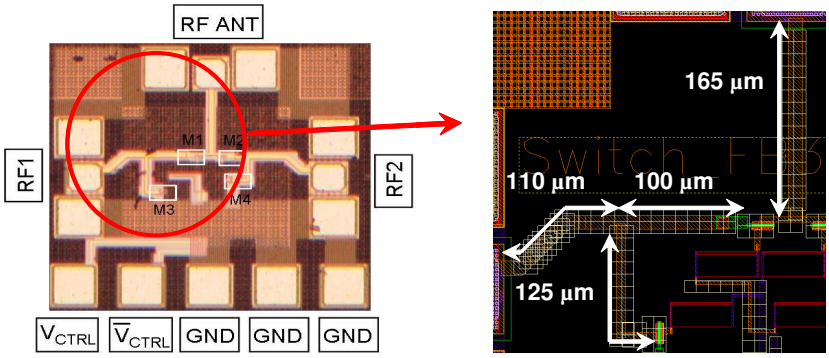
Fig. 7.2.: Illustration of the role of R connected to the gates of the transistors in enhancing the linearity of the RF antenna switch [7].

Both the optimization of the layout of the RF antenna switch or the optimization of the layout of the individual transistors used in the design might significantly affect the performance of the RF antenna switch. The later was introduced in the previous chapters through the comparison of the performance of different transistors in SOI and bulk technologies. The former will be discussed in this chapter.

The presented layout of the RF antenna switch in Fig. 7.1b features an area of 700×650 μm^2. This huge area is mainly occupied by RF pads needed to perform on-wafer measurements (100-μm pitch size pads), whereas the real 8 elements of the switch (4 transistors + 4 resistors) could occupy a much smaller area.

Fig. 7.3 shows the long metal lines needed to connect the RF pads to the ports of the RF antenna switch. The length of the metal lines ranges from 200 to 240 μm. These lines are fabricated using Metal-6 layer, without a ground layer underneath, except for the substrate of the wafer being grounded (taking into account the presence of the thick BOX layer in between). The effect of

these metal lines plays a significant role in determining the performance of the RF antenna switch as presented later in this chapter by employing individual transistor measurements and ADS black-box simulations.



(a) The layout of the switch where the metal lines are highlighted.

(b) The lengths of the connecting metal lines.

Fig. 7.3.: The metal lines connecting the measurement pads to the actual circuit of the RF antenna switch.

7.4 OPERATION

The operation of a RF antenna switch is simple. To allow the passage for transmission between the PA and the antenna, V_{ctrl} is set to HI (or V_{DD}) and $\overline{V}_{\text{ctrl}}$ is set to LOW (or zero). In this case, M2 is turned ON in strong inversion mode while M1 is turned OFF in deep subthreshold mode in order to provide one path only for the signal from the PA to the antenna and prevent it from going to the LNA (see Fig. 7.4). Most of the signal goes through M2 to the antenna. However, a small part of it is coupled to the ground through the C_{OFF} of M4 and through the C_{OFF} of M1 and the R_{ON} of M3. The LNA is tied to the ground via the R_{ON} of M3, so the smaller the value of R_{ON}, the better the LNA is isolated from the signal departing from the PA.

7.5 MEASUREMENT SETUP

Measurements were performed using a 2-port setup, thus it is either the transmission side or the receiver one, while the other side is matched with a 50 Ω. Normally since one of the two series transistors (M1, M2) is ON while the other is OFF, the OFF transistor acts as an open circuit, therefore this setup should provide accurate results. In fact, measurements using a 3-port setup (employing a 4-port PNA-X from Agilent) were performed and compared to the 50 Ω matched environment measurements and results were found to be very close.

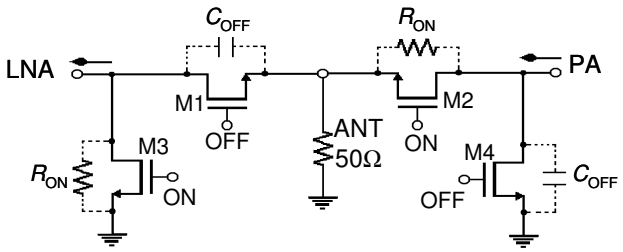


Fig. 7.4.: Transistors states at the moment of transmission through the RF antenna switch.

Hence, for simplicity (especially for calibration and de-embedding), the 2-port measurement environment is used throughout.

Direct on-wafer RF measurements of the RF antenna switch is performed using the 2-port Anritsu 37369A™ vector network analyzer VNA operating between 40 MHz and 40 GHz.

Three sets of RF antenna switches were fabricated and measured on three technologies: PD SOI, FD SOI and DNW Bulk. FB, BT, and DT structures were used in the design with different number of fingers. For each switch, the four transistors are always identical (the same dimensions and the same number of fingers). In the following, the different RF antenna switches are characterized and compared at room temperature and with increasing temperature till 200^{o}C.

7.6 ROOM TEMPERATURE MEASUREMENTS

The comparison of the different RF antenna switches presented in this chapter is realized via the two figures of merit, the insertion loss and the isolation. It should be noticed that these two figures of merit are very dependent, a higher isolation on one side of the switch means a better insertion loss on the other side and vice versa. This is a general rule, however, the real values of these two figures of merit is highly dependent on the values of R_{ON} and C_{OFF}.

PD SOI devices are compared in Fig. 7.5. Starting by the insertion loss of 30 fingers devices, the FB transistor shows a better insertion loss than both the BT and the DT transistors as shown in Fig. 7.5a. On the other hand, the FB transistor presents the worst isolation compared to the other two transistors as presented in Fig. 7.5c. As described earlier, increasing the width of the transistor could reduce the channel ON resistance R_{ON}, hence enhancing its insertion loss. Fig. 7.5b shows the insertion loss of 90 fingers transistors (3 times wider than the previous case). It is clear that the insertion losses of the BT and the DT transistors are enhanced, but only at low frequency. The FB transistor, on the other hand, shows a reduced insertion loss performance. Increasing the number of fingers has two contradictory effects. It reduces the channel ON resistance R_{ON} but in the same time it increases the drain/body and the source/body junction

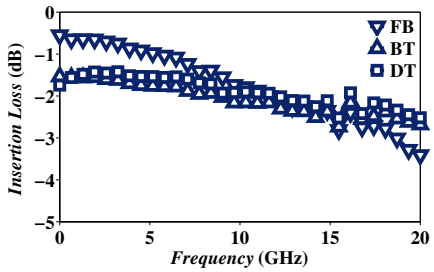
capacitances as well as the parasitic coupling capacitance with the substrate, due to the increased area. The overall performance of the transistor depend on whichever effect is more dominant. In the case of BT transistor, only one junction exits, the one between the drain and the body, whereas the other one between the source and the body is suppressed via the silicide short tying the body to the source (see Fig. 7.6). Therefore, the BT structure features a higher C_{ds} compared to the FB structure. Increasing the number of fingers, has a more pronounced impact on the BT transistor than on the FB transistor. To explain this fact, consider Fig. 7.4. Assuming a passage of the signal from the PA to the antenna, the BT transistor presents a lower R_{ON} of M2 due to an increased number of fingers, while keeping C_{OFF} of M1 and M4 high enough (lower Z_{OFF}) which means better isolation at low frequency (to prevent loss of signal through M4) but as frequency increases, the isolation degrades faster and hence, as seen from Fig. 7.5b, the degradation of the insertion loss of the BT transistors is faster than the FB transistor. In the case of the FB transistor, R_{ON} is also low but C_{OFF} is lower than in the case of the BT transistor, thus a lower isolation of M1 and M4 which means lower insertion loss at low frequency, but is more stable than the BT structure as frequency increases (see Fig. 7.5b and Fig. 7.5d).

From the previous discussion, the importance of M3 and M4 is clear. Fig. 7.5e and Fig. 7.5f highlight this importance. In these two figures, all transistors are turned OFF and the signal is measured as it passes from LNA to PA and from LNA or PA to antenna. In the first case (LNA-to-PA), the isolation is much better than in the case of (LNA-to-ANT) since two OFF transistors are found in the path of the signal, nevertheless, the isolation is much worse than the normal case of operation shown in Fig. 7.5c and Fig. 7.5d. The reason is the absence of the ground tie provided by M3 or M4. When the signal is measured between the LNA or the PA and the antenna in the OFF state, a highly degraded isolation is noticed since it only depends on one OFF transistor and no ground tie is provided.

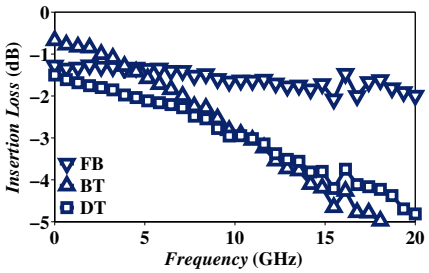
The optimization of both the insertion loss and the isolation is clearly difficult. Enhancing R_{ON} is tied to degrading C_{OFF} and hence the trade off is very tight. The result is obtained if stacked (cascoded) transistors structure is used, as shown in Fig. 7.7. Using this structure, C_{OFF} is divided by three and hence the isolation is improved, however, R_{ON} is multiplied by three which degrades the insertion losses.

The high resistivity (HR) substrate SOI technology is believed to be a remarkable solution for problems related to losses in circuits like RF antenna switches due to the reduction of substrate coupling and cross talk. Nevertheless, the special structure of the DNW protected bulk transistor shows an interesting behavior comparable and even better than that of the HR SOI switch. The idea of using DNW bulk devices to construct a high performance RF antenna switch has been elaborated in different publications [8–11].

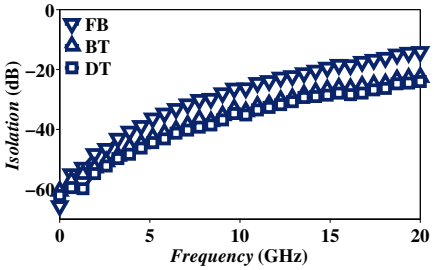
A comparison is held in Fig. 7.8 between the performances of a switch built using a DNW bulk device and a switch built using a PD SOI device. In both cases a FB and a BT structures are used with the same geometry and the same number



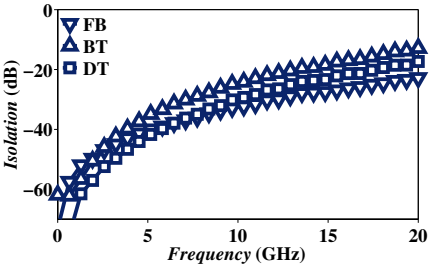
(a) Insertion loss in the RF antenna switch using 30-fingers devices.



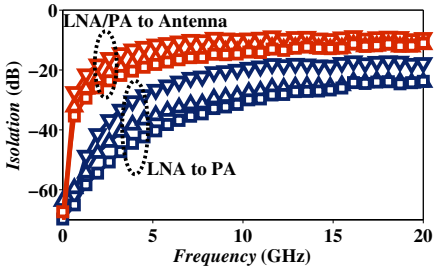
(b) Insertion loss in the RF antenna switch using 90-fingers devices.



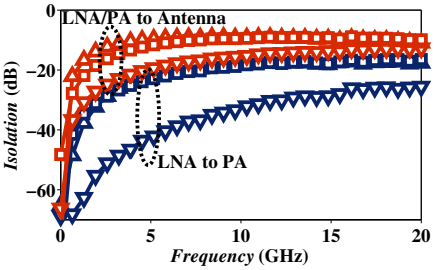
(c) Isolation in 30 fingers devices (from LNA to PA).



(d) Isolation in the RF antenna switch using 90-fingers devices (from LNA to PA).



(e) Isolation in 30 fingers devices in OFF state.



(f) Isolation in the RF antenna switch using 90-fingers devices in OFF state.

Fig. 7.5.: Insertion loss and isolation for the RF antenna switches using PD SOI devices. In the OFF state case, the effect of the transistors M3 and M4 is demonstrated.

of fingers ($L = 0.13$ μm, $W = 2$ μm, and $N_{\text{finger}} = 30$). Despite their standard resistivity (SR) substrate, the DNW bulk devices are capable of competing with the HR PD SOI devices in terms of the insertion loss and the isolation of the RF antenna switch. The reason is the highly suppressed coupling and leakage resulting from the presence of the DNW and the N+ isolation as explained in chapter 2 and chapter 3. It is worth noticing that the BT structure of the DNW

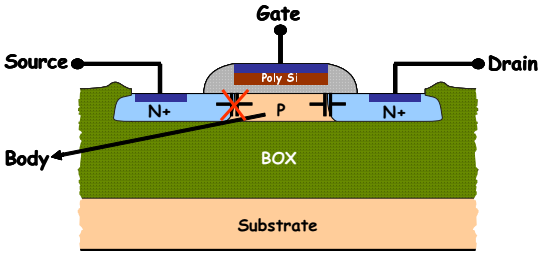


Fig. 7.6.: The FB transistor presents a lower C_{ds} capacitance compared to the BT transistor where the later has a suppressed body-to-source capacitance C_{bs} due to the body-source silicide short.

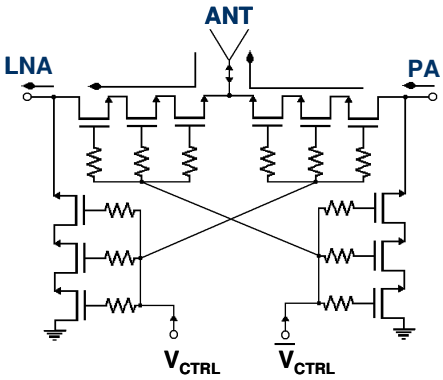
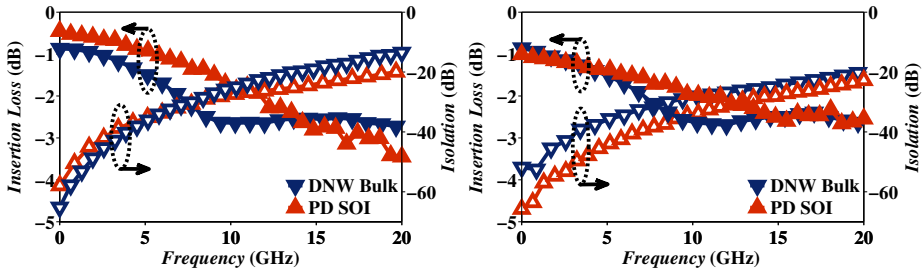


Fig. 7.7.: A RF antenna switch using cascoded transistors structure.

bulk device shows better insertion loss and degraded isolation compared to its PD SOI counterpart. This is the inverse of what is noticed for the FB device. The reason could be related to the optimized layout of the BT structure in the case of the DNW bulk device based on the experience gained during the design and the fabrication of the PD SOI device. In the bulk case, the metallic connections used to tie the body to the source are reduced, as shown in Fig. 7.9, where the number of body contacts is highly reduced in the DNW bulk layout. The result is less parasitic capacitances, hence, better insertion loss behavior and better isolation especially at lower frequencies.

The same RF antenna switch was designed and fabricated using the FD SOI technology on standard resistivity substrate using classical nMOS and GCMOS transistors. However, due to a problem of random metal filling process (used to get homogeneous mechanical rigidity of the wafer), the performance of these switches is highly degraded. Thus, it is not possible to compare their performance to the other switches presented earlier. However, they can be compared to each other and hence they serve as an indication of the advantage of using GCMOS transistors in RF circuits like the RF antenna switch.



(a) FB (b) BT

Fig. 7.8.: A comparison between the insertion loss (solid symbols) and the isolation (empty symbols) of RF antenna switches employing DNW bulk and PD SOI devices in FB and BT structures.

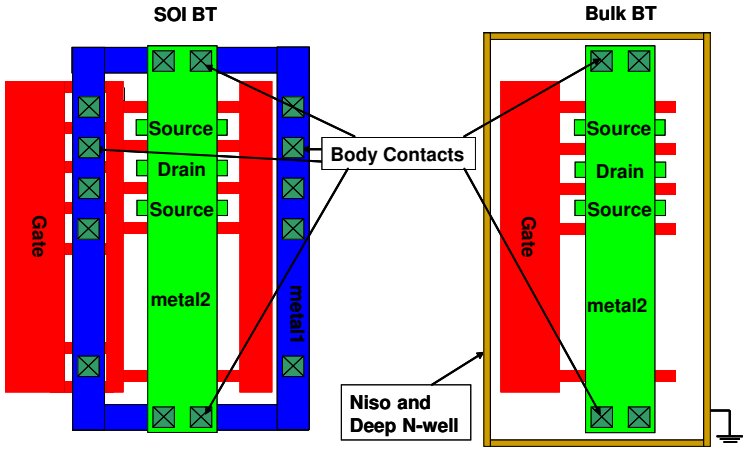


Fig. 7.9.: Layout of BT structures for PD SOI and DNW bulk devices.

Fig. 7.10 compares the behavior of a switch employing a classical FD nMOS of 96 fingers, 2.5 μm width and 0.15 μm length each, and a switch built using a GCMOS of 96 fingers, 2.5 μm width and 0.5 μm length each. The GCMOS device is nearly three times longer than the classical nMOS device, yet it gives a similar performance of insertion loss and isolation at room temperature as presented in Fig. 7.10.

The same effect of increasing the number of fingers (in order to increase the total width) of the transistor is noticed for the classical nMOS and the GCMOS structures of the FD SOI devices. Fig. 7.11 shows that a slightly better insertion loss can be obtained for a 96-finger device compared to a 32-finger device whereas the isolation performance is degraded.

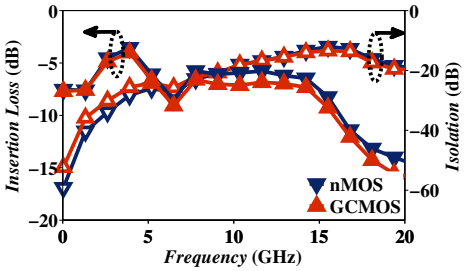
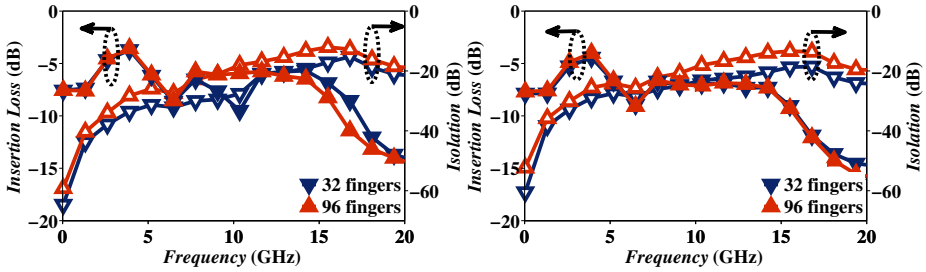


Fig. 7.10.: Insertion loss (solid symbols) and isolation (empty symbols) of classical nMOS and GCMOS FB devices fabricated on a FD SOI standard resistivity substrate technology.



(a) Classical nMOS (b) GCMOS

Fig. 7.11.: The effect of increasing the width (number of fingers) of a transistor as represented by the classical nMOS and the GCMOS structures of the FD SOI devices on the insertion loss (solid symbols) and the isolation (empty symbols) of RF antenna switch.

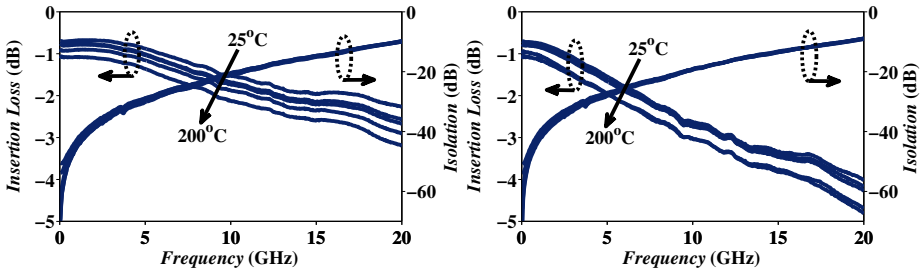
7.7 HIGH TEMPERATURE MEASUREMENTS

The RF antenna switches are mainly used to accomplish the complete integrity of the transceiver circuit with its three main parts: transmitter, receiver, and antenna. In its optimum solution, a System-on-Chip (SoC) combining the three parts is achieved. The drawback of this solution for the RF antenna switch is that it will suffer from the overheating of the whole system, although the switch itself might not generate much heat, since it only uses four transistors and four resistors with no dc drive current in any of them.

Nevertheless, the operation of the RF antenna switch in a high temperature environment did not receive any attention over the years. It was first reported in [12] for PD SOI devices in FB and BT structures then compared between PD SOI and DNW bulk devices in [11].

High temperature has the effect of degrading the insertion loss and the isolation performance of a RF antenna switch. This effect can be seen in Fig. 7.12 for PD SOI devices in both FB and BT structures. Based on the characteri-

zation of these transistors in chapter 3, Fig. 3.53 shows the stability of C_{ds} in OFF state (C_{OFF}) with temperature. On the other hand, Fig. 3.46, Fig. 3.47, Fig. 3.48, and Table 3.9 show the severe degradation (increase) of the drain and source resistances, which would directly affect the R_{ON} of the devices as temperature increases. As a result, while the isolation performance of the switches in Fig. 7.12 are not severely degraded with temperature, the insertion loss is clearly affected by the increased temperature and the increased R_{ON}. Taking the frequency of WLAN application as an example, i.e. 2.54 GHz, the insertion loss degrades by 0.5 dB ($\sim$ 45%) whereas the isolation degrades by 2 dB ($\sim$ 5%) for the BT structure. In the case of the FB structure, the degradation is 0.43 dB ($\sim$ 62%) in the insertion loss and 1.9 dB ($\sim$ 5%) in the isolation. A slightly better stability of insertion loss with temperature is attributed to the BT structure. Consulting Table 3.9, the extrinsic resistances $R_d + R_s$ are slighly more stable for BT compared to FB structures (which can be even related to the accuracy of measurement and extraction). The same applies to the channel resistance variation with temperature which can be derived from the variation of the maximum drain current with temperature. On the other hand, BT structure shows an increase in C_{ds} in OFF state which is approximately double the increase in the case of the FB structure. Therefore, it is the C_{OFF} which highly affects the insertion loss at high temperatures rather than the R_{ON}. But since R_{ON} varies slightly with temperature in the same way for both structures, the isolation behavior also varies slightly and with exactly the same percentage for both strucutres.

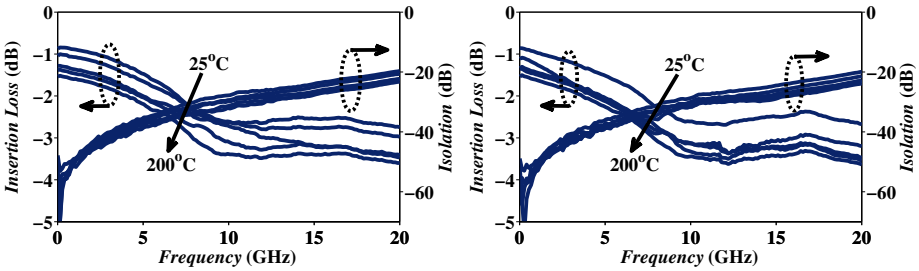


(a) FB (b) BT

Fig. 7.12.: The variation of the insertion loss and the isolation with temperature for RF antenna switches employing FB and BT PD SOI devices.

The same reasoning can be applied to the temperature behavior of RF antenna switch employing DNW bulk devices and shown in Fig. 7.13. To compare its behavior with the PD SOI case, the same frequency is chosen for comparison i.e. 2.54 GHz. For the BT structure, the insertion loss degrades by 0.7 dB ($\sim$ 60%) and the isolation degrades by 2.9 dB ($\sim$ 6.7%). In the case of the FB structure, the insertion loss degrades by 0.7 dB ($\sim$ 70%) whereas the isolation degrads by 6.8 dB ($\sim$ 7.5%). It is clear that the trend is the same as in the PD SOI

devices, BT structure shows less variation of the insertion loss with temperature than the FB structure, whereas the isolation behavior is more or less the same between the two structures. On the other hand, the degradation in the DNW bulk devices is more remarkable than in the case of the PD SOI transistors which is still expected due to the larger junction capacitances in the bulk case.



(a) FB (b) BT

Fig. 7.13.: The variation of the insertion loss and the isolation with temperature of RF antenna switches employing FB and BT DNW bulk devices.

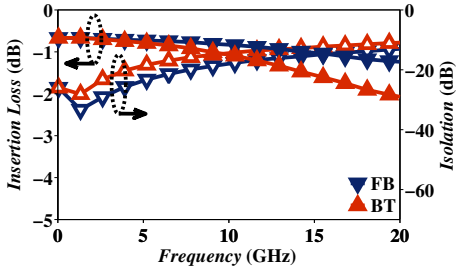
7.8 SIMULATION

This section does not present the simulations performed prior to the design and fabrication of the RF antenna switch. It rather presents the post measurement simulations. This kind of simulations helps to correctly and deeply understand the behavior of the RF antenna switch. It also presents a better methodology to design the RF antenna switch based on detailed analysis of the different elements of the circuit and the layout.

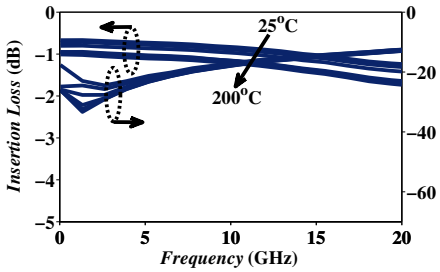
Starting by the main building block of the switch, i.e. the transistor, it is clear that, from the RF point of view, all the transistors used in the RF antenna switch are configured in the common gate operation mode. All the transistors operate in either ON or OFF states, or in other words, V_{GS} equals either 0 or V_{DD} while V_{DS} is always set to 0 V (dc). On-wafer RF measurements are performed on PD SOI FB and BT structures in ON and OFF states starting from room temperature till 200^{o}C. The measured S-parameters are then utilized as a black-box in RF simulations using Advanced Design System (ADS) software [13]. In other words, these S-parameters are used as a look-up table in the RF antenna switch circuit thus generating results as close to the real measurements of the switch as possible. This approach helps to accurately characterize the rest of the elements in the circuit.

7.8.1 Transistors in Common Gate Configuration

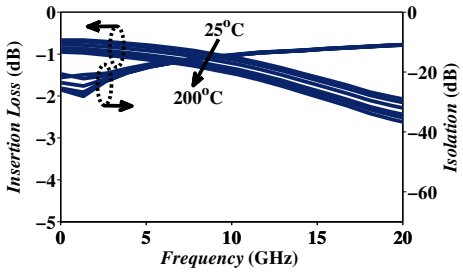
The first step to perform the black-box simulation is to acquire the measured S-parameters of the individual transistors in the ON and OFF states. On-wafer measurements are performed on the PD SOI devices in both FB and BT structures at room temperature and at varying temperature followed by a 1-step (Open) de-embedding procedure. The results are shown in Fig. 7.14. For the ON state, V_{GS} is set to V_{DD} while V_{DS} is kept at 0 V. For the OFF state, V_{GS} and V_{DS} are both set to 0 V. The insertion loss and the isolation characteristics of the transistor are then simply its S_{21} represented in dB[1]. In Fig. 7.14a, the room temperature behavior is shown for both structures.



(a) FB and BT structures at room temperature.



(b) FB structure at varying temperature.



(c) BT structure at varying temperature.

Fig. 7.14.: The variation of the insertion loss and the isolation with temperature for FB and BT structures of the PD SOI devices connected in common-gate configuration.

The tendency of the curves is in accordance with the direct measurements of the RF antenna switch shown earlier, that is the FB structure shows better insertion loss and isolation performances than the BT structure. The absolute values of the insertion loss of the common gate transistors are very close to the values shown earlier of the RF antenna switch. For example, taking the frequency of 2.54 GHz, the switch built using the PD SOI in the FB structure features an insertion loss of −0.69 dB at room temperature whereas the one built using the

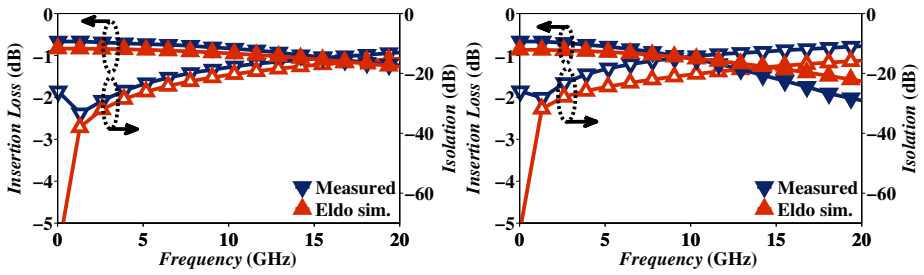
[1]For the S-parameters, the value in dB is calculated using 20Log(the magnitude) since S-parameters are voltage based.

BT structure features an insertion loss of −0.97 dB. The individual transistors feature −0.685 and −0.69 for the FB and the BT structures, respectively. On the other hand, the isolation performance of the individual transistors are worse compared to the isolation performance of the switches presented earlier. This again shows the importance of the implementation of the series-shunt topology used and the role of the two shunt transistors M3 and M4.

7.8.2 Eldo Simulations of Common Gate Transistors

The behavior of the individual transistors is also compared using compact models delivered by the foundry. Simulations are run using Eldo RF [14]. Comparing these simulations to the individual transistors measurements presented in section 7.8.1 helps to evaluate these models at the special conditions of operation of the transistors in the RF antenna switch circuit, i.e. RF behavior for ON/OFF states. Later, the *S*-parameters generated using Eldo RF are also used as black-boxes for ADS simulations of the entire RF Antenna switch.

In Fig. 7.15, a comparison is held between the on-wafer RF measurements and the Eldo RF generated *S*-parameters. As expected, the Eldo RF generated *S*-parameters show better insertion loss and isolation behaviors whereas the measured ones suffer from parasitics and imperfect de-embedding. However, the trend is practically the same. The accuracy of the compact models at the ON/OFF states is also verified.



(a) FB (b) BT

Fig. 7.15.: Comparison of insertion loss (solid symbols) and isolation (empty symbols) behaviors at room temperature for FB and BT structures of the PD SOI devices using on-wafer RF measurements and compact model Eldo RF simulations.

7.8.3 Measurements versus Simulations

The simulation of the RF antenna switch is performed using Advanced Design System (ADS) tool. In a first step the simulation is presented without taking into account the connecting metal lines. Later, the effect of the connecting metal

lines will be simulated using inductors and resistors in order to fit the measured behavior of the RF antenna switch. It should be noticed that in all cases the effect of the RF pads is simulated by means of a 85 fF capacitance added in parallel to the circuit ports (this value is extracted from an Open structure measurements using $\mathrm{Im}(Y_{11})/\omega$).

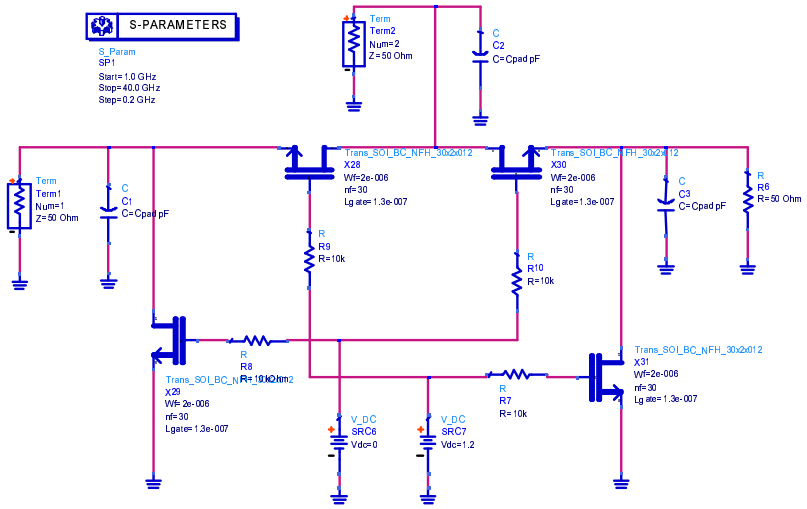
A comparison is held between the measured insertion loss and isolation and two types of simulated insertion loss and isolation. The first is using the measured S-parameters of individual transistors put as black-boxes in the ADS schematic, so it basically acts as a look-up table of the transistor S-parameters. The second is using the extracted S-parameters from Eldo RF simulations using a compact model delivered by the foundry. The extracted S-parameters are again used in ADS as black-boxes (look-up table).

Fig. 7.16 shows the schematic used in ADS to simulate the behavior of the RF antenna switch. The use of the black-boxes is illustrated. In the case of the black-boxes, no dc bias is needed since the S-parameters contained inside the black-boxes are already at the correct bias, either in ON or OFF state, according to the selected scheme of the switch. A standard RF simulation is run and the results are shown in Fig. 7.17. The results show the comparison between the on-wafer measured data of the RF antenna switch and the simulated data, using the two previously mentioned methods, without taking into account the effect of the connecting metal lines (which, as mentioned before, have lengths that range between 200 to 240 μm). It is clear that, in general, the performance is much better without the metal lines compared to actual measured data of RF antenna switch.

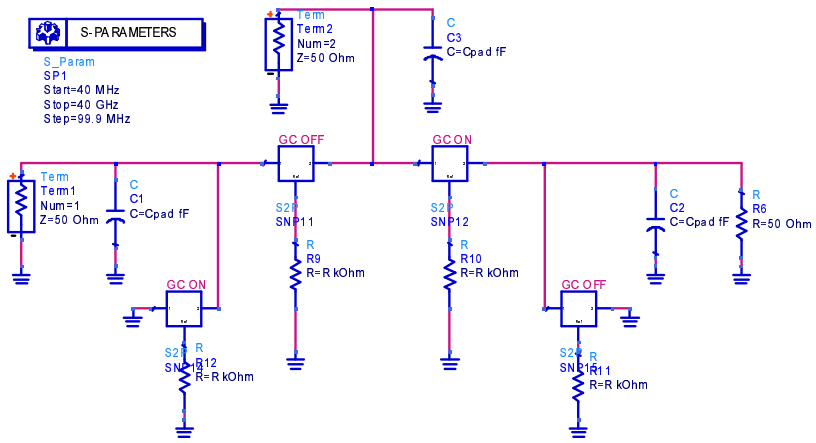
7.8.4 Effect of Metal Lines

In order to reach the best simulation of the metal lines included in the circuit of the RF antenna switch, each line has been replaced by an inductance and a resistance (in series) in the ADS simulation as shown in Fig. 7.18. The complete schematic in ADS after adding the inductances simulating the metal lines is shown in Fig. 7.19. The inductance elements and the associated series resistances are then tuned to achieve the best fitting between the measured and the simulated RF antenna switch behavior.

Fig. 7.20 shows the results for the insertion loss of the simulation and fitting when the black-box of measured common gate transistor is used. In these figures, it is assumed that the black-box and the pads are already represented, hence the difference between the measurement and simulation should be completely due to the metal lines, therefore, aggressive fitting is performed in order to minimize this difference. The values of the used inductance values are shown on the figures and summarized in Table 7.1. Nevertheless, when the same values of inductances are used to fit the isolation curves, the expected perfect fitting could not be achieved. The values of the inductances should be fitted once more to minimize the difference between measured and simulated curves. The reason could be a non accurate extraction of the pad capacitance along with an imperfect measurement



(a) Using standard transistor models.

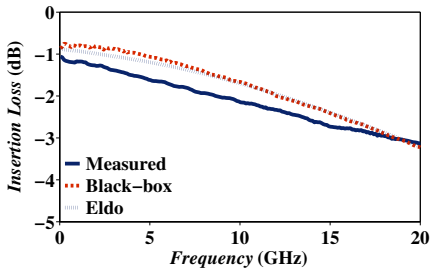


(b) Using black-boxes of measured or Eldo RF simulated S-parameters.

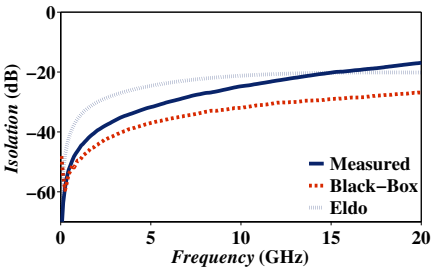
Fig. 7.16.: ADS schematics of the RF antenna switch using the standard transistors models provided by the foundry and using the black-boxes of the measured and Eldo RF simulated S-parameters.

and de-embedding of the common gate individual transistors. A slight difference in the length of the metal lines from one side to the other in the layout could also be one of the reasons behind this difference in the values of inductances.

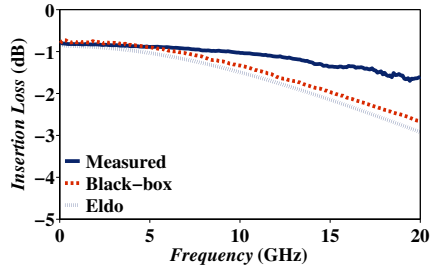
The same approach is repeated using the Eldo RF simulated black-box of S-parameters. Using the same values of inductances that were able to fit the



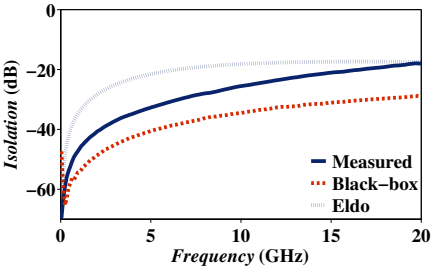
(a) Insertion loss of RF antenna switch using BT structure.



(b) Isolation of RF antenna switch using BT structure.



(c) Insertion loss of RF antenna switch using FB structure.



(d) Isolation of RF antenna switch using FB structure.

Fig. 7.17.: A comparison between the measured performance of the RF antenna switch and the performance simulated using ADS employing the black-boxes (look-up tables) of the S-parameters measured and simulated using Eldo RF of the individual common gate transistors.

curves with the measured black-boxes would not succeed to fit the curves using Eldo simulated black-boxes. However, this could be understood since the two types of black-boxes already showed a difference when compared in section 7.8.2. Nevertheless, the difference is expected to be lower than found and reported in Fig. 7.21.

Despite the inconsistency of the values of the inductances and resistances used to simulate the connecting metal lines, an important fact is clear and evident, which is the pessimistic performance represented by the measured behavior of the RF antenna switch. The metal lines are certain to affect this performance and to show a lower performance than the real behavior of the RF antenna switch without that effect of metal lines. Whether a de-embedding procedure is performed or not, the effect of the metal lines should be removed using a backward simulation technique in order to be able to correctly design the RF antenna switch. In fact, having hands on the real performance of the switch might relax some constraints at the device fabrication level which could have been put assuming a lower than real performance.

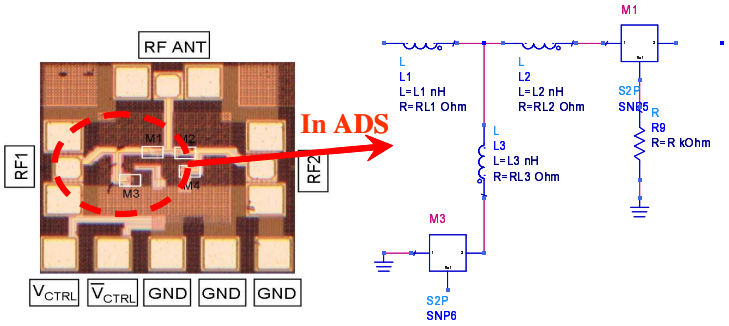


Fig. 7.18.: Illustration of the modeling of the connecting metal lines in the RF antenna switch using ADS.

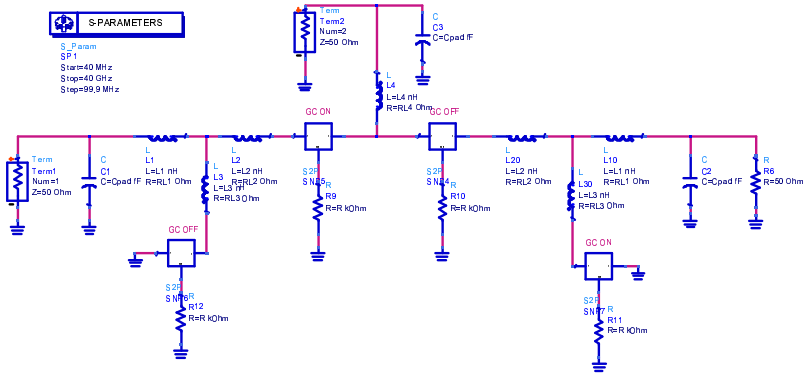


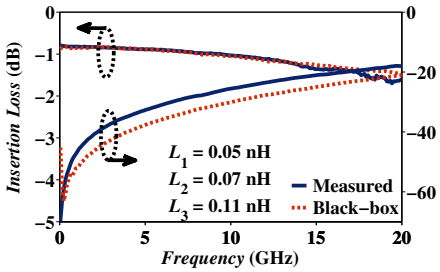
Fig. 7.19.: The complete ADS schematic after adding the inductances used to simulate the effect of the metal lines. Each inductance is tuned individually. A series resistance element is associated with each inductance.

7.8.5 Simple Simulation Approach

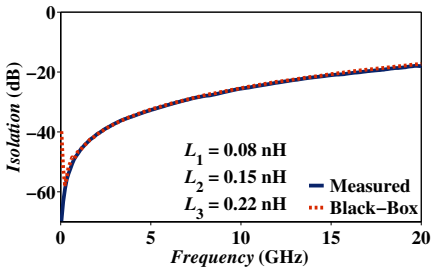
The inconsistency reached in section 7.8.4 makes it a complicated task to remove the effect of the metal lines. In this sub-section, another simple simulation approach is presented.

Fig. 7.3b shows the metal line connecting transistors M1 and M3 to the RF pad. This line is made on metal-6 layer, without a ground line underneath, so when a model of a Thin-Film Micro-Strip (TFMS) line is used to model this line in ADS, it does not fit the measured behavior of the switch.

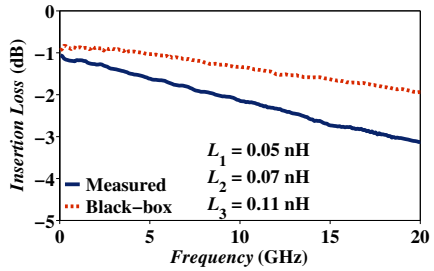
An inductance is added in series with each ON transistor in order to compensate for the inductive effects of the line, taking into consideration a typical value of 1 nH/mm, and using this value as a maximum limit for the tuning performed to fit the measured curves. It is also noticed that a resistance has to be



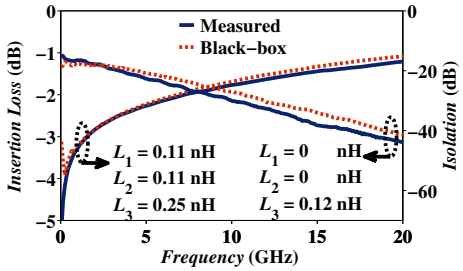
(a) Insertion loss and isolation of RF antenna switch employing FB structure using the same tuned values of inductances.



(b) Isolation of RF antenna switch employing FB structure using independent tuning of inductances.



(c) Insertion loss of RF antenna switch employing BT structure using the same tuned value of inductances as used for the FB structure.



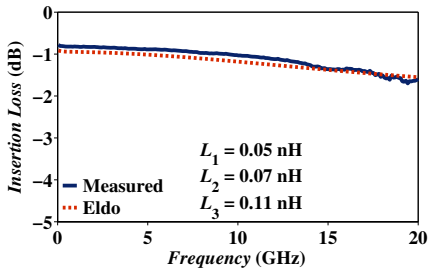
(d) Insertion loss and isolation of RF antenna switch employing BT structure using independent tuning of inductances.

Fig. 7.20.: The illustration of the effect of the metal lines through the comparison of the different performances of the RF antenna switch as measured and as simulated using ADS employing the black-boxes of measured S-parameters and tuned values of inductances and resistances.

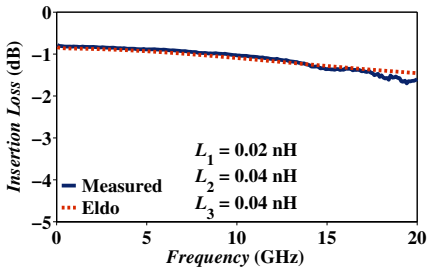
added in series to the ON transistor to correct for the low frequency difference between the measured and the simulated curves. The schematic used is shown in Fig. 7.22.

To have full control on fitting, the box of measured S-parameters of the common gate transistor (which is used to model the OFF transistors) is replaced by a C_{OFF} capacitance. The variation of C_{OFF} while fitting the curves is restricted around the extracted values for the C_{OFF} of the different transistor structures (see Table 7.2).

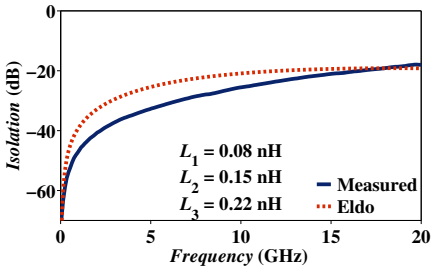
Using these correcting parameters (series inductances and resistances), excellent fitting was found for the RF Antenna switch built using the PD SOI devices, both in FB and BT structures, with regards to the insertion loss and the isolation performances as shown in Fig. 7.23 for 30 fingers transistors and Fig. 7.24 for 90 fingers transistors. Mostly, the same values of the extracted C_{OFF} and R_{ON} are the ones giving the best fitting. The only exception is the isolation curve of the



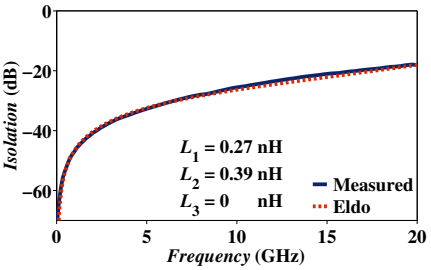
(a) Insertion loss of RF antenna switch employing FB structure using the same values of inductances as in Fig. 7.20a.



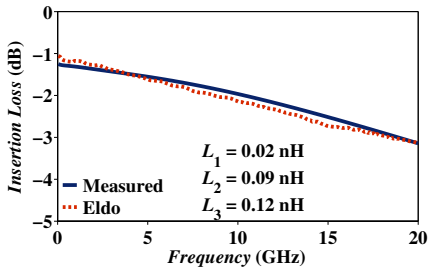
(b) Insertion loss of RF antenna switch employing FB structure using tuned values of inductances.



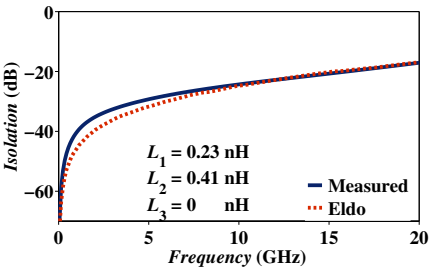
(c) Isolation of RF antenna switch employing FB structure using the same values of inductances as in Fig. 7.20b.



(d) Isolation of RF antenna switch employing FB structure using tuned values of inductances.



(e) Insertion loss of RF antenna switch employing BT structure using tuned values of inductances.



(f) Isolation of RF antenna switch employing BT structure using tuned values of inductances.

Fig. 7.21.: The illustration of the effect of the metal lines through the comparison of the different performances of the RF antenna switch as measured and as simulated using ADS employing the black-boxes of Eldo RF simulated S-parameters and tuned values of inductances and resistances.

switch built using the BT structure of 30 fingers (see Fig. 7.23d). A good fitting is not found unless the measured S-parameters black-box is used (instead of the C_{OFF} variable) and taking into account the pad capacitance of 84 fF (which was

Table 7.1.: The values of the inductances (nH) and the resistances (Ω) used to simulate the effect of the connecting metal lines for the switches built using PD SOI devices in FB and BT structures featuring 30 fingers.

Type	Behavior	L_1	L_2	L_3	L_4	R_1	R_2	R_3	R_4	Fig.
Black-box										
FB	*IL*	0.05	0.07	0.11	0.18	1	0	3	0	Fig. 7.20a
	Iso	0.08	0.15	0.22	0.15	0	23	15	9	Fig. 7.20b
BT	*IL*	0	0	0.12	0.18	3	3	10	0	Fig. 7.20d
	Iso	0.11	0.11	0.25	0.06	0	20	6	9	Fig. 7.20d
Eldo-RF										
FB	*IL*	0.02	0.04	0.04	0.24	0	0	3	0	Fig. 7.21b
	Iso	0.27	0.39	0	0	0	0	0	134	Fig. 7.21d
BT	*IL*	0.02	0.09	0.12	0	2	2	11	1	Fig. 7.21e
	Iso	0.23	0.41	0	0	0	0	0	90	Fig. 7.21f

disregarded for all the other curves, yet a very good fitting is achieved, since the presence of the pad capacitance makes no change to the simulated curves).

It is interesting to notice that a very good fitting is also achieved without even using the black-boxes for the ON transistors. The simple use of the extracted R_{ON} to represent the ON transistors (see Fig. 7.25) can result in a very good fitting (the value of C_{OFF} is kept the same while the value of R_{ON} is finely tuned) as shown in Fig. 7.23e.

Table 7.2.: Characteristics of the RF antenna switches built using PD SOI transistors in FB and BT structures featuring 30 and 90 fingers.

	Insertion Loss (dB)			Isolation (dB)		
Frequency (GHz)	2.4	5	10	2.4	5	10
BT (30 fingers)	−1.165	−1.345	−1.946	−37.16	−30.94	−24.18
FB (30 fingers)	−1.023	−1.152	−1.572	−38.84	−32.89	−26.06
BT (90 fingers)	−0.8068	−1.421	−2.775	−35.21	−27.89	−19.6
FB (90 fingers)	−0.6197	−0.8681	−1.669	−37.43	−30.1	−21.39

	R_{ON} (Ω)	C_{OFF} (fF)
BT (30 fingers)	14	39
FB (30 fingers)	10	46
BT (90 fingers)	4.5	120
FB (90 fingers)	5	102

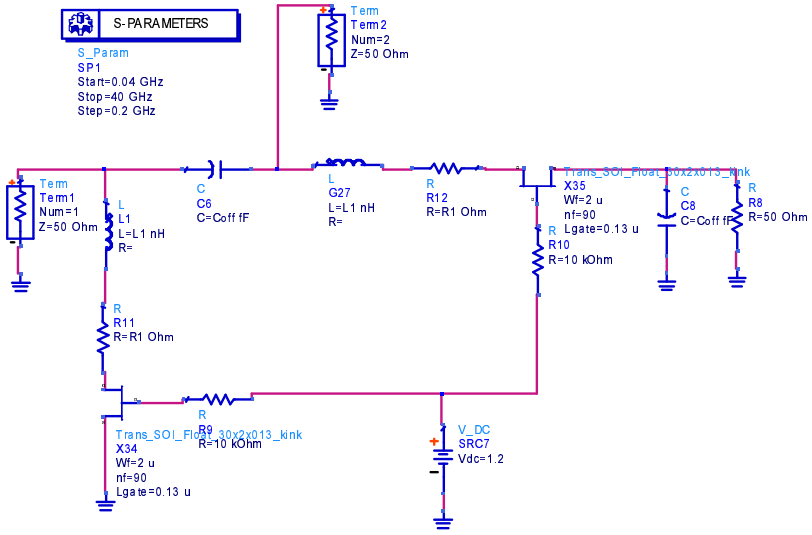
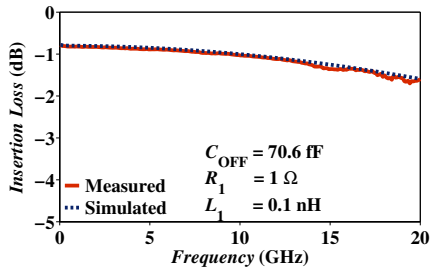


Fig. 7.22.: ADS schematic used to simulate the effect of metal lines using black-boxes of measured S-parameters for the transistors in ON state while using C_{OFF} to represent the transistors in OFF state.

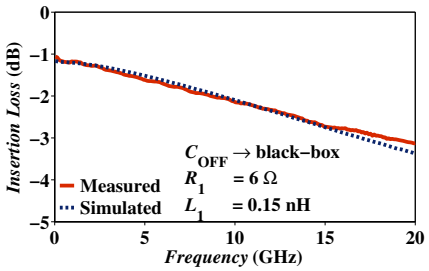
7.9 LINEARITY MEASUREMENTS

The power handling properties or the linearity of the RF antenna switch is characterized using a 4-port Agilent PNA-X. A special calibration kit is associated with these measurements which contains orthogonal SOLR structures. Both single-tone and two-tone measurements are possible using this setup. For the single-tone measurement, a sweep in power from -30 to 10 dBm at a single frequency point is applied to the LNA or the PA port of the RF antenna switch and the output measured at the Antenna port, or vice versa. The calibration step has to be repeated for each frequency point. A power sweep calibration, a response calibration as well as a traditional S-parameters calibration are needed to completely correct for the errors of the equipment (including the embedded power sources and receivers) and the cables. The single-tone measurement allows for the measurement of the 1-dB compression point $P_{\text{1-dB}}$.

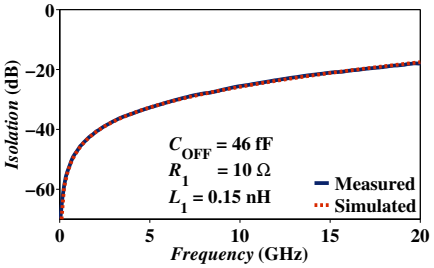
On the other hand, the two-tone measurement does not need any calibration steps since the PNA-X operates as a spectrum analyzer. It applies two signals with a certain frequency offset and having the same power. The measurements are performed using different signal power values ranging from -10 to 10 dBm. A simple calculation allows to evaluate the third intercept point IP_3.



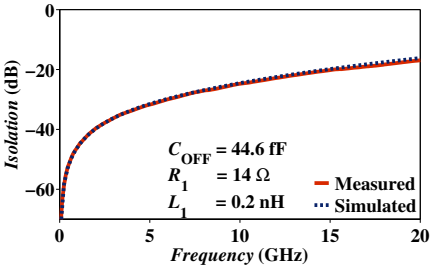
(a) Insertion loss of RF antenna switch employing FB structure.



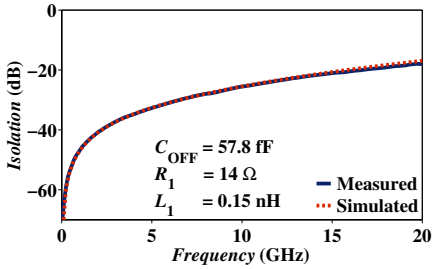
(b) Insertion loss of RF antenna switch employing BT structure.



(c) Isolation of RF antenna switch employing FB structure.



(d) Isolation of RF antenna switch employing BT structure.

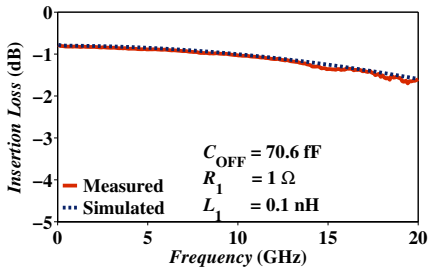


(e) Isolation of RF antenna switch employing FB structure without using the black-box for ON transistor and replacing it with R_{ON}.

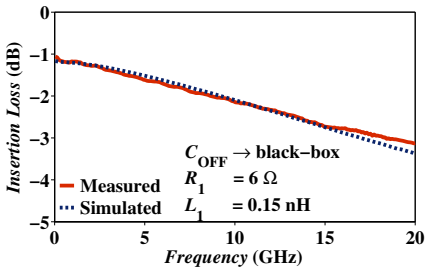
Fig. 7.23.: Comparison between 2-port measurements and ADS simulations using the simple approach for RF antenna switches employing 30 fingers FB and BT PD SOI transistors.

7.9.1 Gain Compression $P_{1\text{-dB}}$

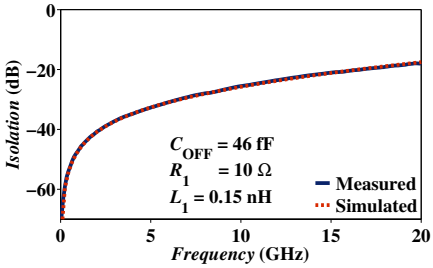
The results of the single-tone measurements for PD SOI devices are shown in Fig. 7.26. The three structures considered in PD SOI are compared using two geometries, one containing devices featuring 30 fingers and the other built using devices featuring 90 fingers. For the 30-fingers case (Fig. 7.26a), the DT switch



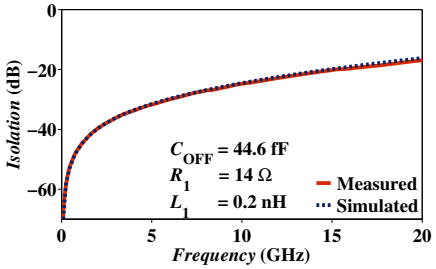
(a) Insertion loss of RF antenna switch employing FB structure.



(b) Insertion loss of RF antenna switch employing BT structure.



(c) Isolation of RF antenna switch employing FB structure.



(d) Isolation of RF antenna switch employing BT structure.

Fig. 7.24.: Comparison between 2-port measurements and ADS simulations using the simple approach for RF antenna switches built using 90-fingers FB and BT PD SOI transistors.

shows a high $P_{1\text{-dB}}$ compared to the other switches but then falls fast as frequency increases. Nevertheless, it is still comparable to the FB switch, whereas the BT switch shows the best power handling capabilities especially the stable behavior with frequency. This better power handling capability is significantly confirmed in the case of switches with 90-fingers transistors (Fig. 7.26b). The connection between the body and the source protects the source/drain-body junctions from becoming forward biased. On the other hand, the floating body (in the FB case) and the body to gate connection (in the DT case) makes the transistors more vulnerable for a forward biased junction which highly affects the compression point of the device as explained in section 7.2.2. Consequently, increasing the number of fingers of the transistor (from 30 to 90) makes this phenomena more manifested.

7.9.2 Third Intercept Point IP_3

The two-tone measurement used to characterize the IP_3 behavior of the switches employs two signals of equal power and a frequency offset of 1 MHz. The power

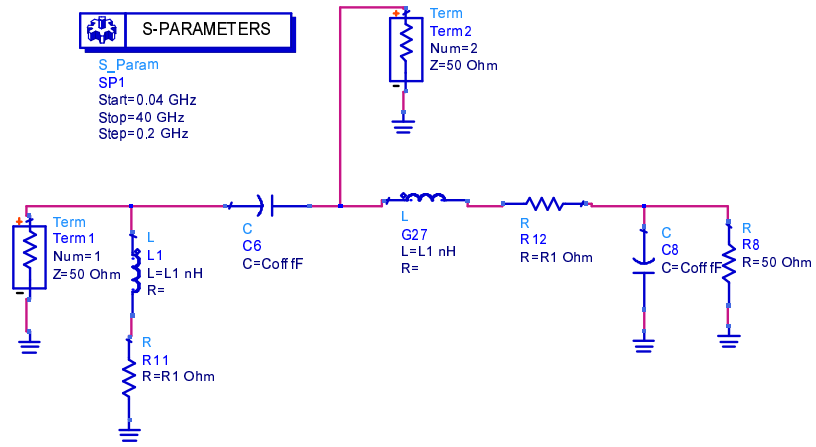
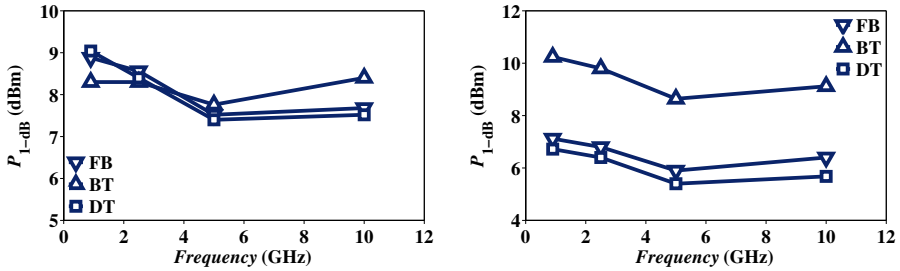


Fig. 7.25.: ADS schematic used to simulate the effect of metal lines using R_{ON} to represent the transistors in ON state and C_{OFF} to represent the transistors in OFF state.

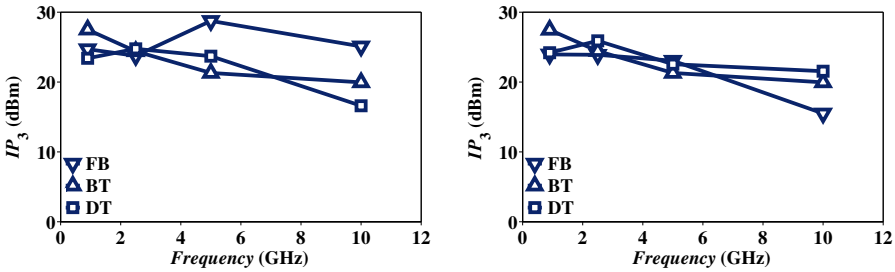


(a) 30 fingers.

(b) 90 fingers.

Fig. 7.26.: The 1-dB compression point, $P_{\text{1-dB}}$, obtained through single-tone measurements, for RF antenna switches using PD SOI devices in FB, BT, and DT structures and two gate compositions; 30 and 90 fingers.

level at the power source is fixed at −7 dBm. For the switches built using transistors of 30-fingers gate, the results are shown in Fig. 7.27a. At 900 MHz, the BT switch shows the highest IP_3 indicating its immunity to intermodulation up till 27.5 dBm. The FB switch comes next with 24.7 dBm then the DT switch with 23.4 dBm. As frequency increases, the IP_3 of the BT switch falls while those of FB and DT switches show a relatively stable behavior. A quite similar behavior is noticed for switches built using 90-fingers transistors as shown in Fig. 7.27b. The values for the three switches are closer than the 30-fingers case, yet the switch using the DT transistor shows a relatively more stable behavior with frequency as compared to the other two switches.



(a) 30 fingers. (b) 90 fingers.

Fig. 7.27.: The third intercept point, IP_3, obtained through two-tone measurements, for RF antenna switches using PD SOI devices in FB, BT, and DT structures and two gate compositions; 30 and 90 fingers.

7.10 CONCLUSION

The design of the RF antenna switch is based on a series of optimization decisions. The designer is limited by the optimization between the three figures of merit of the operation of the switch, i.e. insertion loss, isolation, and power handling (linearity). Practically, the designer should target a certain application with certain requirements and targets to meet. As presented earlier, optimizing the insertion loss could highly affect the isolation and vice versa. The power handling capabilities of the switch, or its linearity, is also an important parameter. The choice of the transistor structure could also help to reach a better optimization between the three figures of merit. It was shown that a special structure of bulk devices, the deep n-well protected transistor, could result in a performance comparable and even better than switches built using comparable SOI technologies. In the same technology the choice of the structure and geometry of the transistor could highly affect its performance.

It was also shown that a simple model of the RF antenna switch, only composed of C_{OFF} and R_{ON} of the transistor is a useful tool to predict the performance of the designed switch. The usual on-wafer measurements could easily underestimate the performance of the switch due to the connecting metal lines which are not simple to completely de-embed in a three terminal circuit like the RF antenna switch. More complicated models, using compact models of the transistors or black-boxes of measured transistors do not add to the accuracy of the simulation of the RF antenna switch. Mostly, compact models are not optimized for the ON/OFF operation of the transistors especially in the RF frequency range. An optimized large-signal (nonlinear) transistor model could be useful if correctly implemented.

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CHAPTER 8

CONCLUSIONS

In this thesis, an elaborated comparison study of three technologies and several device structures including novel structures like the GCMOS and the deep n-well protected bulk devices (see Table 8.1 for a summary of the devices studied in this thesis). As stated in the introduction, the target is not to draw a final conclusion about the best device or a device that outperforms all the other devices. The main objective is to fill the gap between the devices domain and the circuit design domain. A RF circuit designer could find sufficient information through the comparisons presented in this thesis to allow for an optimized circuit design that meets the goals and the requirements of a certain application. The correct choice of the device structure and the technology could be critical for an optimum performance of the RF circuit.

8.1 GENERAL REMARKS

The different characterization schemes presented in this thesis resulted in some important remarks:

– The advantages of SOI over conventional bulk technologies are certain and confirmed through so many publications [1–3]. These advantages are even more important for RF performance based on the reduced capacitances

and substrate coupling [4]. However, taking into account the larger market share owned by bulk technology, it is not unlikely that the SOI would not acquire more market share. In this thesis, the deep n-well protected bulk device has been characterized and compared to the corresponding SOI structures. The comparable performance, and sometimes the better performance of the deep n-well protected bulk device highlights the probability that bulk devices could even regain more market share. Thus the passage SOI to bulk to SOI could still be possible [5]. The area constraint would still be a problem for the deep n-well protected bulk devices, but for simple (yet important) circuits like the RF antenna switch, the area is not a limiting requirement.

– The correct choice of the small-signal equivalent circuit is usually of crucial importance for the correct characterization of a certain device. However, in this these, one standard small-signal equivalent circuit (Fig. 3.40) was used throughout without the need for specific modifications for each transistor technology or structure. The only exception is the DTMOS transistor whose extraction has not been guaranteed using this standard equivalent circuit due the complicated physics associated. A specific equivalent circuit should have been used (Fig. 2.10) which has been out of the scope of this work; i.e. validating different small-signal equivalent circuits. As a consequence, some extractions have not been possible for DTMOS resulting in some vacancies in the tables throughout the thesis. The most critical drawback of these vacancies is the inability to show the advantage of DTMOS in LVLP operation through chapter 4.

– Dynamic Threshold MOSFET (DTMOS) was shown to deliver compatible behavior to FB and BT SOI devices for RF applications. Insertion loss, isolation, and even power handling capabilities of RF antenna switches built using DTMOS show interesting characteristics compared to other switches. The operation of DTMOS in common gate configuration can overcome the limitations of the DTMOS in RF regime of operation.

– The high temperature conditions of operation was shown to be beneficial for low voltage low power applications if the correct biasing scheme is chosen. Contrary to what is well known about device characteristics degradation at high temperatures, it was shown that operating the device at certain points could result in enhancing the dc and RF characteristics of the device as temperature increases. This result could be very important for new applications that require a significant reduction of power consumption while suffering at the same time from increasing temperature conditions due to increased number of transistors per chip or harsh environmental conditions.

– Scaling down the dimensions of the transistors is not always the solution to enhance its performance. Although this trend is fueled by the largest market, which is the digital market, scaling should in all cases slow down since

the physical limits of the silicon are being approached. Research groups are examining several alternatives. In this thesis, the lateral asymmetric channel (or the Graded Channel MOS, GCMOS) is presented as a potential solution. It has been shown that this simple alternative, which is also compatible with mainstream CMOS technology fabrication process, can provide an enhancement in the different aspects of operation including, dc, analog, RF, nonlinear, low frequency noise, and, in this thesis, high temperature operation and high frequency noise.

– Experimental high frequency noise characterization, along with analytical study and noise model parameter extraction, confirmed the lower minimum noise figure of GCMOS over the whole range of operation as compared to the corresponding classical (symmetric channel) MOSFET devices. Not only the minimum noise figure, but also a better noise matching of the device as made evident through a better optimum input reflection coefficient. These advantages where shown to be true for academic scale as well as for industrial commercial technologies. It was also shown to be valid for partially-depleted devices as for fully-depleted devices of nano-scale channel lengths.

– The enhanced RF noise behavior of the GCMOS motivated the verification of the existing noise models. It has been shown that for lateral asymmetric channel devices, as is the case of GCMOS, a 3-parameter model is required to correctly describe the RF noise behavior of the device. The assumption used for the 2-parameter model is clearly violated by the high correlation coefficient which characterizes the lateral asymmetric channel devices. In this thesis, the experimental evidence for this verification has been provided.

– Optimization is always a keyword in the RF circuit design. A trade-off should always be found between the different figures of merit that characterize the performance of the RF circuit. In the case of the RF antenna switch, the three figures of merit: insertion loss, isolation, and power handling, are difficult to be maximized all at the same time. However, the choice of the best device for the targeted application could help achieve a better optimization. Some novel structures could also be beneficial for a successful design of a RF antenna switch. DNW bulk devices were shown to be able to deliver significant optimization between the different figures of merit. DTMOS is another important solution, yet not frequently employed, that could give an optimized performance.

The remarks listed above are the result of an extended characterization of the devices considered in this thesis. A complete cycle of characterization including dc, ac, RF, nonlinear, high temperature, low voltage low power, high frequency noise, and finally circuit level characterization including design, simulation, fabrication, and measurements. The results of these characterization steps

are summarized in Table 8.2 for dc analysis, in Table 8.3 for ac analysis, and in Table 8.4 and Table 8.5 for RF characterization. Table 8.6 shows the low voltage low power LVLP characteristics of the compared devices. Figures of merit are compared at room temperature and then their variation with temperature (per degree Celsius) are also compared. These figures of merit and their variation with temperature are to serve as relative indications not as absolute values. In other words, these are not state-of-the art values of the shown figures of merit but they are to be regarded in the context of comparing different device structures and technologies.

On the other hand, a RF circuit design does not only depend on the choice of the transistor, also known as the active part of the circuit. A crucial aspect of the design is the passive part which includes capacitors, inductors, and resistors. Nevertheless, this thesis does not provide information regarding the passive part, yet this issue is fairly covered in literature [4, 6–9]. Mostly, the published work in the passive domain put the SOI technology ahead for its advantages compared to the bulk technology. On top of these advantages, for RF applications, comes the capability of the SOI technology to suppress crosstalk due to the presence of the buried oxide [4]. In a world in which the trend is to put all the system on one chip, the isolation between the digital circuitry and the analog and RF circuitry is crucial. Apparently, the SOI technology takes the lead in this domain.

8.2 APPLICABILITY

Is it necessary to follow such an extensive characterization cycle for an optimized use of MOSFETs in RF circuits?

The answer comes intuitively from the standard specifications of basic RF circuits. These specifications can be found in any data sheet or website of a commercial product. Taking the low noise amplifier (LNA) as an example, the standard specifications are listed below along with the type of characterization needed to each specification:

- Operating DC Voltage (dc)
- Current Consumption (dc)
- Gain (ac)
- Gain Flatness (ac)
- Frequency Range (RF)
- Input/Output Return Loss (RF)
- Noise Figure (noise)
- 1-dB Compression Point (nonlinearity)
- Operating Temperature (temperature)

Hence, it is clear that, to cover all the aspects of the design of the LNA, an extensive characterization approach, such as the one presented in this thesis, is highly needed. The same applies for other RF circuits like the voltage controlled oscillator (VCO), the power amplifier (PA), the RF antenna switch (as presented in chapter 7), etc.

If a hypothetical example of the design of a LNA is considered, the characterization approach presented in this thesis would take the form presented in the next section.

8.3 THE DESIGN OF A LOW NOISE AMPLIFIER

Based on the proposed characterization approach, the RF circuit designer is basically faced by four phases of design/choice:

- The wafer used in the fabrication of the circuit: bulk or SOI.
- The technology applied: partially-depleted, fully-depleted, or DNW protected (bulk).
- The structure of the transistor: floating-body, body-tied, or dynamic-threshold.
- The channel engineering employed: classical (uniformly doped) or graded channel.

Combining the specifications of the LNA and the above list of choices, a proposed design scheme would be:

- SOI wafer to overcome parasitics in bulk especially for better performance of crosstalk.
- A partially-depleted technology which is more stable and cheaper than fully-depleted technology. Based on Table 8.2 and Table 8.3 PD also shows better stability with temperature especially for subthreshold slope, I_{ON}-to-I_{OFF} ratio (including higher values at room temperature), and leakage current (although FD shows lower leakage at room temperature). In addition, PD features a better location of ZTC points with respect to V_T which promotes it for a better LVLP operation.
- Considering the two structures of the PD SOI devices presented in the different tables at the end of this chapter, a choice of FB structure is evident especially for the better stability with temperature.
- The graded channel MOSFET (GCMOS) is a natural choice for a LNA circuit since it outperforms the classical nMOS in nearly all aspects of operation and for the operation of the LNA it is crucial for the following reasons (comparing two structures of the same drawn channel length):
  - Higher drive current
  - Higher transconductance
  - Higher g_m/I_{DS} ratio
  - Higher Early voltage V_{EA}
  - Higher intrinsic gain A_{v0}
  - Higher cutoff frequencies f_T and $f_{\max}$
  - Maximum of g_m, f_T, and $f_{\max}$ occurring at lower V_{GS} which promotes LVLP operation
  - Kink effect occurring at higher values of V_{DS}
  - Better linearity (IP_3 and $P_{\text{1-dB}}$)

– Lower minimum noise figure $NF_{\min}$ and closer optimum reflection coefficient Γ_{opt} from the 50 Ω cycle on the smith chart (for better matching)

Therefore, based on the characterization approach proposed in this thesis, the decision of a RF circuit designer for a LNA circuit could be a SOI wafer using partially-depleted technology and a floating-body structure with a graded channel engineering.

8.4 CONCLUSION

In this thesis, an extensive characterization approach is introduced to cover the gap between the devices domain and the circuits domain. The characterization flow starts by a complete dc characterization which constitutes the basis for the all the next characterization steps. The figures of merit for the different aspects of dc operation serve later as the building blocks for the figures of merit for the other regimes of operation. The next step is to characterize the device for ac operation. The following step is the RF characterization which covers the cutoff frequencies extraction (current gain cutoff frequency and maximum oscillation frequency) and the extraction of the elements of the small-signal equivalent circuit (extrinsic and intrinsic elements). The extraction of these elements in the OFF state then in the ON state of the transistor helps to acquire a deep understanding of the RF behavior. In addition, these elements form a main part in the figures of merit of the high frequency noise behavior of the transistor. The correct understanding of the small-signal equivalent circuit also provides the grounds for an ameliorated low voltage low power operation, which is the next step in the characterization flow. A new approach for an enhanced design near and below threshold voltage is introduced through the low voltage low power characterization step. The optimized operation of the transistor has a lower limit and an upper limit. The upper limit, the nonlinearities of the transistor, forms the next step in the proposed characterization approach. The nonlinear characterization is crucial for some key RF circuits like the RF antenna switch. The lower limit for the transistor operation is the noise. The high frequency noise behavior is the next characterization step. The high frequency noise is a wide and deep research area that requires experimental, analytical, and modeling aspects of analysis. The accurate noise characterization assists in a successful design of main RF circuits like the low noise amplifier.

In order for this characterization flow to be efficient, it is completely based on accurate on-wafer measurements for a wide range of MOSFET transistors (different wafers, technologies, structures, and channel engineering schemes). The measurements and the characterization flow also cover a wide range of temperature (25^{o}C to 250^{o}C) and a wide range of frequency (dc to 40 GHz). The measured characteristics are then used to extract the different figures of merit (for the different characterization steps) and the elements of the small-signal equivalent circuit (for high frequency operation). For generality, a standard and simple

equivalent circuit is used for all the devices presented in this thesis. The results show the successful application of this equivalent circuit with the exception of one structure (DTMOS) which needs a more complicated equivalent circuit to account for its specific physical structure.

The extensive characterization flow is then evaluated through a detailed study of a key RF circuit; the RF antenna switch. Another evaluation is established by considering a hypothetical design example of a low noise amplifier in the sense of summarizing the concept of this characterization approach.

A similar characterization approach, not included in this thesis, could also be proposed for the passive part of the RF circuit; resistors, inductors, and capacitors.

The proposed characterization approach is, therefore, able to provide the RF circuit designer with the required information for the best choice of the transistors to be used in a specific circuit for a specific application.

Table 8.1.: A summary of the devices considered in this work.

(a) Group 1

	DNW Bulk			PD SOI 1			FD SOI 1	
	FB	BT	DT	FB	BT	DT	FB	BT
	Foundry X						Foundry Y	
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
t_{Si}(nm)	—	—	—	150	150	150	40	40
t_{ox}(nm)	2	2	2	2	2	2	2.5	2.5
t_{box}(nm)	—	—	—	400	400	400	145	145

(b) Group 2

	FD SOI 2				PD SOI 2		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
	Foundry Y, different run				Foundry Z		
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
t_{Si}(nm)	40	40	40	40	100	100	100
t_{ox}(nm)	2.5	2.5	2.5	2.5	4.5	4.5	4.5
t_{box}(nm)	145	145	145	145	400	400	400

Table 8.2.: A summary of the dc characteristics of the devices considered in this work.

(a) Group 1

	DNW Bulk			PD SOI 1			FD SOI 1	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
V_T (V)	0.24	0.28	0.26	0.35	0.36	0.34	0.46	0.47
ΔV_T (mV/^{o}C)	-0.4	-0.63	-0.54	-0.63	-0.68	-0.54	-0.55	-0.53
$g_{m,\text{max}}$ (mS/mm)	780.8	777.1	—	627.3	700.2	—	390	405.1
$\Delta g_{m,\text{max}}$	-1.05	-1.03	—	-0.68	-0.79	—	-0.54	-0.57
S (mV/dec)	77.6	81.2	75	75.3	82	74.3	71.5	75.1
ΔS(%/^{o}C)	0.33	0.33	0.26	0.32	0.31	0.23	0.55	0.28
I_{Leakage} (mA/mm) ($\times 10^{-6}$)	8.6	7.1	6.4	11	2.6	8.1	3.4	2.6
$\Delta\ I_{\text{Leakage}}$ ($\times 10^{-3}$)	8.5	9.5	5.4	10.9	7.2	5.3	15.7	2.7
ZTC_{IDS} (V) (Lin.)	0.43	0.43	0.4	0.55	0.55	0.52	0.63	0.64
ZTC_{gm} (V) (Lin.)	0.27	0.27	0.28	0.4	0.41	0.3	0.48	0.49
$ZTC_{IDS} - ZTC_{gm}$ (Lin.)	0.16	0.16	0.12	0.15	0.14	0.22	0.15	0.15
$ZTC_{IDS} - V_T$ (Lin.)	0.19	0.15	0.14	0.2	0.19	0.18	0.17	0.17
$ZTC_{gm} - V_T$ (Lin.)	0.03	-0.01	0.02	0.05	0.05	-0.04	0.02	0.02
ZTC_{IDS} (V) (Sat.)	0.32	0.51	0.51	0.45	0.63	0.52	0.56	0.6
ZTC_{gm} (V) (Sat.)	0.19	0.3	0.3	0.27	0.42	0.35	0.36	0.39
$ZTC_{IDS} - ZTC_{gm}$ (Sat.)	0.13	0.21	0.21	0.18	0.21	0.17	0.2	0.21
$ZTC_{IDS} - V_T$ (Sat.)	0.1	0.21	0.25	0.16	0.23	0.16	0.21	0.24
$ZTC_{gm} - V_T$ (Sat.)	-0.03	0	0.04	-0.02	0.02	-0.01	0.01	0.03

Table 8.2.: A summary of the dc characteristics of the devices considered in this work.

(b) Group 2

	FD SOI 2				PD SOI 2		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
V_T (V)	0.65	0.64	0.7	0.74	0.55	0.46	0.51
ΔV_T (mV/^{o}C)	−0.58	−0.63	−0.64	−0.7	−0.93	−0.85	−0.87
$g_{m,\max}$ (mS/mm)	453.8	421.3	394.2	362.9	217	261.6	205.8
$\Delta g_{m,\max}$	−0.57	−0.47	−0.54	−0.56	−0.33	−0.44	−0.37
S (mV/dec)	58.5	55	54.8	67.9	76.58	109	88.11
ΔS(%/^{o}C)	0.33	0.35	0.42	0.42	0.36	0.34	0.33
I_{Leakage} (mA/mm) ($\times 10^{-6}$)	4.95	0.18	0.13	0.19	—	—	—
$\Delta\ I_{\text{Leakage}}$ ($\times 10^{-3}$)	10.3	13.4	12.3	10.5	—	—	—
ZTC_{IDS} (V) (Lin.)	0.83	0.8	0.89	0.93	0.7	0.56	0.61
ZTC_{gm} (V) (Lin.)	0.66	0.65	0.71	0.73	0.495	0.43	0.44
$ZTC_{IDS} - ZTC_{gm}$ (Lin.)	0.17	0.18	0.18	0.2	0.205	0.13	0.17
$ZTC_{IDS} - V_T$ (Lin.)	0.18	0.19	0.18	0.19	0.15	0.1	0.1
$ZTC_{gm} - V_T$ (Lin.)	0.01	0.01	0.01	−0.01	−0.055	−0.03	−0.07
ZTC_{IDS} (V) (Sat.)	0.59	0.56	0.58	0.77	0.42	0.55	0.79
ZTC_{gm} (V) (Sat.)	0.44	0.46	0.56	0.68	0.33	0.42	0.59
$ZTC_{IDS} - ZTC_{gm}$ (Sat.)	0.15	0.1	0.02	0.09	0.09	0.13	0.2
$ZTC_{IDS} - V_T$ (Sat.)	0.12	0.01	−0.11	−0.08	−0.06	0.02	0.16
$ZTC_{gm} - V_T$ (Sat.)	−0.03	−0.09	−0.13	−0.17	−0.15	−0.11	−0.04

Table 8.3.: A summary of the analog characteristics of the devices considered in this work.

(a) Group 1

	DNW Bulk			PD SOI 1			FD SOI 1	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
I_{ON}-to-I_{OFF} ($\times 10^6$)	0.0013	0.0071	0.08	0.0075	0.081	95	0.15	0.7
I_{OFF} (mA/mm) ($\times 10^{-6}$)	250000	39000	45000	33000	2400	3100	2800	610
Δ I_{ON}-to-I_{OFF} ($\times 10^{-3}$)	-5.6	-8.5	-8	-7.7	-10.8	-9.8	-13.3	-12.5
Δ I_{OFF} ($\times 10^{-3}$)	5	8.1	7.8	7.3	10.7	10.2	12.8	12.1
V_{EA} @ 25^{o}C (V)	5.1	7.72	—	8.55	24.2	—	10.56	8.44
ΔV_{EA} (mV/^{o}C)	-4.3	-4.8	—	-21.1	-64.2	—	-17.6	-10.7

(b) Group 2

	FD SOI 2				PD SOI 2		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
I_{ON}-to-I_{OFF} ($\times 10^6$)	48	720	2500	1900	3.6	0.292	5.56
I_{OFF} (mA/mm) ($\times 10^{-6}$)	11	0.62	0.15	0.23	58.8	910	28
Δ I_{ON}-to-I_{OFF} ($\times 10^{-3}$)	-18.2	-19.9	-19.9	-18.3	-11.9	-8.82	-12.3
Δ I_{OFF} ($\times 10^{-3}$)	17.6	19.3	18.9	16.2	10.77	7.87	11.78
V_{EA} @ 25^{o}C (V)	4.45	7.78	8.92	14.8	6.5	11.34	17.34
ΔV_{EA} (mV/^{o}C)	-7.7	12.9	54.7	76	7.1	-7.9	-29.6

Table 8.4.: A summary of the RF characteristics: cutoff frequencies and extrinsic resistances.

(a) Group 1

	DNW Bulk			PD SOI 1			FD SOI 1	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
f_T @ 25^{o}C (GHz)	70.8	70.1	24.9	71.8	55.1	62.2	83.4	73.8
$f_{\max}$ @ 25^{o}C (GHz)	211.2	140.3	77.8	200.2	98.6	103.8	114.8	86
$f_{\max}/f_T$ @ 25^{o}C	2.98	2	3.12	2.79	1.79	1.67	1.37	1.17
Δf_T (GHz/^{o}C)	-0.12	-0.11	-0.08	-0.092	-0.062	-0.09	-0.16	-0.08
$\Delta f_{\max}$ (GHz/^{o}C)	-0.56	-0.36	0.7	-0.42	-0.22	0.003	-0.02	-0.19
R_{g} @ 25^{o}C (Ω)	5	4.7	—	5.72	6.96	—	5.99	8.61
R_{d} @ 25^{o}C (Ω)	2.5	2.6	—	2.3	2.35	—	1.76	1.78
R_{s} @ 25^{o}C (Ω)	1.72	1.85	—	1.3	1.63	—	1.3	1.29
ΔR_{g} (Ω/^{o}C) ($\times 10^{-3}$)	7	6	—	1.1	20	—	5	20
ΔR_{d} (Ω/^{o}C) ($\times 10^{-3}$)	5	3	—	5	4	—	0.7	0.04
ΔR_{s} (Ω/^{o}C) ($\times 10^{-3}$)	4	4	—	3	3	—	4	3

Table 8.4.: A summary of the RF characteristics: cutoff frequencies and extrinsic resistances.

(b) Group 2

	FD SOI 2				PD SOI 2		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
f_T @ 25^{o}C (GHz)	49.4	23.4	16.2	13.4	16.8	20.3	17.3
$f_{\max}$ @ 25^{o}C (GHz)	108.7	57.3	38.2	27.4	50.2	65.8	50.6
$f_{\max}/f_T$ @ 25^{o}C	2.2	2.45	2.36	2.04	2.99	3.2	2.92
Δf_T (GHz/^{o}C)	-0.069	-0.018	-0.012	-0.02	-0.035	-0.042	-0.037
$\Delta f_{\max}$ (GHz/^{o}C)	-0.21	-0.096	-0.07	-0.06	-0.11	-0.14	-0.02
R_{g} @ 25^{o}C (Ω)	10.9	5.31	4.23	3.56	5.9	5.03	4.65
R_{d} @ 25^{o}C (Ω)	3.41	4.11	4.29	3.73	6.1	9.2	10.03
R_{s} @ 25^{o}C (Ω)	1.63	1.87	1.17	0.43	6.65	6.6	12.3
ΔR_{g} (Ω/^{o}C) ($\times 10^{-3}$)	-0.3	0.3	0.2	-10	-10	-12	-18
ΔR_{d} (Ω/^{o}C) ($\times 10^{-3}$)	12	11	15	16	30	35	45
ΔR_{s} (Ω/^{o}C) ($\times 10^{-3}$)	7.7	7.4	12	11	28	24	52

Table 8.5.: A summary of the RF characteristics: intrinsic elements.

(a) Group 1

	DNW Bulk			PD SOI 1			FD SOI 1	
	FB	BT	DT	FB	BT	DT	FB	BT
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.15	0.15
W (μm)	2	2	2	2	2	2	5	5
N_{finger}	30	30	30	30	30	30	48	48
OFF state								
C_{gs} @ 25^{o}C (fF/mm)	649.7	653.3	—	618.9	952.3	—	319.4	408.3
C_{gd} @ 25^{o}C (fF/mm)	543.6	529.2	—	557	510.3	—	329.6	349.4
C_{ds} @ 25^{o}C (fF/mm)	447	497.9	—	339.5	677.9	—	146	158.5
ΔC_{gs} (fF/mm/^{o}C)	0.96	1.04	—	0.28	0.5	—	−0.09	0.03
ΔC_{gd} (fF/mm/^{o}C)	0.03	0.045	—	0.11	0.036	—	0.054	0.08
ΔC_{ds} (fF/mm/^{o}C)	0.45	0.35	—	0.21	0.37	—	0.008	−0.036
ON state								
C_{gs} @ 25^{o}C (fF/mm)	1107	1096	—	1032	1742	—	958.9	—
C_{gd} @ 25^{o}C (fF/mm)	610.9	598.9	—	597.8	644.4	—	374.4	358.6
C_{ds} @ 25^{o}C (fF/mm)	310.2	419.2	—	870.6	2232	—	532.5	880.9
G_{mi} @ 25^{o}C (mS/mm)	852.3	855.9	—	703.7	776.8	—	452.1	500.8
G_{dsi} @ 25^{o}C (mS/mm)	176.8	167	—	174	139.6	—	94.36	89.2
ΔC_{gs} (fF/mm/^{o}C)	−0.015	−0.04	—	0.07	−0.12	—	−5.9	—
ΔC_{gd} (fF/mm/^{o}C)	0.05	0.066	—	0.055	0.14	—	0.24	0.11
ΔC_{ds} (fF/mm/^{o}C)	0.24	0.02	—	−0.65	1.95	—	−1.67	−3
ΔG_{mi} (mS/mm/^{o}C)	−0.89	−0.93	—	−0.57	−0.7	—	−0.65	−1
ΔG_{dsi} (mS/mm/^{o}C)	−0.07	−0.057	—	−0.07	−0.005	—	−0.02	−0.04

Table 8.5.: A summary of the RF characteristics: intrinsic elements.

(b) Group 2

	FD SOI 2				PD SOI 2		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
L (μm)	0.15	0.24	0.35	0.5	0.5	0.5	0.5
W (μm)	2.5	2.5	2.5	2.5	3.3	3.3	3.3
N_{finger}	32	48	48	48	12	12	12
OFF state							
C_{gs} @ 25^{o}C (fF/mm)	584.8	556.4	566.1	647.8	598.2	598.2	813.9
C_{gd} @ 25^{o}C (fF/mm)	568.6	470.2	481	510.9	468.7	481.4	472.1
C_{ds} @ 25^{o}C (fF/mm)	150.9	105.6	84.26	86.34	258.1	262.4	268.1
ΔC_{gs} (fF/mm/^{o}C)	0.1	0.11	0.16	0.23	0.81	0.85	0.93
ΔC_{gd} (fF/mm/^{o}C)	0.09	0.064	0.073	0.07	0.2	0.17	0.18
ΔC_{ds} (fF/mm/^{o}C)	−0.08	−0.07	−0.07	−0.09	0.56	0.57	0.36
ON state							
C_{gs} @ 25^{o}C (fF/mm)	1313	1658	2124	3047	2248	2023	1748
C_{gd} @ 25^{o}C (fF/mm)	507.6	924.5	1295	1655	514.7	800.5	871.2
C_{ds} @ 25^{o}C (fF/mm)	245.8	679.3	826.2	285.8	318.1	457.7	350.2
G_{mi} @ 25^{o}C (mS/mm)	537	449.9	391.3	412.4	280.6	315.4	253.1
G_{dsi} @ 25^{o}C (mS/mm)	80.92	47.09	25.42	12.99	20.65	20.61	9.807
ΔC_{gs} (fF/mm/^{o}C)	−0.16	−0.64	−0.47	0.023	0.26	1.1	0.7
ΔC_{gd} (fF/mm/^{o}C)	0.072	0.25	0.38	0.62	0.18	0.42	0.4
ΔC_{ds} (fF/mm/^{o}C)	−0.74	−1.73	−2.08	−0.369	0.51	1.37	0.8
ΔG_{mi} (mS/mm/^{o}C)	−0.43	−0.34	−0.31	−0.55	−0.53	−0.56	−0.43
ΔG_{dsi} (mS/mm/^{o}C)	−0.025	0.04	0.037	0.026	−0.02	0.029	0.033

Table 8.6.: A summary of the LVLP characteristics of the devices considered in this work.

(a) Group 1

	DNW Bulk			PD SOI 1			FD SOI 1	
	FB	BT	DT	FB	BT	DT	FB	BT
V_{DS} = 0.6 V and V_{GS} = ZTC_{IDS}								
$g_{m,max}$ (mS/mm)	720.8	712.8	—	691.7	631.6	—	350	350
V_{GS} @ $g_{m,max}$ (V)	0.76	0.79	—	0.83	0.85	—	1	1
ZTC_{IDS} (V)	0.46	0.52	0.51	0.58	0.64	0.52	0.65	0.66
$ZTC_{IDS} - V_T$	0.24	0.22	0.25	0.29	0.24	0.16	0.3	0.3
Δf_T @ ZTC_{IDS} (GHz/^{o}C)	−0.066	−0.09	—	−0.082	−0.073	—	−0.075	−0.04
P_{dc} @ ZTC_{IDS} @ 25^{o}C (mW/mm)	52.79	65.76	—	57.14	73.98	—	28.7	28.5
P_{dc} @ ZTC_{IDS} @ 200^{o}C (mW/mm)	52.79	65.76	—	57.14	73.98	—	28.7	28.5
Δf_T @ $g_{m,max}$ (GHz/^{o}C)	−0.12	−0.11	—	−0.092	−0.08	—	−0.11	−0.12
P_{dc} @ $g_{m,max}$ @ 25^{o}C (mW/mm)	174.4	175.4	—	148.9	157.3	—	102.1	98.2
P_{dc} @ $g_{m,max}$ @ 200^{o}C (mW/mm)	138.1	144.8	—	125	136.8	—	81.4	79
V_{DS} = 0.6 V and V_{GS} < ZTC_{gm}								
ZTC_{gm} (V)	0.29	0.33	0.33	0.39	0.44	0.44	0.42	0.43
$ZTC_{gm} - V_T$	0.07	0.03	0.07	0.10	0.04	0.08	0.07	0.07
ZTC_{ft} (V)	0.28	0.33	0.3	0.4	0.42	0.46	0.46	0.485
V_{GS} (V)	0.2	0.2	0.2	0.3	0.3	0.3	0.3	0.3
f_T @ 25^{o}C (GHz)	9.2	7.07	3.73	10.54	6.58	9.53	10.91	11.6
f_{max} @ 25^{o}C (GHz)	35	24.66	10.75	37.33	22.24	20.25	17.1	12.48
P_{dc} @ 25^{o}C (mW/mm)	11.81	1.71	2.83	2.367	1.567	3.97	0.862	0.668
Δf_T (GHz/^{o}C)	0.041	0.05	0.034	0.029	0.032	0.038	0.027	0.017
Δf_{max} (GHz/^{o}C)	0.044	0.09	0.05	0.055	0.039	0.11	0.013	0.024
ΔP_{dc} (mW/mm/^{o}C)	0.045	0.035	0.045	0.034	0.038	0.063	0.008	0.0073

Table 8.6.: A summary of the LVLP characteristics of the devices considered in this work.

(b) Group 2

	FD SOI 2				PD SOI 2		
	nMOS	GC	GC	GC	nMOS	FB GC	BT GC
V_{DS} = 0.6 V and V_{GS} = ZTC_{IDS}							
$g_{m,max}$ (mS/mm)	429.4	379.2	327.4	300.5	181.6	219.3	202.1
V_{GS} @ $g_{m,max}$ (V)	—	—	—	—	1.4	1.1	1.1
ZTC_{IDS} (V)	—	—	—	—	0.72	0.69	0.79
$ZTC_{IDS} - V_T$	—	—	—	—	0.24	0.16	0.16
Δf_T @ ZTC_{IDS} (GHz/^{o}C)	—	—	—	—	−0.011	−0.031	−0.02
P_{dc} @ ZTC_{IDS} @ 25^{o}C (mW/mm)	—	—	—	—	8.86	15.1	13.96
P_{dc} @ ZTC_{IDS} @ 200^{o}C (mW/mm)	—	—	—	—	8.86	15.1	13.96
Δf_T @ $g_{m,max}$ (GHz/^{o}C)	—	—	—	—	−0.03	−0.038	−0.03
P_{dc} @ $g_{m,max}$ @ 25^{o}C (mW/mm)	—	—	—	—	77.1	66.4	43.6
P_{dc} @ $g_{m,max}$ @ 200^{o}C (mW/mm)	—	—	—	—	50.2	45.9	31.7
V_{DS} = 0.6 V and V_{GS} < ZTC_{gm}							
ZTC_{gm} (V)	—	—	—	—	0.5	0.43	0.51
$ZTC_{gm} - V_T$	—	—	—	—	0.02	−0.1	−0.12
ZTC_{ft} (V)	—	—	—	—	0.56	0.47	0.56
V_{GS} (V)	—	—	—	—	—	0.2	0.3
f_T @ 25^{o}C (GHz)	—	—	—	—	—	0.24	0.03
f_{max} @ 25^{o}C (GHz)	—	—	—	—	—	19.94	—
P_{dc} @ 25^{o}C (mW/mm)	—	—	—	—	—	0.019	0.007
Δf_T (GHz/^{o}C)	—	—	—	—	—	0.006	0.006
Δf_{max} (GHz/^{o}C)	—	—	—	—	—	0.2	—
ΔP_{dc} (mW/mm/^{o}C)	—	—	—	—	—	0.001	0.002

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APPENDIX A

DE-EMBEDDING: S-PARAMETERS

In on-wafer measurements, an accurate de-embedding step is crucial. As shown in section 3.1.1 and section 3.1.2, the reference plane of measurement is set at the pads structure after the calibration step and the de-embedding step is needed to move it to the edges of the transistor or the device-under-test (DUT) as shown in Fig. A.1.

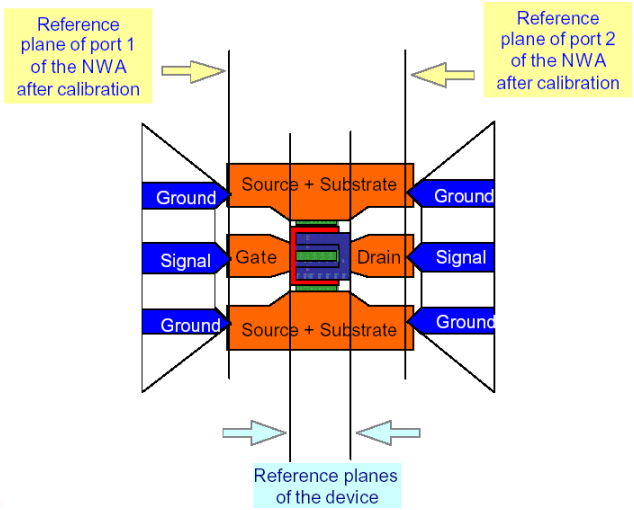

Fig. A.1.: Reference planes after a successful calibration and de-embedding procedures (Source: Agilent Technologies [1]).

Literature is rich in research work that deal with the de-embedding subject for on-wafer measurements [2–14]. In this thesis, a simple open-short de-embedding is employed. The results are quite satisfactory, therefore there is no need for a more complicated procedure.

The same test structure used for the on-wafer measurements of the DUT is repeated twice, once with the transistor removed whereas the rest of the test structure remains the same (open structure) and once with the transistor removed whereas the pads are shorted together (short structure), as shown in Fig. A.2. The S-parameters of these test structures are then measured at every frequency point and each temperature point used in the measurement of the DUT. The simple procedure shown in Fig. A.2 is then applied in order to remove the parallel parasitic impedance and the series parasitic admittance shown in Fig. A.3.

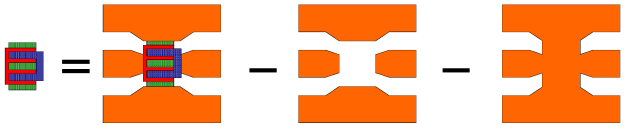

Fig. A.2.: A schematic illustration of the de-embedding procedure.

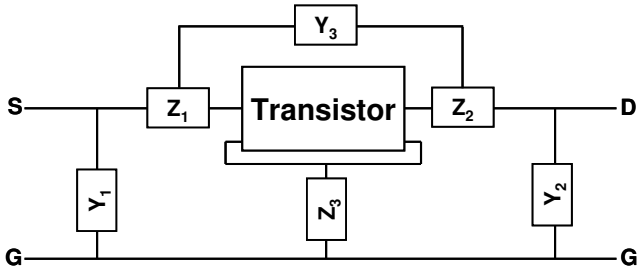

Fig. A.3.: A schematic illustration of the parallel parasitic impedances and the series parasitic admittances associated with the pad structure.

The de-embedding procedure illustrated in Fig. A.2 is summarized in the following simple steps:

- The total (measured) S-parameters, S_{Total}, are transfered into a Y-parameters representation Y_{Total}[1].
- The measured Y-parameters of the open structure is then subtracted from Y_{Total}.

$$Y_{\text{DUT-Open}} = Y_{\text{Total}} - Y_{\text{Open}} \tag{A.1}$$

- The resulting Y-parameters ($Y_{\text{DUT-Open}}$) are then converted into Z-parameters ($Z_{\text{DUT-Open}}$).
- The de-embedded Z-parameters of the DUT are then obtained by subtracting the measured Z-parameters of the short structure from $Z_{\text{DUT-Open}}$:

$$Z_{\text{DUT}} = Z_{\text{DUT-Open}} - Z_{\text{Short}} \tag{A.2}$$

[1]For all the transformations between different electrical representation (i.e. S, Y, Z, or A) see Appendix C.

– The de-embedded Z-parameters can be easily converted to any other representation (S, Y, etc).

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APPENDIX B

DE-EMBEDDING: NOISE

The measurement of the high frequency noise using the Tuner method deliver four parameters: $NF_{\min}$, R_n, and $Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}}$ (see section 6.4.2 for details). In the case of on-wafer measurements, the pad-parasitics network highly affects the noise parameters measured using the Tuner method. The calibration of the Tuner (presented in Appendix G) along with the calibration of the vector network analyzer (VNA) and the de-embedding of the measured S-parameters (see Appendix A) are not enough to remove this pad-parasitics network from the four noise parameters. The procedure described in this Appendix is used in this work to achieve the de-embedding of the noise parameters.

B.1 THEORETICALLY

This section gives the theoretical basis for the noise de-embedding procedure. The test structure used to measure RF transistors is presented in Fig. B.1 which illustrates the RF measurement pads (Ground-Signal-Ground GSG pads). For the current used technologies, the pads are usually 50 μm x 50 μm. This big area of metal layers highly affect the four noise parameters. This test structure can be represented as 2-port network as shown in Fig. B.2.

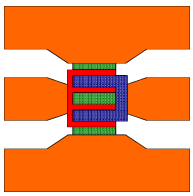

Fig. B.1.: The test structure for on-wafer measurements of RF transistors including the transistor and the Ground-Signal-Ground (GSG) pads.

Fig. B.2.: The 2-port representation of the test structure.

As explained in chapter 6, the output network of the pads (Open_{out}) does not affect the noise performance of the DUT. Therefore, the input network (Open_{in}) only is considered in this de-embedding procedure.

To get (Open_{in}), the complete Open is split into two parts (Open_{in}) and (Open_{out}) using the network shown in Fig. B.3.

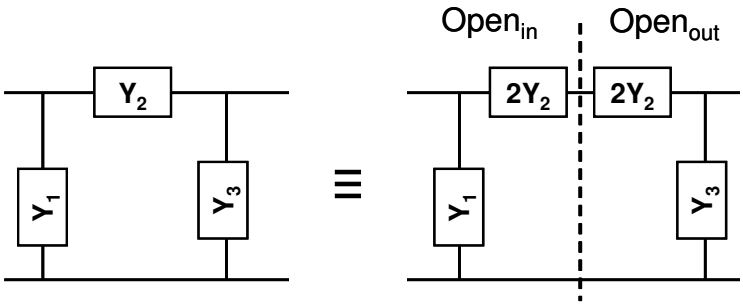

Fig. B.3.: The 2-port representation of the test structure.

If the admittance of the complete Open structure is given by

$$Y_{\text{Open}} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{B.1}$$

therefore, the input part Y_{OpenIn} is given by

$$Y_{\text{Open}_{\text{IN}}} = \begin{bmatrix} Y_1 + 2Y_2 & -2Y_2 \\ -2Y_2 & 2Y_2 \end{bmatrix} = \begin{bmatrix} Y_{11} - Y_{12} & 2Y_{12} \\ 2Y_{12} & -2Y_{12} \end{bmatrix} \tag{B.2}$$

Next, the noise de-embedding is based on the relation

$$[C_{A_{\text{total}}}] = [A_{\text{Open}_{\text{IN}}}]\,[C_{A_{\text{DUT}}}]\,[A_{\text{Open}_{\text{In}}}]^{+} + \left[C_{A_{\text{OpenIN}}}\right] \tag{B.3}$$

where $C_{A_{\text{total}}}$ is the total chain matrix (DUT+pads), $A_{\text{Open}_{\text{IN}}}$ is the chain representation of $Y_{\text{Open}_{\text{IN}}}$, $C_{A_{\text{OpenIN}}}$ is the chain matrix of the input network of the open structure, and $C_{A_{\text{DUT}}}$ is the chain matrix of the DUT only (or the de-embedded chain matrix). The later, $C_{A_{\text{DUT}}}$, is the only unknown in the previous equation since the other variables are calculated from measured data as follows [1]:

$C_{A_{\text{total}}}$ is calculated directly from the measured four noise parameters:

$$\begin{aligned}\left[C_{A_{\text{total}}}\right] &= \begin{bmatrix} \overline{e^2} & \overline{ei^*} \\ \overline{e^*i} & \overline{i^2} \end{bmatrix} \\ &= 4kT_0\Delta f \begin{bmatrix} R_n & \dfrac{NF_{\min}-1}{2} - R_nY_{\text{opt}}^* \\ \dfrac{NF_{\min}-1}{2} - R_nY_{\text{opt}} & R_n\left|Y_{\text{opt}}\right|^2 \end{bmatrix}\end{aligned} \tag{B.4}$$

To calculate $C_{A_{\text{OpenIN}}}$, $C_{Y_{\text{OpenIN}}}$ is first calculated from:

$$C_{Y_{\text{OpenIN}}} = 2kT\Re\left\{Y_{\text{Open}_{\text{IN}}}\right\} \tag{B.5}$$

then $C_{A_{\text{OpenIn}}}$ is calculated as (see Appendix D)

$$\left[C_{A_{\text{OpenIN}}}\right] = [T]\left[C_{Y_{\text{OpenIN}}}\right][T]^{+} \tag{B.6}$$

where $[T]$ in this case is equal to:

$$[T] = \begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix} \tag{B.7}$$

Therefore, $C_{A_{\text{DUT}}}$ is directly calculated from:

$$\left[C_{A_{\text{DUT}}}\right] = \left[A_{\text{Open}_{\text{In}}}\right]^{-1}\left\{\left[C_{A_{\text{total}}}\right] - \left[C_{A_{\text{OpenIn}}}\right]\right\}\left\{\left[A_{\text{Open}_{\text{IN}}}\right]^{+}\right\}^{-1} \tag{B.8}$$

B.2 PRACTICALLY

The steps of the de-embedding procedure is summarized as follows:

- Y_{Open} and A_{Open} are calculated from measured S_{Open}[1].
- $C_{A_{\text{total}}}$ is calculated from measured noise parameters using (B.4).
- $C_{A_{\text{total}}}$ is converted to $C_{Y_{\text{total}}}$ using Appendix D.
- $C_{Y_{\text{Open}}}$ is calculated using (B.5).
- $C_{Y_{\text{DUT}}} = C_{Y_{\text{total}}}$ - $C_{Y_{\text{Open}}}$.[2]
- $C_{Y_{\text{DUT}}}$ is converted to $C_{A_{\text{DUT}}}$ using Appendix D.
- The de-embedded four noise parameters are then calculated using (B.4) as follows: For simplicity, the de-embedded $C_{A_{\text{DUT}}}$ is called C_A. Therefore,

$$R_n = \frac{C_{A_{11}}}{4kT} \tag{B.9}$$

[1]For all transformations between different electrical representation (i.e. S, Y, Z, or A) see Appendix C.

[2]If a short structure is available, an extra step can be added where $C_{Y_{\text{DUT}}}$ is converted to $C_{Z_{\text{DUT}}}$ which is then used to get $C'_{Z_{\text{DUT}}} = C_{Z_{\text{DUT}}} - C_{Z_{\text{Short}}}$.

$$|Y_{\text{opt}}|^2 = \frac{C_{A_{22}}}{4kTR_n} \tag{B.10}$$

$$B_{\text{opt}} = \frac{\Im\{C_{A_{12}}\} - \Im\{C_{A_{21}}\}}{8R_n kT} \tag{B.11}$$

$$G_{\text{opt}} = \sqrt{|Y_{\text{opt}}|^2 - B_{\text{opt}}^2} \tag{B.12}$$

$$NF_{\text{min}} = 2\left[\frac{C_{A_{12}}}{4kT} + R_n Y_{\text{opt}}^*\right] + 1 \tag{B.13}$$

B.3 INTRINSIC NOISE PARAMETERS

In chapter 6, the four noise parameters are presented in their "intrinsic" form, which is the noise parameters of the transistor after removing the effect of the thermal noise of the extrinsic resistances R_{g}, R_{s}, and R_{d}. The procedure to calculate these intrinsic noise parameters is very similar to the procedure explained above for the de-embedding of the noise parameters. It simply consists of:

- The extrinsic impedance matrix Z_{ext} is calculated as:

$$Z_{\text{ext}} = \begin{bmatrix} R_{\text{g}} + R_{\text{s}} & R_{\text{s}} \\ R_{\text{s}} & R_{\text{d}} + R_{\text{s}} \end{bmatrix} \tag{B.14}$$

- The impedance matrix of the DUT Z_{DUT} is calculated from the de-embedded measured S-parameters of the DUT.
- The intrinsic impedance matrix of the DUT Z_{int} is calculated as $Z_{\text{int}} = Z_{\text{DUT}} - Z_{\text{ext}}$. This is needed for the T matrix required from the transfer from $C_{A_{\text{DUT}}}$ to $C_{Z_{\text{DUT}}}$ in the next step.
- The chain matrix of the DUT (calculated from (B.4) and using the de-embedded noise parameters) $C_{A_{\text{DUT}}}$ is converted into the impedance representation $C_{Z_{\text{DUT}}}$.
- The intrinsic impedance matrix $C_{Z_{\text{int}}}$ is calculated from

$$C_{Z_{\text{int}}} = C_{Z_{\text{DUT}}} - 4kTZ_{\text{ext}} \tag{B.15}$$

- The intrinsic chain matrix $C_{A_{\text{int}}}$ is then calculated from $C_{Z_{\text{int}}}$.
- The intrinsic noise parameters are calculated from $C_{A_{\text{int}}}$ using (B.9) to (B.13).

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APPENDIX C
TRANSFORMATION OF ELECTRICAL MATRICES

Any electrical two-port network, as the one shown in Fig. C.1, can be represented in one of the following representations:

– Impedance representation (Z-parameters):

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \end{aligned} \tag{C.1}$$

– Admittance representation (Y-parameters):

$$\begin{aligned} I_1 &= Y_{11}V_1 + Y_{12}V_2 \\ I_2 &= Y_{21}V_1 + Y_{22}V_2 \end{aligned} \tag{C.2}$$

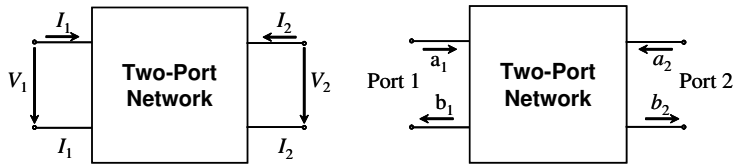
– Chain representation ($ABCD$-parameters or simply A-parameters):

$$\begin{aligned} V_1 &= A_{11}V_2 - A_{12}I_2 \\ I_1 &= A_{21}V_2 - A_{22}I_2 \end{aligned} \tag{C.3}$$

– Scattering representation (S-parameters):

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \tag{C.4}$$

The passage from one electrical representation to another is assured through simple mathematical calculations as shown in the table presented at the end of this appendix [1–3]. Notice that, all matrices are normalized with respect to the characteristic impedance Z_0, i.e. $Z = Z(\text{from table}) \times Z_0$, $Y = Y(\text{from table}) \times \dfrac{1}{Z_0}$, etc. Also, the source and load impedances are assumed to be equal to Z_0.



(a) Z, Y, and A parameters. (b) S-parameters.

Fig. C.1.: Two-port network representations.

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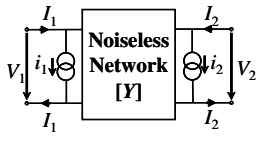
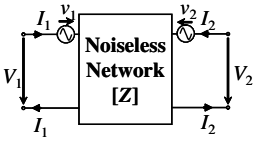
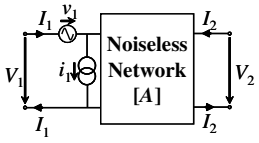
	$[S]$	$[Z]$	$[Y]$	$[A]$
$[S]$	$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$	$S_{11} = \frac{(Z_{11}-1)(Z_{22}+1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$ $S_{12} = \frac{2Z_{12}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$ $S_{21} = \frac{2Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$ $S_{22} = \frac{(Z_{11}+1)(Z_{22}-1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}}$	$S_{11} = \frac{(1-Y_{11})(1+Y_{22}) + Y_{12}Y_{21}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$ $S_{12} = \frac{-2Y_{12}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$ $S_{21} = \frac{-2Y_{21}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$ $S_{22} = \frac{(1+Y_{11})(1-Y_{22}) + Y_{12}Y_{21}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}}$	$S_{11} = \frac{A_{11}+A_{12}-A_{21}-A_{22}}{A_{11}+A_{12}+A_{21}+A_{22}}$ $S_{12} = \frac{2(A_{11}A_{22}-A_{12}A_{21})}{A_{11}+A_{12}+A_{21}+A_{22}}$ $S_{21} = \frac{2}{A_{11}+A_{12}+A_{21}+A_{22}}$ $S_{22} = \frac{-A_{11}+A_{12}-A_{21}+A_{22}}{A_{11}+A_{12}+A_{21}+A_{22}}$
$[Z]$	$Z_{11} = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$ $Z_{12} = \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$ $Z_{21} = \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$ $Z_{22} = \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\frac{1}{\det(Y)} \begin{bmatrix} Y_{22} & -Y_{12} \\ -Y_{21} & Y_{11} \end{bmatrix}$	$\frac{1}{A_{21}} \begin{bmatrix} A_{11} & \det(A) \\ 1 & A_{22} \end{bmatrix}$
$[Y]$	$Y_{11} = \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$ $Y_{12} = \frac{-2S_{12}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$ $Y_{21} = \frac{-2S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$ $Y_{22} = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$	$\frac{1}{\det(Z)} \begin{bmatrix} Z_{22} & -Z_{12} \\ -Z_{21} & Z_{11} \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\frac{1}{A_{21}} \begin{bmatrix} A_{22} & -\det(A) \\ -1 & A_{11} \end{bmatrix}$
$[A]$	$A_{11} = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{2S_{21}}$ $A_{12} = \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}}$ $A_{21} = \frac{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}{2S_{21}}$ $A_{22} = \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{2S_{21}}$	$\frac{1}{Z_{21}} \begin{bmatrix} Z_{11} & \det(Z) \\ 1 & Z_{22} \end{bmatrix}$	$\frac{1}{Y_{21}} \begin{bmatrix} -Y_{22} & -1 \\ -\det(Y) & -Y_{11} \end{bmatrix}$	$\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}$

APPENDIX D

NOISE MATRICES

The different representations of noise sources results in different noise correlation matrix representations as summarized in Table D.1 by Hillbrand and Russer in 1976 [1]:

Table D.1.: Noise correlation matrices of different representations.

	Admittance Representation	Impedance Representation	Chain Representation
Equivalent Noise Circuit			
Correlation Matrix	$C_Y = \begin{bmatrix} C_{i_1 i_1^*} & C_{i_1 i_2^*} \\ C_{i_2 i_1^*} & C_{i_2 i_2^*} \end{bmatrix}$	$C_Z = \begin{bmatrix} C_{v_1 v_1^*} & C_{v_1 v_2^*} \\ C_{v_2 v_1^*} & C_{v_2 v_2^*} \end{bmatrix}$	$C_A = \begin{bmatrix} C_{vv^*} & C_{vi^*} \\ C_{iv^*} & C_{ii^*} \end{bmatrix}$
Electrical Matrix	$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}$

The manipulation of complex noisy two-ports requires the transformation from one representation to another in order to simplify and solve the noise problem as explained in section 6.2.2 [1]. The transformation is achieved through a

Table D.2.: Transformation from one representation of noise correlation matrix to another.

		From $[C]$		
		Admittance	Impedance	Chain
To $[C']$	Admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$
	Impedance	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$
	Chain	$\begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

simple equation:

$$[C'] = [T]\,[C]\,[T]^{+} \tag{D.1}$$

where $[C']$ is the new required noise correlation matrix representation, $[C]$ is the original noise correlation matrix, $[T]$ is the transformation matrix, and the superscript + denotes the Hermitian conjugate (transposed conjugate) of the transformation matrix. Table D.2 summarizes the different transformation matrices needed for the different possible transformation schemes [1].

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APPENDIX E

ANALYTICAL FORMULA FOR THE INTRINSIC ASSOCIATED GAIN

A derivation is presented hereafter for the intrinsic associated gain G_{ass} which depends only on the intrinsic characteristics of the device [1].

The general equation that describes associated gain in FETs was previously introduced as [2]

$$G_{\text{ass}} = \frac{|Y_{21}|^2 \, \Re(Y_{\text{opt}})}{|Y_{11} + Y_{\text{opt}}|^2 \, \Re(Y_{\text{out}})} \tag{E.1}$$

with Y_{out} being the output admittance and expressed as

$$Y_{\text{out}} = \frac{Y_{11}Y_{22} - Y_{12}Y_{21} + Y_{22}Y_{\text{opt}}}{Y_{11} + Y_{\text{opt}}} \tag{E.2}$$

The intrinsic admittance matrix of the transistor can be calculated from Fig. E.1 as

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} j\omega\left(C_{\text{gs}} + C_{\text{gd}}\right) & -j\omega C_{\text{gd}} \\ G_{m\text{i}} & G_{\text{dsi}} + j\omega\left(C_{\text{gs}} + C_{\text{gd}}\right) \end{bmatrix} \tag{E.3}$$

whereas $Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}}$ can be expressed as [3]

$$G_{\text{opt}} = \omega C_{\text{gg}} \sqrt{\frac{R}{P}} \sqrt{1 - C^2} \tag{E.4}$$

$$B_{\text{opt}} = \omega C_{\text{gg}} \left(C \sqrt{\frac{R}{P}} - 1 \right) \tag{E.5}$$

where $C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}}$.

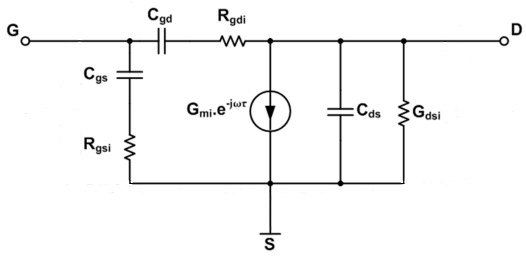

Fig. E.1.: Small-signal equivalent circuit used to characterize devices in high frequency regime of operation.

It is easier to analyze (E.1) part by part:

$$\begin{aligned} |Y_{11} + Y_{\text{opt}}|^2 &= |j\omega C_{\text{gg}} + G_{\text{opt}} + jB_{\text{opt}}|^2 \\ &= \omega^2 C_{\text{gg}}^2 \frac{R}{P} \end{aligned} \tag{E.6}$$

$$Y_{\text{out}} = G_{\text{dsi}} + \frac{j\omega C_{\text{gd}} G_{mi}}{j\omega C_{\text{gg}} + G_{\text{opt}} + jB_{\text{opt}}} \times \frac{G_{\text{opt}} - j\left(\omega C_{\text{gg}} + B_{\text{opt}}\right)}{G_{\text{opt}} - j\left(\omega C_{\text{gg}} + B_{\text{opt}}\right)} \tag{E.7}$$

Therefore

$$\begin{aligned} \Re\left(Y_{\text{out}}\right) &= \frac{G_{\text{dsi}}\omega^2 C_{\text{gg}}^2 \frac{R}{P} + \omega^2 C_{\text{gd}} C_{\text{gg}} G_{mi} C \sqrt{\frac{R}{P}}}{\omega^2 C_{\text{gg}}^2 \frac{R}{P}} \\ &\approx \frac{C_{\text{gd}}}{C_{\text{gg}}} \frac{G_{mi} C}{\sqrt{\frac{R}{P}}} \end{aligned} \tag{E.8}$$

Then, applying (E.4)–(E.8) into (E.1), the intrinsic associated gain can be expressed as

$$G_{\text{ass}} = \frac{f_T}{f} \frac{\sqrt{1 - C^2}}{C} \frac{C_{\text{gg}}}{C_{\text{gd}}} \tag{E.9}$$

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APPENDIX F

F_{50} CALCULATION

F.1 SIMPLIFIED EXPRESSION

In this derivation, the effect of pad capacitances is neglected. The noise figure of a system with a source of admittance $Y_\mathrm{s} = G_\mathrm{s} + jB_\mathrm{s}$ [1, 2]

$$F = NF_\mathrm{min} + \frac{R_n}{G_\mathrm{s}} \left| Y_\mathrm{s} - Y_\mathrm{opt} \right|^2 \tag{F.1}$$

where

$$NF_\mathrm{min} = 1 + 2R_n \left(G_\mathrm{opt} + G_\mathrm{cor} \right) \tag{F.2}$$

For a source of 50 Ω impedance ($Y_\mathrm{s} = G_0 = 20$ mS), the noise figure F_{50} is given by [3]

$$\begin{aligned} F_{50} &= NF_\mathrm{min} + \frac{R_n}{G_0} \left| G_0 - Y_\mathrm{opt} \right|^2 \\ &= NF_\mathrm{min} + \frac{R_n}{G_0} \left[\left(G_0 - G_\mathrm{opt} \right)^2 + B_\mathrm{opt}^2 \right] \\ &= 1 + 2R_n G_\mathrm{opt} + \frac{R_n}{G_0} \left[G_0^2 + G_\mathrm{opt}^2 - 2G_0 G_\mathrm{opt} + B_\mathrm{opt}^2 \right] \\ &= 1 + R_n G_0 + \frac{R_n}{G_0} \left[G_\mathrm{opt}^2 + B_\mathrm{opt}^2 \right] \end{aligned} \tag{F.3}$$

where the equivalent noise resistance is given by [4]

$$R_n = \frac{\left(R_\mathrm{g} + R_\mathrm{s} \right) g_m + P}{g_m} \tag{F.4}$$

$$
\begin{aligned}
G_{\text{opt}}^2 + B_{\text{opt}}^2 &= \frac{\omega^2 C_{\text{gg}}^2}{\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right]^2} \left[PR\left(1 - C^2\right)\right. \\
&\quad \left. + \left(P + R - 2C\sqrt{PR}\right)(R_{\text{g}} + R_{\text{s}})\, g_m\right] \\
&\quad + \frac{\omega^2 C_{\text{gg}}^2}{\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right]^2} \left(C\sqrt{PR} - P\right)^2 \\
&= \frac{\omega^2 C_{\text{gg}}^2}{\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right]^2} \left[PR\left(1 - C^2\right)\right. \\
&\quad \left. + \left(P + R - 2C\sqrt{PR}\right)(R_{\text{g}} + R_{\text{s}})\, g_m + C^2 PR + P^2 - 2CP\sqrt{PR}\right] \\
&= \frac{\omega^2 C_{\text{gg}}^2}{\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right]^2} \left[P\left(P + R - 2C\sqrt{PR}\right) + \right. \\
&\quad \left. \left(P + R - 2C\sqrt{PR}\right)(R_{\text{g}} + R_{\text{s}})\, g_m\right] \\
&= \frac{\omega^2 C_{\text{gg}}^2}{\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right]^2} \left(P + R - 2C\sqrt{PR}\right)\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right] \\
&= \frac{\omega^2 C_{\text{gg}}^2}{\left[P + (R_{\text{g}} + R_{\text{s}})\, g_m\right]} \left(P + R - 2C\sqrt{PR}\right)
\end{aligned}
\tag{F.5}
$$

$$
\frac{R_n}{G_0} \times \left(G_{\text{opt}}^2 + B_{\text{opt}}^2\right) = \frac{\omega^2 C_{\text{gg}}^2}{G_0 g_m} \left(P + R - 2C\sqrt{PR}\right) \tag{F.6}
$$

Therefore, the simplified form of F_{50} can be written as:

$$
F_{50} = 1 + \left(R_{\text{g}} + R_{\text{s}} + \frac{P}{g_m}\right) G_0 + \frac{\omega^2 C_{\text{gg}}^2}{G_0 g_m} \left(P + R - 2C\sqrt{PR}\right) \tag{F.7}
$$

In this case, the effect of pad capacitances, C_{p}, can be accounted for, approximatively, by adding another term to F_{50} as follows:

$$
F_{50} = 1 + \left(R_{\text{g}} + R_{\text{s}} + \frac{P}{g_m}\right) G_0 + \frac{\omega^2 C_{\text{gg}}^2}{G_0 g_m} \left(P + R - 2C\sqrt{PR}\right) + \frac{P}{Gm} G_{\text{cor}} \tag{F.8}
$$

where

$$
G_{\text{cor}} \approx \Re\left(Y_{11}\right) \approx R_{\text{i}} C_{\text{tot}}^2 \omega^2 \tag{F.9}
$$

with

$$
C_{\text{tot}} = C_{\text{gg}} + C_{\text{p}} \tag{F.10}
$$

However, this is not an exact representation of the effect of the pad capacitance on the noise figure.

F.2 EXACT EQUATION (WITH PADS)

Starting by the general equation of F_{50}

$$F_{50} = NF_{\min} + \frac{R_n}{G_0} \left| Y_{\mathrm{s}} - Y_{\mathrm{opt}} \right|^2 \tag{F.11}$$

The right hand side can be analyzied as follows:

$$\begin{aligned} \left| Y_{\mathrm{s}} - Y_{\mathrm{opt}} \right|^2 &= \left(G_0 - G_{\mathrm{opt}} \right)^2 + \left(\omega C_{\mathrm{p}} - B_{\mathrm{opt}} \right)^2 \\ &= G_0^2 - 2G_0 G_{\mathrm{opt}} + G_{\mathrm{opt}}^2 + \omega^2 C_{\mathrm{p}}^2 + B_{\mathrm{opt}}^2 - 2\omega C_{\mathrm{p}} B_{\mathrm{opt}} \end{aligned} \tag{F.12}$$

$$R_n = R_{\mathrm{g}} + R_{\mathrm{s}} + \frac{P}{g_m} \tag{F.13}$$

$$G_{\mathrm{opt}} = \frac{\omega C_{\mathrm{tot}}}{\left[P + \left(R_{\mathrm{g}} + R_{\mathrm{s}} \right) g_m \right]} \sqrt{PR\left(1 - C^2\right) + \left(P + R - 2C\sqrt{PR} \right) \left(R_{\mathrm{g}} + R_{\mathrm{s}} \right) g_m} \tag{F.14}$$

$$B_{\mathrm{opt}} = \frac{\omega C_{\mathrm{tot}}}{\left[P + \left(R_{\mathrm{g}} + R_{\mathrm{s}} \right) g_m \right]} \left(C\sqrt{PR} - P \right) \tag{F.15}$$

$$G_{\mathrm{opt}}^2 = \frac{\omega^2 C_{\mathrm{tot}}^2}{\left[P + \left(R_{\mathrm{g}} + R_{\mathrm{s}} \right) g_m \right]^2} \left[PR\left(1 - C^2\right) + \left(P + R - 2C\sqrt{PR} \right) \left(R_{\mathrm{g}} + R_{\mathrm{s}} \right) g_m \right] \tag{F.16}$$

$$B_{\mathrm{opt}}^2 = \frac{\omega^2 C_{\mathrm{tot}}^2}{\left[P + \left(R_{\mathrm{g}} + R_{\mathrm{s}} \right) g_m \right]^2} \left(C\sqrt{PR} - P \right)^2 \tag{F.17}$$

$$NF_{\min} = 1 + 2R_n G_{\mathrm{opt}} \tag{F.18}$$

Therefore, substituting (F.12)–(F.18) in (F.11):

$$\begin{aligned} F_{50} &= 1 + 2R_n G_{\mathrm{opt}} + \frac{R_n}{G_0} \left(G_0^2 - 2G_0 G_{\mathrm{opt}} + G_{\mathrm{opt}}^2 + \omega^2 C_{\mathrm{p}}^2 + B_{\mathrm{opt}}^2 - 2\omega C_{\mathrm{p}} B_{\mathrm{opt}} \right) \\ &= 1 + 2R_n G_{\mathrm{opt}} + R_n G_0 - 2R_n G_{\mathrm{opt}} + \frac{R_n}{G_0} G_{\mathrm{opt}}^2 + \frac{R_n}{G_0} \omega^2 C_{\mathrm{p}}^2 + \frac{R_n}{G_0} B_{\mathrm{opt}}^2 \\ &\quad - \frac{R_n}{G_0} 2\omega C_{\mathrm{p}} B_{\mathrm{opt}} \\ &= 1 + \left(R_{\mathrm{g}} + R_{\mathrm{s}} + \frac{P}{g_m} \right) G_0 + \frac{R_n}{G_0} \left(G_{\mathrm{opt}}^2 + B_{\mathrm{opt}}^2 + \omega^2 C_{\mathrm{p}}^2 - 2\omega C_{\mathrm{p}} B_{\mathrm{opt}} \right) \end{aligned} \tag{F.19}$$

Taking into account that:

$$\frac{R_n}{G_0} \times \left(G_{\mathrm{opt}}^2 + B_{\mathrm{opt}}^2 \right) = \frac{\omega^2 C_{\mathrm{tot}}^2}{G_0 g_m} \left(P + R - 2C\sqrt{PR} \right) \tag{F.20}$$

and

$$\begin{aligned}\frac{R_n}{G_0}\times\left(\omega^2C_{\mathrm{p}}^2-2\omega C_{\mathrm{p}}B_{\mathrm{opt}}\right) &= \frac{\omega^2C_{\mathrm{p}}^2\left[P+\left(R_{\mathrm{g}}+R_{\mathrm{s}}\right)g_m\right]}{G_0g_m}\\ &\quad-\frac{2\omega C_{\mathrm{p}}\left[P+\left(R_{\mathrm{g}}+R_{\mathrm{s}}\right)g_m\right]}{G_0g_m}\times\frac{\omega C_{\mathrm{tot}}}{\left[P+\left(R_{\mathrm{g}}+R_{\mathrm{s}}\right)g_m\right]}\left(C\sqrt{PR}-P\right)\\ &= \frac{\omega^2C_{\mathrm{p}}^2\left[P+\left(R_{\mathrm{g}}+R_{\mathrm{s}}\right)g_m\right]}{G_0g_m}-\frac{2\omega^2C_{\mathrm{tot}}C_{\mathrm{p}}}{G_0g_m}\left(C\sqrt{PR}-P\right)\\ &= \frac{\omega^2}{G_0g_m}\left\{C_{\mathrm{p}}^2\left[P+\left(R_{\mathrm{g}}+R_{\mathrm{s}}\right)g_m\right]-2C_{\mathrm{p}}C_{\mathrm{tot}}\left(C\sqrt{PR}-P\right)\right\}\end{aligned} \tag{F.21}$$

The exact formula of F_{50} with the pad capacitances taken into account is written as:

$$\begin{aligned}F_{50} = 1+&\left(R_{\mathrm{g}}+R_{\mathrm{s}}+\frac{P}{g_m}\right)G_0\\ &+\frac{\omega^2}{G_0g_m}\left\{C_{\mathrm{tot}}^2\left(P+R-2C\sqrt{PR}\right)+C_{\mathrm{p}}^2\left[P+\left(R_{\mathrm{g}}+R_{\mathrm{s}}\right)g_m\right]\right.\\ &\qquad\left.-2C_{\mathrm{p}}C_{\mathrm{tot}}\left(C\sqrt{PR}-P\right)\right\}\end{aligned} \tag{F.22}$$

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APPENDIX G

NOISE MEASUREMENTS: TUNER CALIBRATION

The measurements of the four noise parameters ($NF_{\min}$, R_n, and Y_{opt}) presented in chapter 6 are achieved using the Tuner method (see section 6.4.2). The tuner noise measurement system utilized in this work is represented in Fig. G.1. The main equipments employed are a HP4142B semiconductor parameter analyzer, a HP8510C vector network analyzer (VNA) controlled by ICCAP 2006B software, a mechanical tuner system from Maury Microwaves in the 1-8-GHz frequency range, an Agilent E440A noise meter, and a noise source.

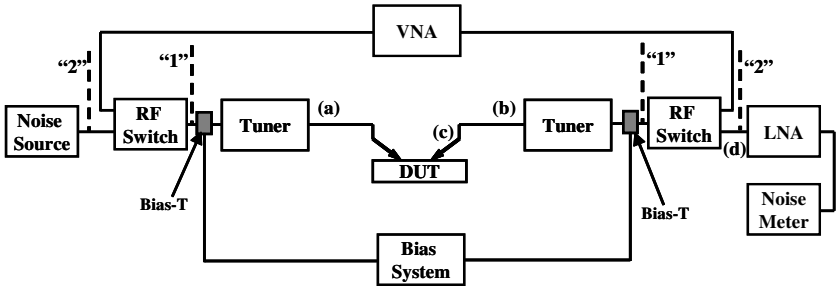

Fig. G.1.: Tuner measurement setup

In order to calibrate such a complicated system, a special procedure has to be followed:

(1) Make one-port (S-parameters) calibration using the VNA connected at (a) and connecting the three standards *open*, *short*, and *load* at the reference plane "1".

(2) Repeat step (1) but this time by connecting the three standards at "2".

(3) Subtract (1) from (2) to obtain the S-parameters of the "RF switch" separately.

(4) Connect the noise source to measure its losses. Note that the Agilent E440A biases the noise source in pulses, whereas we need to measure the reflection of the noise source in "Hot" state, thus we use another voltage source to bias the noise source at 28 V.

(5) Connect the VNA to (b) to start calibrating the other path as in steps (1) and (2).

(6) To characterize cable (c), we measure the S-parameters (one-port calibration) from (d) till (b) then from (d) till DUT, then subtract to get cable (c) separately.

(7) Repeat step (7) for the input path.

(8) Perform a two-port S-parameters calibration for the whole system.

(9) Perform a noise calibration versus frequency (12 impedance points).