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Characterization, modelling and mitigation of substrate-induced effects in RF GaN-on-Si technology

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Thesis submitted in partial fulfillment
of the requirements for the degree of
Docteur en sciences de l'ingénieur et technologie

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Version of August 2024.

Acknowledgements

A PhD thesis is only a personal achievement in appearance. As I conclude this journey, I can only see my name on the first page of this thesis as hiding many others, for each of the many persons that helped me reach this milestone. I hope these few words will reach them.

The exploration of RF substrates started more than 6 years ago, when I visited Jean-Pierre Raskin inquiring about topics for a Master's thesis. Since then, he has been an incredibly supporting advisor. I have had the pleasure to benefit from his expertise, interest in my work and dedication to empower me as a researcher. Also outside of the lab, I am grateful to have met a very authentic and passionate person.

It was never officially the case, but I always felt fortunate to have two advisors. I would like to thank Bertrand Parvais to have given me the opportunity to integrate his group at imec. I greatly appreciated his availability and enthusiasm, along with his valuable industrial point of view. I was always happy to chat about almost anything in the office, around the coffee machine or on a lunch run.

I would like to thank the members of my jury: Jean-Pierre Raskin, Bertrand Parvais, Dimitri Lederer, Sachin Yadav, Herwig Hahn and Cesar Roda Neve for making the time to read this thesis and contribute to its improvement. It is my honor to share with you the results of my work.

During these almost five years, I was always hovering between two institutions, UCLouvain and imec. Neverthless, all colleagues on both sides helped me to get a sense of belonging. At UCLouvain, I want to thank the RF SOI group for the great atmosphere on the third floor. More particularly, I would like to acknowledge the insightful discussions with Martin Rack, his critical eye and unfailing assistance in measurement-related issues.

At imec, I have found in the Devint team a group of semiconductor

experts which have been a constant source of learning for me. Most of all I would like to thank Sachin Yadav. Since the very beginning of my time at imec, he has been a true mentor for me. His involvement in my daily progress and broad expertise have been incredibly important in my growth as a scientist. I am also grateful for the long philosophical discussions that would sometimes prolong the technical meetings. For the explorations we did together on life cycle analysis, I would also like to thank the soon-to-be sustainability expert Benjamin Vanhouche.

The many hours spent in measurement labs have been made possible by the lab staff and managers. In Welcome, I would like to thank Pascal Simon for taking care of the facility and providing us with the best equipment, while always being of assistance and ready to help to solve our various problems. I also would like to thank the Winfab team, and more particularly Nicolas André for assisting me in the cleanroom. I am also thankful for the assistance of the administrative staff in the Maxwell building, which greatly contribute to an enjoyable and efficient work environment.

In addition, I want to acknowledge the stimulating collaborations I was lucky to share with Incize (Gilles Scheen, Romain Tuyaerts), CEA-leti (Erwan Morvan) and AIXTRON SE (Herwig Hahn, Christof Mauder).

More personally I would like to thank my family and friends, both from university with the Revue team and from my childhood in Arlon, for their support and precious moments in their presence which I always cherished. I was also immensely lucky to enjoy the athletic company of my training group at the Racing Club de Bruxelles. They have helped me find the essential balance between the mind and the body, and gave me energy to achieve all sorts of goals.

I will never thank my parents enough for their rock solid support. They were always ready to assist me in any way, and I owe the timely delivery of this dissertation to them.

Finally, I thank Alice. Her smile and her presence by my side have made all the challenges of the past years so much easier to overcome.

Abstract

Future telecommunication generations require semiconductor technologies that can deliver large RF power to the antenna with excellent efficiency and linearity at RF and mm-wave frequencies. For these applications, the widespread CMOS technology platform is outperformed by wide bandgap semiconductors such as GaN. In order to deploy GaN circuits in infrastructure and user equipment, its heterointegration on Si substrates brings the advantage of large-area wafer availability and lower cost than other, better-suited substrates such as SiC. However, the Si substrate suffers from parasitic conductivity that can couple to the overlying circuitry and degrade its performance.

This thesis proposes a systematic analysis of the substrate RF performance of GaN-on-Si substrates, at all levels of the material stack. The main goal of this work is to understand the different contributions to the degraded substrate performance.

To do so, several characterization and modelling methods are used. The existing RF substrate characterization techniques are extended by allowing the measurement of the drift of effective resistivity and harmonic distortion over time when the substrate is stressed. Interface characterization techniques are applied to the particular case of high resistivity Si-based substrates with thick dielectrics. Physics-based models are developed to describe the experimental observations and predict the impact of the substrate on RF circuits.

The key message of this dissertation is that contributions to the substrate-related parasitic effects emerge at all levels of the GaN-on-Si material stack. In Si, the undesired diffusion of group III atoms changes the doping, along with the thermal activation of bulk dopants during the various process steps. The interface between Si and the III-N layers also significantly contributes,

with the formation of charge that is highly dependent on process conditions. The text bridges between material characterization, electrical properties and modelling to explain the observed effects. Finally, the semiconducting nature of the upper buffer layers leads to an entirely new phenomenon, where the slow movement of charge trapped in deep levels related to C doping changes the substrate RF figures of merit over time. A fundamental approach is taken to explain this behavior.

RF circuits can be significantly affected by a lossy, non-linear substrate. Two important application for GaN-on-Si are focused upon. The RF switch suffers from the harmonic distortion induced by the substrate, requiring a co-optimization of the substrate and the device to reach high linearity. For the power amplifier, power dissipation in the substrate takes place which reduces the efficiency of the transistor.

More practically, this thesis contributes to the field of GaN-on-Si by providing guidelines to consistently fabricate high-performance substrates. Controlling the parasitic doping in Si and the charge at AlN/Si interface are, together, the key to low-loss GaN-on-Si. Specifications on substrate effective resistivity can also be reached, giving targets to the epitaxial development. At the same time, attention must be given to limit the environmental impact of GaN-on-Si, which is for the moment higher than state-of-the-art Si-based substrates.

List of Publications

[1] **P. Cardinael**, A. Divay, I. Charlet, E. Morvan, and J.-P. Raskin, "A physics-based substrate model for RF loss estimation in GaN-on-Si HEMTs," *IEEE Transactions on Electron Devices*, 2024, Submitted.

[2] **P. Cardinael**, S. Yadav, H. Hahn, M. Zhao, S. Banerjee, B. Kazemi Esfeh, C. Mauder, B. O'Sullivan, U. Peralagu, A. Vohra, R. Langer, N. Collaert, B. Parvais, and J.-P. Raskin, "AlN/Si interface engineering to mitigate RF losses in MOCVD grown GaN-on-Si substrates," *Applied Physics Letters*, 2024, In press.

[3] M. Perrosé, P. Acosta Alba, S. Reboh, J. Lugo, C. Plantier, **P. Cardinael**, M. Rack, F. Allibert, F. Milesi, X. Garros, and J.-P. Raskin, "Local interface RF passivation layer based on helium ion-implantation in high-resistivity silicon substrates," presented at the International Microwave Symposium, Washington, DC, 2024.

[4] B. Vanhouche, **P. Cardinael**, L. Boakes, L.-A. Ragnarsson, C. Rolin, J.-P. Raskin, and B. Parvais, "Environmental analysis of RF substrates," presented at the Electronics Goes Green 2024, Berlin, Germany, Jun. 2024.

[5] H. Hahn, C. Mauder, M. Marx, Z. Gao, P. Lauffer, O. Schön, P. T. John, S. Yadav, S. Banerjee, **P. Cardinael**, J.-P. Raskin, B. Parvais, and D. Fahle, "Depleted AlN/Si interfaces for minimizing RF loss in GaN-on-Si HEMTs," presented at the CS Mantech, Tucson, AZ, May 2024.

[6] **P. Cardinael**, S. Yadav, B. Parvais, and J.-P. Raskin, "Effect of buffer charge redistribution on RF losses and harmonic distortion in GaN-on-Si substrates," *IEEE Journal of the Electron Devices Society*, vol. 12, pp. 322–330, Apr. 2024.

[7] **P. Cardinael**, S. Yadav, M. Rack, U. Peralagu, A. Alian, B. Parvais, N. Collaert, and J.-P. Raskin, "Contribution of substrate harmonic distortion to GaN-on-Si RF switches linearity," *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 3, pp. 298–301, Mar. 2024.

[8] G. Scheen, R. Tuyaerts, **P. Cardinael**, E. Ekoga, K. Aouadi, C. Pavageau, A. Rassekh, M. Nabet, S. Yadav, J.-P. Raskin, B. Parvais, and M. Emam, "GaN-on-porous silicon for RF applications," in *2023 53rd European Microwave Conference (EuMC)*, Sep. 2023, pp. 842–845.

[9] B. Parvais, S. Yadav, M. Zhao, and **P. Cardinael**, "Semiconductor substrates and methods of producing the same," U.S. Patent 2023039 5376A1, Dec. 7, 2023.

[10] **P. Cardinael**, S. Yadav, M. Zhao, M. Rack, D. Lederer, N. Collaert, B. Parvais, and J.-P. Raskin, "Time dependence of RF losses in GaN-on-Si substrates," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 688–691, Jun. 2022.

[11] N. Collaert, A. Alian, A. Banerjee, G. Boccardi, **P. Cardinael**, V. Chauhan, C. Desset, R. ElKashlan, A. Khaled, M. Ingels, B. Kunert, Y. Mols, B. O'Sullivan, U. Peralagu, N. Pinho, R. Rodriguez, A. Sibaja-Hernandez, S. Sinha, X. Sun, A. Vais, B. Vermeersch, S. Yadav, D. Yan, H. Yu, Y. Zhang, M. Zhao, J. Van Driessche, G. Gramegna, P. Wambacq, B. Parvais, and M. Peeters, "III-V/III-N technologies for next generation high-capacity wireless communication," in *2022 International Electron Devices Meeting (IEDM)*, Dec. 2022, pp. 11.5.1–11.5.4.

[12] H. Yu, B. Parvais, U. Peralagu, R. Y. ElKashlan, R. Rodriguez, A. Khaled, S. Yadav, A. Alian, M. Zhao, N. De Almeida Braga, J. Cobb, J. Fang, **P. Cardinael**, A. Sibaja-Hernandez, and N. Collaert, "Back barrier trapping induced resistance dispersion in GaN HEMT: Mechanism, modeling, and solutions," in *2022 International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2022, pp. 30.6.1–30.6.4.

[13] Q. Courte, M. Rack, M. Nabet, **P. Cardinael**, and J.-P. Raskin, "High-temperature characterization of multiple silicon-based substrate for RF-IC applications," *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 620–626, 2022.

[14] **P. Cardinael**, S. Yadav, M. Zhao, M. Rack, D. Lederer, N. Collaert, B. Parvais, and J.-P. Raskin, "Impact of III-N buffer layers on RF losses and harmonic distortion of GaN-on-Si substrates," in *ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC)*, Grenoble, France: IEEE, Sep. 13, 2021, pp. 303–306.

[15] B. Parvais, R. ElKashlan, H. Yu, A. Sibaja-Hernandez, B. Vermeersch, V. Putcha, **P. Cardinael**, R. Rodriguez, A. Khaled, A. Alian, U. Peralagu, M. Zhao, S. Yadav, G. Gramegna, J. V. Driessche, and N. Collaert, "Transistor modelling for mm-wave technology pathfinding," in *2021 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2021, pp. 247–250.

[16] Q. Courte, M. Rack, M. Nabet, **P. Cardinael**, and J.-P. Raskin, "High-temperature characterization of novel silicon-based substrate solutions for RF-IC applications," in *ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC)*, Sep. 2021, pp. 187–190.

[17] S. Yadav, **P. Cardinael**, M. Zhao, K. Vondkar, A. Khaled, R. Rodriguez, B. Vermeersch, S. Makovejev, E. Ekoga, A. Pottrain, N. Waldron, J.-P. Raskin, B. Parvais, and N. Collaert, "Substrate RF losses and non-linearities in GaN-on-Si HEMT technology," in *2020 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2020, pp. 8.2.1–8.2.4.

Contents

Introduction

Context

Technological requirements for wireless telecommunication are becoming more stringent with the advent of future generations such as 5G or 6G. These future generations are characterized by a growth of data traffic (by increase of the number of connected devices or by the amount of data being exchanged), which requires an increased bandwidth as well as the advent of complex modulation schemes. Transmission of data under those constrains requires highly linear components, in order to accurately discriminate symbols in the modulation constellations (characterized by high peak-to-average ratios) and to prevent spreading to adjacent channels.

Consequently, the power amplifier found in the front-end-module will need to function at a large back-off from its saturation power. To achieve acceptable signal-to-noise ratios, the technology on which the power amplifier is based should enable a large power output. At the same time, it should be efficient to minimize power loss. As the overall power consumption of the cellular network increases, a high efficiency can represent significant savings, both financially and in terms of greenhouse gases emissions.

The semiconductor technology landscape offers different candidates to realize these circuits. A survey of recent literature shows that in the frequency bands of interest, the traditional Si-based power amplifiers are outperformed by other technologies based on III-V or III-N semiconductors such as GaN (Fig. 1a). GaN shows attractive material properties which allow high electric fields, high current and high power density (Fig. 1b)[1].

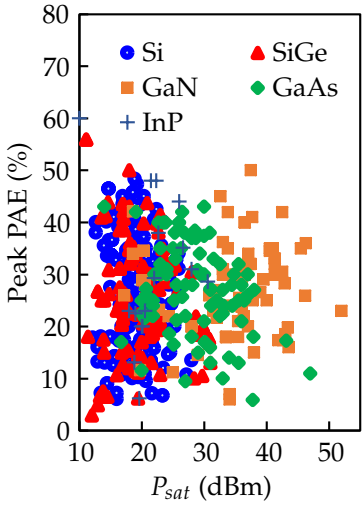
[1]The output power figure of merit for benchmarking semiconductor materials is defined as $FoM = JFoM^2 \frac{\pi \varepsilon_s W_g}{8 f_T} \left(1 - \frac{V_k}{V_{BD}}\right)$, where $JFoM$ is the commonly used Johnson figure of merit [1].

However, bulk GaN wafers are currently not available at a reasonable cost. The material is typically integrated heterogeneously as a thin film on a different substrate, namely SiC or, in the early stages of development, sapphire. These solutions are costly, and prevent the penetration of GaN into more large-scale applications such as user equipment.

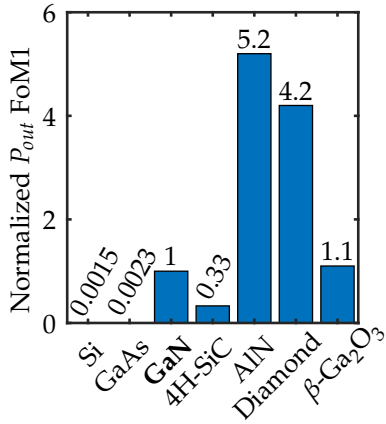
GaN-on-Si proposes to overcome these limitations by combining the attractive GaN technology with the low cost and maturity of CMOS technology, also offering large-area wafers. Potentially, other components of the front-end module such as the RF switch or the low-noise amplifier could also benefit from this platform.

While the power performance of GaN devices integrated on Si wafers is becoming more and more competitive, a suitable platform for RF applications must also limit the losses, crosstalk and non-linearities along the signal path. Although part of these parasitic effects are linked to the transistor, the engineered substrate plays a pivotal role. In particular, the use of a semiconducting substrate such as Si leads to a degradation of the RF substrate properties compared to standard substrates [2]. Poor substrate performance is known to alter the functioning of a wide variety of components in the RF front-end-module.

- Interconnects suffer from signal loss and distortion.
- Digital switching noise can propagate through the substrate and interfere with other devices.
- RF switches experience additional non-linearities originating in the substrate.
- RF power dissipates in the substrate during large-signal operation of the power amplifier, degrading its efficiency.



(a) Survey of power amplifiers from 20 GHz to 50 GHz. Data from [3].



(b) Output power for a given cutoff frequency f_T. GaN shows an almost 1000x improvement in FoM compared to Si. Reproduced from [1]. ©Springer Nature 2020

Fig. 1 GaN power amplifiers outperform Si in terms of saturated power while maintaining high efficiency. This is owing to the superior material properties of GaN, showing a almost 100-fold improvement in the ouput power figure of merit compared to Si.

Objectives of this thesis

The GaN-on-Si stack presents more substrate-induced parasitic effects than its competitors based on semi-insulating substrates. To help enable the adoption of GaN-on-Si as a relevant candidate for RF and mm-wave circuits, it is important to improve the substrate performance.

To that aim, this thesis considers three scientific questions.

Understanding *What are the main contributions to degraded substrate performance in GaN-on-Si and what is the role played by the complex epitaxial stack in it?*

Predicting *To what extent does the substrate affect the functioning and figures of merit of key target applications for RF GaN-on-Si, namely the RF switch and the power amplifier? what are the substrate specifications for a limited impact?*

Improving *How can engineers tune the fabrication process to ensure the manufacturing of high-performance GaN-on-Si substrates?*

In order to answer these questions, significant methodological contributions are needed, that can percolate beyond the case of GaN-on-Si. Charge movement in semiconductor stacks must be understood and modelled, which is backed by strong insights on the material physics. Characterization techniques existing (e.g. for SOI substrates) are extended and generalized to any Si-based RF substrate. Novel modelling approaches are also developed.

Because the issue stems from the materials and has effects up to the circuit level, this work bridges between semiconductor physics, TCAD, electrical modelling, and electrical characterization.

Finally, an additional transversal scientific question is considered to help establish a more sustainable RF technology landscape.

Assessing *What is the environmental impact of GaN-on-Si compared to other competing technologies that offer state-of-the-art substrate performance?*

Outline: the GaN-on-Si epitaxial stack

This thesis is structured as an analysis of every level of the GaN-on-Si material stack, from bottom to top, from the perspective of substrate-related parasitic effects. Its outline is represented schematically in Fig. 2.

Chapter 1 begins by presenting the main RF characterization techniques aimed at measuring the performance of Si-based substrates. The Si substrate is discussed in detail together with its contributions to RF loss. The impact of various steps of the GaN-on-Si process on the substrate performance is studied. The evolution of Si with temperature, which can be elevated under high power-density GaN HEMTs, is also examined.

Chapter 2 focuses on the region which mostly determines substrate performance, namely the AlN nucleation layer and its interface with Si. Experimental techniques available to characterize the interface are presented and tested. Then, the engineering of this interface to minimize substrate loss is discussed. The important effect of a process parameter on the interface charge is demonstrated and modelled.

Chapter 3 provides an in-depth study of the effect of the upper III-N layers on the performance of the overall substrate. The semi-insulting nature of these materials leads to charge redistribution mechanisms, which are first analyzed from a theoretical point of view. Then, two novel characterization setups are introduced to experimentally demonstrate the time dependence of substrate performance. These effects are finally reproduced in a TCAD environment.

Chapter 4 discusses the impact of the GaN-on-Si substrates on two functional blocks of importance for applications in front-end modules. First, the contribution of substrate-induced harmonic distortion on the linearity of RF Switches is presented by comparing common-gate HEMT and CPW structures. Secondly, the power loss caused by a lossy substrate under the HEMT is measured and modelled to predict the PAE penalty caused by the substrate.

Chapter 5 takes a step back and offers a comparative life cycle analysis of different Si substrates. The place of GaN-on-Si in a landscape of Si-based RF substrates is discussed from an ecological standpoint. An alternative option to prevent substrate loss is presented in the form of GaN-on-Porous Si. Global conclusions from this thesis are finally taken.

Chapter 5: Comparative life-cycle analysis, perspectives and conclusions

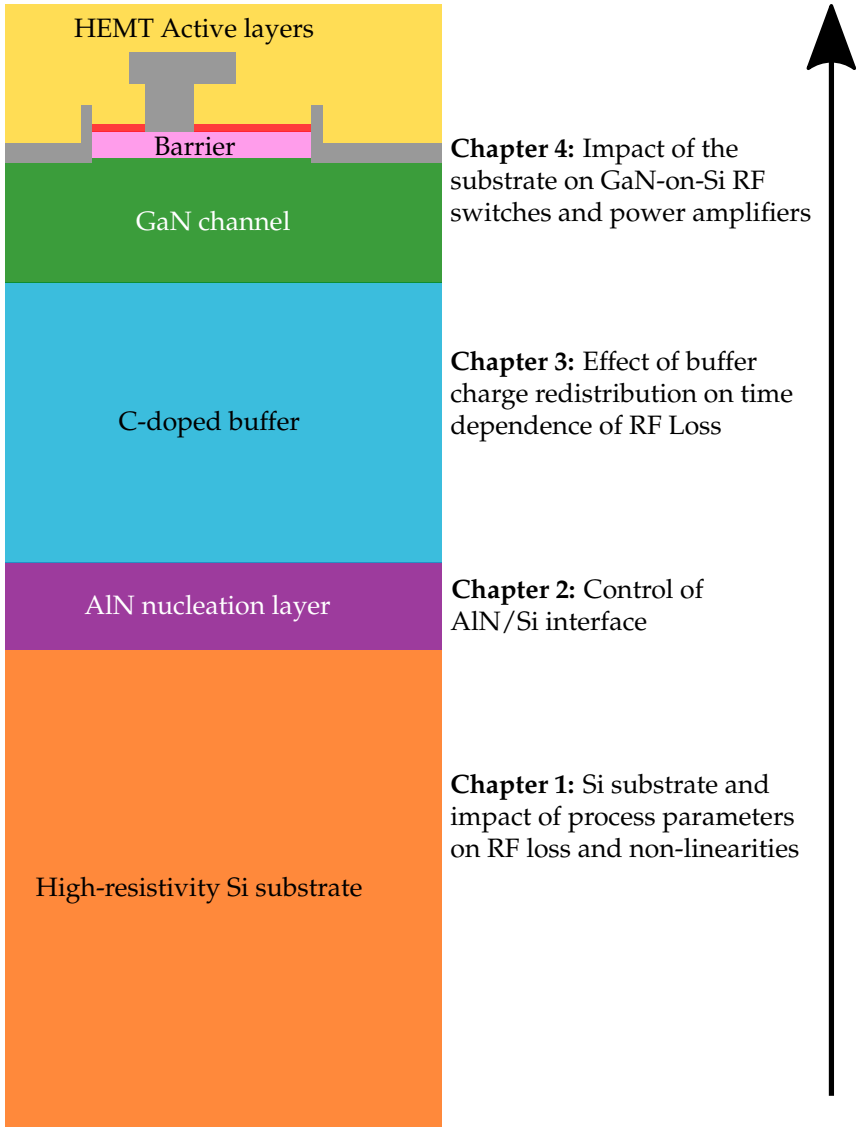


Fig. 2 The structure of this thesis can be visualized as going from the bottom to the top of the GaN-on-Si material stack and analyzing every part of it from the angle of substrate loss and non-linearities.

1

GaN-on-Si substrates for RF Applications

1.1 Introduction

The technological choice of using a Si wafer as a substrate for the epitaxial growth of GaN, rather than more traditional options such as SiC and sapphire, is driven by low cost and availability of large-area wafers. However, it brings additional challenges. These difficulties originate from the material properties of Si, which are compared to other substrates in Table 1.1.

Firstly, the lattice mismatch of Si to GaN is the highest among the three substrates. This renders the growth of GaN more challenging and originally led to a more defective GaN layer. Secondly, the thermal conductivity of Si is relatively low compared to SiC. Since the main target applications for GaN within the RF space are power amplifiers which dissipate heat (power amplifiers are not ideally efficient), thermal management can become an issue in GaN-on-Si devices. Finally, the resistivity of Si is finite. High resistivity (HR) Si is used in this thesis, which is defined by a resistivity above $3\,\mathrm{k}\Omega \cdot \mathrm{cm}$, or a doping level below $4 \times 10^{12}\,\mathrm{cm}^{-3}$ for p-type Si. This brings the entirely new concern of substrate-induced parasitic effects. Crosstalk, substrate loss and non-linearities all originate in the semiconducting Si wafer. Such an issue is unheard of in traditional GaN circuits, but is well known in the realm of radio frequency silicon on insulator (RFSOI) circuits

Material	HR Si	SiC	Sapphire	GaN
Lattice constant (nm)	0.54	0.31	0.48	0.32
Thermal Conductivity (W/cm K)	1.56	4.9	0.23	2.1
Resistivity ($\Omega \cdot$ cm)	>3 k	$> 10^7$	$> 10^{11}$	-

Table 1.1 Material properties of different substrates for GaN epitaxy. Data taken from [11].

[4]. For the SiO_2/Si system, the use of high resistivity Si has been proposed to decrease the associated loss and crosstalk [5]. However, the effective resistivity (ρ_{eff}) sensed by the circuits stays orders of magnitude below the nominal resistivity of the substrate due to the formation of a parasitic surface conduction (PSC) layer close to the Si surface [6], [7]. In SOI, the PSC layer originates due to the presence of fixed charges at the SiO_2/Si interface, which attract a large concentration of free carriers at the surface. The suppression of the PSC layer using an engineered trap-rich layer below the oxide has been a key enabler in the deployment of RFSOI technology for RF switches [8]–[10]. GaN-on-Si stacks exhibit a similar effect with similar consequences, although its origin is different. Also, the mitigation techniques used in RFSOI cannot be easily transferred to GaN-on-Si.

In this chapter, the investigation of the substrate-related effects begins with the bottom most layer, the starting Si wafer. In Section 1.2, a brief description of the GaN technology is given, with an emphasis of the specific aspects related to the use of a HR Si wafer. The epitaxial and thermal challenges are introduced.

In Section 1.3, the RF characterization methods employed throughout this thesis are introduced. The small-signal figure-of-merit ρ_{eff} and the large-signal harmonic distortion (HD) measurement are the two important tools that allow the quantification of substrate performance.

Section 1.4 investigates the impact of several important parameters of the GaN-on-Si process on substrate performance. The main cause for degraded ρ_{eff} is presented along with the effects of several high-temperature steps on the electrical characteristics of the Si substrate.

Finally, Section 1.5 tackles the stability of substrate performance with temperature. Because of the high power density of GaN circuits, it is important to understand the different mechanisms leading to change in ρ_{eff} and HD as the operating temperature increases.

1.2 GaN-on-Si technology for 5G and beyond front-end-modules

In this section, the necessary information is provided about GaN-on-Si technology. An overview of the different integration approaches is presented. Epitaxial growth, which has important influence on RF performance of the substrate, is discussed. The architecture of a high electron mobility transistor (HEMT) is briefly described with its functioning principle. Finally, some target applications for GaN-on-Si are important to mention as they determine the need for high-performance RF substrate.

1.2.1 GaN heterogeneous integration schemes

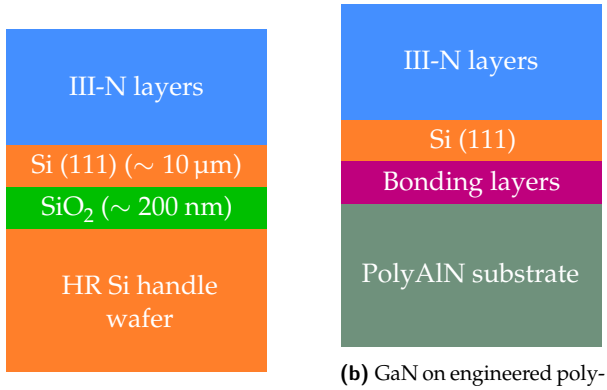
Because no bulk GaN substrates are available, RF GaN electronics have been enabled by heterointegration, i.e. integration of a GaN film on a different substrate. The earliest GaN HEMTs developped in the 1990's were integrated by heteroepitaxy on Al_2O_3 (sapphire) substrates [12]. The epitaxial route was pursued, and the substrate material was changed to SiC for its higher thermal conductivity allowing record power density, and finally to Si which constitutes the subject of this thesis. However, other integration schemes currently exist at various stages of maturity.

GaN-on-SOI

GaN HEMTs have been successfully fabricated by heteroepitaxy on SOI wafers, in which the top Si film ($\sim$ 10 µm-thick) is oriented in the (111) direction to allow a classical GaN-on-Si process flow [13], [14]. GaN-on-SOI (Fig. 1.1a) is an attractive approach from the vertical breakdown voltage, which is improved compared to a similar epitaxial stack on bulk Si. Furthermore, it offers potential compatibility with the excellent substrate performance of SOI. Indeed, a trap-rich layer could in theory be placed below the buried oxide. The thermal resistance introduced by the buried oxide is expected to be a point of concern for the high power densities offered by GaN.

GaN-on-engineered substrate

Another approach, developed by Qromis, consists in replacing the handle Si wafer by an engineered wafer made out of polycrystalline AlN (Fig. 1.1b) [15]. Here, the interest for RF lies in the ideal electrical properties of the AlN wafer and its high thermal conductivity. However, a Si film is still required for III-N epitaxy. This solution is currently mainly looked into for power GaN electronics, but could also support RF applications in the future.



(a) GaN-on-SOI

(b) GaN on engineered poly-AlN substrate

Fig. 1.1 Schematic representation of two alternative integration schemes for RF GaN.

GaN-on-(semi-)insulator substrates

GaN-on-SiC devices are currently boasting impressive high power performance at mm-wave frequencies and are the subject of the most advanced device optimization research [16], [17]. Because of the semi-insulating properties of the SiC wafer, the RF performance of the substrate is close to ideal [2]. Even though GaN-on-SiC constitutes the vast majority of commercially available GaN electronics, such semi-insulating materials will not be discussed in the rest of this thesis as they hold less scientific interest from the substrate loss and non-linearity perspective. This is also the case for insulator materials such as sapphire or diamond, where only dielectric losses can take place.

1.2.2 Epitaxial growth of GaN-on-Si substrates

GaN thin films can be grown on Si substrates using molecular beam epitaxy (MBE) or metalorganic chemical vapor deposition (MOCVD). The latter is seen as the method of choice for large-scale production due to its high growth rate and scalability. All experimental material in this thesis was grown using MOCVD. The wafers used are 200 mm, (111) high resistivity p-type (doped with B) Si wafers fabricated using the Czochralski (CZ) process. In MOCVD, the III-N layers are formed by the chemical reaction of two precursors in the vapor phase: one for the group-III component and NH_3 for nitrogen. For Al, the precursor is trimethylaluminum (TMAl). For Ga,

it is trimethylgallium (TMGa). The chemical reaction takes place at high temperature (800 °C to 1200 °C) and allows the growth of very thin layers [18]. Two main types of MOCVD reactors exist [19].

Vertical flow reactor. The gases are introduced directly above the wafers and thus flow vertically;

Horizontal flow reactor. The chemicals are introduced in the center of the chamber in close proximity to the wafers and then flow radially above the wafers. This type of reactor is branded as a planetary reactor by Aixtron.

In this thesis, GaN-on-Si samples are grown using a Veeco vertical flow reactor in imec's 200 mm fab, with the exception of the samples in Chapter 2 which are grown in a Aixtron G5 planetary reactor.

The MOCVD process is extremely complex and its complete description is out of the scope of this thesis. It however important to identify the main process parameters of importance for substrate performance.

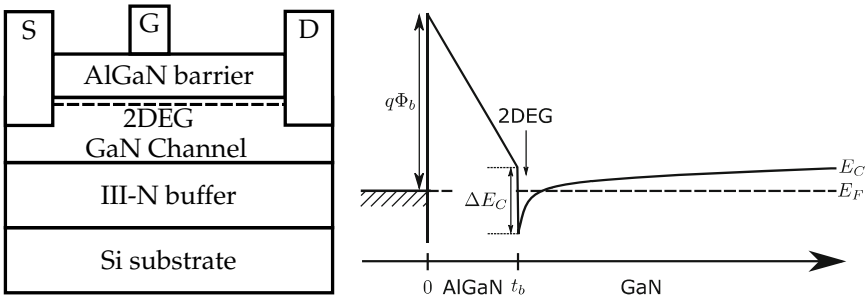
i. The process temperature can be tuned. Growth temperature has a significant impact on the epitaxial material quality [20], [21]. Furthermore, the thermal budget of MOCVD growth will be shown to be determining the amount of dopant diffusion in Si.

ii. The Si surface can undergo in-situ pretreatment before the growth starts. This treatment typically takes the form of the intentional flowing of one of the two precursors (e.g., TMAl) in the reactor chamber for a certain time.

Because of the large lattice constant mismatch between Si and III-N layers, significant strain builds up in the stack. This causes wafer bow and warp but can also lead to wafer breakage. Finally, it should be noted that processing HR (low-doped) Si wafers complicates the MOCVD growth. Indeed, Si wafers with low doping are known to be more brittle because dopant atoms can act as barriers that block dislocations. Consequently, 1.15 mm-thick Si wafers are used for improved mechanical stability, which is thicker than the industry standard of 725 µm.

1.2.3 GaN RF and mm-wave HEMTs

The fundamental building block of GaN circuits is the transistor, which takes the form of a HEMT. The cross-section of a typical device is shown in Fig.



(a) Schematic (not to scale) of a basic HEMT device.

(b) Band diagram of the AlGaN/GaN heterojunction. Reproduced from [1]. ©Spriner Nature 2020.

Fig. 1.2 The high electron mobility transistor is the basic building block for GaN circuits.

1.2a, with the corresponding band diagram in Fig. 1.2b. HEMT devices are based on the formation of a heterojunction between a barrier layer (AlGaN) and the GaN channel. The presence of surface states at the upper surface of the AlGaN barrier as well as the spontaneous and piezoelectric polarization difference between the two materials then gives rise to a 2-dimensional electron gas (2DEG) at the AlGaN/GaN interface [22], [23]. The 2DEG is present across the entire wafer and constitutes the channel of the transistor. Taking advantage of the field effect, it is possible to apply bias on the gate electrode (separated from the 2DEG by a barrier layer) to turn the transistor off. GaN HEMTs are depletion-mode, normally-ON devices by design. A lot of effort is spent on enabling enhancement-mode HEMTs, which are of high interest for RF circuits as they remove the need for a negative power supply, thereby reducing the design of the power amplifier circuit [24].

GaN HEMT devices show exceptional high-frequency and high-power performance. Indeed, the mobility in the undoped GaN material, saturation velocity and carrier density in the 2DEG is very high, allowing HEMTs reach outstanding cutoff frequencies. For instance, f_{MAX} values of more than 300 GHz have been reported for HEMTs on SiC substrates with 50 nm gate length in [16], and even above 500 GHz for more aggressive 20 nm devices in [25]. Recent developments in GaN-on-Si devices are approaching these values with f_{MAX} above 170 GHz in [26], [27] or even higher in [28]. The power density reaches 8 W/mm across a wide frequency band (until 94 GHz) for SiC substrates [17]. The current record for GaN-on-Si is getting competitive with SiC at 6.6 W/mm [27].

1.2.4 Target applications for GaN-on-Si

The attractive material properties of GaN make it a particularly relevant candidate for functional blocks such as the power amplifier, which benefits from the large power density and efficiency of GaN HEMTs (Fig. 1.3). Very little GaN-on-Si is currently commercially deployed, but the application space is predicted to grow [29].

Three frequency bands for future telecommunication generations are foreseen to be at least partially filled by GaN-on-Si [29], [30].

1. 5G frequency range 2 (FR2), or 5G mm-wave, with frequency bands around 28 GHz and 39 GHz.
2. 6G FR3 and bands around 8 GHz and 13 GHz.
3. FR1 or sub-6 GHz 5G, with bands between 3 GHz and 6 GHz

For telecommunication infrastructure, efficiency and linearity are the most important aspects. GaN-on-Si is competing with GaN-on-SiC for the realization of the power amplifier, where it could offer competitive performance at a lower cost.

In handsets, where cost and chip size are key, GaN-on-Si is expected to grow, also for the PA block. Here, the competing technologies are the well-established CMOS and GaAs platforms. GaN-on-Si can offer a higher power density and efficiency, which allows to reduce the footprint of the circuit, thereby also reducing RF parasitics (e.g. capacitance). For portable devices, the potential of integrating GaN devices alongside CMOS is also interesting [31].

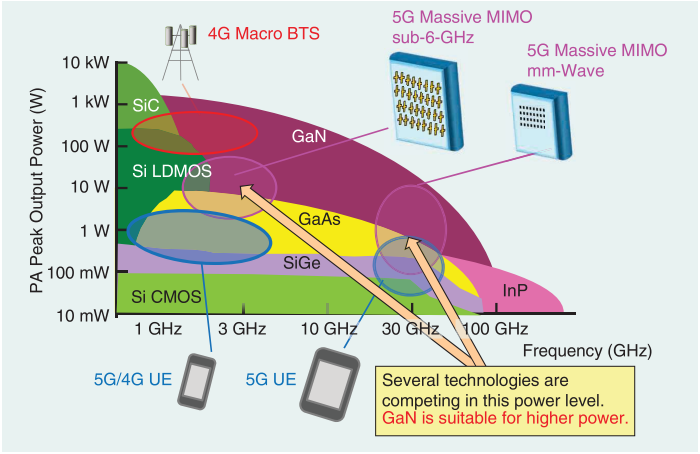


Fig. 1.3 Semiconductor technologies for 4G and 5G. The application space for GaN is at the high-power end of the spectrum. Reproduced from [32]. ©2021 IEEE.

1.3 Small- and large-signal characterization methodology

1.3.1 Substrate RF losses in CPW lines

In semiconductor technologies aimed at RF applications such as SOI or GaN-on-Si, circuits or devices can couple to the conductive Si substrate. At DC operation, such circuits are isolated from the conductive Si by the insulating Buried Oxide (BOX) or the semi-insulating III-N buffer for SOI or GaN-on-Si, respectively. However, as the frequency of the signals being processed increases, the impedance of those capacitive layers decreases and the substrate is being sensed by the overlying circuits. This conductive path leads to loss that can be detrimental to both active and passive devices:

- In RF switches, where a non-zero RF leakage current through the substrate can exist in the off-state [33];
- In Power Amplifiers (PA), RF power dissipation in the substrate can lead to a decrease of efficiency (see Chapter 4);
- In inductors, the quality factor can be degraded by a conductive path between the inductors traces [34];
- In coplanar waveguide (CPW) lines, RF current flowing from the signal electrode to the ground plane through the substrate causes insertion loss.

In this section, the focus is put on CPW lines, as they can also be used as a powerful characterization vehicle to precisely quantify the performance of the underlying substrate. The CPW line is a commonly used transmission line topology in modern monolithic microwave integrated circuits (MMIC's) [35]. On high resistivity substrates and at frequencies above a few hundreds of MHz, the CPW line functions in quasi-TEM mode and an infinitesimal section of it can be described by the equivalent circuit in Fig. 1.4. The general expression for the propagation constant of such a transmission line is given by Eq. 1.1 [36].

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)\,(G + j\omega C)} \tag{1.1}$$

When the loss is small, which is the case for most CPW lines studied in this thesis, the attenuation constant is given by 1.2, where $Z_0 = \sqrt{\frac{L}{C}}$ is the

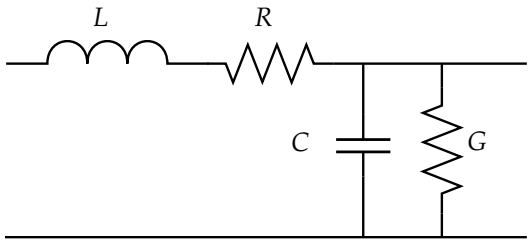


Fig. 1.4 Equivalent circuit of an infinitesimal length of transmission line.

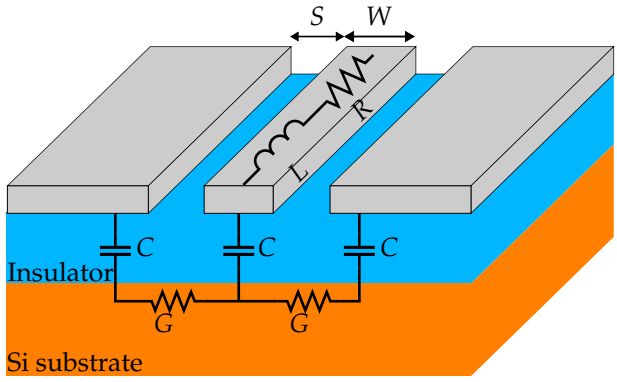


Fig. 1.5 Schematic representation of a CPW line and the equivalent circuit elements representing it. The important dimensions of signal conductor width (W) and slot width (S) are also indicated.

characteristic impedance of the line.

$$\alpha = \frac{1}{2}\left(\frac{R}{Z_0} + GZ_0\right) \tag{1.2}$$

Eq. 1.2 shows that there are two contributions to loss, as represented in Fig. 1.5:

- The resistive part (R), governed by the properties of the metal used to fabricate the line (thickness, width, material) and the skin effect;
- The conductive part (G), representing substrate losses.

While the attenuation constant can be readily extracted from measured S-parameters, it should not be used directly for characterizing substrate performance. Indeed, α contains the resistive component of loss R, and is

consequently dependent on the CPW processing. Isolating G is required for fair comparison.

1.3.2 Effective resistivity and parasitic surface conduction layer

Parasitic surface conductance in HR Si-based substrates

There are mostly two ways a PSC layer can originate in HR Si and decrease the ρ_{eff} of the engineered substrate.

Doping The most obvious way to decrease the resistivity of a semiconductor is to dope it. The PSC layer can be formed by parasitic doping, and this is the case for GaN-on-Si (see Section 1.4.2). Other possibilities include contamination by, e.g. B atoms.

Field effect Semiconductor substrates' carrier concentration depends on the local electric field. In engineered RF substrates, the field effect originates from the presence of charges in the dielectric or semi-insulating layers. This charge can take different forms (interface fixed charge, ionic charges, polarization charges, trapped charges at different locations). For SOI substrates, the main cause of degraded substrate performance is the unavoidable presence of a high density of fixed interface charges between SiO_2 and Si. Regarding GaN-on-Si, Chapter 2 discusses interface charges between AlN and Si. In Chapter 3, the importance of trapped charges in the III-N buffer will be shown.

Definition of the effective resistivity figure of merit

The effective resistivity (ρ_{eff}) figure-of-merit was introduced to overcome the limitations of α exposed in Section 1.3.1 [37], [38]. It is given by:

$$\rho_{eff} = \frac{F_{bot}(DIMS)}{G}, \tag{1.3}$$

in which G is the measured equivalent shunt conductance (see Fig. 1.4) and F_{bot} is a function of the CPW cross section. It represents the distribution of the field lines in the CPW structure and is originally used to separate the top and bottom contributions to the capacitance:

$$C = \varepsilon_0 \left(\varepsilon_{r,top} F_{top} + \varepsilon_{r,bot} F_{bot}\right) \tag{1.4}$$

F_{bot} is calculated using the closed-form expressions given in [39].

The benefit of using ρ_{eff} is illustrated in Fig. 1.6. The resistive part of the total loss α is effectively removed. Going a step further than sepa-

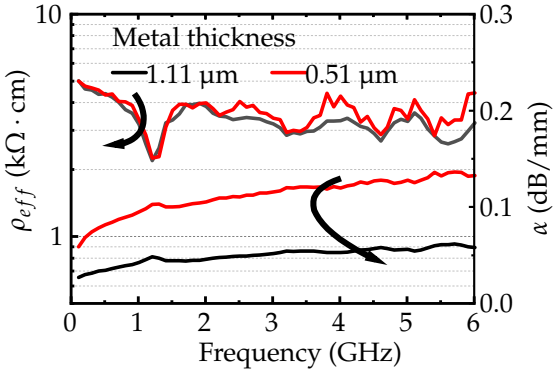


Fig. 1.6 Effective resistivity and insertion loss measured on two different CPW lines deposited on two identical GaN-on-Si substrates. The use of effective resistivity allows to probe the substrate loss independently of the CPW metal stack. Reproduced from [40]. ©2020 IEEE.

rating R and G, ρ_{eff} can be compared with the nominal resistivity of the HR Si wafer to assess the significance of any PSC layer. For a given CPW line cross-section (see below), ρ_{eff} also represents the resistivity of a homogeneous substrate leading to the same substrate loss as the physical non-homogeneous substrate. In that respect, it can also be used to simplify the material stack in an electromagnetic simulator.

Dimension dependence of ρ_{eff}

Because the F_{bot} factor in Eq. 1.3 is dependent on the dimensions of the CPW line, ρ_{eff} itself changes with dimensions. In Fig. 1.7, the impact of the spacing between the CPW signal and ground lines (S) is studied for different substrates and dielectric thicknesses (t_{diel}). Non-uniform Si substrates with higher conductivity at the surface (PSC layer), representing realistic Si after III-N growth are implemented in a model that will be described in Chapter 4. Realistic values for S range from 3 µm to 50 µm. ρ_{eff} is averaged in a frequency range where the quasi-TEM mode exists and which is relevant for FR2 and FR3 bands (5 GHz - 20 GHz).

For a relatively thin dielectric such as an AlN nucleation layer (dashed lines), ρ_{eff} decreases as S decreases. A smaller S translates into a shallower penetration of the electric field lines. Because the Si is more conductive close to the surface, the resistivity seen by the CPW line is smaller. For the thicker dielectric representing a complete GaN-on-Si stack (continuous

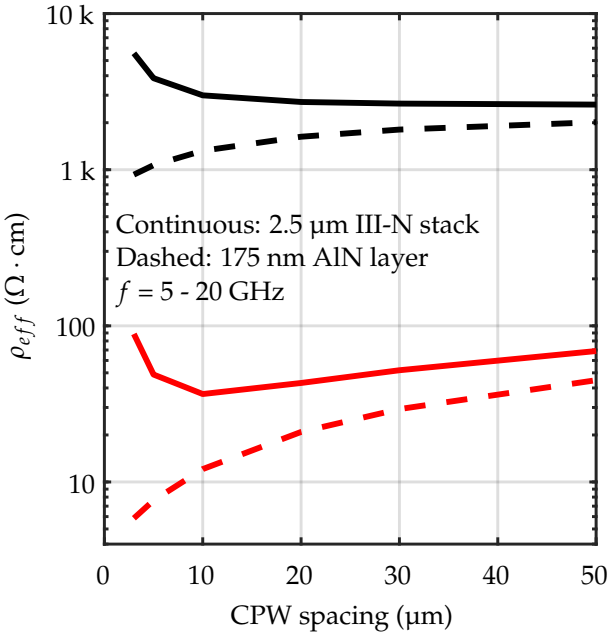


Fig. 1.7 Simulated dependence of effective resistivity on the dimensions of the CPW line, for two different dielectric thicknesses relevant to this work. Two different realistic doping profiles are considered to illustrate the case of a poor (red) and quasi-lossless (black) substrate.

lines), the same decrease of ρ_{eff} with decreasing S is observed until $S \approx 10$ µm. Then, ρ_{eff} increases. This can be explained by the thickness of the dielectric, which becomes comparable to S. In this case, the electric field lines are found in the highly resistive dielectric layer rather than in Si.

In general, a thicker dielectric also shows a higher ρ_{eff} for a given Si substrate, simply because the separation between the CPW line and the conductive substrate is larger. This effect is more noticeable for small spacings. In the rest of this thesis, the majority of the measured CPW lines will have $S > 30$ µm. The standard dimension set being used consist in a signal trace width of 85 µm and a signal-to-ground spacing of 50 µm. For such $S >> t_{diel}$, the effect of dimensions as well as dielectric thickness is limited.

1.3.3 Substrate-induced harmonic distortion

The complex modulation schemes used in present and future wireless FEMs imposes stringent requirements on the linearity of these systems. While some degree of non-linearity is induced by the active devices, the RF substrate can also significantly contribute [41]. Transmission lines are affected, but also also active components such as the RF Switch (see Chapter 4).

Semiconductor substrates are non-linear by nature. A CPW line is first considered. The concentration of free carriers contributing to the G (and, in a lesser extent, C) terms (Fig. 1.4) is dependent on the bias that is applied on the metal trace of the CPW line through the so-called field effect. If a large signal is to be transmitted, the semiconductor substrate sees a time-varying bias. Provided that the free carriers are given sufficient time to respond, their concentration will change as a response to the large signal. This leads to a modulation of G and generates harmonics: the substrate-induced harmonic distortion (HD).

Substrate HD is measured using a CPW line as test structure in a dedicated setup (Fig. 1.8). A fundamental tone is injected by a vector network analyzer (VNA) at the input of the CPW line. Because the output power of the VNA is limited and does not allow measurement of very linear substrates, an external amplifier is included in the path from the VNA to the DUT. After being amplified by the non-linear amplifier, band pass filters are inserted before the DUT input to ensure that no harmonics are present. A power calibration at the DUT input is then required. The power calibration is performed by connecting the input path (composed of cables, amplifier,

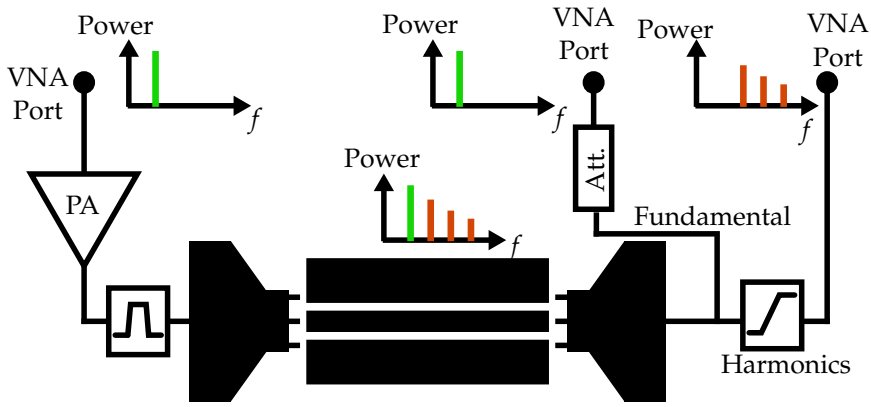
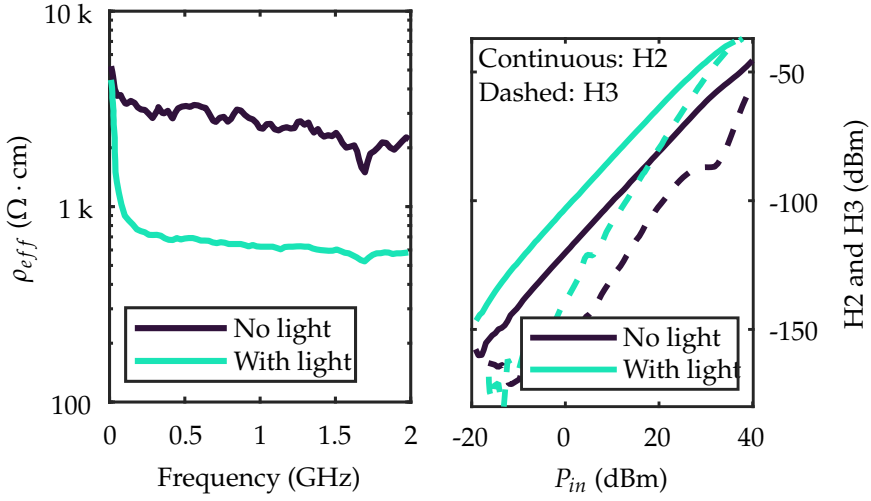


Fig. 1.8 Simplified schematic of the harmonic distortion measurement setup. Filters and internal VNA circuitry are omitted for clarity.

filters) to one of the VNA receivers. The RF power at the VNA output is then automatically adjusted by a feedback from the VNA receiver to account for the combination of losses and gain along the path. Furhermore, to correctly take into account the power loss occurring in the RF probes, subsequent calibration steps involving a coaxial and an on-wafer Thru standard are required. The procedure is described in detail in [42]. The fundamental tone at the output of the CPW line (H1), after being amplified by the PA and suffering a low amount of loss, is attenuated in a dedicated path to avoid damaging the VNA receptors. For adequate detection of the second and third harmonics (H2 and H3), a separate receptor is used without attenuator after filtering out H1. A simplified schematic of the resulting setup is shown in Fig. 1.8. The setup used in this work can achieve a maximum input power of $\sim$25 dBm at the device input and has a noise floor of ~ -120 dBm.

1.3.4 The influence of light on RF measurements

The RF measurements of GaN-on-Si samples are highly sensitive to ambient light, as shown in Fig. 1.9. A strong degradation of RF performance is seen when the sample is not protected from the light. This is caused by increased generation of free carriers in Si, which is assisted by light passing through the III-N layers. Consequently, all measurements in this thesis are performed under dark conditions, which will be the condition the substrate will be in when integrated in the package.



(a) Effective resistivity. A 3× decrease is observed under ambient light.

(b) Harmonic distortion. H2 and H3 are ∼20 dB higher when the measurement is performed in ambient light (continuous lines).

Fig. 1.9 The effect of ambient light on the RF measurement results. Due to carrier photogeneration, the substrate performance is significantly degraded in ambient light conditions. The sample is a GaN-on-Si stack where growth was stopped after the GaN channel. CPW dimensions are W/S=85 µm/50 µm. Courtesy of Incize.

1.4 Influence of process parameters on RF losses and non-linearities in GaN-on-Si substrates

In this section, the characterization methods described above will be used to quantify the substrate performance of GaN-on-Si stacks. First, the change in bulk Si conductivity during thermal cycling. The diffusion of Al and Ga atoms is then identified as one of the main causes for decreased substrate performance. The influence of a selection of key process steps is also studied.

1.4.1 Starting silicon wafer and thermal dopant activation

The use of high-resistivity Si as a handle wafer for RF application is well-established since extensive studies for SOI have shown significant reduction in crosstalk and substrate loss [4]. Similarly, HR Si has been used for the development of GaN-on-Si technology for RF applications (low-resistivity Si is favored in power electronics) [43], [44].

From a practical point of view, processing HR Si wafers is more complex than standard resistivity Si because HR Si is more brittle. Indeed, dopants act as obstacles for the propagation of dislocations that can cause breakage of the wafer. Since the epitaxy of III-N layer often induces strain and wafer bow or warp, the risk of breakage is higher. For this reason, thicker 1.15 mm HR Si wafers are preferred to the more commonly used 725 µm-thick wafers traditionally used in SOI. As the GaN-on-Si fabrication methods mature, the industry is currently aiming toward the use of 725 µm-thick starting Si wafers [45].

An important aspect of Si wafers in GaN-on-Si is the presence of interstitial oxygen (O_i) atoms. The crucible in which the Si is melted, made out of SiO_2, dissolves into the Si during the Czochralski process forming the ingot. A residual oxygen concentration is then found in Si. The concentration is usually in the order of 1 to 20 parts per million atoms (ppma).

When the material is kept at temperatures in the range of 300 °C to 500 °C, these O_i can form clusters of a few (1-4) oxygen atoms, which become electrically active as thermal donors (TDs). These donors act as n-type dopants. The wafer always spends some time in the critical temperature range during MOCVD or further processing, such that a certain degree of TD activation always occurs. In HR Si, a high O_i concentration ($[O_i]$) can cause the subsequent n-type doping to dominate over the low intentional p-type doping and flip the polarity of the substrate. This will become apparent

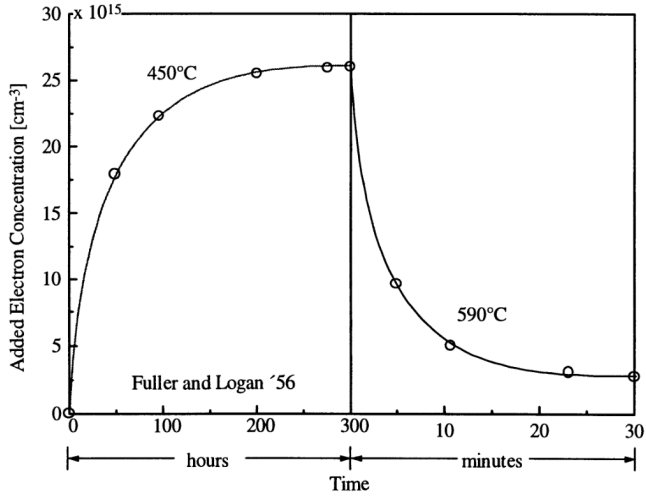


Fig. 1.10 Evolution of the added electron concentration by TD activation as a function of time (i) in the critical temperature range for activation and (ii) in the deactivation annealing temperature range. Reproduced from [46].

in Fig. 1.13. To dissolve the O_i clusters and deactivate the TDs, it is possible to anneal the wafer at a temperature of 600 °C to 650 °C and then cooling it relatively quickly to avoid re-formation. The activation and subsequent suppression of TDs is shown in Fig. 1.10. The formation rate of TDs is dependent on $[O_i]$, such that a controlled $[O_i]$ is desirable to prevent TD activation in the time of processing [47], [48].

1.4.2 Thermal budget and III-N epitaxy

The epitaxy of the nitride layers on the Si wafer is critical for RF loss. One of the main contributions to the formation of the PSC layer originates during epitaxial growth.

During this high temperature (above 1000 °C) process, Al and Ga atoms can diffuse into the Si close to its surface. Evidence of this diffusion has been widely reported in literature using secondary ion mass spectroscopy (SIMS) performed from the backside of the substrate. An example is displayed in Fig. 1.11. The quantity of diffused Al exceeds the Ga level by approximately one order of magnitude because Ga is only introduced after the growth of the AlN nucleation layer and cannot easily diffuse through this layer.

Since Al and Ga are group 3 elements, they can act as p-type dopants. If

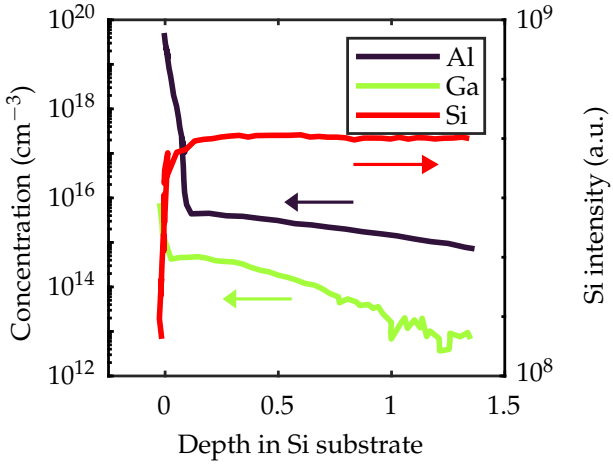


Fig. 1.11 SIMS evidence of Al and Ga diffusion in the Si substrate after the growth of the III-N epitaxial stack until the GaN channel. The detection limit lies at a concentration of 1×10^{13} cm^{-3}. Reproduced from [49].

Stack	Total III-N thickness	AlN thickness
A	$\sim 2.535\,\mu$m	200 nm
B	$\sim 2.505\,\mu$m	175 nm
C	$\sim 1.305\,\mu$m	175 nm

Table 1.2 Description of the three GaN-on-Si stacks considered for the comparison of Al and Ga diffusion.

their concentration close to the surface is higher than the B-doping in the bulk, the parasitic doping gives rise to a PSC layer. It is demonstrated in [49] that a majority of the diffused atoms become electrically active dopants.

An increased diffusion leads to a more conductive PSC layer and a degraded substrate performance. The diffusion in influenced by many different factors, such as thermal budget, AlN nucleation layer, or MOCVD growth conditions.

To isolate the contribution of epitaxy, three different epitaxial GaN-on-Si stacks are considered. The stacks are described in Table 1.2. The growth is stopped after the GaN channel and before the AlGaN barrier which would form the HEMT heterojunction and 2DEG, completely dominating the substrate conductivity over Si. Further HEMT processing steps will be considered in Section 1.4.3. They are all grown on B-doped 200 mm 3-6

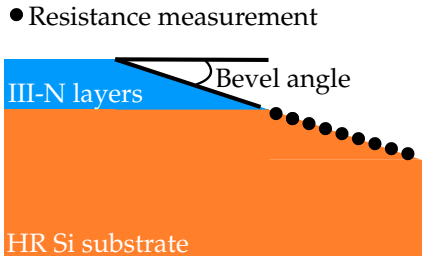


Fig. 1.12 Schematic of the spreading resistance profiling technique. The bevel angle is usually very shallow ($< 0.05°$) to allow a high depth resolution.

$k\Omega \cdot cm$ Cz-Si wafer in a Veeco MOCVD reactor.

The method of choice to characterize the spatial distribution of dopants in a semiconductor material is Spreading Resistance Profiling (SRP). The technique is represented schematically in Fig. 1.12. By cutting the surface of the wafer at a shallow angle, it allows to measure both the polarity (p-type or n-type) and the resistivity of Si as a function of depth.

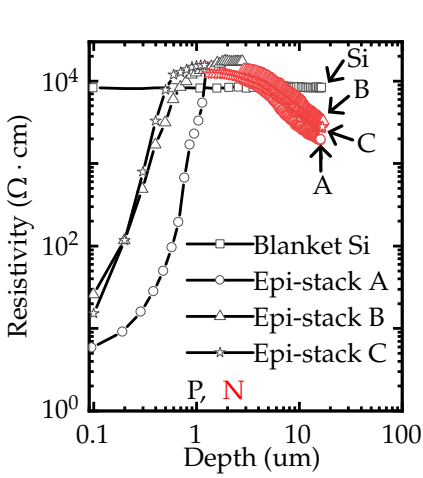
The SRP profiles of the three different GaN-on-Si stacks and their corresponding ρ_{eff} is shown in Fig. 1.13.

All epitaxial stacks show conductivity type inversion in the bulk. Originally p-type, the Si wafers flips to n-type after TD activation during the thermal cycling. This leads to the formation of a weakly doped p-n junction close to the Si surface.

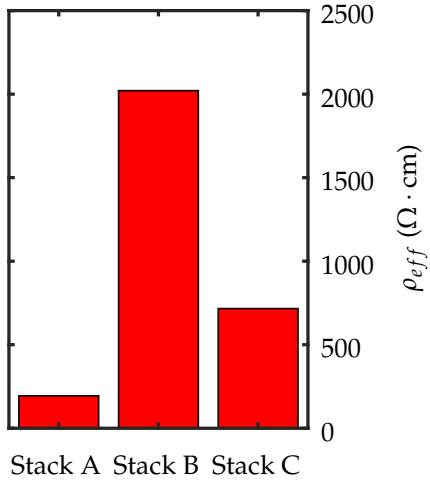
Epitaxial stack A clearly shows a higher surface doping than the two other stacks. This is reflected in its degraded surface performance. It should be noted that stack A and stack B present a comparable buffer thickness, but the process for stack B has been optimized to limit the total thermal budget, more specifically the AlN nucleation layer has been optimized (see Chapter 2). Epitaxial stack C shows a well-controlled diffusion, similar to stack B. However, its substrate performance is slightly degraded. This can be attributed to a combination of two factors:

1. A closer proximity of the CPW line to the PSC layer due to a thinner buffer and (see Fig. 1.7);
2. A higher [O_i] leading to higher TD activation. The latter factor slightly degrades the resistivity in Si bulk, which can cause a decrease in ρ_{eff}.

Once the epitaxy has been optimized to limit Al and Ga diffusion in Si, subsequent processing steps can influence the overall substrate performance. This is discussed in the following sections.



(a) Spreading resistance profiles of the starting Si wafer and of the Si wafer after MOCVD growth of the three epitaxial stacks. Depth is counted from Si surface. Reproduced from [40]. ©2020 IEEE.



(b) Effective resistivity for the three epitaxial stacks, averaged over a few frequency points around 2 GHz W/S=85 µm/50 µm.

Fig. 1.13 Spreading resistance profiling in GaN-on-Si substrates, providing evidence of Al (and Ga) diffusion close to the Si surface and acting as p-type dopants to form the PSC layer.

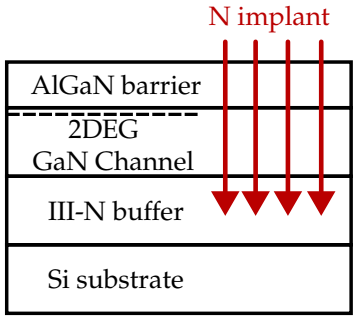


Fig. 1.14 Schematic representation of the ion implantation step used to suppress the 2DEG where it is not needed.

1.4.3 HEMT processing

Once the III-N layers (including the AlGaN barrier forming the 2DEG) have been grown, further steps are required to fabricate functioning HEMTs. These steps can impact the substrate performance. The implant performed to isolate the devices and the rapid thermal annealing of the metallic contacts are considered.

Isolation implant

In wide bandgap semiconductors, isolation of HEMTs is most often achieved using ion implantation (Fig. 1.14). In the case of GaN-on-Si, nitrogen ions are implanted at high energy and suppress the 2DEG in regions where isolation is required [50]. In imec's process, this implantation is performed in three successive steps after the growth of the AlGaN barrier [51]:

I. 75 keV and a dose of $8 \times 10^{12}\,\mathrm{cm}^{-2}$
II. 150 keV and a dose of $2 \times 10^{13}\,\mathrm{cm}^{-2}$
III. 375 keV and a dose of $3 \times 10^{13}\,\mathrm{cm}^{-2}$

The implant can be accurately simulated using the TRIM software [52]. The results are displayed in Fig. 1.15. The defects caused by the N implant are reaching a depth of $\sim$ 600 nm from the AlGaN surface. No defect formation is expected in the Si substrate, which lies more than 2 µm from the AlGaN surface. Still, the implant can affect substrate performance. As shown in Fig. 1.16, the successive implantation steps slightly degrade ρ_{eff}. This is attributed to the high concentration of defects in the upper III-N layers which create additional charge, analogously to an added oxide charge in

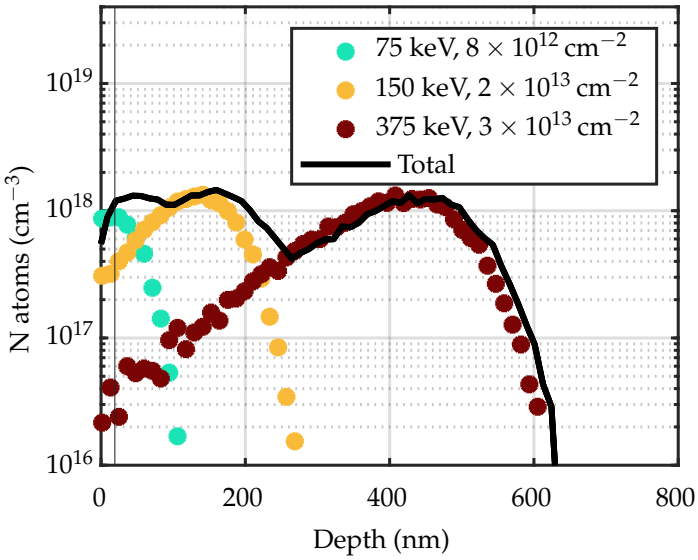


Fig. 1.15 Simulated nitrogen ion concentration as a function of depth from the AlGaN barrier surface. The considered barrier thickness is 19 nm (indicated by the vertical line), under which 1 µm of GaN is used to represent the channel and CGaN buffer layers

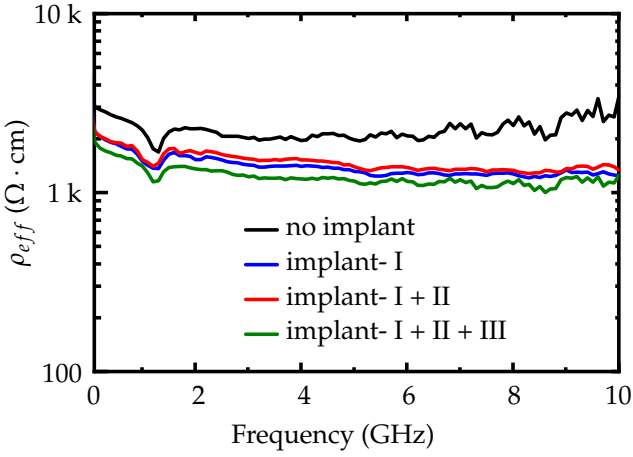


Fig. 1.16 Effective resistivity measured on four separate samples representing the successive N ion implantation steps. Reproduced from [40]. ©2020 IEEE.

Wafer Name	Resistivity (kΩ · cm)	[O_i] (ppma)
HRS-1	3-6	unspecified (likely > 5 ppma)
HRS-2	7.53	3.8
HRS-3	4.30	3.0

Table 1.3 Different Si wafers used for the study of the impact of thermal annealing on substrate performace.

SOI. The PSC layer is more conductive leading to more RF loss. ρ_{eff} is most degraded for the full implant (steps I, II and III). However, using only steps I and II leads to no further decrease in ρ_{eff} compared to step I.

The combination of steps I and II also leads to the best HD performance. This can be understood from the bias dependence of the G parameter, which is linked to HD (this is mostly correct for implanted regions which show limited time-dependent effects, see Chapter 3). For implants I and II, G shows almost no bias dependence in the -35 V to 20 V range.

Thermal annealing

After the isolation implant, the fabrication of metal contacts is another important step in the fabrication of HEMT devices. These steps involve deposition of dielectric layers and rapid thermal annealing (RTA) to form high-quality ohmic contacts [53]. The RTA step is performed at a temperature of 565 °C. Because this temperature is close to the TD annihilation temperature (see Fig. 1.10), it is important to study the effect of RTA on Si resistivity, which impacts substrate performance.

To do so, three different Si starting wafers are considered, all of which underwent MOCVD growth of the epitaxial stack B (see Table 1.2), i.e. without the AlGaN barrier. Their important parameters are noted in Table 1.3. After growth, they are cut and separate pieces are subjected to RTA (90 s) at temperatures of 400 °C, 500 °C and 600 °C. The averaged ρ_{eff} after RTA are show, in Fig. 1.17. For all samples, ρ_{eff} is degraded by the 400 °C RTA. Since this temperature is in the range of TD activation temperatures, the RTA can cause more oxygen atoms to form clusters and dope the bulk Si, making it more n-type and decreasing ρ_{eff}. Wafers HRS-2 and HRS-3 show a relatively temperature independent ρ_{eff} degradation after the 400 °C, 500 °C and 600 °C RTA. Possibly, a certain degree of TD annihilation can takes place at these more elevated temperatures. For Wafer HRS-1, the higher [O_i] leads to more efficient TD activation and increased doping.

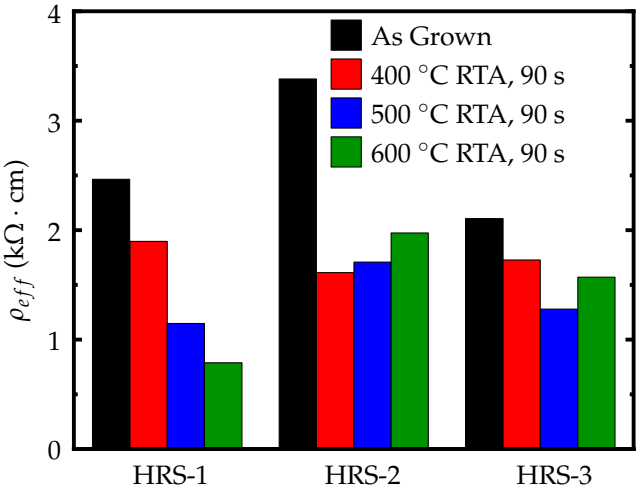


Fig. 1.17 Effective resistivity averaged from 0.9 to 5.11 GHz for epitaxial stack B grown on different Si wafers and subjected to different rapid thermal annealing conditions. Reproduced from [40]. ©2020 IEEE.

1.4.4 Benchmarking substrate performance

The performance of a given substrate can be quantified by the combination of its ρ_{eff} and HD. These two quantities are usually correlated [54]. Indeed, for ρ_{eff} values above a few tens of $\Omega \cdot$ cm, a more resistive substrate will have less free carriers that can be modulated by the large-signal bias. The two figures of merit (FOM) only depend on the CPW cross-section dimensions, so it is possible to fairly compare substrate technologies with each other by characterizing them using a common standard CPW line. The GaN-on-Si substrates are benchmarked against state-of-the-art SOI substrates in Fig. 1.18.

The SOI samples contain trap-rich SOI substrates fabricated in a university environment (TR SOI), SOI substrate without trap-rich layer (HR SOI) and commercially available RFeSI substrates ([54], [55]). GaN-on-Si substrates are all fabricated using imec's process, with the exception of one existing reference [2]. Both fully processed stacks and stacks where MOCVD growth is stopped after the GaN channel are included. The CPW line dimensions are chosen to be comparable.

Owing to dopant in-diffusion limiting and buffer engineering [20], [21], imec's GaN-on-Si substrates are reaching competitive performance compared to the state of the art in terms of substrate performance. GaN-on-SiC,

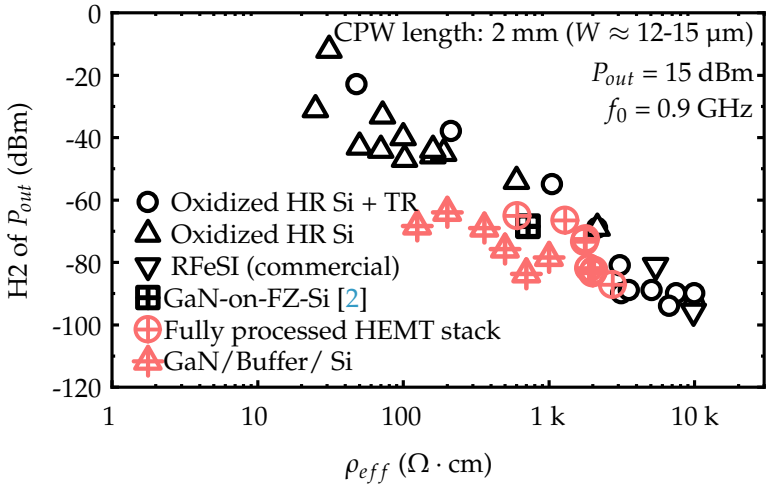


Fig. 1.18 Benchmark of imec's GaN-on-Si substrate performance. Fully processed HEMT stacks are reaching low levels of distortion and high effective resistivity comparable to trap-rich (TR) SOI substrates.

which is not displayed here but is measured in [2], presents a H2 below -105 dBm (noise floor) and cannot be placed on Fig. 1.18.

1.4.5 Known limitations of the substrate performance figures-of-merit

ρ_{eff} and H2 are well-established figures-of-merit in the SOI world for almost 20 years. State-of-the-art SOI substrates for RF applications typically present little variation in the thickness of their buried oxide: 0.2 µm to 0.4 µm SiO_2 films constitute the majority of the substrates found in literature for RF. Furthermore, the cause for degraded ρ_{eff} in SOI is always the presence of positive fixed charges at the Si/SiO_2 interface, which means that the free carrier distribution in Si does not vary significantly from sample to sample. In that sense, ρ_{eff} and H2 can be linked quite easily to physical parameters such as the density of oxide interface charges[1].

The application of these CPW metrics to GaN-on-Si exposes some of their limitations. Some of the shortcomings stem from the dimension dependence shown in Fig. 1.7.

- For a given conductivity of the PSC layer, increasing the thickness of

[1]This is true in the absence of a trap-rich layer. Whenever such a layer is included, its properties (trap density and distribution) cannot be determined from CPW measurements.

the III-N layers will improve the FoM without actually modifying the conductivity of the substrate. This is especially true for CPW spacings comparable to the III-N thickness.

- A fair comparison between different substrate technologies requires a choice of a standard CPW line.

Another drawback arises from the complex nature of the GaN-on-Si stack.

- Depending on the process conditions and thermal budget, the free carrier distribution can vary drastically and have different origins. The CPW FoM do not give any indication about the extent of the PSC layer into the Si substrate or the presence of any charges in the III-N layer.

In this thesis, whenever GaN-on-Si substrates are compared with Si/SiO_2-based substrates, a standard CPW is used with a signal line width and slot width of $\sim 26\,\mu m$ and $\sim 12\,\mu m$, respectively. To elucidate the extent of the PSC layer and its contributions, the CPW metrics are not sufficient and other techniques are required such as SRP or capacitance-based measurements (see Chapter 2).

1.5 Temperature dependence of substrate performance

GaN HEMTs stand out for their power density [56]. For GaN-on-Si, the current record for a 150 nm-long device is a saturated output power of 6.6 W/mm at a drain voltage of 20 V and operating frequency of 28 GHz [27]. At the same time, the efficiency of this device is $\sim$ 40 %. One of the main challenges of GaN-on-Si is the low thermal conductivity of Si ($\sim$ 150 $W \cdot m^{-1} \cdot K^{-1}$) compared to traditional substrates such as SiC ($\sim$ 490 $W \cdot m^{-1} \cdot K^{-1}$). The lower thermal conductivity of the substrate leads to an increased self heating of the device, but also to an increase in temperature in the region below the device. In this section, the impact of an increase of temperature on substrate performance is discussed.

1.5.1 Physical origin of the temperature dependence

To illustrate the different physical phenomena at play, a simple 1-D structure is considered in a TCAD environment. It consists of a HR-Si substrate with a background doping of $1.7 \times 10^{12}\,cm^{-3}$ (p-type), corresponding to $\rho = 7.5\,k\Omega \cdot cm$. An additional surface doping (p-type) is included close to the Si surface to form a PSC layer. The doping profile is taken from SRP measurements (Section 1.4). A 2.505 µm-thick insulator with a permittivity corresponding to the equivalent permittivity of the III-N stack is added. No fixed charge or traps are included in the simulation. The temperature is increased from 50 °C to 200 °C, representing realistic values of operation temperature. The Lombardi model is used to model the mobility in Si [57]. It models the doping (impurity scattering) and temperature (phonon scattering) dependence of mobility.

The resulting resistivity profiles are shown in Fig. 1.19. Resistivity is calculated as:

$$\rho(y) = \left(q\left(\mu_p(y)p(y) + \mu_n(y)n(y)\right)\right)^{-1}. \tag{1.5}$$

Several observations can be made.

- Far from the Si surface, the resistivity significantly decreases with temperature. More than one order of magnitude difference is seen between the simulations at 50 °C and 200 °C.
- Close to the Si surface, a non-monotonous change of resistivity seems to take place, with first an increase in resistivity then, at 200 °C, a decrease.

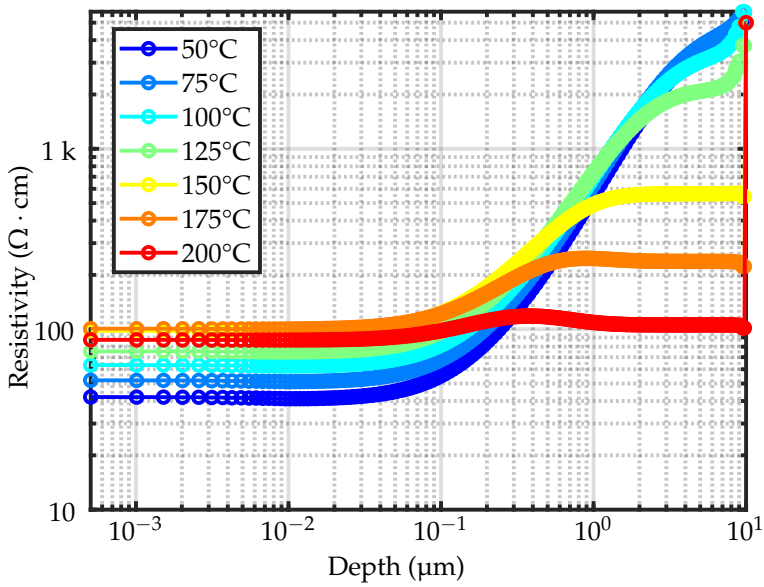


Fig. 1.19 Simulated resistivity profiles for increasing temperature. Different trends are observed close to the Si surface or in the Si bulk. The background doping is set at $1.8 \times 10^{12}\,\mathrm{cm}^{-3}$ and the Al parasitic doping profile is included in the first few micrometres of Si.

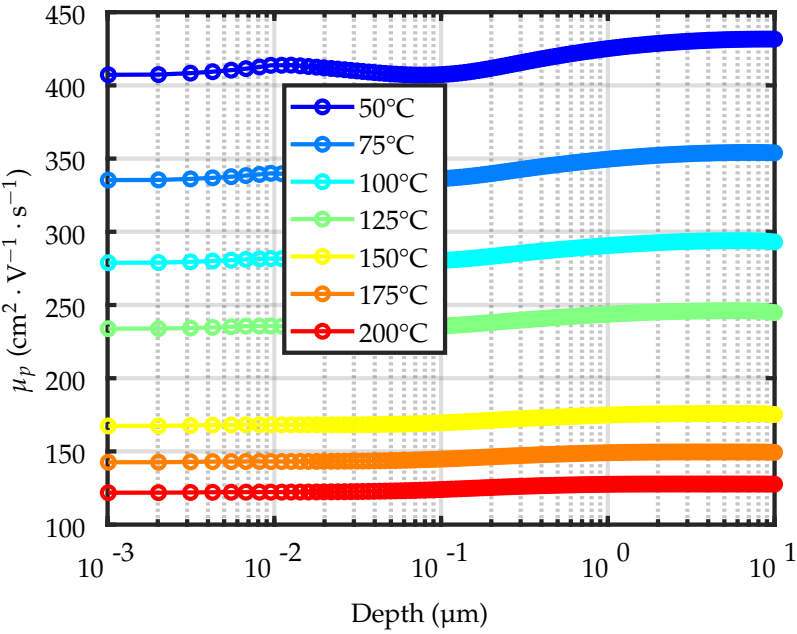


Fig. 1.20 Simulated hole mobility as a function of depth from the Si surface for different temperatures.

Mobility decrease

The hole mobility (main contributors to ρ in a p-type wafer) is plotted in Fig. 1.20. The doping considered here is lower than $1 \times 10^{16}\,\mathrm{cm}^{-3}$. Mobility reduction by impurity scattering is negligible for such low doping values, which explains why there is little variation of μ_p with depth. A significant reduction of μ_p with temperature is however present, and is caused by scattering with phonons. μ_p decreases from $\sim 400\,\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$ at 50 °C to $\sim 120\,\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$ at 200 °C. The temperature dependence of μ_p is modelled in the Lombardi model as follows:

$$\mu_p(T) = \mu_{p,300} \left(\frac{T}{300} \right)^{-2.2} . \tag{1.6}$$

Carrier concentration increase

In addition to mobility decrease, the free carrier concentration is also affected by temperature. The simulated hole concentration is displayed in Fig. 1.21. While the surface hole concentration is only slightly affected, an

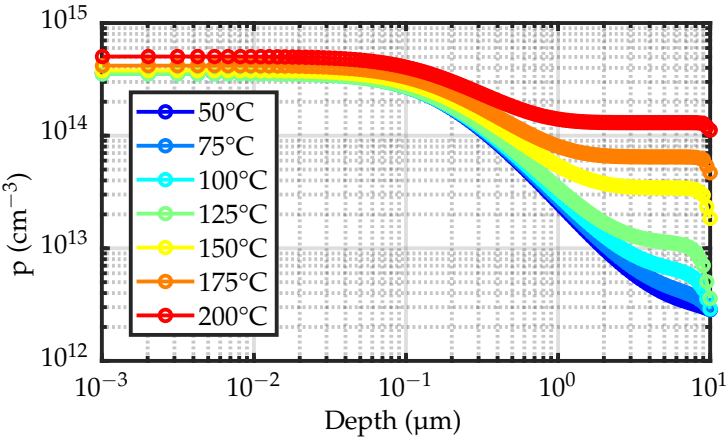


Fig. 1.21 Simulated hole concentration as a function of depth from the Si surface for different temperatures.

increase of almost two orders of magnitude in p is observed far from the Si surface. At thermal equilibrium, the intrinsic carrier concentration is given by:

$$n_i = M_C^{1/2} T^{3/2} \exp\left(-\frac{E_g}{2kT}\right), \tag{1.7}$$

in which M_C is number of equivalent minima in the conduction band and E_g the bandgap energy. n_i is $\sim 1 \times 10^{10}\,\mathrm{cm}^{-3}$ at room temperature and increases exponentially to $\sim 2 \times 10^{14}\,\mathrm{cm}^{-3}$ at 200 °C. When n_i exceeds the hole concentration imposed by the doping in the bulk Si, p increases to respect the relation $pn = n_i^2$. Since doping is very low in the bulk, p almost follows the increase of n_i.

The increase in bulk hole concentration has the largest effect on resistivity (exponential dependence versus quadratic dependence on temperature for μ_p). Indeed, from Fig. 1.19 it is clear that ρ changes more in the bulk than close to the surface.

Overall, the different contributions to the resistivity change with temperature are summarized in Fig. 1.22. For low doping, the n_i increase kicks in at relatively low temperatures. For higher doping, μ first degrades, increasing ρ. Then, at a higher temperature, the n_i increase starts to dominate.

Simulated effective resistivity

The 1-D simulated resistivity profiles are used in a 2-D small-signal simulation of a cross-section of a CPW line. The extracted G is converted to ρ_{eff}

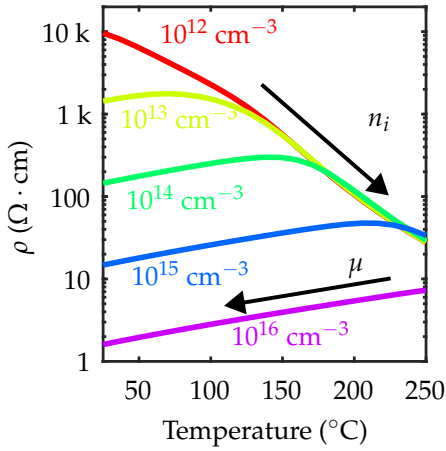


Fig. 1.22 Temperature dependence of resistivity for different doping concentrations. The combined effects of mobility and intrinsic carrier number are visible.

following Eq. 1.3. The results, taken at 5 GHz, are displayed in Fig. 1.23.

Until 100 °C, ρ_{eff} slightly increases. This can be explained by an already significant decrease in μ_p, but negligible increase in p. At higher temperatures, ρ_{eff} drops to $\sim 100\,\Omega \cdot$ cm. This is caused by the strong increase in n_i in the bulk Si. In order to maintain substrate performance, the temperature in Si should not increase above 125 °C.

The simulated temperature trend differs from the measured evolution of ρ_{eff} with temperature, which is shown in 1.24. First, no initial increase in ρ_{eff} is observed at moderate temperatures. Secondly, the drop observed at 150 °C in the simulations already occurs at 125 °C in the measurements. These discrepancies could be due to interface traps, which are not considered in the simulation but would affect the evolution of mobility with temperature. Furthermore, the bulk Si doping in the measured substrate could be slightly different from the simulated one.

1.5.2 Estimation of the temperature increase

A 2-D thermal simulation in a dedicated simulation framework is performed to estimate the substrate temperature [58], [59]. A realistic III-N stack with a 1.15 mm-thick Si substrate is considered and the chuck temperature is fixed at 25 °C. Thickness dependence of the cross-plane thermal conductivity of the III-N materials is accounted for by solving the Boltzmann transport equation. The results for different DC power densities are shown in Fig.

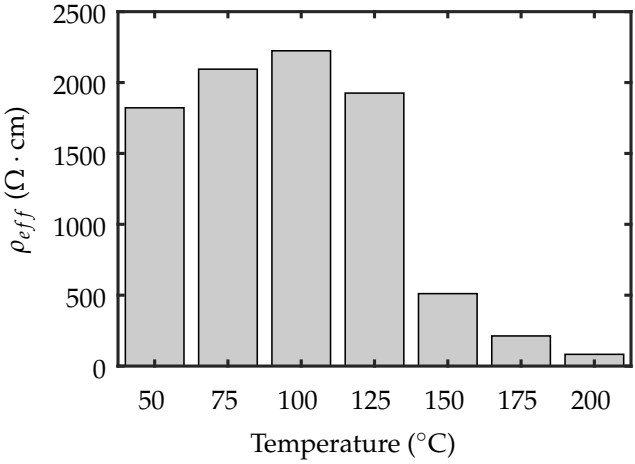


Fig. 1.23 Simulated effective resistivity using the resistivity profiles of Fig. 1.19. CPW dimensions are: a central conductor width of 85 µm and slot width of 50 µm. Data is taken at 5 GHz. Total III-N thickness: 2.505 µm.

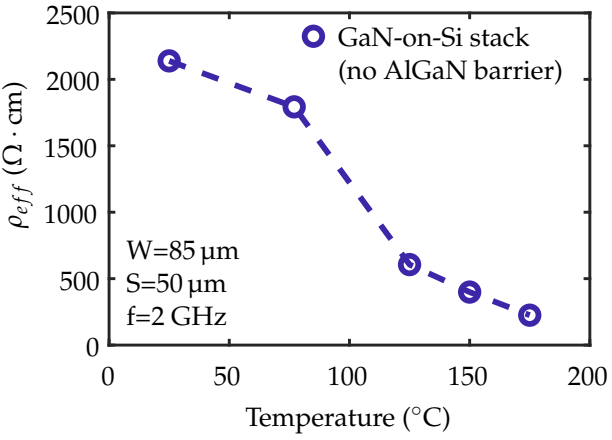


Fig. 1.24 Measured effective resistivity as a function of chuck temperature. Total III-N thickness: 2.505 µm. The DC bias is set to 0 V.

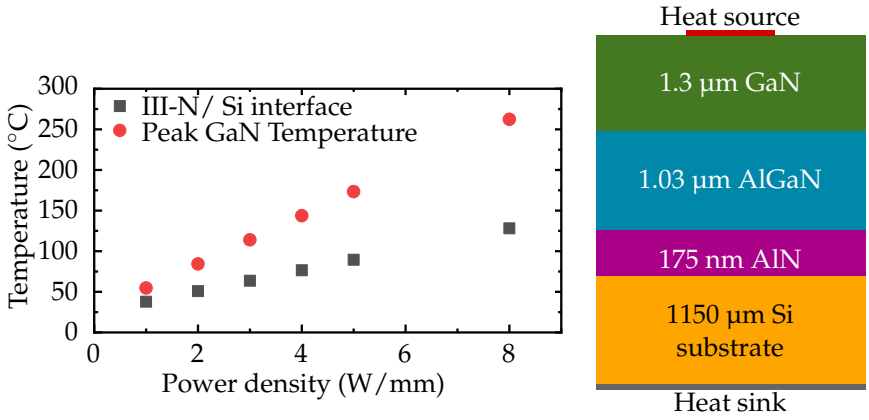


Fig. 1.25 Simulated temperature increase at the HEMT level and at the surface of Si for a realistic GaN-on-Si stack. Results reproduced from [40]. ©2020 IEEE.

1.25.

While the GaN close to the device can heat up to above 200 °C, the thick buffer allows the temperature at the III-N/Si interface to stay limited. Indeed, even for power densities close to the record of 6.6 W/mm [27], the temperature stays below 100 °C. However, if the power density of GaN-on-Si further improves to 8 W/mm, thermal management will become an issue as substrate performance is predicted to degrade.

Thermal simulation and characterization of III-N epitaxial stacks is out of the scope of this thesis, but valuable insights can be found in [59]. In particular, it is predicted that the temperature mostly drops across the 1.03 µm-thick superlattice strain relief buffer which presents the largest thermal resistance of all layers. Comparatively, the remaining temperature drop across the thick Si substrate is low. The thinning down of the substrate before packaging will therefore only have a limited impact on the results of Fig. 1.25. Conversely, the thinning down of the superlattice strain relief buffer could increase the temperature at Si surface.

1.5.3 Experimental evidence of H2 and effective resistivity variation

Fig. 1.26 shows the measured H2 power as a function of temperature for a GaN-on-Si sample without 2-DEG and a full HEMT stack. H2 stays at acceptable levels (below -80 dBm) for both samples until 100 °C then degrades significantly. This is in good agreement with the predicted ρ_{eff} evolution of Fig. 1.23.

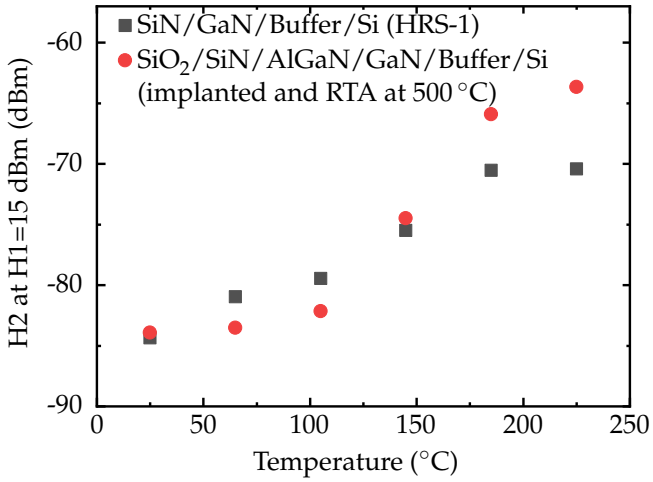


Fig. 1.26 Experimental evidence of second harmonic power variation with temperature. Reproduced from [40]. ©2020 IEEE.

1.6 Chapter summary

In this first chapter, the substrate-related parasitic effects were analyzed from the angle of the semiconducting HR Si substrate, which is where parasitic conductivity takes place in the form of a PSC layer.

After briefly presenting the technological distinctiveness related to GaN-on-Si, the RF characterization techniques for quantifying Si-based RF substrates' performance were introduced. ρ_{eff} was shown to be a better small-signal FOM than insertion loss, and the measurement of RF harmonic distortion was explained. Still, these two quantities are dependent on the CPW cross section dimensions, which is why a standard line must be used for benchmarking.

Then, the impact of important process steps was discussed. The diffusion of Al and Ga atoms was shown to be the key contributor to RF loss. Further, the thermal budget of MOCVD or RTA steps, can lead to TD activation, which effects the substrate performance by doping the Si. The isolation implant, which is performed under passive structures, also has an electrical effect although it does not penetrate Si. The large number of defects formed by the implanted N ions appears to create charge which changes the ρ_{eff}.

Finally, the temperature dependence of the Si substrate and the PSC layer was explained. Because GaN circuits are expected to dissipate large amounts of heat, the substrate performance must be stable at high temperature. It was shown that the PSC layer and the bulk Si are governed by mobility decrase and n_i increase respectively. For high-performance GaN-on-Si substrates ($\rho_{eff} > 1\,\mathrm{k\Omega \cdot cm}$), the ρ_{eff} and HD were shown to be stable until $\sim$100°C, which is sufficient for power densities up to $\sim$6 W/mm.

2

Electrical study of AlN/Si interface

2.1 Introduction

The first epitaxial layer of the GaN-on-Si stack to be investigated is the AlN nucleation layer. Its main role is to prevent meltback etching of the Si substrate by Ga. In the early stages of GaN-on-Si development, is has been noticed that direct growth of GaN on Si caused Ga-rich droplets to etch into the Si at high temperature, resulting in polycrystalline material instead of the desired monocrystal. To improve the termal stability of GaN, the inclusion of an AlN nucleation layer proved to be an effective solution [60], [61]. Furthermore, AlN has a smaller lattice mismatch with GaN compared to Si.

The AlN nucleation layer strongly affects the breakdown voltage of the GaN-on-Si stack, as well as the crystalline quality of the subsequent III-N layer [62]–[68]. The growth temperature and the pretreatment of the Si surface are two particularly impactful process parameters.

Together with the development of a high-quality AlN layer, the formation of a parasitic conductive channel channel at the interface between AlN and Si has been noticed and linked to a degraded substrate loss. A lot of attention has been given to the identification of the factors leading to the

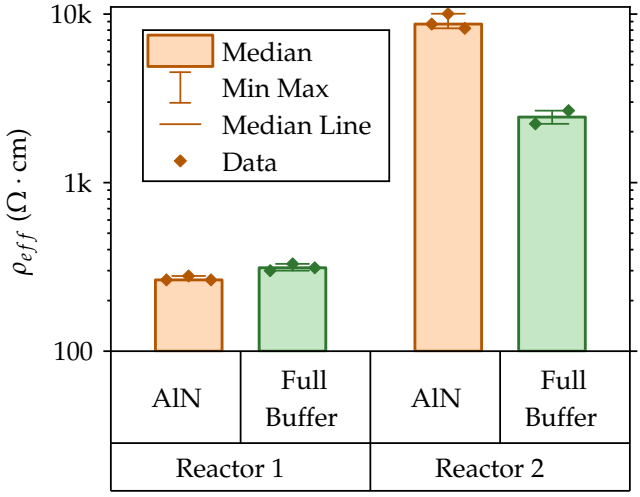


Fig. 2.1 Effective resistivity (averaged between 1 GHz and 5 GHz) for AlN and full buffer stacks grown in different MOCVD reactors. The effective resistivity of the AlN-only stack and the full GaN-on-Si buffer stack are correlated: the substrate performance of an AlN/Si structure is determining the performance of the full stack. W/S = 85 µm/50 µm.

PSC layer [44], [49], [67], [69]–[75]. Indeed, the growth of the AlN layer is seen as the determining process step in terms of substrate loss. This is exemplified in Fig. 2.1 for samples grown in different reactors and in Fig. 2.2 for different AlN growth temperatures. When the nucleation layer is not well optimized (i.e., the AlN/Si stack shows a low ρ_{eff}) as in Reactor 1, the substrate performance cannot be recovered by the subsequent growth of the III-N layers. Conversely, a high ρ_{eff} for AlN/Si (Reactor 2) translates into good substrate performance for the full stack. The simple AlN/Si structure thus determines the full GaN-on-Si stack substrate performance. Therefore, its study and the engineering of its substrate performance are of highest importance.

As discussed in Chapter 1, one leading cause is the diffusion of Al atoms which dope the Si [69]. However, when the doping is kept under control (through e.g. low temperature AlN growth), a PSC layer can still form. The process conditions leading to a reduced diffusion are out of the scope of this thesis, but more information can be found in [20], [21], [69]. The polarity of the PSC layer is controversial, and seems to depend on the precise process conditions in the MOCVD reactor: a n-type layer has been

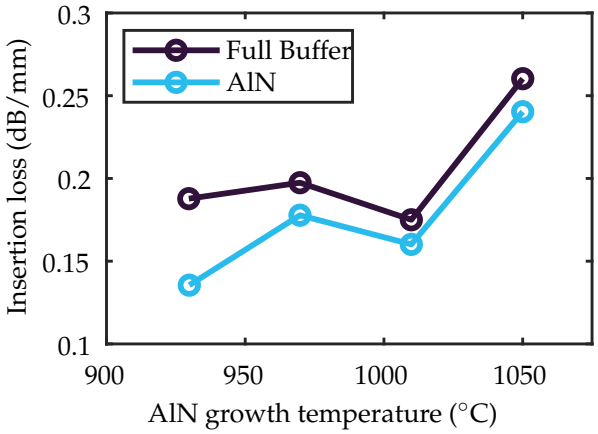


Fig. 2.2 CPW loss at 10 GHz for a full GaN-on-Si buffer and a AlN/Si structure, for different AlN growth temperatures. A clear correlation exists between the two curves. W/S = 85 µm/50 µm. Reproduced from [76].

identified in [44], [67], [70], but the authors in [69], [72], [73] report a p-type layer. As a consequence, the solutions proposed in literature to suppress the parasitic channel and improve RF loss in GaN-on-Si are limited to a given process window and might not be valid for all types of MOCVD reactors. For instance, the impact of an interfacial silicon nitride (SiN_x) is seen as beneficial in [72] but detrimental in [44]. Some mitigation techniques involve additional process steps such as compensation doping, which is impractical from doping control perspective [71], [75].

This chapter aims to achieve a unified understanding of the AlN/Si structure from a RF loss perspective, to determine a more universal way of keeping the PSC layer under control. In Section 2.2, an array of interface characterization techniques will be presented, with a focus on the measurement of electrical properties of HR Si/dielectric structures such as the AlN/Si system.

A different structure, the semi-vertical metal-insulator(oxide)-semiconductor (MI(O)S) capacitor, is introduced in Section 2.3. Its original goal is to overcome the large series resistance in $C-V$ and $G-V$ measurements, but it also allows the design of transistor-like devices and Hall effect measurement pads. The fabrication process is discussed in detail and validated on AlN/Si structures.

Finally, in Section 2.4, techniques relying on a vertical MIS capacitor

will be applied to build a solid representation of the AlN/Si structures. It will lead to specific and universal process guidelines to fabricate high-ρ_{eff} GaN-on-Si epitaxial stacks. For the first time, the link between material physics, electrical properties and RF characterization will point to the main cause of PSC layer formation, and ways to mitigate it.

2.2 Interface characterization techniques

This section provides an overview of the different electrical and material characterization techniques available to study an interface such as AlN/Si. The techniques presented here are all available in UCLouvain Welcome platform and require little sample processing or preparation, i.e. a signal metal deposition and patterning step. The techniques can also be applied on other MIS or MOS systems such as SiO_2-Si or Al_2O_3-Si. They provide a necessary technical basis for the subsequent detailed study and engineering of the AlN/Si interface that is presented in Section 2.4. The case of more complex MIS structures such as the full GaN-on-Si stack is dealt with in Chapter 3.

The physical quantities that can be obtained are listed hereafter.

- PSC layer conductivity type
- PSC layer sheet resistance
- bulk Si conductivity type
- Interface fixed charge
- Interface traps

After presenting capacitance and conductance based methods and the back-side Hall effect technique along with their respective limitations, this section is concluded by guidelines for selection of the most appropriate method.

2.2.1 Capacitance and conductance measurements

Capacitance and conductance measurements allow extraction of almost all interface properties of a MIS or MOS systems [77]. In this section, the different extraction procedures are briefly described, with an emphasis on the difficulties encountered when dealing with high resistivity substrates. AlN/Si or SiO_2/Si samples are used to illustrate the methods.

Measurement setup

On-wafer C(G)-V measurements are performed in a dark environment on a temperature-controlled chuck. A Keysight B1500A semiconductor analyzer is used together with a capacitance meter unit (CMU). One terminal is connected to the chuck, and the other one to the gate probe, as represented in Fig. 2.3. All connections are done using triaxial cables.

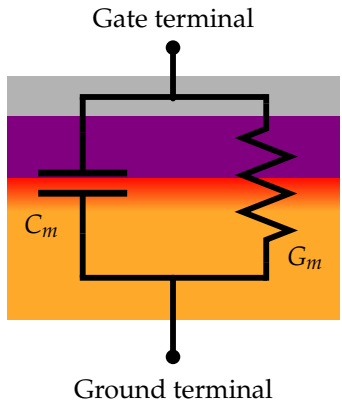


Fig. 2.3 Schematic of the capacitance and conductance measurement of a MI(O)S structure. The capacitance meter unit provides the values of the parallel-connected elements G_m and C_m.

Interface charge extraction

Interface charge is generally regarded as a main contributor to substrate parasitic effects in SOI technology, and its characterization is thus fundamental. For GaN-on-Si, Section 2.4 discusses the similar significance of interface charge. The charge at the interface between AlN and Si ($Q_{f,INT}$) is extracted from the flatband voltage, which is defined as the gate voltage corresponding to zero band bending in Si:

$$V_{FB} = \phi_{MS} - \frac{Q_{f,INT}}{C_{AlN}} - \frac{Q_{it}(\phi_s)}{C_{AlN}}, \tag{2.1}$$

in which ϕ_{MS} is the metal-semiconductor workfunction difference and Q_{it} is the interface trapped charge, which depends on the surface potential ϕ_s. As indicated by Eq. 2.1, fixed and trapped charge contribute similarly to V_{FB} and it is not possible to separate them. Here, it is assumed that $Q_{it} \ll Q_{f,INT}$. $Q_{f,INT}$ is then extracted as $Q_{f,INT} = \Delta V_{FB} C_{AlN}$, where ΔV_{FB} is the change of V_{FB} due to the interface charge compared to the charge-free case.

V_{FB} can be easily calculated for the case of uniform doping in Si. However, when surface doping is present such as in AlN/Si stacks, its extraction is not straightforward. If the distribution of dopants is known (e.g., from SRP measurements) then it is possible to compute the theoretical V_{FB}. In other cases approximations can be used. In this thesis, the following method

is employed [78]:

$$V_{FB} = V\text{corresponding to the max}\left(\frac{d^2\left(\frac{1}{C^2}\right)}{dV^2}\right) \tag{2.2}$$

From Eq. 2.1, the knowledge of ϕ_{MS} is also required to obtain a good estimate of $Q_{f,INT}$. However, for the case of AlN/Si, the combination of a relatively thick dielectric (low C_{AlN}) and high $Q_{f,INT}$ (typical V_{FB} in the tens of volts) makes the incertitude induced by an approximate ϕ_{MS} ($\sim$ 1 V) limited. It is possible to calculate ϕ_{MS} if the interface charge is assumed to be independent of AlN thickness. This assumption is valid if the effect of strain is limited, which is expected for relaxed layers. Then, fabrication of samples with different AlN thickness can provide ϕ_{MS} from the y-intercept of the V_{FB} versus thickness curve:

$$V_{FB} = \phi_{MS} - \frac{Q_{f,INT}t_{AlN}}{\varepsilon_{AlN}}. \tag{2.3}$$

The extraction of ϕ_{MS} is attempted in Fig. 2.4 for AlN thicknesses ranging from 140 nm to 220 nm. Because of the large dielectric thickness (i.e., the datapoints are far from the y axis), the linear fit contains a large uncertainty, with a 95 % prediction interval $\sim$ 10 V wide for ϕ_{MS}. It is certainly more accurate to use a ϕ_{MS} from literature, extracted for lower dielectric thicknesses such as done in [79]. For Ti/AlN/Si stacks, ϕ_{MS} is theoretically predicted to be $\sim$ 0.1 V. [80].

Interface traps extraction using the conductance method

States in the Si bandgap at the AlN/Si interface can cause pinning of the Fermi level at the surface and contribute to low RF loss [4]. The characterization of the interface trap density (D_{it}) in the bandgap generally relies on $C-V$ and $G-V$ measurements of the MIS capacitor.

The preferred method is generally referred to as the conductance method. It is based on the evolution with AC frequency and DC bias of the conductance G_p as displayed in the equivalent circuit of Fig. 2.5a. A general description of the method, as well as the importance of the subtraction of the dielectric capacitance (C_{AlN}) are presented in Appendix B. In this section, a particularly important and limiting aspect of the conductance method when used on high resistivity Si substrates is highlighted: the de-embedding of the series resistance (R_s).

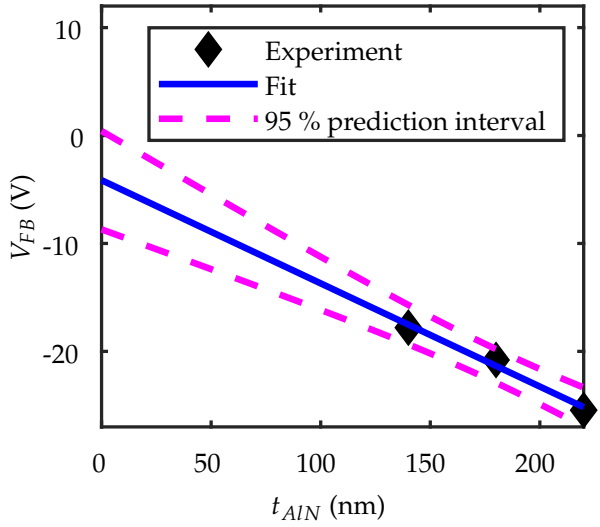


Fig. 2.4 Fabrication of samples with different AlN thicknesses can allow the extraction of the metal-semiconductor workfunction difference by extrapolation to the y-intercept of the flatband voltage versus thickness graph. However, a large uncertainty can exist.

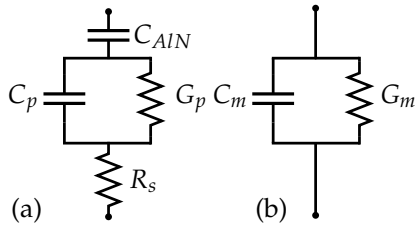


Fig. 2.5 (a) Equivalent circuit of the AlN/Si MIS capacitor in depletion. The bulk Si substrate is represented by the series resistance R_s. (b) Measured admittance

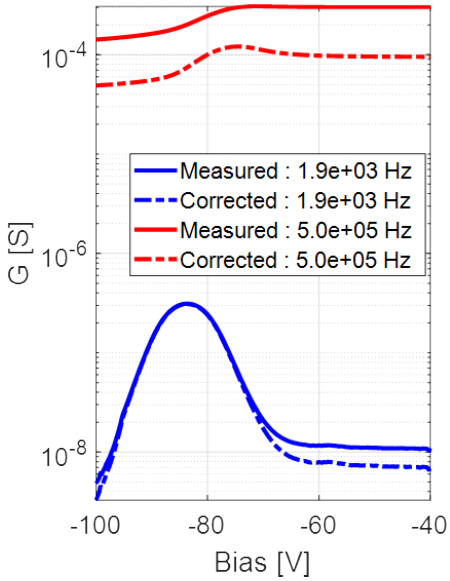


Fig. 2.6 Conductance versus bias curves measured on an SOI substrate with $\rho_{Si} = 20\,\Omega \cdot$ cm. The de-embedding of R_s is important even at such moderate resistivities as conductance peaks can be hidden in the raw data (particularly at high frequencies). Here $R_s \approx 60\,\Omega$

Series resistance

For high resistivity Si, the series resistance (R_s) is important as it can dominate the measured admittance and complicate the extraction of G_p. R_s originates from the high resistance of the 1.15 mm-thick Si substrate between the chuck and the Si surface. It can be measured in strong accumulation, where the equivalent circuit in Fig. 2.5a simplifies to a series connection of C_{AlN} and R_s. R_s is then given by:

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2}, \tag{2.4}$$

where G_m and C_m are the measured conductance and capacitance, respectively. R_s is then de-embedded for the extraction of G_p. Fig. 2.6 demonstrates the importance of R_s deembedding even for relatively low Si resistivities. To attempt to overcome the R_s limitation in the conductance methods, semi-vertical MI(O)S capacitor are introduced in Section 2.3.

Interface traps extraction using the Terman method

When the conductance method cannot be applied, e.g. if the peaks in G_p are hidden by R_s or are found at frequencies beyond the equipment's specifications, the Terman method can be used for D_{it} estimation [77], [81]. It is based on the stretch-out of the $C-V$ curve in the presence of traps, where an increment of bias on the gate is not compensated by a change in ϕ_s (leading to a change in capacitance) but by a change in trap occupation (leading to no change in capacitance). More exactly, it is the stretchout of the $V_G - \phi_s$ curve that gives D_{it}:

$$D_{it} = \frac{C_{AlN}}{q}\frac{d\Delta V_G}{d\phi_s}. \tag{2.5}$$

In Eq. 2.5, ΔV_G is the difference between the experimental gate voltage and the ideal, trap-free V_G. This method is well-suited for thick dielectrics, as the $C-V$ stretchout (ΔV_G) increases with increasing dielectric thickness [82]. For the Terman method to be accurate, it requires:

- A relation between gate voltage and surface potential, that can be computed if the doping is known. This implies that SRP or SIMS data containing the distribution of Al and Ga dopants must be available. Such a curve can also be extracted from an experimental $C-V$ curve measured at a sufficiently low frequency, such that both interface traps and minority carriers are given sufficient time to respond to the AC excitation
- A true high-frequency C-V curve which constitutes the ideal, trap-free C-V, where interface traps do not respond to the AC voltage but do respond to slow changes in gate bias. In the case of a thick dielectric on HR Si, the main difficulty resides in R_s-related parasitic effects that change the shape of the $C-V$ curve at high frequency.

In this thesis, both of the experimental curves required for the Terman method are quite difficult to produce. An alternative can be the use of a TCAD environment to generate these curves. Provided that the SRP data is available, the interface fixed charge is well extracted, and the dielectric thickness and permittivity are well-known, it is possible to generate accurate low frequency and trap-free $C-V$ curves. This method will be applied on AlN/Si samples in Section 2.4.

In summary, while some aspects are made more complex by the presence of HR Si and/or thick AlN layers, the methods based on conductance and

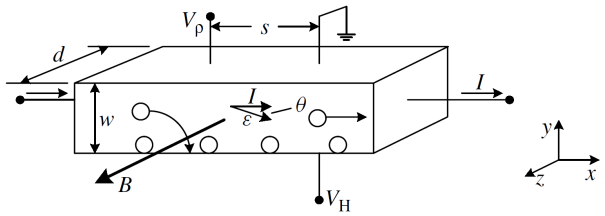


Fig. 2.7 Slab of semiconductor considered for the theoretical Hall effect equations. The directions of current, magnetic field and Hall voltage are indicated. Reproduced from [78].

capacitance measurements constitute a useful toolbox to reliably obtain electrical properties of the AlN/Si interface.

2.2.2 Resistivity measurement by Hall effect

A direct measurement of the conductivity and mobility of the Si is not possible using the methods described above. Furthermore, while SRP can provide resistivity profiles, the sample preparation requires the removal of the top dielectric layer and its associated charges which can have a significant impact on the conductivity. The Hall effect allows in theory direct measurement of carrier density, conductivity type and mobility.

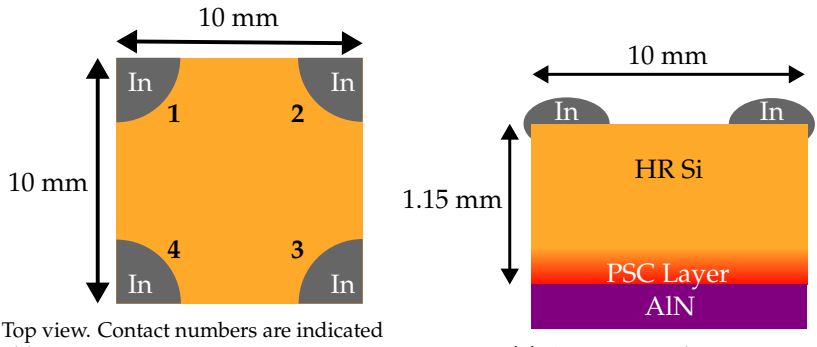
Hall effect

When a slab of semiconductor material (Fig. 2.7) in which a DC current I flows is subjected to a magnetic field B, the free carriers undergo a force perpendicular to the current and the magnetic field. This force deflects the free carriers and, when current flow in the direction perpendicular to I and B is prevented, leads to a voltage at steady state (V_H). The direction of this voltage is dependent on the carrier type. The Hall coefficient is then defined as:

$$R_H = \frac{dV_H}{BI}, \tag{2.6}$$

where d is the size of the sample in the direction of B (see Fig. 2.7). R_H can then directly be connected to the carrier concentration if either holes or electrons are in majority:

$$p = \frac{1}{qR_H}; n = -\frac{1}{qR_H}. \tag{2.7}$$



(a) Top view. Contact numbers are indicated in bold.

(b) Cross-sectional view.

Fig. 2.8 Schematic of the sample geometry for the backside Hall effect measurement. Indium dots are melted with a soldering iron on the Si surface to achieve satisfactory contact.

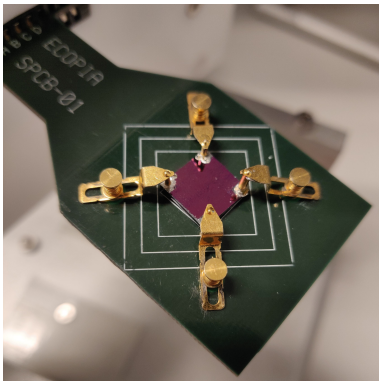
If the resistivity ρ of the slab is measured without the magnetic field (i.e., a 4-point measurement using the V_ρ terminal in Fig. 2.7), it is then possible to extract the hole or electron mobility:

$$\mu = \frac{R_H}{\rho}. \tag{2.8}$$

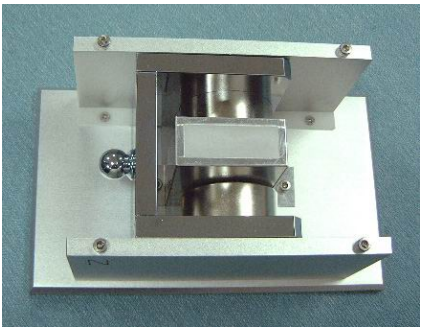
In practical setups, the implementation of a slab of material similar to Fig. 2.7 is not straightforward as electrical contacts have to be made on different sides of the material. A more practical implementation takes the form of a Van der Pauw geometry such as shown in Fig. 2.8a. Four In contacts are soldered at the surface of the sample which is then placed in a sample holder as shown in Fig. 2.9a. The sample holder is placed in a magnetic field oriented in the thickness direction. For such a structure, it is possible to derive a formulation for the material resistivity:

$$\rho = \frac{\pi t}{\ln 2} \frac{R_{12,34} + R_{23,41}}{2} F, \tag{2.9}$$

where F is a function of $R_r = \frac{R_{12,34}}{R_{23,41}}$ and is equal to 1 for square samples. The resistances are defined as follows. For $R_{12,34}$, current enters through contact 1 and leaves through contact 2. The voltage is measured between terminals 3 and 4. Eq. 2.9 is valid for any sample shape, provided that the contacts are formed at its circumference and that the sample contains no



(a) PCB sample holder and electrical connections



(b) 1.0 T magnet. The sample holder is placed between the two poles of the magnet.

Fig. 2.9 Pictures of the Hall effect measurement setup Ecopia HMS-3000.

holes. The mobility can be calculated from:

$$\mu = \frac{d\Delta R_{24,13}}{B\rho}. \tag{2.10}$$

$\Delta R_{24,13}$ is the difference between $R_{24,13}$ with and without magnetic field. It should be noted that the Hall effect method requires DC access to the material to be characterized. Consequently, soldering the In contacts on the AlN surface cannot provide any result in Si. Here, the method is applied to the backside of the sample, as represented in Fig. 2.8b.

Experimental results from the backside Hall effect method

To exemplify the potential of the Hall effect measurement, two sets of AlN/Si samples are considered. They are described in Table 2.1. Reactors A and B are two copies of the Aixtron G5 MOCVD reactor, installed in two different cleanrooms.

MOCVD Reactor	Wafer Name	ρ (k$\Omega \cdot$ cm)	[O_i] (ppma)
	A1	3-6	unspecified (likely > 5 ppma)
A	A2	4.3	3.0
	A3	6.8-7.7	3.9
	B1	3-6	unspecified (likely > 5 ppma)
B	B2	unknown	unspecified (likely > 5 ppma)
	B3	6.8-7.7	3.9

Table 2.1 Description of the AlN/Si samples to illustrate the applications of backside Hall effect method

Sample	Polarity	ρ ($\Omega \cdot$ cm)	Carrier density (cm^{-3})	Mobility ($cm^2/(Vs)$)	ρ_{eff} ($\Omega \cdot$ cm)
A1	P	364	1.1×10^{14}	156	113
A2	P	356	9.4×10^{13}	187	104
A3	P	1110	8.5×10^{13}	66	107
B1	N	5200	9.4×10^{11}	1290	280
B2	N	1200	3.5×10^{12}	1190	249
B3	N	9900	4.9×10^{11}	1280	347

Table 2.2 Results from the Hall effect measurements on AlN/Si samples. Effective resistivity values are averaged over a frequency range from 1 to 5 GHz and are measured on CPW lines with W/S = 85 µm/50 µm.

All samples from Reactor B showed conductivity type inversion in Si bulk in the SRP profiles. No SRP was measured on samples from Reactor A. The ρ_{eff} for all samples is low, between $100\,\Omega \cdot$ cm to $400\,\Omega \cdot$ cm, indicating the presence of a strong PSC layer.

The Hall data is reported in Table 2.2. For the samples of reactor A, the polarity is measured as p-type, meaning that no bulk polarity inversion due to TD has occured. In this case, the measured resistance consists in a parallel connection of the bulk resistance (R_{Si}) and the PSC layer resistance (R_{PSC}). Since $R_{PSC} \ll R_{Si}$, the equivalent resistivity is low, with a high carrier density. The mobility is lower than the hole mobility expected in bulk Si ($\sim 450\,\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$). This could be due to the degradation of the mobility close to the Si surface, as this region is dominating in the overall μ [78].

For the samples of reactor B, a n-type conduction is extracted. The bulk Si has inverted, as was already measured with SRP. Interestingly, the resistivity extracted is high, more than one order of magnitude higher than the measured ρ_{eff}. This can be explained by the presence of a p-n junction between the PSC layer (p-type) and the bulk (n-type). In DC, the PSC layer is effectively disconnected from the Hall effect measurement terminals. The resistivity in the bulk being high and mobility not limited by surface scattering effect, the properties of a HR n-type Si material are extracted with μ close to the theoretical value for electrons (max. $1400\,\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$).

In summary, the Hall effect technique allows direct extraction of the resistivity, carrier density, conductivity type and mobility of a semiconductor. It can provide valuable information about the substrate doping and help confirm other measurements. However, interfacial properties can be hidden by the presence of a deep p-n junction. The sample preparation is quite simple, with only dicing and In soldering required. No additional metal deposition or lithography steps are needed, making it a fast method for a first characterization.

2.2.3 Summary

The complex nature of the AlN/system with fixed interface charge, non-homogeneous doping featuring p-n junctions in Si, and possibly interface trapped states, necessitates characterization techniques beyond the simple CPW measurements typically used to evaluate its RF performance. In this section, two different measurement categories were presented.

Top-down capacitance and conductance measurements contain a large

quantity of information. In particular, fixed equivalent interface charge is easily extracted from the flat-band voltage. Further techniques can provide the distribution of interface traps in the Si bandgap. However, the most precise method, which is based on AC conductance measurements, is hindered by the presence of a large series resistance induced by the HR Si substrate. The Terman method based on the stretch-out of the $C-V$ curve can be applied but requires a comparison with reference curves which are not straightforward to produce. A TCAD model, when available, can help. Since dot capacitors are usually available and fabricated alongside CPW lines, no additional sample preparation is required and $C(G)-V$ measurements will be the preferred technique in the later sections of this chapter.

Flipping the sample upside down, the Hall effect technique applied from the backside is well-suited to high resistivity substrates. A relatively simple measurement and sample preparation allows the extraction of an aggregated substrate conductivity and free carrier mobility and concentration. However, following O-related TD activation, a p-n junction can appear close to the Si front surface and prevent electrical access to the interface. Consequently, The resistance obtained can be significantly different from the effective resistivity measured with a CPW line.

In the next section, a different, more complex characterization structure will be presented to overcome the limitations exposed here.

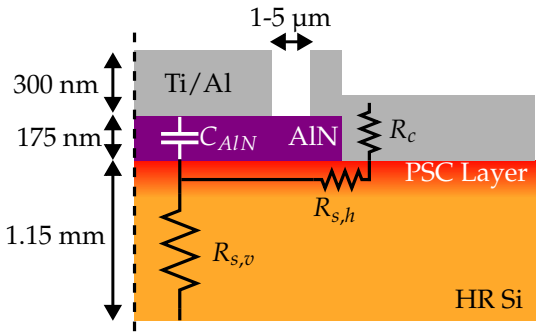


Fig. 2.10 Schematic cross-section of the semi-vertical MI(O)S capacitor proposed to limit the effect of series resistance on $G-V$ measurements. Different dimensions for the electrodes are considered.

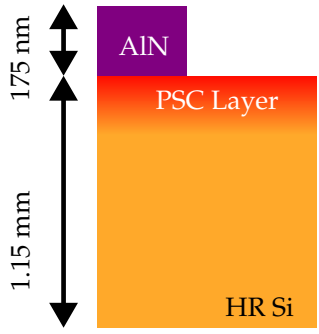
2.3 Fabrication of semi-vertical MO(I)S capacitors

In this section, a potential way to overcome the limitations of the conductance method presented in Section 2.2.1 is presented. Because the majority of the series resistance of the MIS capacitor originates from the ~1 mm-thick, highly-resistive Si substrate, a lateral connection to the dielectric/Si interface could significantly shorten the resistive path. The semi-vertical MO(I)S capacitor is presented in Fig. 2.10. The backside contact to the Si substrate is replaced by a lateral contact after etching of the dielectric, where it is expected that $R_{s,h} + R_c \ll R_{s,v}$.

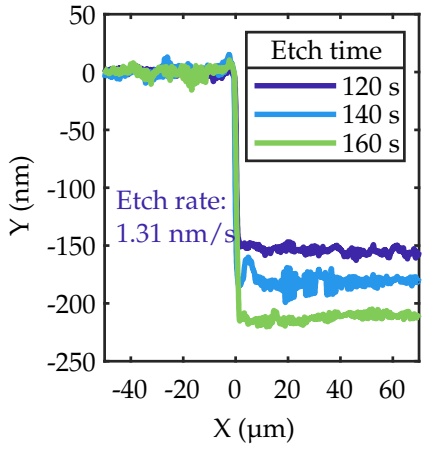
The challenge of fabricating such characterization structure resides in the dielectric etching. Incomplete etching would create a capacitive contact to the Si, whereas overetching past the PSC layer would lead to more resistive contact.

2.3.1 Process flow

The fabrication of the semi-vertical MI(O)S capacitors requires only few process steps, starting from a AlN/Si or SiO_2/Si stack. All are performed in the Winfab facilities. The samples consist of a 175 nm-thick (confirmed by ellipsometry) AlN layer on a HR Si substrate. The process contains no high-temperature steps that could lead to activation or annihilation of TDs in the Si substrate.



(a) Cross-section schematic of the structure measured after AlN etching.



(b) Profilometry data after AlN etching for times ranging from 120 s to 160 s. The incomplete AlN etching after 120 s allows determination of the etch rate.

Fig. 2.11 Determining AlN etch rate.

Resist spinning and patterning

A standard photoresist (AZMir 701) is deposited on the AlN surface at a spin rate of 3000 rpm, providing a resist thickness of ∼1 µm. It then undergoes the typical lithography steps:

1. Soft bake at 100 °C for 90 s;
2. Exposure to UV light. The dose is set to 190 mJ/cm^2;
3. Post bake at 110 °C for 90 s;
4. Development using the AZ726 developer.

AlN etching

AlN is notoriously resistant to etching. However, a dry etching using Cl_2(25 sccm)/BCl_3(5 sccm)/Ar(20 sccm) was found to give satisfying results. To determine the etching rate, three different wafers are etched for times ranging from 120 s to 160 s. After etching, the resist is stripped and etching depth is measured using profilometry as shown in Fig. 2.11. The resulting etch rate is calculated as 1.31 nm/s, allowing precise control over the thickness of the AlN layer. Fig. 2.12 shows a SEM image of one sample after complete etching. Some degree of under etching is visible but not critical

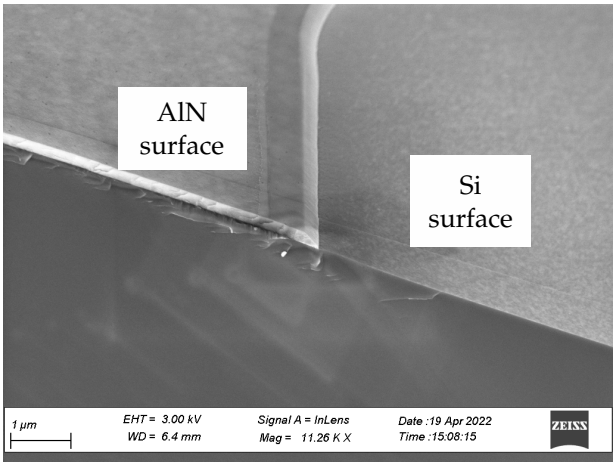


Fig. 2.12 SEM imaging of the AlN/Si stack after complete etching.

as the characterization structures all show more relaxed dimensions in the micrometer range. A ∼10 nm overetching (i.e., 10 nm into Si) is accounted for in the etch time to ensure complete removal of AlN. Finally, after etching, the wafers are cleaned in an oxygen plasma environment.

Second resist spinning and patterning

The resist for metal lift-off is the AZ nLOF 2000, which is applied at 3000 rpm for a 2 µm thickness. The subsequent steps are slighlty adapted to this different resist:

1. Soft bake at 100 °C for 60 s;
2. Alignment and exposure to UV light. The dose is set to 120 mJ/cm^2;
3. Post bake at 105 °C for 60 s;
4. Development using the AZ726 developer.

Metal deposition and lift-off

The metal stack used for both Si and AlN contacts consists of 10 nm Ti (used as an adhesion layer) followed by 500 nm Al, deposited by e-beam evaporation. Prior to the deposition, it is critical to remove the native SiO_2 layer that was formed naturally after exposure of the Si surface. This step is performed as close in time as practically possible to the loading of the wafers in the evaporation vacuum chamber. A 3 s dip in a buffered HF bath

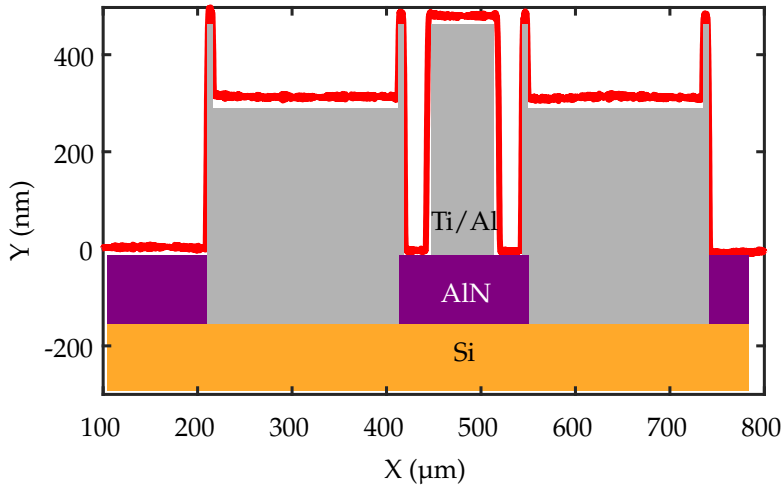


Fig. 2.13 Measured depth profile of the semi-vertical structure after successful lift-off.

removes the SiO_2 and prevents it from forming again but is only stable for a few tens of minutes.

Final structure

The finished structure after lift-off is presented in Fig. 2.13. The slight overlap between the etching and metallization allows Si to nowhere be directly exposed and always be covered always by AlN or metal. The profilometry validates the fabrication process.

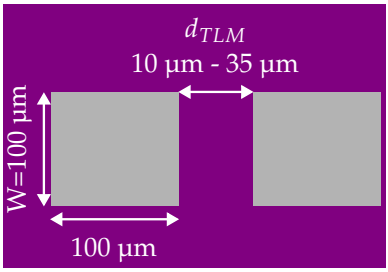
2.3.2 Electrical characterization

Once the characterization structures are successfully fabricated, electrical characterization is performed to validate them.

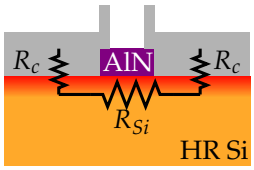
Contact on Si

The transfer length method (TLM) is used to characterize the contact resistivity [78]. Square pads separated by a distance ranging from 10 µm to 35 µm are used (Fig. 2.14a). The total resistance measured is given by:

$$R_{tot} = 2R_C + R_{Si}, \tag{2.11}$$



(a) Top view.



(b) Cross-section view.

Fig. 2.14 Structures used for transmission line method of contact resistance characterization.

in which R_c is the contact resistance and R_{Si} the resistance of Si (Fig. 2.14b). R_{Si} is given by:

$$R_{Si} = R_{sh} d_{TLM} / W, \tag{2.12}$$

in which R_{sh} is the sheet resistance of the PSC layer (in Ω/sq) and d_{TLM} and W are dimensions defined in Fig 2.14a.

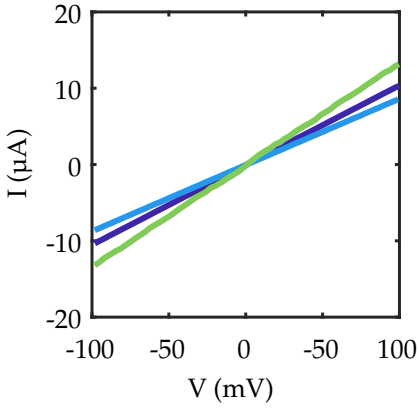
The fabrication of several structures with varying t_{TLM} allows the extractions of several quantities of interest by performing a linear regression of R_{tot} versus d_{TLM}.

- R_C can be extracted from the y-axis intercept of the linear regression;
- R_{sh} is provided by the slope;
- The x-axis intercept gives the transfer length (L_T). L_T characterizes the current distribution below the square contacts, which is not uniform: most of the current from the metal to Si flows close to the contact edge, and decreases nearly exponentially. L_T is the distance over which a $\sim 1/e$ fraction of the current flows.

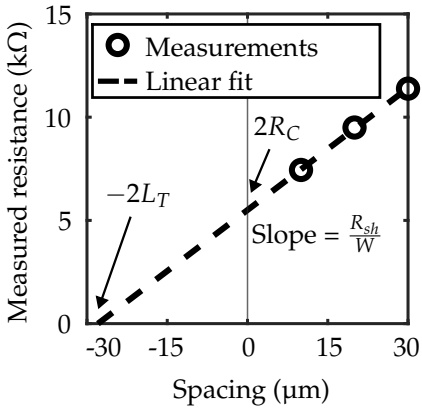
Those quantities then permit the extraction of the specific contact resistivity (ρ_c, in $\Omega \cdot \mathrm{cm}^2$) using the following relation:

$$\rho_c = L_T.^2 R_{sh}$$

Fig. 2.15a first shows that an ohmic contact on Si could be achieved. Indeed, all measured I-V curves show a linear relation respecting Ohm's law. Next, the regression for three different spacings (Fig. 2.15) gives a contact resistance of $R_c = 2.76\,\mathrm{k}\Omega$, a sheet resistance of $R_{sh} = 19.7$



(a) Current-voltage charateristics for three different TLM spacings. A linear I-V relationship indicates the formation of an ohmic contact.



(b) Total measured resistance versus TLM spacing. A clear linear trend allow extraction of the contact resistance at the y-axis intercept.

Fig. 2.15 Electrical results of the transfer length method structures.

Ω/sq and a transfer length of $L_T = 14.0\,\mu m$. This translates into a specific contact resistivity of $\rho_c = 384\,m\Omega \cdot cm^2$. This value is fairly high. As a comparison, contact resistivities in Si MOSFETS are typically lower than $1\,\mu\Omega \cdot cm^2$. However, the ohmic nature of the contact allows further use of the characterization structures.

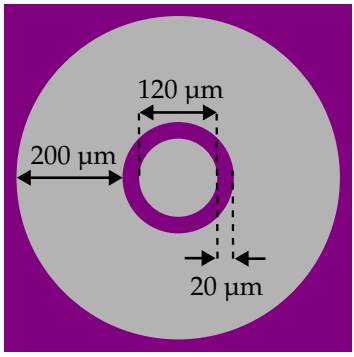
The sheet resistance obtained by the TLM method is difficult to relate to the resistivity of Si because of the highly non-uniform resistivity profile. Indeed, for non-uniform layers or thickness t, R_{sh} is given by:

$$R_{sh} = \frac{1}{\int_0^t \frac{1}{\rho} dx}.$$

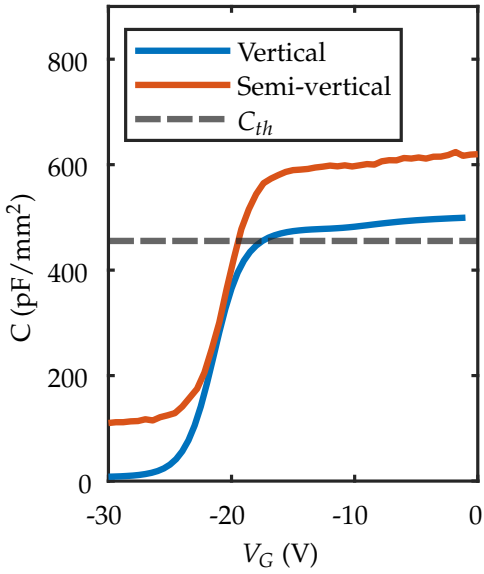
Even when the PSC layer is isolated from the bulk Si by a p-n junction (e.g., a p-type PSC layer on a n-type bulk), the depth of the junction would be needed to obtain the resistivity of the PSC layer.

C-V measurements

Concentric capacitors are used for C-V measurements such as represented in Fig. 2.16a. The gate consists of a circular pad with a radius of 60 μm. The total area of the Si contact is $\sim 2.3 \times 10^{-3}\,cm^2$. Fig. 2.16b shows the $C - V$ measurements on both vertical and semi-vertical capacitors. The



(a) Schematic of the semi-vertical MIS capacitor under study. The central contact is on AlN, the ring contact is on Si.



(b) Normalized capacitance of a vertical (500 µm by 500 µm square pad) and semi-vertical capacitor on the same wafer as a function of gate bias. The theoretical value for C_{AlN} is indicated in black. f = 10 kHz.

Fig. 2.16 Experimental results for the semi-vertical MIS capacitor.

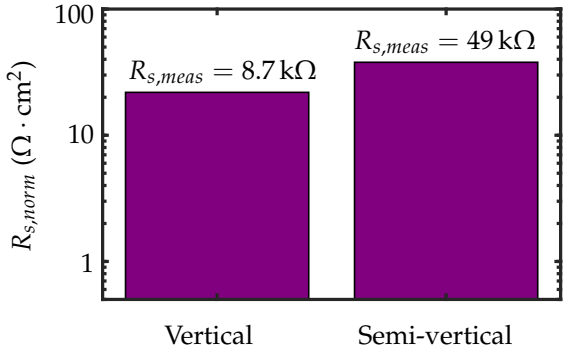


Fig. 2.17 Normalized series resistance extracted from $C-V$ measurements (see Fig. 2.16b) a vertical and semi-vertical MIS capacitor located on the same die ($f = 10$ kHz). The use of the semi-vertical structure leads to an increase in the series resistance. Absolute values of series resistance are also included.

curves match qualitatively, validating the electrical function of the semi-vertical structures. However, the capacitance normalized by the area of the gate electrode (A_g) is higher than what is predicted by the parallel-plate expression $C_{AlN} = \varepsilon_{AlN} A_g / t_{AlN}$. This indicates that the effective pad area for the semi-vertical capacitor is larger than the physical pad, likely due to lateral fringing field that is nonexistent in the vertical structure.

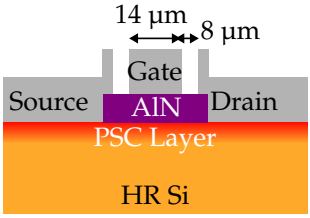
From the measurements, it appears that the Si has been flipped to n-type during AlN growth. Furthermore, electrons are the majority carriers close to the Si surface at $V_G = 0$ V (deduced from the negative V_{FB}). This means that the diffusion of Al atoms (forming a p-type PSC layer) is dominated by a positive charge at the interface between AlN and Si (causing a n-type layer). This phenomenon will prove to be crucial in the understanding and optimization of the AlN/Si interface in Section 2.4.

Series resistance

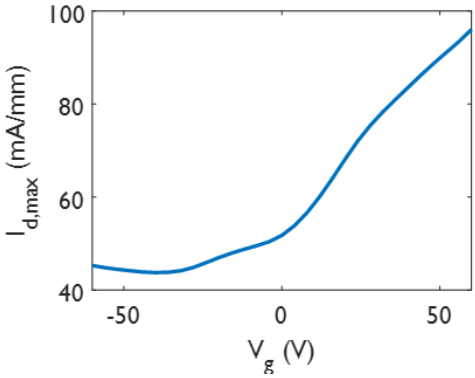
R_s is extracted according to Eq. 2.4 at a frequency of 10 kHz. It is normalized to the gate area A_g as follows:

$$R_{s,norm} = R_{s,meas} A_g. \tag{2.13}$$

The results are shown in Fig. 2.17. Clearly, the implementation of the semi-vertical structure did not lead to an improvement in R_s despite the reduction of the HR Si contribution. Two possible causes can be pointed out.



(a) Cross-section of the transistor-like structure.



(b) I_D-V_G characteristic of the three terminal device. Althoug a large off-state current exists, the device exhibits a threshold voltage in accordance with the $C-V$ measurement.

Fig. 2.18 A three terminal structure based on the semi-vertical process can function like a transistor.

i. The ground contact area is significantly larger in the vertical structure. When the capacitor is biased in strong accumulation and a PSC layer with the same polarity exists across the entire wafer, the effective area forming the ground electrode can be much larger than the gate electrode (see Section 2.4). Since the ground contact in the vertical capacitor is virtually unlimited, the series resistance can be relatively low compared to the semivertical case (see Fig. 2.16a).

ii. The semi-vertical contact resistance on Si is high and dominated over HR Si. This is however unlikely. Indeed, considering a contact resistivity of $r_c = 276\,\mathrm{m\Omega \cdot cm^2}$ and the area of the ground electrode of Fig. 2.16a, the contact should account for $\sim 122\,\Omega$, a negligible value compared to the measured $49\,\mathrm{k\Omega}$.

Furthermore, the designed devices only present limited gate pad area which could anyhow prevent the decrease of the absolute R_s.

Transistor-like devices

The semi-vertical process also allows fabrication of three-terminal devices similar to a MOSFET (Fig. 2.18a). The PSC layer constitutes the channel and source and drain electrodes are contacting Si. While the design of these structures could be significantly improved by e.g. DC isolation of the

transistor or fabrication of concentric ring-shaped devices, their electrical behavior is as expected. Consider the $I_D - V_G$ curve in Fig. 2.18b. It shows a certain degree of gate control over the conductivity of the channel, with an increase in I_D from $\sim$ 50 mA/mm in the off-state to $\sim$95 mA/mm in the on-state. The large off-state current is due to the design of the device, allowing conductive paths between source and drain to exist beyond the gate. Interestingly, the treshold voltage (V_t) of this transistor appears to be close to the V_{FB} measured on the semi-vertical MIS capacitor (Fig. 2.16b).

2.3.3 Summary and future work

First steps in developing the semi-vertical process and characterization techniques have been taken in this thesis. While functional devices have been fabricated, more work is required to explore their potential.

The process could be further optimized by improving the Si contacts by e.g. annealing at $\sim$ 400 °C. Also, the lithography parameters on AlN are not ideal as some resist delamination has been observed along with resolution issues that were problematic for small lateral spacing devices.

Also, some important features are lacking in the design of the devices. Circular pads for the TLM characterization have been shown to be easier to model than square pads [78]. As mentioned above, a better design for the three-terminal structures is possible, e.g. by considering a ring-FET like design. Furthermore, Hall effect pads in a geometry compatible with the measurement setup available in Welcome would be of interest to overcome the limitation of the backside method.

Because of the current shortcomings of the existing three-terminal devices, the complete AlN/Si interface study undertaken in Section 2.4 is performed on classical vertical MIS capacitors. An estimation of interface trap density can be obtained using the Terman method, but finer characterization would require an improved three-terminal structure.

TMAl predose (cm^3)	Sample Denomination	
	Reactor A	Reactor B
7.7	A8	B8
30.7	A31	B31
61.3	A61	B61

Table 2.3 Description of the different samples considered for the study of the impact of trimethylaluminum predose on RF loss.

2.4 AlN/Si interface engineering

In this section, the characterization techniques presented above are applied to build a complete understanding of the AlN/Si interface. For the first time, all aspects of the RF loss degradation in AlN/Si stacks are considered together: dopant diffusion, interface trapped and fixed charge, and the AlN layer itself. This is done through extensive electrical and material characterization, coupled with TCAD simulations grounded in semiconductor physics.

AlN/Si stacks with varying trimethylaluminum (TMAl) predose constitute the case study. The TMAl predose has been recenly shown to be an important factor regarding RF loss [74], [83], [84]. In contrast with existing studies, the TMAl predose is unambiguously linked to precise electrical properties of the AlN/Si interface and shown to be a key determining factor in the RF loss. Following the experimental and simulatory investigation, a method is proposed to solve the issue of decreased effective resistivity in GaN-on-Si stacks regardless of the fabrication equipment. It is demonstrated by the fabrication of an AlN/Si sample with $\rho_{eff} \approx 8\,k\Omega \cdot cm$.

2.4.1 Devices and experiment

Two series of 200 mm AlN/Si samples produced in different cleanrooms and MOCVD reactors (Reactors A and B) are studied. All samples consist of a 175 nm-thick AlN layer grown in separate AIXTRON G5+ C Planetary reactors. The starting Si wafers are 200 mm high-resistivity Si ($>4\,k\Omega \cdot cm$) with interstitial oxygen concentration ($[O_i]$) lower than 5 p.p.m.a for Reactor A and unspecified $[O_i]$ for Reactor B. In both series, the TMAl predose was varied from $7.7\,cm^3$ to $61.3\,cm^3$ as described in Table 2.3. Following AlN growth, coplanar waveguide (CPW) lines were patterned directly on the AlN surface, also in separate labs and with different metal stacks. A signal line width (W) and signal-to-ground spacing (S) of 17 µm and 10 µm,

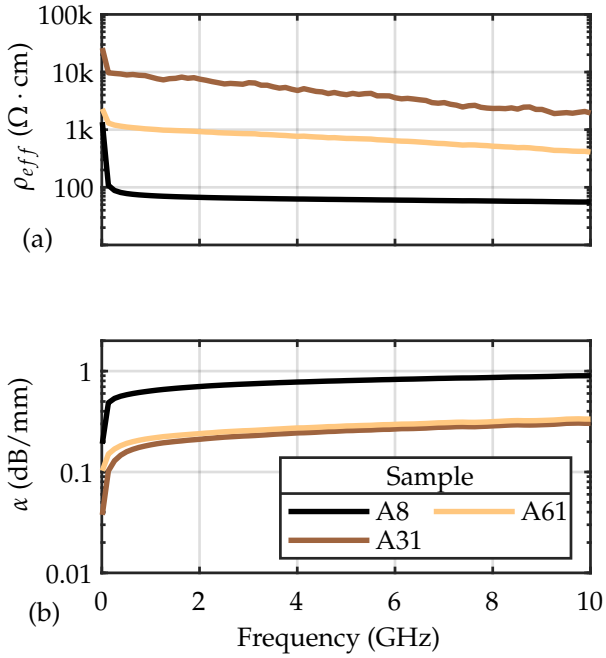


Fig. 2.19 (a) Effective resistivity and (b) total insertion loss for the CPW lines on representative dies on AlN/Si samples produced in Reactor A. W/S = 17 µm/10 µm

respectively, are used for samples of Reactor A. For Reactor B, W = 36.6 µm and S = 20 µm.

2.4.2 RF characterizaton

S-parameters measurements were performed in dark conditions at 25 °C and the effective substrate resistivity was extracted as described in Chapter 1. For such $S \gg t_{AlN}$, the dimension-induced difference in ρ_{eff} is expected to be limited [85]. The results are shown in Fig. 2.19a. A strongly non-linear impact of TMAl predose on substrate RF performance is observed. An improvement by ∼2 orders of magnitude in ρ_{eff} is achieved from sample A8 ($\rho_{eff} \cong 60\,\Omega \cdot$ cm) to sample A31 ($\rho_{eff} \cong 7\,\text{k}\Omega \cdot$ cm), and ρ_{eff} then decreases when the predose is further increased to sample A61 ($\rho_{eff} \cong 900\,\Omega \cdot$ cm). $\rho_{eff} > 5\,\text{k}\Omega \cdot$ cm is reached for sample A31, corresponding to a quasi-lossless substrate [9]. The CPW losses (α), which include both the

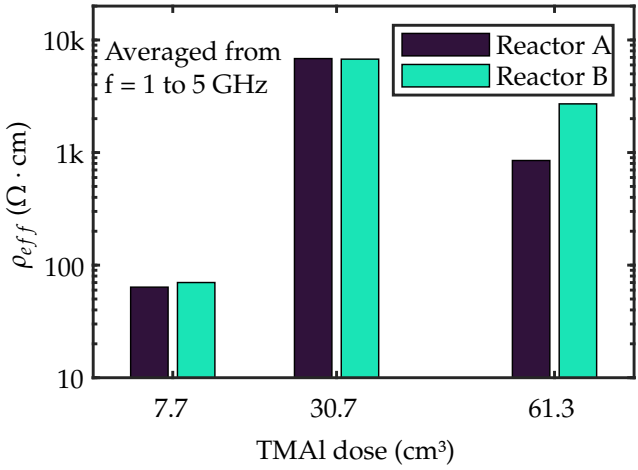


Fig. 2.20 TMAl predose strongly impacts ρ_{eff}. The effect is independent of the reactor or starting Si wafer. W/S = 17 µm/10 µm and 36.6 µm/20 µm for Reactor A and B, respectively.

metallic and substrate losses and are depicted in Fig. 2.19b for the three samples. This effect can be accurately reproduced in a different reactor and for different starting HR Si substrates (Fig. 2.20).

Such a difference in ρ_{eff} can cause a more than 30 dB difference in substrate HD. Large-signal measurements at 0.9 GHz are performed and the results are shown in Fig. 2.21. The trends observed in ρ_{eff} are observed in HD as well, with poor HD for sample A8, excellent HD for sample A31, and a degradation in HD for sample A61.

In the following, additional physical characterization will help to understand the origin of this non-linear effect and to straightforwardly identify the TMAl predose for which ρ_{eff} is the highest.

2.4.3 Material characterization

The significant difference in ρ_{eff} indicates a change in Si surface conductivity, which could be caused by doping. Al in-diffusion and consequent Si doping is known to be affected by process conditions [69].

Spreading resistance profiling

To measure the surface doping, Spreading Resistance Profiling (SRP) measurements were taken on all three samples from Reactor A. SRP data can

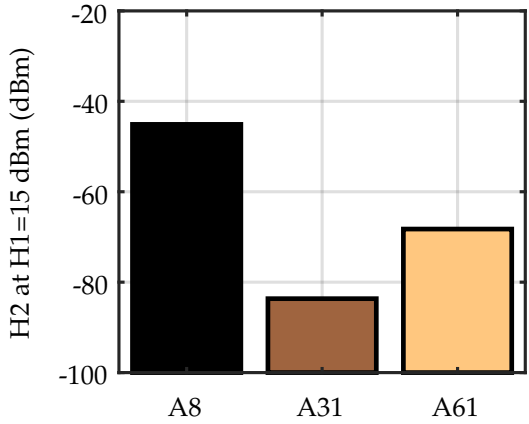


Fig. 2.21 Harmonic distortion measured in dark conditions at 25 °C and 0 V DC bias for the three samples of reactor A. The trends observed in the small-signal measurements are confirmed here, with an almost 40 dB difference between sample A8 and sample A31. f = 0.9 GHz. CPW length = 2 mm. W/S=23.4 µm/12.5 µm.

reveal the presence of ionized dopants resulting from Al diffusion during MOCVD growth for depths into Si ranging from ∼20 nm to a few µm. However, fixed charges or traps located at the interface or in the AlN layer cannot be revealed by SRP as the AlN layer is removed for the measurement of the bevelled Si surface (see Fig. 1.13a). The spreading resistance profiles in Fig. 2.22 show a limited Al in-diffusion for the three samples and the resistivity stays above ∼60 Ω · cm for the entire profile. The dopant profile is following Fick's second law for all samples, with nominal diffusion lengths of 43 nm, 50 nm and 88 nm for samples A8, A31 and A61, respectively. A slightly increased dopant diffusion is seen for sample A61. The charge corresponding to the increased surface doping can be calculated as:

$$Q_{dop} = \int_0^{t_{PSC}} (N_A - N_{A,bulk})\, dy, \tag{2.14}$$

in which $N_{A,bulk}$ is the doping far from the surface and t_{PSC} is the PSC layer thickness, defined as the depth at which $N_A = N_{A,bulk}$. Integrated doping results are shown in the inset of Fig. 2.22. The difference in charge between the three samples is lower than 5×10^9 cm^{-2} and is not sufficient to explain any difference in ρ_{eff}, as could be confirmed by TCAD simulations. Also, all samples show p-type conductivity for the entire profile (i.e. until ∼20 µm depth), meaning that no significant interstitial oxygen-related TD

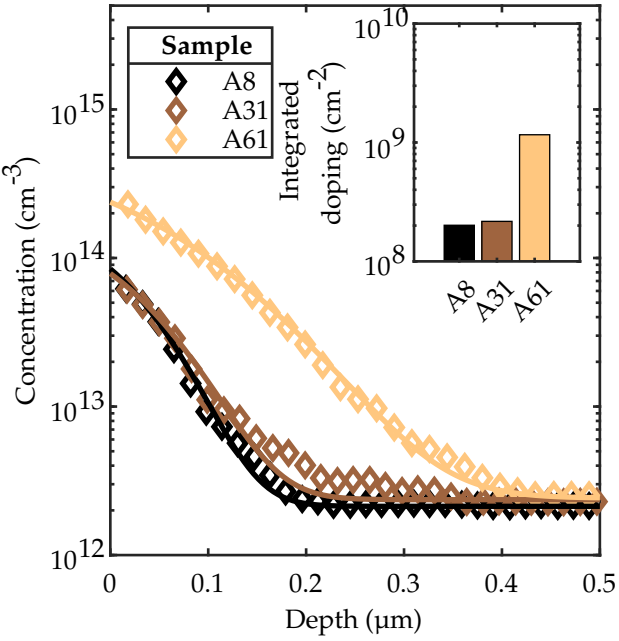


Fig. 2.22 SRP measurement for all three AlN/Si samples of Reactor A. Best fit for Fick's second law is included in continuous lines. Inset: the sheet carrier concentration induced by the surface doping is lower than 2×10^9 cm^{-2} for the three samples. The SRP data shows p-type conductivity for the full profile in all samples.

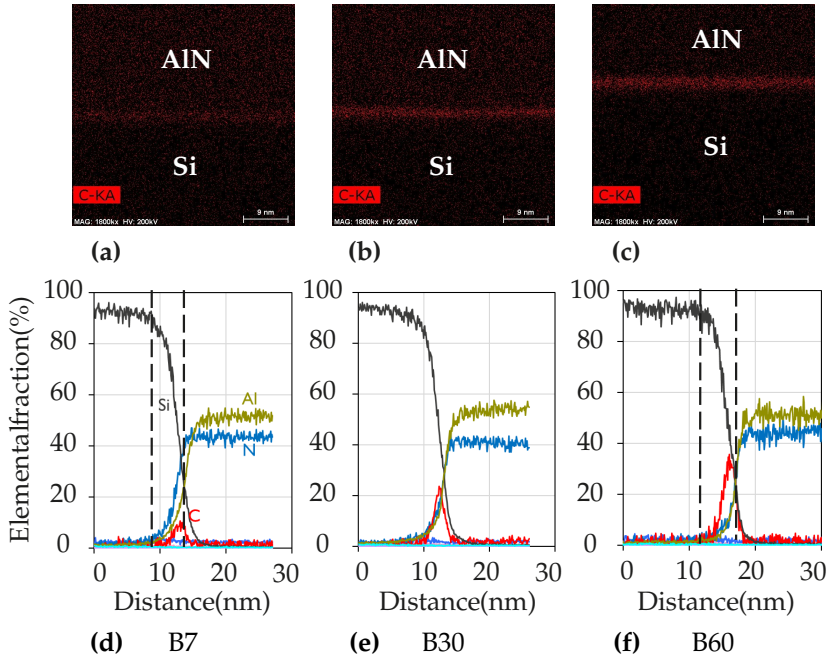


Fig. 2.23 Physical characterization of Reactor B samples. (a-c) STEM images reveal the presence of a C-rich interfacial layer between AlN and Si. (d-f) EDS scans along a cross-section of the AlN/Si interface show an evolution of interfacial layers' composition as TMAl predose is increased. Lower predose favours the formation of SiN, while higher predose produces a higher fraction of SiC at the interface.

activation (which would be n-type) is taking place.

STEM and EDS

Furthermore, scanning transmission electron microscope (STEM) and energy dispersive spectroscopy (EDS) images indicate the presence of a SiC_xN_y layer between AlN and Si. As seen in Fig. 2.23, the composition of this ∼5 nm-thick layer measured with EDS changes from a SiN_x-like layer to a SiC_x-like layer when TMAl predose is increased. This layer cannot be detected by SRP and additional electrical characterization is required to understand its electrical impact.

2.4.4 Barrier height

I-V sweeps were measured to get more insight on the vertical carrier transport mechanisms close to the interface and across the AlN layer. Results are shown in Fig. 2.24a and in Fig. 2.24b-d as a function of $\sqrt{E}$, where the electric field E across the AlN layer was calculated as:

$$E_{AlN} = \frac{V_{gate} - \phi_s}{t_{AlN}}, \tag{2.15}$$

for which the surface potential ϕ_s was extracted from the C-V curves (see later). At low fields, the fit to Schottky Emission (SE) mechanism is made difficult by the high measurement noise at low current levels. The SE current is given by [86]:

$$J_{SE} = \frac{4\pi q m^* (kT)^2}{h^3} \exp\left[\frac{-q\left(\phi_B - \sqrt{\frac{qE_{AlN}}{4\pi\varepsilon_{AlN}}}\right)}{kT}\right], \tag{2.16}$$

in which m^* is the electron's effective mass and ϕ_B is the barrier height. For E > ~1 MV/cm, a Poole-Frenkel (PF) mechanism can be well fitted to the experimental curves for all three samples. This behaviour is consistent with recent literature on MOCVD AlN/Si [67], [87]. In this bias region, the current is given by [86]:

$$J_{PF} = q\mu_{AlN} N_c E_{AlN} \exp\left[\frac{-q\left(\phi_T - \sqrt{\frac{qE_{AlN}}{\pi\varepsilon_{AlN}}}\right)}{kT}\right], \tag{2.17}$$

in which μ_{AlN} is the mobility inside AlN layer, N_c the density of states in the conduction band, ϕ_T the depth of traps in AlN, and ε_{AlN} the permittivity. μ_{AlN} and N_C were taken from literature [88]. The extracted activation energies are 1.30 eV, 1.25 eV and 1.31 eV for samples A8, A31 and A61, respectively, indicating the presence of a defect level in the AlN layer independently of the TMAl predose. With no significant difference in activation energies or current densities, it is assumed in the following that the band alignment between AlN and Si is not modified by the TMAl predose. The possibility of a different interface fixed or trapped charge which could affect the conductivity of the Si surface is now investigated.

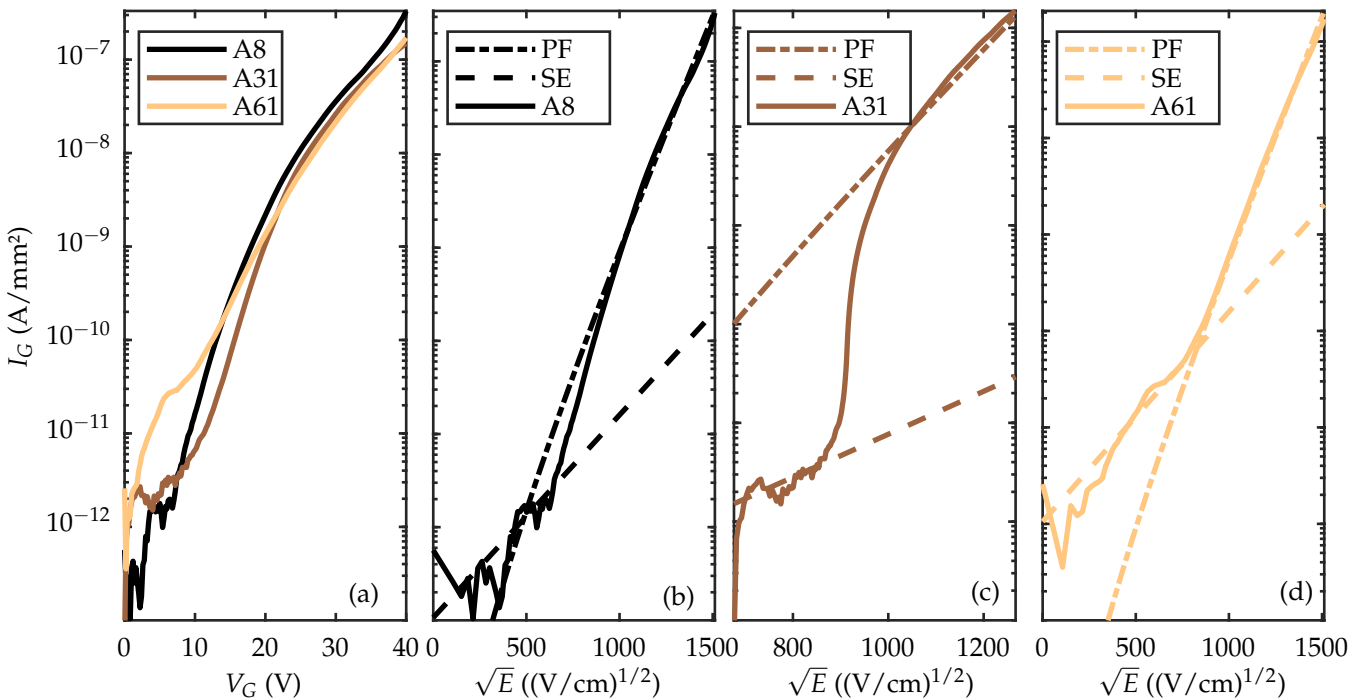


Fig. 2.24 (a) I-V sweeps for all samples from reactor A. (b-d) Leakage current plotted against $\sqrt{E}$ including best fits for SE and PF mechanisms for samples (b) A8, (c) A31, and (d) A61.

2.4.5 Interface charge and traps

Evolution of $Q_{f,int}$ with TMAl predose

Top-down metal-insulator-semiconductor (MIS) capacitor C-V measurements were taken at a frequency of 1 kHz on dot capacitors (area: 0.4 mm²) and are shown in Fig. 2.25. The same trends can be seen in the samples from Reactor B (Fig. 2.26), confirming that the following arguments are valid for different processing environments. A significant V_{FB} shift difference is observed as the TMAl predose is modified. As SRP indicates negligible variation in surface doping and AlN electrical properties appear to be identical for all three samples, the entirety of the V_{FB} shift can be attributed to interface charge. Interface fixed charge can be extracted as described in Section 2.2.1 and V_{FB} is estimated from the $max\left(\frac{d^2C^{-2}}{dV^2}\right)$ criterion. For the samples which present hysteresis, an average between forward and reverse sweep is used. Interestingly, Q_{int} presents a linear evolution with TMAl predose (Fig. 2.27). For low predose (sample A8), a native positive charge exists in the AlN/Si system. This charge could either be natively present in the SiN_x layer or could consist of AlN spontaneous polarization charge, which is positive and of the order of $\sim 1 \times 10^{13}$ cm^{-2} [67], [70]. Then, as predose is increased, the gradual increase of the C fraction in the interfacial layer leads to formation of negative interface charge compensating the initial Q_{int}. Further predose increase can make the interface strongly negatively charged, as in sample A61. A large interface charge (positive or negative) attracts free carriers (electrons or holes, respectively) to the Si surface and causes a decreased ρ_{eff}. For sample A31, the lowest remaining interface charge leads to the highest ρ_{eff}.

Anomalous low-frequency CV for positive $Q_{f,int}$

A positive interface charge for low predose also explains the anomalous "low-frequency" C-V response in inversion regime of sample A8. Indeed, the minority carrier response time in silicon is typically larger than 1 ms and thus, at an AC frequency of 1 kHz only majority carriers at the depletion layer edge can respond, leading to a low measured capacitance in inversion region. To explain this anomaly, consider the TCAD simulations in Fig. 2.28.

With highly positive Q_{int} such as sample A8, an electron inversion layer is present across the entire wafer at a bias of 0 V. For $V_G < V_{FB}$ (Fig. 2.28a, left), holes are attracted under the gate electrode. However, beyond the gate electrode, no bias is applied and the electron inversion layer still exists. This electron-rich layer is separated from the bulk Si and the accumulation

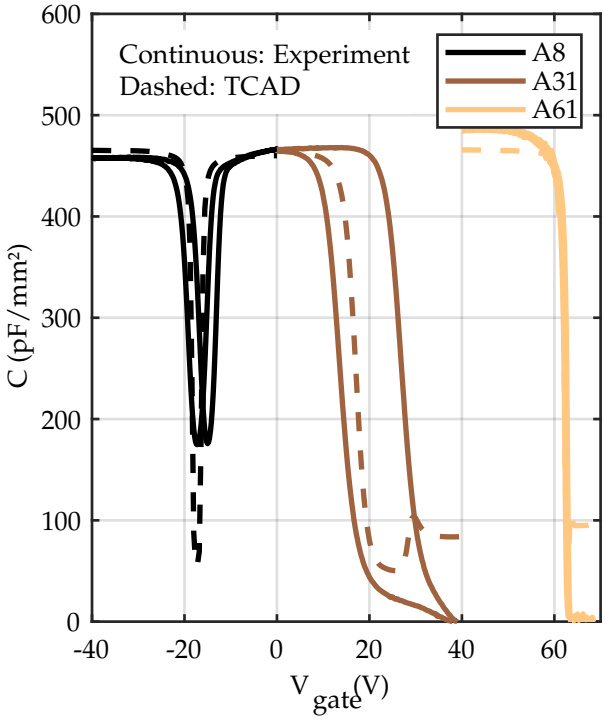


Fig. 2.25 Top-down C-V measurements of the AlN/Si stacks for samples of Reactor A. Vastly different trends are observed depending on the TMAl predose. TCAD modelling taking into account charges, SRP doping and interface traps shows a good match to experiments. f=1 kHz.

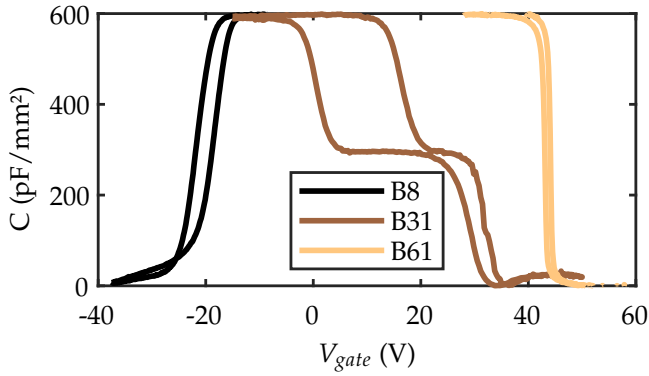


Fig. 2.26 Measured C-V curves for the samples of Reactor B. The trends in Fig. 2.25 are also found here. The apparent intermediate plateau and subsequent drop in C for sample B31 is attributed to deep depletion of the Si substrate that is not well captured by the TCAD model, perhaps because of a difference in sweep rate. f=1 kHz.

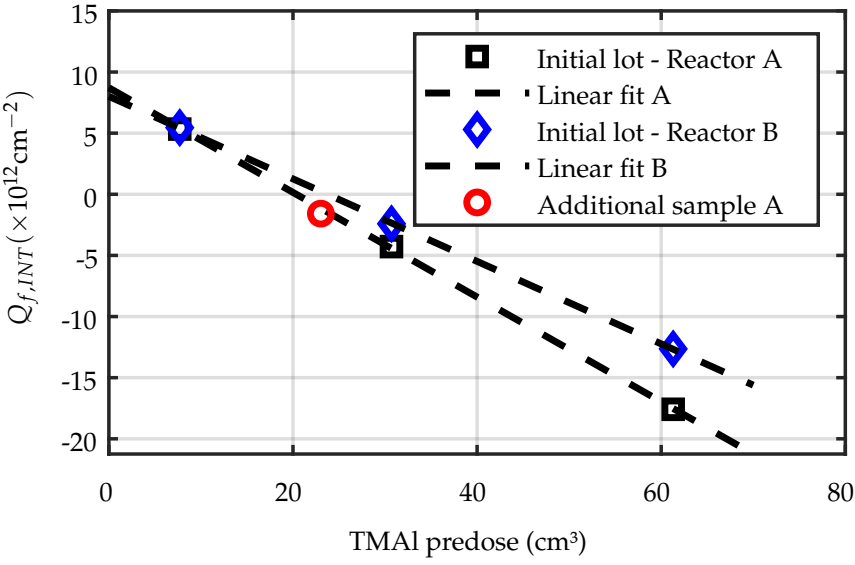


Fig. 2.27 Interface fixed charge extracted from the C-V curves in Figs. 2.25 and 2.26 plotted against TMAl predose. A linear dependence is revealed. The additional sample with intermediate predose confirms the linear trend for reactor A.

layer (p-type) by a resistive pn junction. The area associated with the hole accumulation layer is comparable to the gate electrode. For $V_G > V_{FB}$ (Fig. 2.28a, right), electrons are attracted to the gate electrode. These electrons are directly connected to the electron-rich layer found beyond the gate electrode, making it accessible for AC current to flow and providing a source of minority carriers. The capacitance associated with the extended conductive layer is large and increases the value of the depletion capacitance. Consequently, the measured capacitance rises to a value close to C_{AlN}.

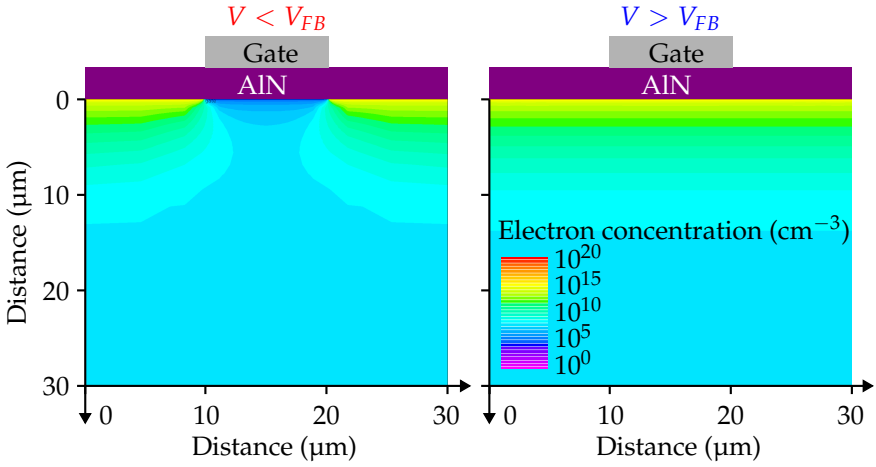
The connection of the conductive electron-rich layer and the depletion capacitance forms a low-pass filter [77]. When the AC frequency is increased (Fig. 2.28b), the effective area contributing to the capacitance decreases, and consequently the measured inversion capacitance decreases. This so-called PSC filter effect is represented in blue in (Fig. 2.28b). On the accumulation side of Fig. 2.28b, the effect of R_s is observed. R_s decreases the measured capacitance in accumulation and depletion, although in a different fashion than the PSC filter effect.

Interface traps

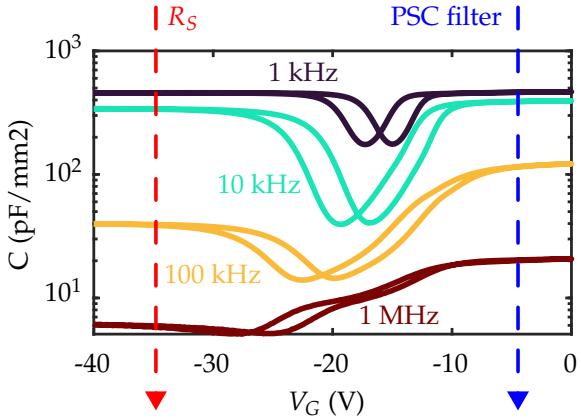
For accurate TCAD modelling, the interface trap density (D_{it}) was extracted for the curves in Fig. 2.25 using the Terman method described in Section 2.2.1. Ideal C-V curves were constructed in TCAD using the SRP doping profiles of Fig. 2.22 to compute the "trap-free" $\phi_s - V_g$ relationship. For the experimental curves, ϕ_s is extracted following the method described in [89]. The difference between ideal and measured $\phi_s - V_g$ then provides a rough estimate of D_{it}. D_{it} of $6 \times 10^{11}\,\mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$, $2 \times 10^{12}\,\mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$ and $4 \times 10^{11}\,\mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$ are extracted at midgap for samples A8, A31 and A61, respectively. When those traps are added as bulk defects into the 5 nm-thick interfacial layer, a reasonably good match between the steady-state TCAD model and experiments is obtained. The higher D_{it} for sample A31 can contribute to the high ρ_{eff}: as the Fermi level at the Si surface is pinned by the high density of traps, the formation of a conductive layer is prevented, and the effective resistivity is high.

Additional ultra-low loss AlN/Si sample

The physical arguments presented above are finally confirmed by fabrication of an additional sample in Reactor A. A predose of $\sim 23\,\mathrm{cm}^{-3}$ was chosen to approach the ideal case of no interface charge in Fig. 2.27. All other process conditions are kept unchanged. As shown in Fig. 2.27, the interface charge extracted from C-V measurements of this additional sample (Fig.

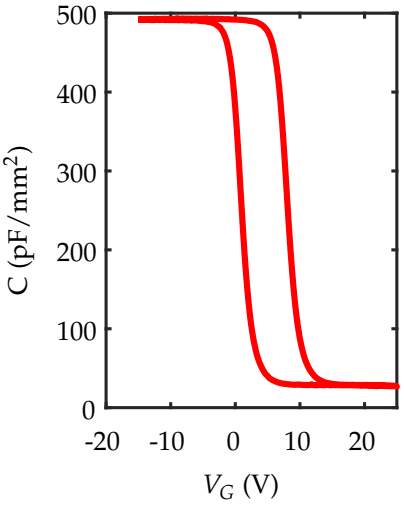


(a) Simulated spatial distribution of electrons in Si for sample A8. (left) $V_G < V_{FB}$ and (right) $V_G > V_{FB}$

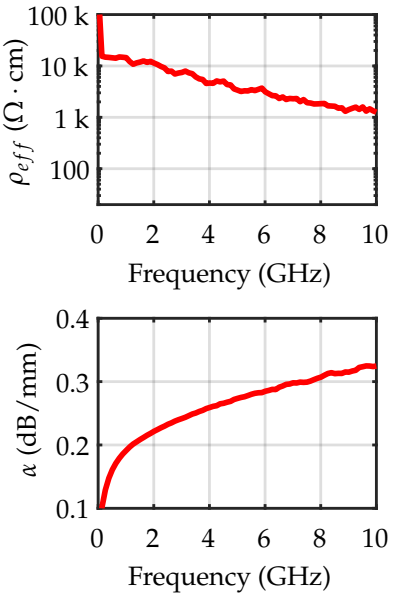


(b) Capacitance measurements for sample A8 at different frequencies. The arrows indicate the phenomenon responsible for the frequency dispersion.

Fig. 2.28 Simulation and measurement insights provide an understanding of the unexpected C-V trend observed in sample A8.



(a) Capacitance measurements, showing a flat-band voltage closer to 0 V correspond to low interface charge. f = 1 kHz.



(b) Effective resistivity and total insersion loss measured on a typical die demonstrate an ultra-low loss substrate. W/S = 17 µm/10 µm.

Fig. 2.29 Electrical characterisation of the additional sample fabricated after optimisation of the TMAl predose.

2.29a) follows the linear relationship found for the initial lot. Furthermore, RF measurements (Fig. 2.29b) reveal exceptionally high $\rho_{eff} > 8\,\mathrm{k\Omega \cdot cm}$ which is above the value of A31.

2.4.6 Bias dependence of substrate performance

The insights gained from previous sections allow a deep understanding of the variation of substrate HD with DC bias for the different samples. These experimental results are presented in Fig. 2.30.

Firstly, it can be seen that the additional sample achieves outstanding HD with H2 = -88 dBm at 0 V, which is comparable to commercially available trap-rich SOI substrates. However, a significant bias dependence is observed for sample A31 and the additional sample. Correlating the onset of the degradation of HD with the $C - V$ measurements of Fig. 2.25, it is clear that HD is degraded when the MIS capacitor is biased in inversion. When V_{FB} is close to 0 V, this implies that substrate performance can be poor even at

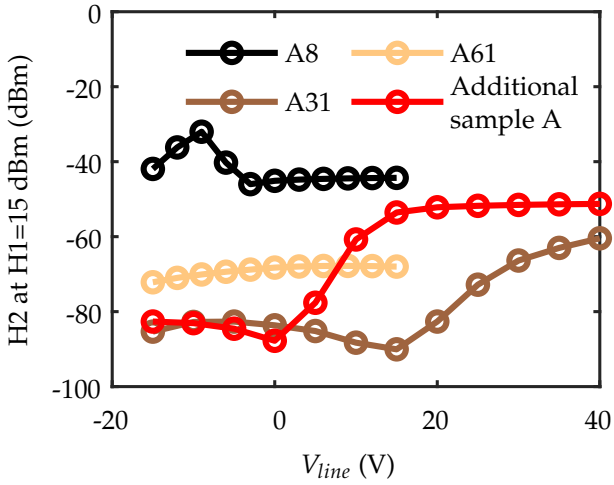


Fig. 2.30 Harmonic distortion measured in dark conditions at 25 °C and a fundamental frequency of 0.9 GHz for all samples fabricated in reactor A, including the additional sample. The bias on the central trace of the CPW line is varied. CPW length = 2 mm. W/S=23.4 µm/12.5 µm.

relatively low bias values.

A similar trend was observed for SOI substrates in [90]. It can be explained by the formation of lateral depletion regions in Si between the region below the signal electrode, which is inverted, and the region below the ground electrode, which is accumulated. These depletion regions are expected to be highly non-linear and contribute to the additional HD.

The bias dependence of HD brings to light an important trade-off between excellent HD (additional sample) and good HD over a wide bias range (sample A31, with a more positive V_{FB}). Furthermore it further shows the importance of TD activation in bulk Si. Indeed, the polarity of Si must be known and controlled in order to choose V_{FB} as positive or negative, and thus avoid the inverted state of the MIS capacitor in relevant operation ranges of DC bias.

However, those requirements become more relaxed as the full 2.505 µm-thick GaN-on-Si buffer is grown. Indeed, the $\sim 10\times$ thicker dielectric will stretch the curves in Fig. 2.30 by a similar factor, i.e. flattening the drastic onset of HD degradation and pushing V_{FB} away.

2.4.7 Guidelines for high-performance GaN-on-Si substrates

The learnings percolating from this section suggest a procedure to reach highly resistive AlN/Si stacks without needing a complex design of experiment (DOE) or the use of additional process steps.

i. Production of one sample with low TMAl predose, corresponding to positive charge in the interfacial layer;
ii. Production of one sample with large predose, corresponding to highly negative charge;
iii. Extraction of the interface charge for samples i and ii;
iv. Linear interpolation to determine the precise predose leading to the close-to-ideal case of no net interface charge.

Furthermore, it can be expected that the methodology described here can be applied for complete HEMT stacks as the upper III-N layers only slightly shift the y-intercept of Fig. 2.27 by formation of additional predose-independent charge. Indeed, it has been observed during the learning cycles of the epitaxy process that the RF loss of full HEMT stacks and the corresponding AlN/Si stacks could be correlated, as shown in Fig. 2.1.

Finally, particular care should be given to the control of bulk Si polarity as well as the relevant range of DC bias in which the substrate will operate, in order to preserve good substrate performance for the entire bias range.

2.5 Chapter summary

In this chapter, the AlN/Si stack was studied as a determining area for substrate-induced parasitic effects in GaN-on-Si technology.

The first part of the chapter discussed the electrical toolbox available to characterize the AlN/Si structure, and more generally all MI(O)S-like stacks aimed at RF applications. The well-known vertical capacitance and conductance measurements are a powerful and versatile technique, even though their interpretation can be made more complicated by the combination of a relatively thick dielectric and a HR Si substrate which increases the series resistance. A more direct measurement of the substrate conductivity was also considered. The backside Hall effect measurement on Van der Pauw samples allows to obtain some information about the conductivity of the bulk and the surface of Si, together with the polarity and mobility. A key advantage of this method is that is does not require the removal of the dielectric layer.

Next, the semi-vertical MI(O)S capacitor structure was introduced as a potential solution to limit the series resistance issue pointed out in vertical C- and G-V measurements. The concept was implemented in a first demonstrator, fabricated in the Winfab facility. Ohmic contacts on the PSC layer were achieved, with however a relatively high contact resistance. The C-V measurements were also demonstrated. The expected decrease in R_s was not observed but potential improvements in the design were pointed out. The semi-vertical structure also allows the fabrication of novel, 3 terminal-structures which function like a MOSFET with the PSC layer as a channel.

Finally and most importantly, a complete understanding of the AlN/Si system was presented, linking process parameters, material properties and electrical characteristics. The main takeaway points are summarized below.

- The change in TMAl predose modifies the composition of the AlN/Si interface. More particularly, the interface is N-rich for low predose values, and C-rich for high predose.
- ρ_{eff} is particularly sensitive to TMAl predose, with an apparent non-linear relationship showing a maximum ρ_{eff} for a certain predose.
- The increase in relative C fraction at the interface comes together with negative fixed charge at the interface. Notably, the charge shows a linear correlation with TMAl predose.

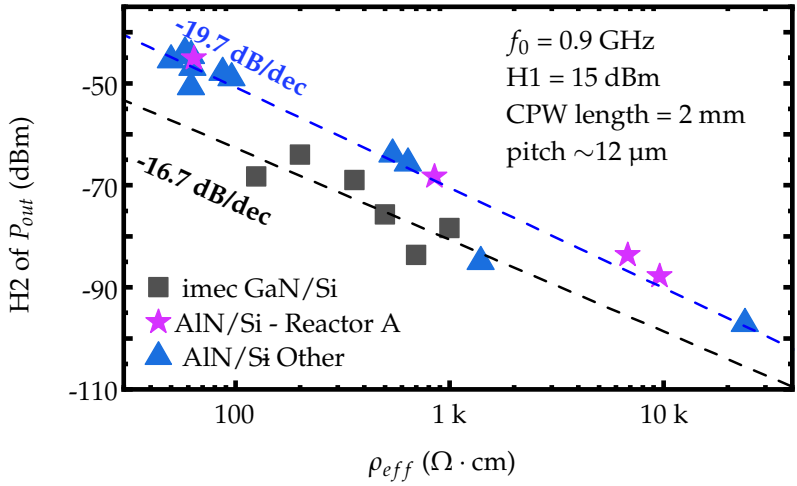


Fig. 2.31 Benchmark plot for small- and large-signal performance of GaN-on-Si substrates and AlN/Si stacks. A correlation is observed between ρ_{eff} and harmonic distortion, with the samples where TMAl predose was varied (pink stars) also following the correlation. The other AlN/Si samples (blue triangles) represent additional samples grown in various MOCVD reactors in various locations.

- By tuning the TMAl predose (a process requiring the fabrication of only two samples and simple characterization), it is possible to achieve an AlN/Si interface with almost zero charge and exceptionally high ρ_{eff}.

The procedure presented for AlN/Si interface engineering can also be applied on full-stack GaN-on-Si substrates.

The interface optimization study has lead to the fabrication of AlN/Si stack with excellent RF performance. As presented in Fig. 2.31, a sample with optimized TMAl predose reaches ρ_{eff} close to 10 kΩ · cm and H2 of -88 dBm.

3

Buffer charge redistribution

3.1 Introduction

In Chapter 2, the interface between the AlN nucleation layer and Si was studied and optimized for reduced substrate loss and non-linearity. In this chapter, the next part of the GaN-on-Si material stack is tackled. Following AlN, a complex strain-relief buffer must be grown. Because of the lattice mismatch between AlN and GaN, direct growth of a GaN layer on top of AlN will lead to a high number of dislocations or even cracks, and more generally a poor crystalline quality GaN layer incompatible with the high mobility requirements of an RF transistor [91]. It is thus necessary to reduce the strain and dislocation density to reach the highest possible GaN channel quality, which is done using a so-called buffer. This buffer can take the form of an Al_xGa_yN graded composition buffer, where the Al fraction is graded from x = 100 % (nucleation layer) to x = 0 % (GaN channel). It allows progressive annihilation of dislocations and subsequent improved crystal quality (Fig. 3.2). However, most of the state-of-the art GaN-on-Si technologies (including imec GaN-on-Si) use a superlattice structure to achieve the progressive improvement of crystalline quality (Fig. 3.1). The superlattice consists in a succession of a high number of thin AlN/AlGaN pairs. The many interfaces created by the superlattice structure are able to effectively filter out dislocations. The overlying GaN layers end up with a decreased dislocation density [92].

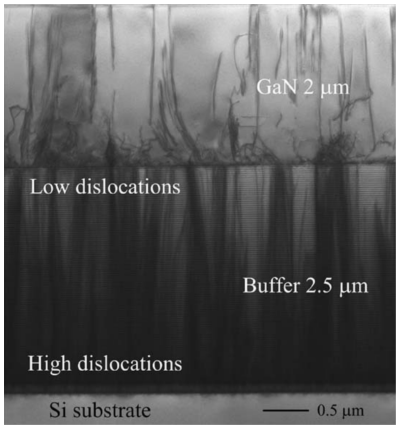


Fig. 3.1 Cross-sectional TEM image of a GaN-on-Si buffer, showing the reduction of dislocation density by using a superlattice buffer. Reproduced from [93]. © 2012 IEEE

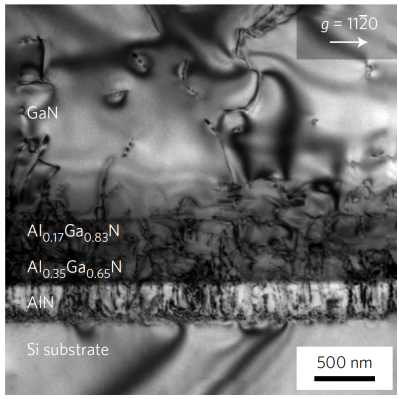


Fig. 3.2 Cross-sectional TEM image of a GaN-on-Si buffer using a 2-step graded Al_xGa_yN strain-relief buffer. Reproduced from [94]. Reproduced with permission from Springer Nature

The final element in the GaN-on-Si stack before reaching the GaN channel of the active device is a GaN buffer. Following the strain-relief buffer, a thick ($\sim$ 1 µm is typical) GaN layer is grown to further improve the crystal quality and reduce the dislocation density. Vertically, the higher dislocation density in GaN-on-Si films compared to GaN films grown on better-matched substrates such as SiC leads to a reduction in V_{br}. For lateral devices, the lower critical field of Si is decreasing the V_{br}. Another contributor to V_{br} decrease are nitrogen vacancies which artificially make the GaN material n-type. To compensate these vacancies, the introduction of a doped GaN buffer has been found to help recover high V_{br} values and reduce he vertical leakage [95]. Fe and C are the two most commonly used compensation dopants in GaN. Since the imec process uses a C-doped GaN buffer (cGaN), this chapter will not discuss Fe doping. The C concentrations used to fabricate highly-resistive buffers range from 10^{18} cm^{-3} to 5×10^{19} cm^{-3}. However, these dopants act as traps: the energy level which they typically occupy in the GaN bandgap is significantly further away from the valence band than kT, preventing them from being fully ionized in all conditions. Consequently, they can give rise to undesired parasitic effects, the most famous of which is the dynamic R_{ON} effect.

Abnormal drift in the HEMT R_{ON} (also called current collapse) when

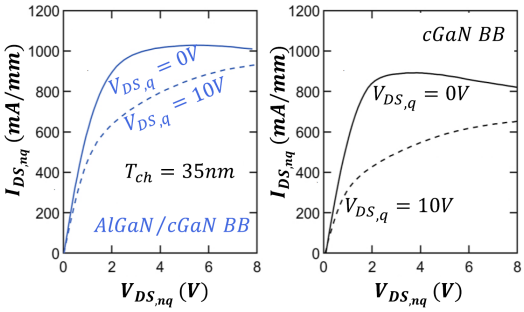


Fig. 3.3 (right) Pulsed-IV evidence of the R_{ON} dispersion effect caused by trapping in the cGaN layer. The effect is more significant when a high quiescent voltage is used. (left) Engineering of the back-barrier can help mitigate the current-collapse in RF HEMTs. Reproduced from [96]. © 2023 IEEE

the device is stressed for a long time is a widely reported issue. Charge trapping occurs in the cGaN layer which in turn causes the 2DEG density at the GaN/AlGaN interface to change over time. Consequently, the device performance can be degraded when a high drain voltage is applied for a long time. It is possible to mitigate the impact on the HEMT performance by engineering the back-barrier of the device, for example with a composite AlGaN/cGaN back-barrier as shown in Fig. 3.3 [96]. The importance of providing sufficient transport paths in the buffer is also a proven leverage [97].

In this chapter, it will be shown for the first time that such dispersion effects can also manifest themselves in RF substrate figures-of-merit ρ_{eff} and HD. This chapter is a deep dive into the bias dependence of substrate FOM, taking into account the time-dependent aspect which is dominating dispersion effects. It is important to measure and understand the bias dependence of ρ_{eff}, as inspection of the ρ_{eff} versus bias curve is often a good indicator of the harmonic distortion of a particular substrate. This correlation between the bias dependence of ρ_{eff} and HD has been shown for SOI substrates [54], but the complex nature of GaN-on-Si epitaxial stacks brings additional effects that should be considered. Furthermore, a degradation of ρ_{eff} with bias is detrimental for substrate-sensitive active blocks such as the RF switch or the power amplifier (see Chapter 4).

In particular, trapping in the cGaN layer is described in the context of substrate loss. A custom experimental setup is developed to demonstrate this effect. Slow trapping/detrapping mechanisms in the upper III-N layers

are shown to effect substrate RF FOM. With help of TCAD modelling, the transient effects are reproduced and guidelines are provided for their mitigation.

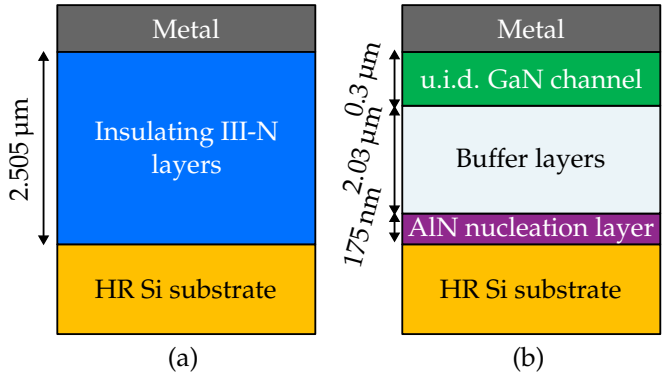


Fig. 3.4 (a) Schematic of a MIS structure in which a single insulating layer is used to represent the III-N epitaxial stack. (b) More accurate 3-layer representation of the epitaxial stack. Charge redistribution takes place in the buffer layers.

3.2 Charge redistribution in GaN-on-Si MIS capacitors

3.2.1 GaN-on-Si as an MIS structure

The complex nature of GaN-on-Si stacks makes modelling them a difficult task, especially in a TCAD environment. Such stacks typically contain more than 10 individual layers with different material properties (see Fig. 3.1). Regarding RF substrate loss description however, it is helpful to treat the CPWs fabricated on a GaN-on-Si stack as simple Metal Insulator Semiconductor (MIS) structures.

As a first step, all the III-N layers (AlN nucleation, buffers and channel) are represented by a single equivalent insulator, such as represented in Fig. 3.4a. This significant simplification allows to apply the well-known theory of Metal Oxide Semiconductor (MOS) capacitors to GaN-on-Si [77]. Several hypotheses need to be verified for it to be valid.

1. Negligible DC current across the III-N layers or Si, in order to assume thermal equilibrium in the Si substrate. As it will become clear later, thermal equilibrium is not achieved in the buffer layers due to charge redistribution but it is required in Si to assume that it responds immediately to the change in buffer charge.
2. No conductive layer inside the epitaxial stack: only free carriers in the Si substrate can respond to small- or large-signal excitation.

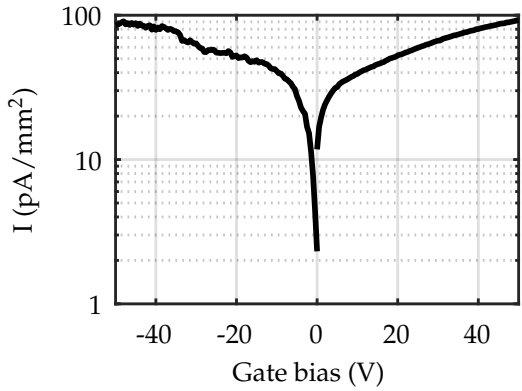


Fig. 3.5 Vertical leakage current measured for a 2.505 µm-thick GaN-on-Si stack with a 175 nm-thick AlN nucleation layer. The growth was stopped before the AlGaN barrier. The current remains under 100 pA/mm^2 for the bias range of interest.

3. Negligible current injection from the CPW metal into the GaN channel, or from the Si substrate into the AlN layer. None of the redistribution mechanisms do modify the total charge of the epitaxial stack.

DC current across the AlN/Si interface exists and has been investigated in Section 2.4.4. However, when the full buffer is grown on top of the nucleation layer, the DC voltage drop across the AlN/Si interface becomes small compared to the applied voltage because the buffer is usually ten times thicker than the AlN layer. The measured DC current for a full stack (Fig. 3.5) ends up being negligible for the range of bias voltages considered here ($|V_{chuck}| \leq 50$ V).

Furthermore, there is no layer in the III-N stack with sufficient conductivity to contribute significantly to conductive RF loss. Free carrier concentration in the bulk III-N materials is many orders of magnitude lower than in silicon and careful optimisation of the buffer structure suppressed any undesired two-dimensional electron/hole gas (2DEG/2DHG). This has been confirmed by capacitance measurements, where capacitance in strong accumulation (C_{acc}) corresponds to the full III-N stack thickness (t_{III-N}):

$$C_{acc} \cong \varepsilon_{III-N} \frac{A}{t_{III-N}} \tag{3.1}$$

Finally, current injection from the top metallization into the GaN channel,

if any, does not contribute significantly to the observed stress/relaxation sequences. As will be described later, passivating the GaN channel with a 140 nm-thick SiO_2 layer does not alter the bias- or time-dependence of ρ_{eff}. The previous considerations allow us to ignore any DC current from the CPW traces to the chuck and to consider the complex GaN-on-Si substrate as a variation of the extensively studied MOS structure with additional charge redistribution mechanisms inside the insulator layers.

3.2.2 Flatband voltage and charge redistribution

For MIS or MOS systems, the number of free carriers at the surface of silicon is determined by the difference between the applied voltage (V_g) and the flat-band voltage (V_{FB}). For example, the electron density at the AlN/Si interface is expressed as (for a n-type substrate):

$$n_{INT} = N_D \exp v_s, \tag{3.2}$$

in which N_D is the bulk doping level and v_s is the band bending at the Si surface. V_{FB} corresponds to the gate voltage to be applied for zero band bending in silicon (i.e., for $n_{INT} = n_D$), and is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_{III-N}}{C_{III-N}}, \tag{3.3}$$

where ϕ_{MS} is the metal-semiconductor workfunction, Q_{III-N} is the equivalent interface buffer charge per unit area contributing to V_{FB} and C_{III-N} is the capacitance per unit area of the semi-insulating III-N layers. In most cases and especially in GaN-on-Si where Q_{III-N} is large, ϕ_{MS} is lower than 1 V and V_{FB} is dominated by the second term of Eq. 3.3. The presence of a non-zero Q_{III-N} will lead to a flat-band shift (ΔV_{FB}) compared with the theoretical charge-free case.

For the classical case of the SiO_2/Si system, the oxide charge is entirely confined in a region close to the oxide/silicon interface and is independent of bias [77]. In such cases, Eq. 3.3 is valid as is, with Q representing the sheet charge at the interface. However, due to the semi-insulating nature of III-N buffers, GaN-on-Si buffer charge can consist of a non-trivial spatial distribution of trapped charges and free carriers. Q_{III-N} is then given by:

$$Q_{III-N} = \frac{1}{t_{III-N}} \int_0^{t_{III-N}} xq(x)dx \tag{3.4}$$

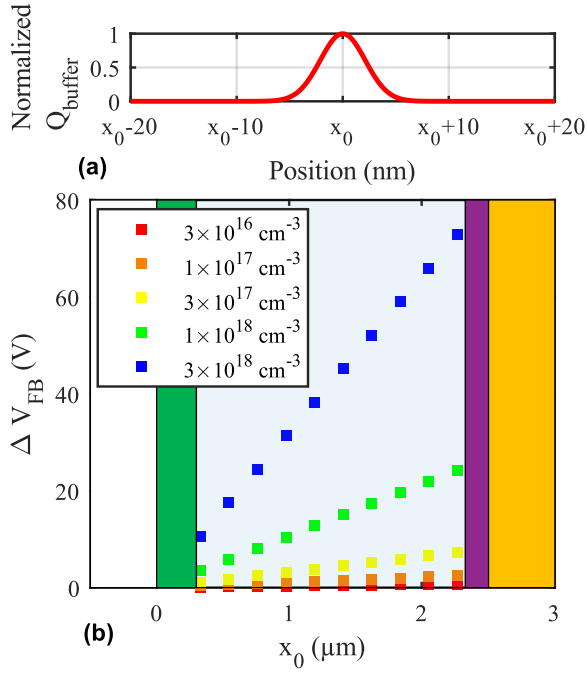


Fig. 3.6 (a) Charge distribution used in the simulated MIS stack. (b) Flat-band voltage shift calculated for the charge distribution shown in (a). The position of the peak charge is varied from the GaN channel/buffer interface to the buffer/AlN interface. ΔV_{FB} depends on the charge density, but also on its position in the buffer.

Where $q(x)$, the space-dependent charge per unit volume, is integrated from the metal/III-N interface ($x = 0$) to the AlN/Si interface ($x = t_{III-N}$). Eq. 3.4 demonstrates that equivalent interface charge, and consequently V_{FB} is dependent on the spatial distribution of charge. For instance, charges located closer to Si will lead to a greater modulation of V_{FB} and consequently of n_{INT}.

As will become apparent in the following sections, the charge distribution in the III-N layers is dependent on time and bias. Under non-equilibrium conditions, charge redistribution can take place, thus modifying the Q_{III-N} according to Eq. 3.4.

3.2.3 Modelling

Flat-band voltage

Following the theoretical considerations of Section 3.2.1 for a 2-layer (III-N and Si) MIS system, a slightly more complex system is now considered in a TCAD environment to better represent the physical epitaxial stack (Fig. 3.4b). This stack contains three layers:

1. The AlN nucleation layer, which does not contain mobile charge;
2. The buffer layers are replaced by a single equivalent layer, in which charge redistribution is taking place;
3. The unintentionally doped (u.i.d.) GaN channel. A background doping (n-type) is considered, with $N_D = 1 \times 10^{16}\,\mathrm{cm}^{-3}$.

The Si substrate is n-type. As is often the case in GaN-on-Si, the thermal budget associated with epitaxial growth leads to activation of TDs, inverting the polarity of the entire Si wafer from p-type to n-type. The bulk and surface doping levels are corresponding to SRP measurements. Instead of C trap levels in the buffer, a simple positive charge distribution $q(x)$ sharply localized around a variable depth x_0 is added (Fig. 3.6a). The DC simulation is repeated for different values of x_0 and $q(x)$.

Firstly, Fig. 3.6b shows the calculated ΔV_{FB} for this MIS structure according to Eq. 3.3. As an example, a charge peak with a density of $1 \times 10^{18}\,\mathrm{cm}^{-3}$ located at $x_0 = 1\,\mu\mathrm{m}$ from the GaN channel surface causes a flat-band shift of ~10 V. By sweeping the position of the peak charge x_0 from the GaN channel/buffer interface to the buffer/AlN interface, the integrand in Eq. 3.4 is modified and consequentlyΔV_{FB} changes by a factor exceeding 3. While the effect is limited for low charge, for the highest charge density studied ($3 \times 10^{18}\,\mathrm{cm}^{-3}$, comparable to active C doping concentration in GaN-on-Si buffers [98]), up to 60 V shift is theoretically possible.

Interface carrier concentration

Secondly, the resulting change in ρ_{eff} is considered. The shift in V_{FB} caused by charge redistribution across the semi-insulating layers will in turn affect the conductivity of the PSC layer (G_{PSC}) and ρ_{eff}. Indeed, changing V_{FB} is equivalent to applying a corresponding bias on the MIS structure, attracting or pushing free carriers away from the AlN/Si interface. The carrier concentration will be modulated according to Eq. 3.2 and PSC conductivity

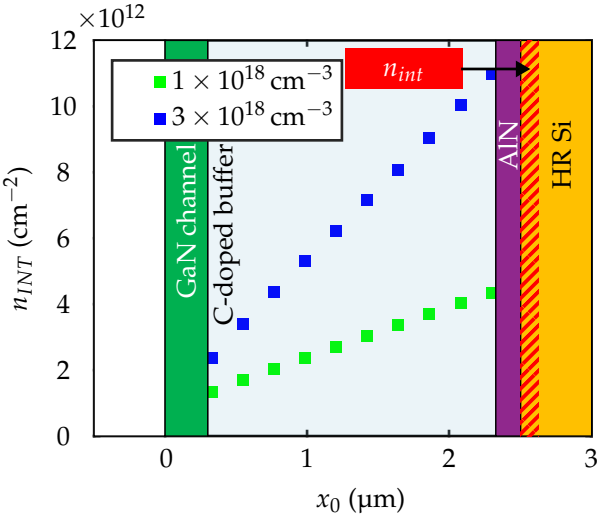


Fig. 3.7 Interface free carrier sheet density for different positions of the localized charge. For high peak charge, n_{INT} is strongly affected by buffer charge location.

will be affected accordingly:

$$G_{PSC} \sim q\left(p_{INT}\mu_p + n_{INT}\mu_n\right). \tag{3.5}$$

Because of the non-uniform doping profile in Si, the execution of this exercise is more practical in a TCAD environment. Fig. 3.7 shows the simulated evolution of free electron concentration close to the surface of a high-resistivity n-type Si substrate (n_{INT}) for different positions of a positive charge distributed according to Fig. 3.6a. n_{INT} was obtained by integrating the electron concentration n over the first µm of Si.

A reliability issue for low-loss substrates

It is important to mention that the considerations above only become relevant for high-ρ_{eff} substrates. To exemplify this, consider the 2D extension of the 1-D system of Fig. 3.4. Electrodes are added on top of the III-N stack to represent the cross-section of a CPW line. A small-signal simulation of this 2D structure allows extraction of ρ_{eff} as a function of the position of the localized charge x_0. Three different Si substrates are considered for the simulation. The p-type doping profile close to Si surface responsible for the PSC layer and measured by spreading resistance profiling (SRP) is included

and multiplied by 1 (physical profile), 10 and 100 (hypothetical high-loss substrates) to obtain ρ_{eff} values of 1100 $\Omega \cdot$ cm, 550 $\Omega \cdot$ cm and 120 $\Omega \cdot$ cm, respectively.

As expected from Section 3.2.3, ρ_{eff} is affected by the position of the charge peak (x_0) for all substrates, as shown in Fig. 3.8. The simulated ρ_{eff} has been normalized to its value when x_0 is in the middle of the buffer. However, the relative variation is more significant for the high-ρ_{eff} substrate (up to ~15 % variation) than for the low-ρ_{eff} one (negligible variation). Indeed, a given ΔV_{FB} will impose a charge compensation in Si, Δn_{INT}, that is independent of the substrate resistivity. In case of a high ρ_{eff}, the initial n_{INT} is relatively low, so that:

$$\Delta n_{INT} \gg n_{INT}. \tag{3.6}$$

Consequently, a significant ρ_{eff} modulation is achieved. However, for a highly conductive PSC layer (low ρ_{eff}), the number of free carriers at the interface is very large. The flatband shift being independent of Si, the following relation is verified:

$$\Delta n_{INT} \ll n_{INT}, \tag{3.7}$$

and the relative ρ_{eff} modulation is lower.

Furthermore, this implies that the buffer charge redistribution has a more significant effect at room temperature. As temperature increases, thermally generated free carriers in the Si substrate contribute to its conductivity increase, and thus the decrease of the ρ_{eff}. This effect has been discussed in detail in Chapter 1. Consequently, the relative variation of ρ_{eff} during the stress experiments at 190 °C is expected to be more limited compared with 50 °C.

Inclusion of C traps and transient simulation

Now that the interplay between the spatial distribution of charge and ρ_{eff} has been discussed, the actual C doping can be included in the model to match experimental data. Carbon is modelled as a dominant acceptor trap level ($E_t = E_v + 0.9$ eV), compensated by shallow donor traps with a compensation ratio of 50%. The capture cross-section is set to 1×10^{-13} cm^{-2}. This is the most common way of representing C doping in GaN-on-Si [99]. The acceptor traps can be neutral when empty or negatively charged when ionized (filled with an electron).

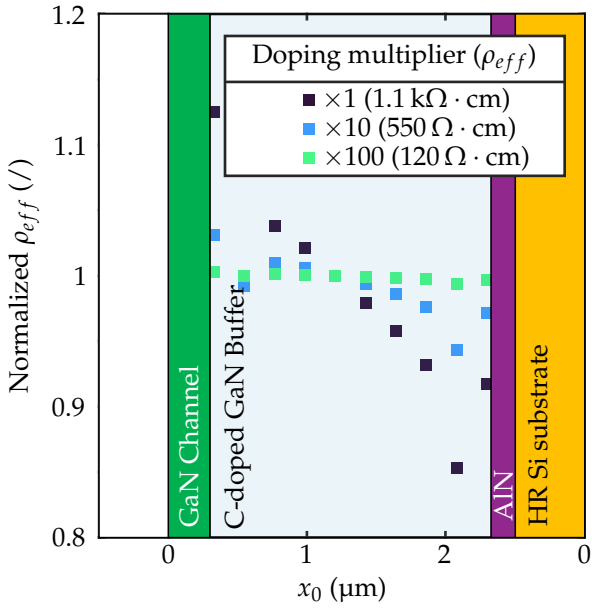


Fig. 3.8 Variation of normalized ρ_{eff} as a function of the position of the localized charge (peak density: 3×10^{17} cm^{-3}) for three different substrates showing typical ρ_{eff} values. The relative variation is strongest for the substrate showing highest ρ_{eff}.

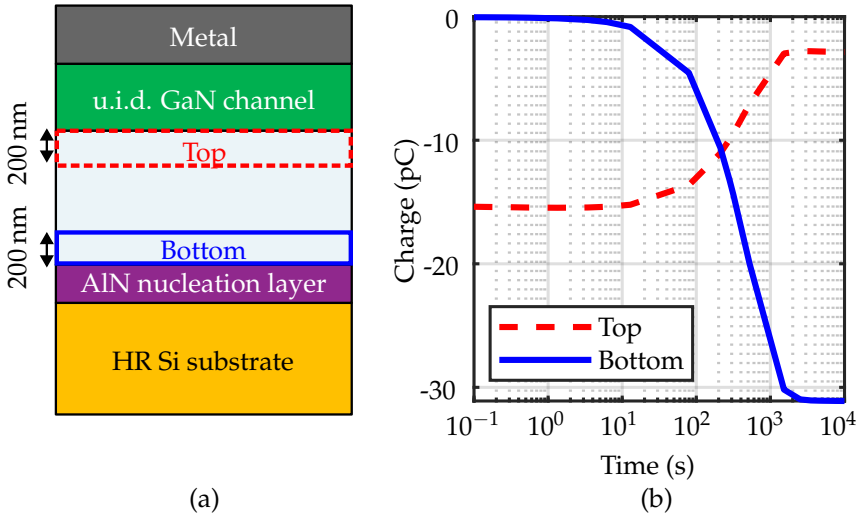


Fig. 3.9 (a) Schematic of the simulated structure, with the regions of interest highlighted. The C doping is set to $1 \times 10^{19}\,\mathrm{cm}^{-3}$ and the simulated area is 1 $\mu\mathrm{m}^2$. (b) Simulated evolution of space charge (consisting mainly of ionized C traps) responding to a bias step from 0 V ($t < 0$) to +50 V ($t > 0$). The charge redistribution is taking place over ~1000 s. Temperature is set to 25 °C

To exemplify a typical charge distribution process, a voltage step from 0 V ($t < 0$) to +50 V ($t > 0$) is imposed on the Si substrate. The space charge (consisting mainly of ionized C traps) is then tracked over time. Two regions of interest are considered, in which the charge is integrated: the top and bottom of the C-doped buffer. Times greater than 100 ms are considered to ensure the Si substrate is at thermal equilibrium [100]. Then, the voltage drop across Si is negligible compared to the voltage drop across the III-N stack.

The positive voltage imposed on the substrate attracts negative charge towards the bottom of the buffer and positive charge at the top. C traps at the bottom of the buffer progressively become ionized, which can also be seen as emitting holes. The holes then move towards the top of the buffer to be captured by ionized traps, making the top of the buffer progressively less negatively charged. This redistribution process can be seen as a gradual change in the $q(x)$ function in Eq. 3.4, which in turns modifies V_{FB}. This can be more clearly seen by analyzing vertical cutlines taken at increasing stress

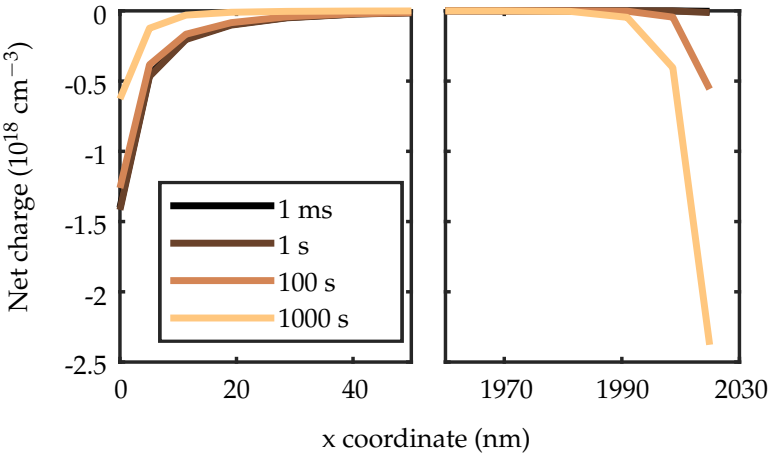


Fig. 3.10 TCAD simulated evolution of space charge (consisting mainly of ionized C traps) responding to a bias step from 0 V ($t < 0$) to +50 V ($t > 0$). Cutlines are taken at increasing stress times. The X coordinate is measured from the upper surface of the C-doped buffer. Temperature is set to 25 °C

times, as shown in Fig. 3.10, which is a different view of the simulation performed in Fig. 3.9.

The conduction process for holes and more generally the modelling of the response to a step in bias is discussed in more detail in Section 3.5.

In the next sections, an experimental study of the time-dependent processes introduced here is presented and interpreted with help of the charge redistribution concept.

3.3 Devices and characterization setup

3.3.1 Samples under study

The samples of interest for the study of time dependence of ρ_{eff} are represented in Fig. 3.11. The epitaxial stacks (samples A1,A2,A3 and B) used in this study have been grown using imec's GaN-on-Si buffer recipe, in a Veeco Turbodisc Maxbright reactor. All III-N/Si samples use a starting HR Si wafer originating from the same supplier. These p-type (B doping) wafers have a nominal resistivity specified between 3 and 6 $k\Omega \cdot cm$ and their interstitial oxygen concentration is not specified. In addition to the epitaxial stacks, an oxidized HR Si wafer is also studied as a reference (Sample C). Here, the nominal resistivity of the Si wafer is $>5\,k\Omega \cdot cm$. A 200 nm-thick SiO_2 layer was deposited by plasma-enhanced physical vapour deposition (PECVD) to reproduce a typical HR SOI substrate used for partially-depleted (PD) SOI technology. The main characteristics of each sample are summarized in Table 3.1 and are detailed hereafter.

Sample name	Starting Si	Epitaxial stack	Additional processing
A1	3-6 kΩ · cm	Full ∼ 2.51 µm GaN-on-Si HEMT buffer	CPW metal
A2	3-6 kΩ · cm	Full ∼ 2.51 µm GaN-on-Si HEMT buffer	140 nm SiO_2 + CPW metal
A3	3-6 kΩ · cm	Full ∼ 2.51 µm GaN-on-Si HEMT buffer	140 nm SiO_2 + N isolation implant + CPW metal
B	3-6 kΩ · cm	175 nm AlN nucleation layer	8.5 nm Al_2O_3 + CPW metal
C	>5 kΩ · cm (n-type)	200 nm PECVD SiO_2	CPW metal

Table 3.1 Description of the samples used in this study

Sample A1 comprises the full HEMT buffer stack including the 300 nm-thick GaN channel. To avoid the highly conductive 2DEG at the surface of the channel, growth was stopped before the AlGaN barrier forming the heterojunction. Sample A2 underwent the same epitaxial grown as sample A1. Additionally, a 140 nm-thick SiO_2 layer was deposited after the growth. The purpose of this layer is to prevent any leakage current across the III-N layers and verify that the observed phenomena are not caused by such leakage. Indeed, while the materials used are semi-insulators, a non-negligible leakage current could exist at high vertical electric fields and potentially cause transient effects. Sample A3 also has the same epitaxial stack as samples A1 and A2 and the additional SiO_2 layer like sample A2. Then, the 3-step N isolation implant is performed. The implant procedure and its impact have been described in Chapter 1. Both implanted and un-implanted stacks are of importance. The implanted epitaxial stack is seen by all passive structures such as transmission lines and inductors. The un-implanted stack will lie below active circuitry such as the RF Switch or PA which are sensitive to substrate loss and distortion (see Chapter 4).

For sample B, growth was stopped after the AlN nucleation layer. Then, a $\sim$ 8.5 nm-thick Al_2O_3 layer was deposited using atomic layer deposition (ALD). The deposition was performed in a Cambridge Nanotech Fiji equipment available in the Winfab platform. The purpose of the Al_2O_3 passivation can be understood from Fig. 3.12, which shows the vertical current density (current per unit area) for un-passivated and passivated AlN. Un-passivated AlN shows a moderate current density for a small-area electrode but a significantly higher current density for a large-area electrode. It is known that current across epitaxial AlN layers can flow through pits [101]. A limited number of pits are present under the 0.01 mm² electrode and much more under the 1.5 mm² electrode, allowing more current which does not necessarily scale linearly with area. A high leakage current makes applying bias on the CPW line difficult and is an artefact of treating with an AlN-only stack (i.e., it would not be present for full-stack samples, where vertical leakage is more limited). After ALD passivation, the current is suppressed.

Finally, sample C represents a SOI reference which is not expected to show any transient phenomena.

Following sample fabrication and processing, CPW metal was deposited and patterned on all samples.

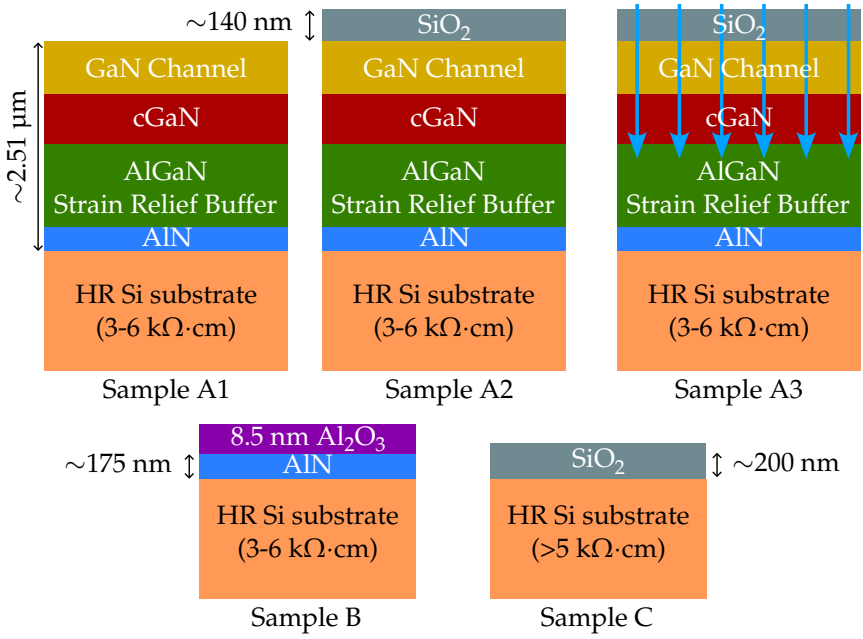


Fig. 3.11 Representation of the different samples used to study time-dependent phenomena in GaN-on-Si stacks.

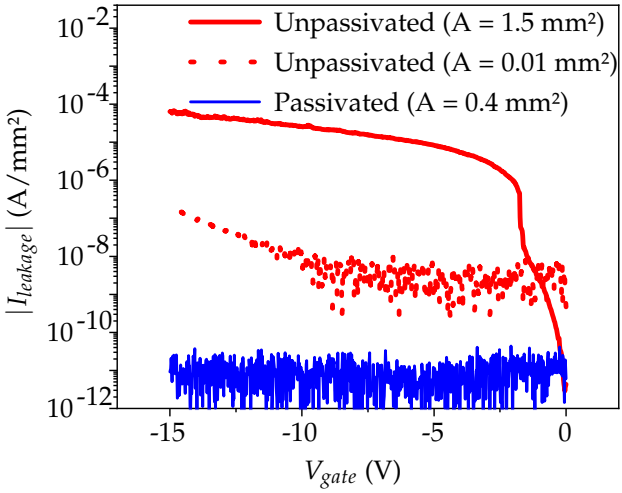


Fig. 3.12 A high leakage current across the AlN layer can take place. The current density is significantly higher on large-area electrodes, indicating the contribution of pits. Al_2O_3 passivation of the AlN layer suppresses the leakage current.

3.3.2 Characterization procedure

The small- and large-signal setup is identical to what has been described in Chapter 1. Two different measurement procedures are investigated here.

Hysteresis measurement

In the first one (hysteresis measurment), the chuck bias is swept in the following sequence: 0 V $\longrightarrow |V_{max}| \longrightarrow -|V_{max}| \longrightarrow$ 0 V. Chuck bias is swept rather than CPW central conductor bias to ensure a uniform polarization of the interface. The bias ramp rate is set to 10 V/min. The value of V_{max} is 50 V for full GaN-on-Si stacks but is adapted to 15 V for samples B and C which have much thinner dielectric layers.

Stress-relaxation sequences

In the second sequence (represented schematically in Fig. 3.13), stress-relaxation sequences are imposed on the chuck. Chuck bias and VNA trigger are synchronized by the controller PC, which also tracks stress and relaxation time. Logarithmically spaced time delays are imposed between each RF measurement, represented by the blue squares in Fig. 3.13. The time resolution and smallest time step of this setup is of ∼100 ms, corresponding to the sum of PC-VNA communication, VNA acquisition and VNA saving

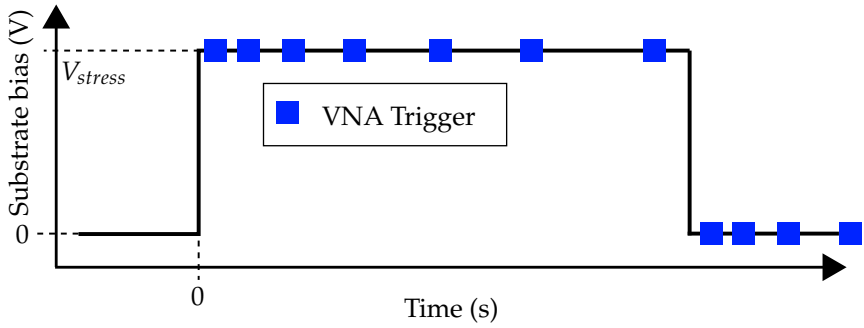


Fig. 3.13 Schematic of the stress-relaxation measurement sequence. The VNA trigger sequence is controlled by a Matlab script on the controller PC.

times. DC bias ramp time is shorter than 1 ms. Only 11 frequency points are measured around a frequency $f_0 = 2$ GHz to reduce the VNA acquisition time associated with a full frequency sweep. In sufficiently resistive substrates ($\rho_{eff} > 2$ k$\Omega\cdot$ cm), 2 GHz is high enough for the CPW line to have transitioned from the slow-wave mode to the quasi-TEM mode. This truncation of the frequency sweep was also adopted in the first measurement sequence.

Application to large-signal measurements

To apply the stress-relaxation sequence to large-signal measurements and obtain sufficient time resolution, it is necessary to reduce the duration of the power sweep usually associated with such measurements. To do so, only 5 points of the input power sweep were used, centred around $P_{in} = 15$ dBm. A power level of 15 dBm is chosen for its common use in substrate linearity reports.

Front side and chuck bias

Throughout this chapter, the bias is applied to the chuck (backside) rather than on the central conductor of the CPW line. This latter choice is typical in SOI literature and allows straightforward correlation (in terms of flatband voltage) with $C - V$ measurements where bias is also applied on the front side.

The reasons for preferring chuck bias in the experiments presented here are twofold.

1. The internal bias tees of the VNA are limited to ± 40 V. This means that applying more than 40 V between the signal (central trace of the

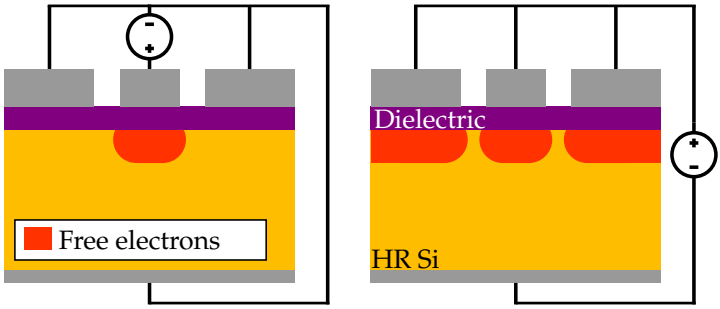


Fig. 3.14 Schematic representation of the free electrons distribution when the bias is applied on the signal trace of the CPW line (left) or on the chuck (right).

CPW line) and the ground (ground planes of the CPW line) of the coaxial RF cable requires the use of external bias tees. It is thus easier to apply the bias directly on the chuck and keep the signal and ground traces of the CPW line at the same DC bias.

2. Applying the bias on the chuck leads to a potential difference between the chuck and all traces of the CPW line, versus only the central trace in the classical case (Fig. 3.14). This induces a more uniform distribution of the free carriers at the Si surface, which is preferred because CPW measurements can then be better interpreted with 1-D charge redistribution models.

In addition, the existing literature for AlGaN/GaN HEMTs (R_{ON} degradation experiment) also generally considers a backside bias.

It should be noted that physical surface state obtained with the bias applied on the chuck corresponds to the opposite bias applied on the central conductor. For clarity, graphs as a function of DC bias employ a $-V_{chuck}$ on the x-axis, which can be understood as an equivalent top bias.

3.4 Hysteresis in GaN-on-Si substrates

3.4.1 Harmonic distortion prediction by inspection of effective resistivity versus bias curves

In SOI technology, a correlation between harmonic distortion and ρ_{eff} has been observed for a wide variety of samples in [54]: as ρ_{eff} increases, the substrates were observed to be more linear. More specifically, while the absolute value of effective resistivity had an impact, it was the bias dependence of ρ_{eff} that had the most significant influence. Varying the bias applied on the CPW line and measuring the $\rho_{eff}(V_{bias})$ (or $G(V_{bias})$, which is equivalent) curve could then provide a first-order prediction of harmonic distortion.

The link between $\rho_{eff}(V_{bias})$ and harmonic distortion has recently been shown to be more subtle [100]. Indeed, the small-signal bias sweep is taken at thermal equilibrium of the Si substrate for each bias point, whereas the large-signal excitation presents a period that is too short to ensure continuous equilibrium. Consequently, the two measurements do not take place in the same conditions from the point of view of Si. For instance, the Si surface polarity cannot be inverted as a response to the 900 MHz large signal, as thermal carrier concentration requires at least a few ms. However, free carriers can still be attracted or pushed away from the Si substrate in such short times if sufficient reservoirs are available (e.g. a PSC layer directly connected to the region below the CPW line).

While the HD-$\rho_{eff}(V_{bias})$ correlation is not so straightforward, the bias dependence of ρ_{eff} can still be used as a tool for bias regions relatively far from the flatband voltage. A highly bias-dependent ρ_{eff} is likely to be a signature of a strongly non-linear substrate.

In GaN-on-Si, further issues related to time dependence are preventing this simple techniques to be used. This section demonstrates those issues experimentally.

3.4.2 Origin of hysteresis in effective resistivity

The results of the so-called hysteresis measurements for all considered samples are displayed in Fig. 3.15. For the samples presenting hysteresis, the peak voltage difference (ΔV_p) is defined as the difference, in volts, between the two points where ρ_{eff} is maximal (forward and reverse seep). Because ρ_{eff} is normally highest around the flatband voltage V_{fb}, ΔV_p can be seen as a measure of the flatband voltage shift induced by time-dependent

effects.

Full HEMT un-implanted stack

Sample A1 (full stack, no passivation or implant) shows a significant hysteresis, with $\Delta V_p = \sim 40\,\text{V}$. This is in strong contrast with sample B (passivated AlN/Si), for which the two sweep directions are superposed. Because the Si substrate and AlN/Si interface are identical for samples A and B, the cause for the hysteresis can be pinpointed to the III-N layers. Furthermore, a similar trend is seen for both samples Al and A2 (full stack with 140 nm SiO_2 passivation), which indicates that vertical leakage or carrier injection is not the cause of the observed behavior as the thick passivation layer in sample A2 would effectively prevent any DC leakage.

The voltage ramp rate (10 V/min) imposed on the chuck is too slow to put the Si substrate out of equilibrium [100]. However, it seems to be shorter than the time constant of buffer charge redistribution processes. The considerations of Section 3.2.1 point to an explanation for the hysteresis.

When the chuck bias is changed, charge redistribution occurs continuously in the C-doped III-N buffer layers. The equivalent charge seen by Si (Q_{III-N}) is modified and so is V_{FB}. When the bias reaches $V_{chuck} = 50\,\text{V}$ (first quarter of the total sweep), the flatband voltage of the MIS structure is different than in the beginning of the experiment as some redistribution has occured. Because the time constants corresponding to the redistribution processes are significantly longer than the duration of a voltage sweep (and perhaps asymetrical), the flatband voltage at 0 V on the reverse sweep is different than before the measurement. Consequently, a flatband voltage shift is observed.

The Si substrate responds to both the change in V_{FB} and in V_{chuck} in a complex manner, but can be considered instantaneous with respect to the voltage ramp rate. The charge imposed by the change in V_{chuck} can be provided by both Q_{III-N} and free carriers at the surface of Si. A simpler experiment to better isolate the contributions is described in the next section.

Compared to SOI substrates, an additional layer of time dependence now has to be considered when investigating the response of the GaN-on-Si substrate to large-signal excitation. The relevant time scales are as follows.

- $\sim 1\,\text{ns}$: period of the large signal
- $\sim 1\,\text{ms}$: time required for the Si substrate to reach thermal equilibrium
- $10 - 10,000\text{s}$: time required for the III-N buffer to achieve equilibrium through charge redistribution processes.

Because of the buffer charge redistribution, the inspection of a $\rho_{eff}(V)$ to predict HD is impractical.

AlN/Si and SOI reference

The $\rho_{eff}(V_{chuck})$ trend of samples B and C can be correlated to their top-down metal-insulator-semiconductor (MIS) capacitance-voltage curve in Fig. 3.16: ρ_{eff} is highest at bias points close to the depletion region of the C-V curve. For samples B and C, the difference in ρ_{eff} between the positive and negative chuck bias regions can be explained by the higher mobility of electrons compared to holes. An electron-rich PSC layer is favored by negative V_{chuck}, causing a lower ρ_{eff} in that region.

Interestingly, conductivity at 0 V is n-type for sample B, despite a starting p-type bulk Si and Al/Ga back-doping during AlN growth. This inversion of the polarity of the bulk Si has already been described in Chapter 1 and can be linked to activation of TDs induced by interstitial oxygen atoms. This is the reason why sample B has C-V characteristics similar to an n-type SOI substrate such as sample C.

Implanted stack

Compared to the un-implanted samples A1 and A2, samples A3 shows a lower ρ_{eff}, which is attributed to an additional buffer fixed charge, but limited hysteresis. Actually, while ρ_{eff} is slightly decreased, the implant step leads to a strong reduction of its bias dependence, especially for positive V_{chuck}. This is attributed to possible Fermi level pinning in the upper half of the GaN bandgap due to N-implantation. The very large density of defects induced in the buffer layers by N ions could lead to the formation of a trap-rich-like buffer, which then supports most of the charge to compensate V_{chuck}. Buffer charge redistribution and change in the free carrier population at Si surface then become negligible. This effect seems to be most significant in one part of the bandgap, where the N-induced defect levels are found. It is predicted that these levels lie about 1 eV from the conduction band [50], [103].

3.4.3 Temperature dependence of hysteresis

To further investigate the dynamic effect, $\rho_{eff}(V)$ scans were performed at different chuck temperatures (Fig. 3.17). A decrease in overall ρ_{eff} can be observed due to lower bulk HRSi resistivity at higher temperatures (see also Section 1.5). More interestingly, the hysteresis reduces with temperature. For example, a ΔV_p of only ~10 V is observed at 175 °C as compared to ~40

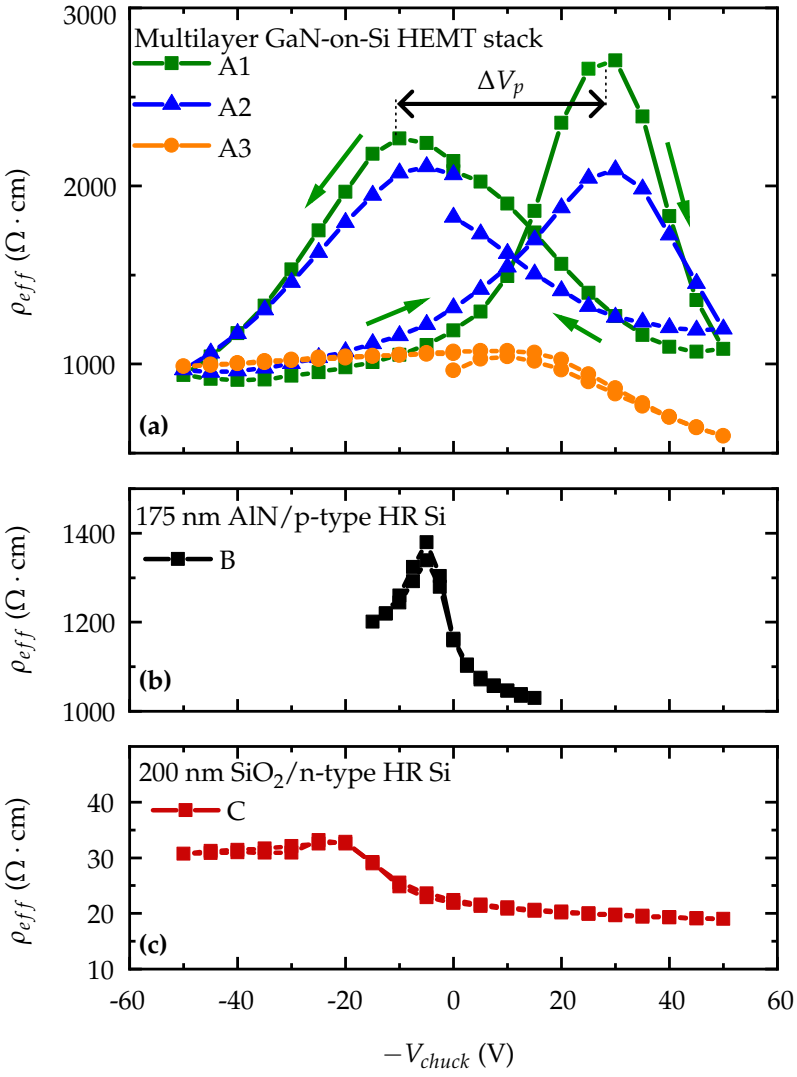


Fig. 3.15 Bias dependence of ρ_{eff} for all studied samples at room temperature. The significance of the hysteresis can be quantified with the ΔV_p quantity. For all samples, CPW slot width is S = 50 µm and bias ramp rate is 10 V/min. Temperature is 25 °C. Reproduced from [102]. ©2021 IEEE.

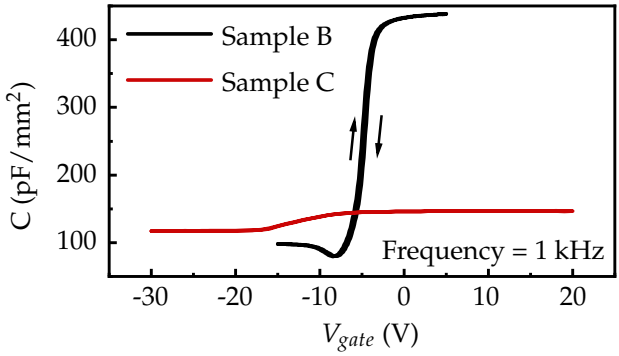


Fig. 3.16 Top-down MIS C-V measurements for sample B (AlN/Si) and C (SiO_2/n-type HR Si reference). Reproduced from [102]. ©2021 IEEE.

V at 25 °C. This can only indicate an acceleration of the charge redistribution as temperature increases. The high temperature [$\rho_{eff}(V)$] curve is thus closer to an equilibrium curve. In [104], it was shown that time constants in heavily C-doped buffers strongly decrease with temperature. Consequently, hysteresis related to the slow emission of buffer traps reduces, and the high temperature [$\rho_{eff}(V)$] curve is closer to an equilibrium curve.

Because the chuck bias is varied continuously in the hysteresis experiment, it is difficult to obtain an estimate of the time a GaN-on-Si stack needs to reach thermal equilibrium. In the next section, the response of $\rho_{eff}(V)$ to a more simple bias step will be examined.

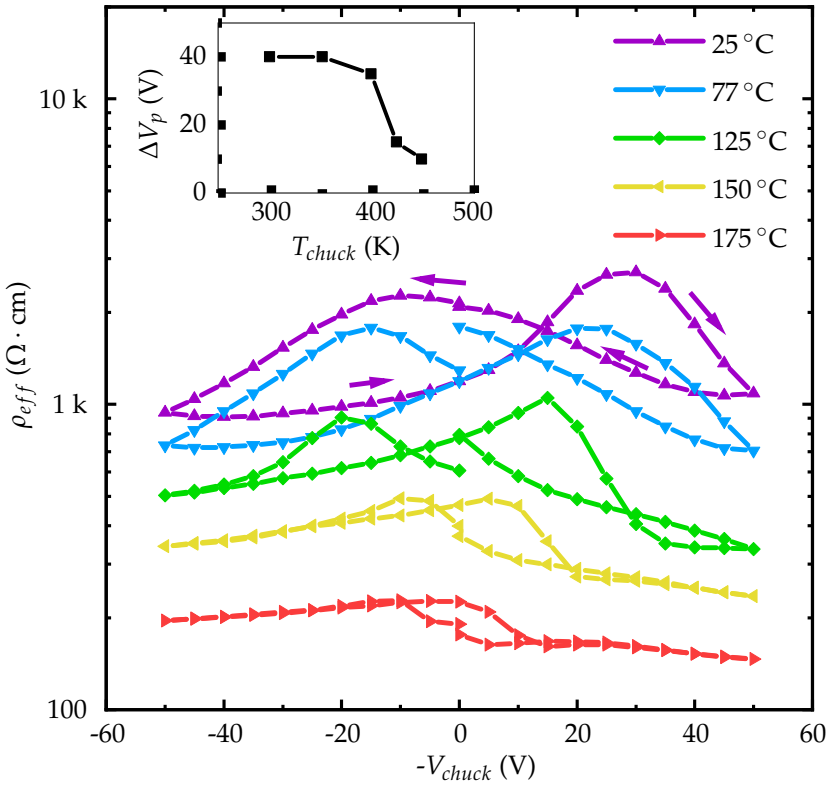


Fig. 3.17 ρ_{eff} of sample A1 versus chuck bias at different chuck temperatures. Both ρ_{eff} and the hysteresis decrease as the chuck temperature is increased. Inset : the trap-induced flatband shift (measured by ΔV_p) is lower at higher temperatures. Reproduced from [102]. ©2021 IEEE.

3.5 Stress-relaxation sequences and their modelling

A backside bias step constitutes a simpler stimulus compared to a continuously varying voltage. Furthermore, the GaN-on-Si stack is inevitably experiencing a stressed condition in an actual circuit: drain bias values can be on the order of several tens of volts, sustained for a long time. The stress-relaxation sequences thus constitute an important case study from the application perspective as well.

From a more fundamental point of view, stress-relaxation sequences taken at different temperatures can allow extraction of activation energies in order to elucidate the limiting mechanism.

3.5.1 Time dependence of effective resistivity under stress

The small-signal stress-relaxation sequences are taken at temperatures ranging from 50 °C to 190 °C. Effective resistivity is extracted and normalized at each temperature to the second measured point. The normalization ensures that only time-dependent processes in the buffer are observed and discards the temperature-dependence of ρ_{eff}. The second point is chosen because a large time uncertainty can exist on the first point. After each stress sequence, a 10,000 s relaxation time allows complete return to thermal equilibrium and ensures an identical initial state for all measurements.

Sample A1 (un-implanted)

At 50 °C, the un-implanted GaN-on-Si substrate shows a ρ_{eff} of $\sim 1.2\,\mathrm{k\Omega \cdot cm}$ at 0 V. From Fig. 3.18 the following experimental observations can be made:

- Time to steady-state for both bias conditions exceeds 1,000 s at the lowest considered temperature of 50 °C;
- At temperatures of 50 and 100 °C, ρ_{eff} changes by a factor of 2 over the stress phase;
- Steady-state is reached at shorter periods of time as temperature increases;
- Relative variations of ρ_{eff} are smaller at higher temperatures.

An Arrhenius dependence is obtained for the experimental time constants. The activation energies corresponding to the thermally activated mechanisms extracted from the Arrhenius plots of Fig. 3.19. Energies of 0.57

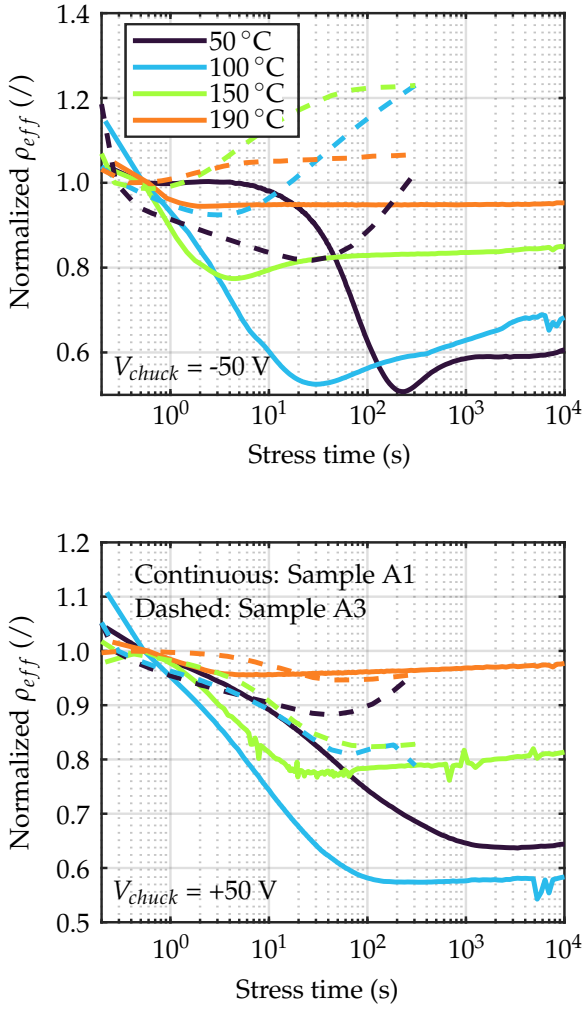


Fig. 3.18 Experimental stress sequences samples A1 and A3, for chuck temperature ranging from 50 °C to 190 °C: (a) V_{chuck} = -50 V and (b) V_{chuck} = +50 V. The data is normalized to the 2nd measured point to remove the absolute decrease of ρ_{eff} with temperature. The CPW line used has signal line width of 85 µm and slot width of 50 µm, with a length of 4 mm.

eV and 0.44 eV are found for the stress biases of V_{chuck} = +50 V and V_{chuck} = -50 V, respectively. Those values, while in range with energies often found in GaN devices by other means [105], [106], are different from the 0.9 eV typically reported for C traps at low doping levels. Such barrier reduction has been observed and could be linked to Poole-Frenkel conduction [107]. It should be noted that no measurable DC current was observed for the entirety of the stress/relaxation sequence, i.e. there is no leakage at the AlN/Si interface.

Sample A3 (implanted)

At 50 °C, the implanted GaN-on-Si substrate shows a ρ_{eff} of $\sim 1.0\,\mathrm{k\Omega \cdot cm}$ at 0 V. Although the isolation implant slightly degrades ρ_{eff}, such a highly-resistive substrate can still be considered quasi-lossless and is well suited for high-quality passives integration. For this sample, time-dependent effects were more limited: less than 20% variation of ρ_{eff} is observed during the stress phase. The high density of defects induced by the N implant leads to strong Fermi level pinning in the buffer and furthermore additional buffer charge lowering the ρ_{eff}. When ρ_{eff} decreases, the conductivity of the PSC layer increases and thus reduces its sensitivity to buffer charge change (see Section 3.2.3). Consequently, all subsequent analysis will focus on the un-implanted sample A1. Indeed, while it seems that passive structures lying on implanted regions (sample A3) will be protected from the time-dependence of ρ_{eff}, active devices will lie on top of MIS structures similar to sample A. A degradation of ρ_{eff} over time of this MIS stack could affect switch distortion or power amplifier efficiency, as will be shown in Chapter 4.

3.5.2 Time dependent modelling of GaN-on-Si substrates

Activation energy and transport mechanisms

In literature, Carbon doping in GaN usually results in a deep trap level located ~0.9 eV from the valence band. However, the activation energies extracted from the curves in Fig. 3.19 are significantly lower than that. This suggests that capture and emission from the C level directly to the valence band is not the dominating process. Rather, a reduction of the apparent activation energy can be caused by a different transport mechanism than drift-diffusion [107]. Charge redistribution can then be limited by transport of charge to the traps (e.g. from the top to the bottom of the buffer).

Two possible mechanisms are considered here and fitted to the exper-

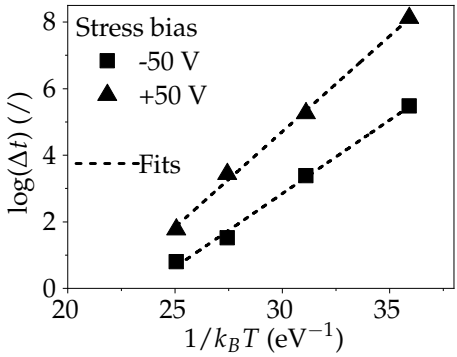


Fig. 3.19 Arrhenius plots for the stress phase in both bias conditions. The extracted activation energies are 0.44 eV and 0.57 eV for -50 V and +50 V stress bias, respectively.

imental data. Those models are found to describe well the transport of charge in C-doped GaN-on-Si buffers assisted by dislocations.

i. Poole-Frenkel transport (PF) [108], [109]. Originally used to describe mobility in organic semiconductors, this model has been found to work well in disordered regions such as dislocation-rich GaN. The Poole-Frenkel mobility is given by:

$$\mu = \mu_0 \exp\left(\frac{-\Delta E}{kT}\right) \exp\left(\left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right), \tag{3.8}$$

in which ΔE is the energy level of the defect contributing to transport, E is the electric field and β, γ are fitting parameters which are taken from [108] (where the authors used an identical material stack to the one studied here, but in a lateral experiment). The values of these parameters can be found in Table 3.2.

ii. Variable-range hopping (VRH) [110]. This model has also been found to describe well transport through dislocations. The mobility model is given by:

$$\mu \cong \frac{\nu_0 b}{E}\left[1 + \frac{2\exp\frac{qE_\sigma{}^2}{kT}}{\exp\frac{qbE}{kT} - 1}\right]^{-1}, \tag{3.9}$$

in which ν_0 is the hopping frequency, E_σ represents the energy spread of the trap distribution, and b is the hopping distance. All of these

Parameter	Value
β	0
γ	-0.019
ΔE	0.44 eV
b	1.1 nm
ν_0	1×10^{11} Hz
E_σ	80 meV

Table 3.2 Parameters used in Poole-Frenkel and variable-range hopping mobility models.

parameters are directly taken from [110] and are reported in Table 3.2.

The models for mobility can be used to fit experimental time constants in the following way:

$$J = q\mu E \tag{3.10}$$

$$\frac{\Delta Q}{\Delta t} = q\mu E \tag{3.11}$$

$$\Delta t \propto \frac{1}{\mu E} \tag{3.12}$$

The time required to transport a given charge ΔQ is proportional to $1/\mu E$. Experimentally, Δt is defined as the time necessary for ρ_{eff} to reach 95 % of its steady-state value or the time at which the dip in ρ_{eff} occurs, depending on the bias condition.. It is assumed that the charge to be displaced to reach a steady-state of ρ_{eff} is independent of temperature. Then, the time required to reach steady-state can be used in Eq. 3.12 to fit the model for μ.

The electric field in the C-doped buffer is difficult to quantify. Indeed, potential drop across the epitaxial stack is not necessarily uniform, meaning that some regions could show larger electric field than others. E is thus temporarily left as a fitting parameter.

The best fit for both considered mechanisms is displayed in Fig. 3.20. Clearly, the Poole-Frenkel model achieves the best match to experimental data, which is consistent with [108] and with what was observed for AlN/Si structures in Chapter 2. The fitting electric field is 1.93×10^5 V/cm. This is comparable with a case of uniform voltage drop across the epitaxial stack $E = V_{chuck}/t_{epi}$, leading to a field of 2×10^5 V/cm.

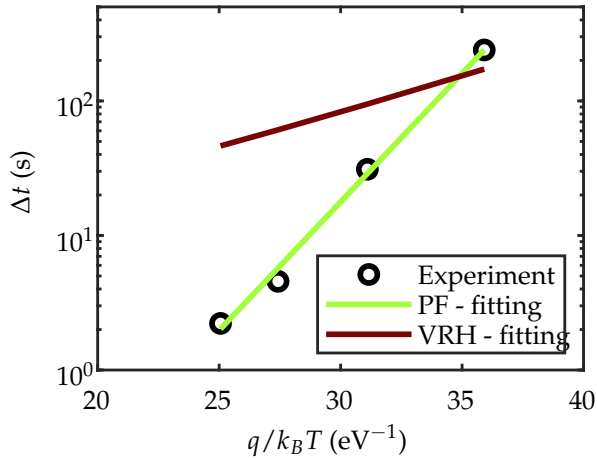


Fig. 3.20 Best fit with data for the two considered transport mechanisms for the condition $V_{chuck} = -50\,\mathrm{V}$. The Poole-Frenkel model describes best transport in this case.

Reproduction of time-dependent effective resistivity

While the Poole-Frenkel model could potentially be implemented in the TCAD environment [111], a simpler approach was considered here.

i. A wide range of μ_0 in Eq. 3.8 is used to generate mobilities μ at a temperature of 50 °C.

ii. The mobilities are implemented as standard in-band drift-diffusion mobilities and a time-dependent simulation is performed for each μ.

iii. The best-fitting μ_0 at 50 °C is used to perform the time-dependent simulations at the other temperatures. In this case, $\mu_0 = 320\,\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$.

Fig. 3.21 shows the simulated normalized ρ_{eff} during the stress phase (V_{chuck} = +50 V) for sample A. A qualitative match with experimental data is achieved.

It is important to note that the best possible match required a slight modification to the simulated structure represented in Fig. 3.4. Instead of considering the entirety of the buffer layers (GaN buffer + superlattice) to be C-doped as is suggested by SIMS measurements, including C traps only in the C-doped GaN leads to a better quantitative match.

The activation energy extracted from the simulated curves (0.62 eV) is also close to the experimental one (0.57 eV). The calibrated and validated

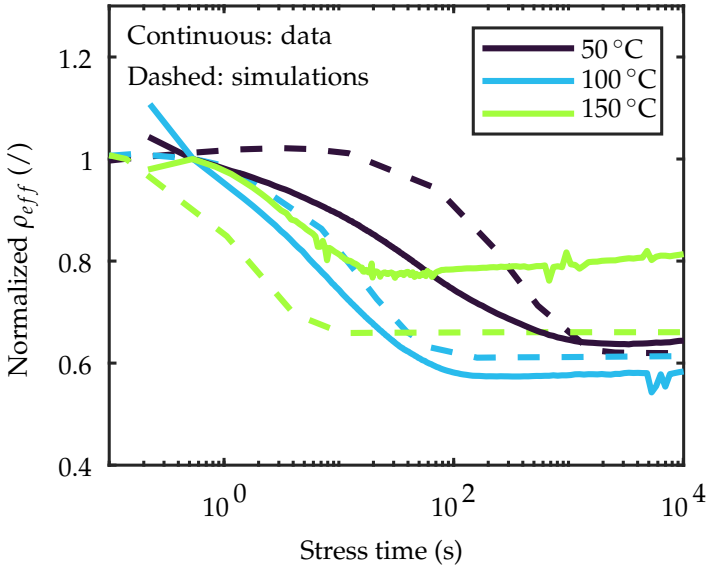


Fig. 3.21 Simulated and measured normalized effective resistivity during the stress phase (V_{chuck} = +50 V). Long time constants and temperature-dependent features observed experimentally are reproduced by the 2D TCAD model.

TCAD model is used in the following to investigate the key parameters responsible for the slow charge redistribution. The impact of carbon doping concentration, buffer thickness and transport in the buffer are investigated.

Parametric study

To mitigate the slow time dependence of ρ_{eff} under stress, two approaches can be imagined:

i. Reducing the bias dependence of the Si surface. This would require the implementation of a trap-rich layer in Si, which could take the form of Poly Si. This is out of the question to preserve good epitaxy conditions.

ii. Accelerate the charge redistribution process so that the substrate parameters stay reasonably constant. Several approaches can be imagined: buffer thickness reduction, C doping reduction or mobility enhancement.

First, Fig. 3.22 considers the possible reduction of the C-doped buffer thickness. The top and bottom regions are defined in the same way as in

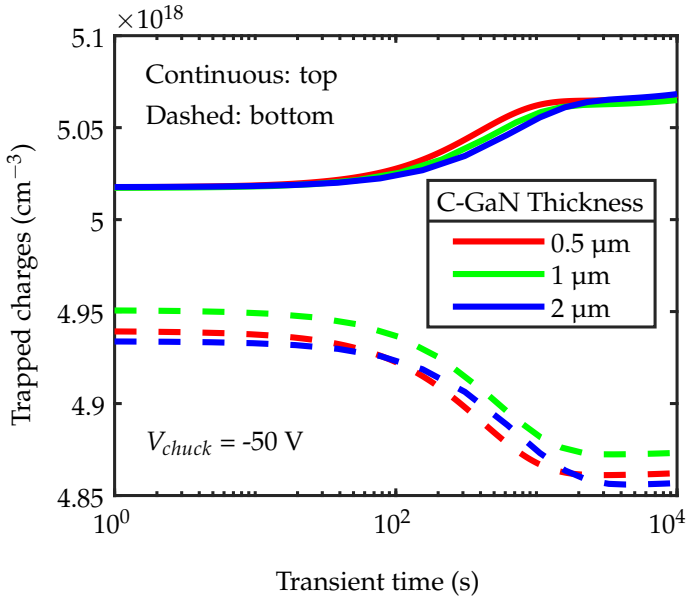


Fig. 3.22 Modifying the thickness of the C-doped buffer does not accelerate the charge redistribution process.

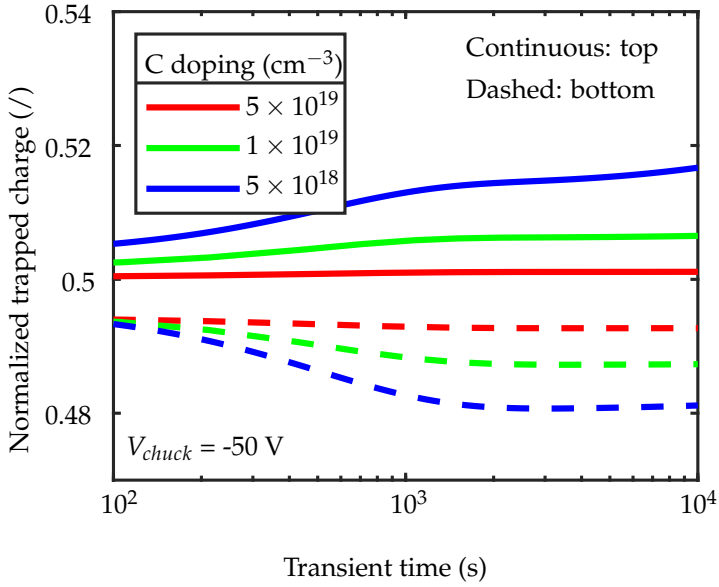


Fig. 3.23 Evolution of trapped charge for different C doping. Proportionally more charge is being redistributed for low doping, but the process does not accelerate.

Fig. 3.9. With less distance to be crossed by the mobile charges during the redistribution process, the steady state could be achieved faster. A slight acceleration is seen in Fig. 3.22 when thinning the cGaN from 2 µm to 0.5 µm, but the sensitivity to buffer thickness is low. The effect of thinning down the buffer on the zero-bias ρ_{eff} is not considered. With a thinner buffer, the thermal budget of the MOCVD growth decreases, which might limit the Al diffusion and lead to a less conductive PSC layer.

Next, Fig. 3.23 examines different realistic C dopings, ranging from 5×10^{18} cm^{-3} to 5×10^{19} cm^{-3}. To better interpret the results, the trapped charge is normalized to its value at t_0^+. The relative fraction of charge participating in the redistribution process increases with decreasing doping, which makes sense as the same bias condition is imposed on the chuck requiring the same amount of mirror charge. However, the rate of redistribution is not affected by C doping.

Note that the change of C doping is known to modify the transport mechanisms in the buffer [104]. In the simulation of Fig. 3.23, the C concentration is kept in a range where no change is expected and blocking properties of C are preserved.

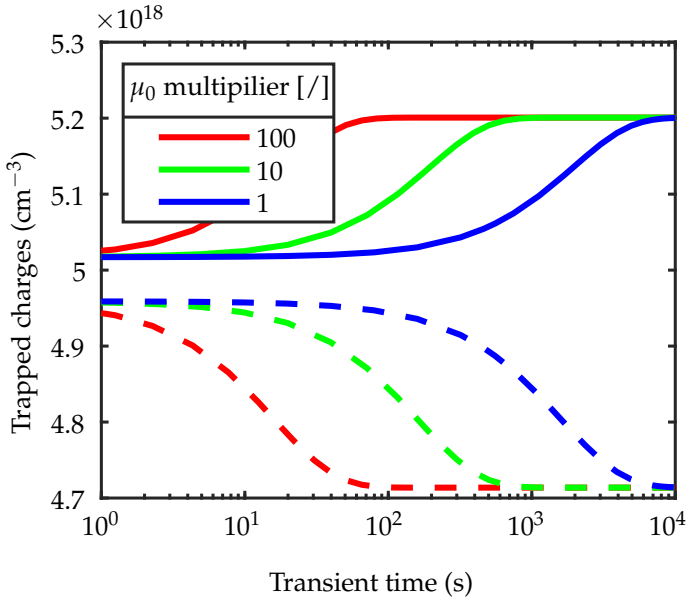


Fig. 3.24 Increasing the zero-field mobility leads to a significant acceleration of the charge redistribution.

Finally, the zero-field mobility μ_0 in Eq. 3.8 is modified. A multiplicative factor of 1 (experimental fit), 10 and 100 is applied. The results in Fig. 3.24 suggest a significant impact of the mobility on the redistribution. Indeed, the limiting factor for charge redistribution is the Poole-Frenkel transport of charge from the top to the bottom of the cGaN, and not the emission of charge from C traps (which would show in Fig. 3.23). The increase in zero-field mobility can be seen as an increase in the number of transport paths across the buffer, e.g. dislocations. The importance of providing a sufficient number of such vertical leakage paths has already been highlighted in [97]. Here, an increase by a factor 100 of μ_0 leads to a similar decrease of the time constant.

In summary, it is difficult to completely avoid the bias- and time-dependence of substrate properties in non-implanted GaN-on-Si stacks, which is intrinsically linked to the presence of a high concentration of C. The drift of ρ_{eff} with time can, however, be mitigated by improving the vertical transport across the cGaN.

3.5.3 Evidence in time dependence of harmonic distortion

Fig. 3.25 shows the experimental variation of H2 and H3 during chuck bias stress sequences for the selected temperatures of 50 °C and 150 °C in sample A. Experimental conditions are identical to those in Fig. 3.18. In all experiments, H2 dominated H3 by more than 20 dB, which is expected for substrate-induced HD from SOI studies [90]. At 50 °C, H2 values are below -75 dBm for the bias conditions explored here, proving the technological relevance of an optimized GaN-on-Si technology compared with RF SOI [54]. Over the considered stress time of 10,000 s, a time dependence of H2 is observed. Similar to ρ_{eff}, H2 only reaches steady-state after more than 1,000 s for both bias conditions. Although variations in H2 over that period are limited to 5 dB, these results highlight an additional reliability concern for substrates subjected to prolonged bias stress. Because H3 is low and close to the equipment noise floor, time dependence can only be seen at +50 V and 50 °C, where a ∼5 dB increase is observed. At 150 °C, HD degrades as expected compared with 50 °C, mostly due to the increase of the intrinsic free carriers number in Si. The time dependence cannot clearly be separated from the measurement noise. Also, the larger minimal time step in the HD setup complicates observation of variations occurring over less than 10 s. Such variations can be expected from ρ_{eff} changes in Fig. 3.18 and the difference between pre-stress HD (symbols in Fig. 3.25) and the first measured point in the stress sequence.

In addition to the slow charge redistribution and V_{FB} change, the PSC layer also sees the RF bias imposed by the large-signal excitation of the HD measurement. HD is dictated by the bias sensitivity of the PSC layer to the large-signal excitation only, because variations in buffer charge take place over times significantly longer that the large signal period ($f_0^{-1} = \sim 1\,\text{ns}$). However, the slow change of the MIS V_{FB} during the stress sequence can alter both G_{PSC} and its sensitivity to rapid bias changes. For example, in response to a change in V_{FB} change the PSC could be in a state of strong accumulation (less bias-sensitive conductivity, low HD) or closer to depletion (highly bias-sensitive conductivity, high HD). Consequently, it is difficult to correlate the time dependence of ρ_{eff} to that of HD. Indeed, predicting HD during the stress sequence would require the knowledge of instantaneous G_{PSC} ($V_{large-signal}$) curves at each point in time.

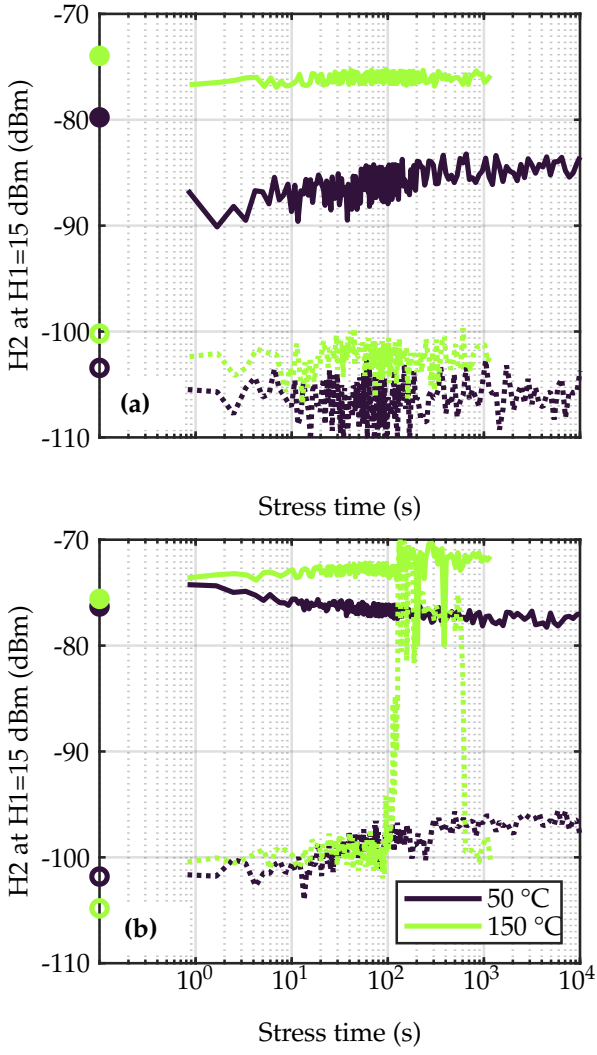


Fig. 3.25 Experimental variation of 2nd (continuous) and 3rd (dotted) harmonic power at the output of 2 mm-long CPW lines of sample A while stressing the chuck at (a) -50 V and (b) +50 V. Because measurement acquisition time is larger for HD measurement compared with S-parameters, the experimental time resolution is only of $\sim$ 1 s. Symbols indicate the pre-stress measurement. The sudden increase of H3 at 150 °C is a measurement artefact.

3.5.4 Relaxation of effective resistivity

The relaxation phase is now briefly discussed. The sample A1 was subjected to a chuck bias stress (V_{stress} = +/- 50 V) during 300 s. After switching back the chuck bias to 0 V, the sample was allowed to relax for up to 5,000 s, during which ρ_{eff} was monitored at logarithmically spaced intervals. In this case, ρ_{eff} is normalized to the final point, supposed to represent the steady-state value of ρ_{eff}. Relaxation curves showing ρ_{eff} versus time for the two V_{stress} situations are displayed in Fig. 3.26 as a function of temperature. Similar trends than the stress phase can be observed.

However, their interpretation requires more caution. Indeed, after 300 s stress, some curves have not yet reached a steady-state condition. The subsequent recovery phase is then started from a different initial state (i.e. a different spatial distribution of charge in the buffer). This issue is exemplified in Fig. 3.27. Three successive stress-relaxation sequences are performed with stress times of (i) 100 s, (ii) 1,000 s and (iii) 10,000 s. Relaxation is set to 10,000 s for each sequence. For 1,000 s and 10,000 s stress time, a steady stressed state is reached and the corresponding relaxation curves are superposed on each other. However, when the stress is stopped after only 100 s, the relaxation curve is significantly different because no steady stressed state was reached.

While it is clear that the relaxation phase is strongly conditioned by the achievement of a steady state during stress, the different stress curves are not drastically different even though no clear return to thermal equilibrium is reached after 10,000 s of relaxation. This is why the focus is best put on the stress phase.

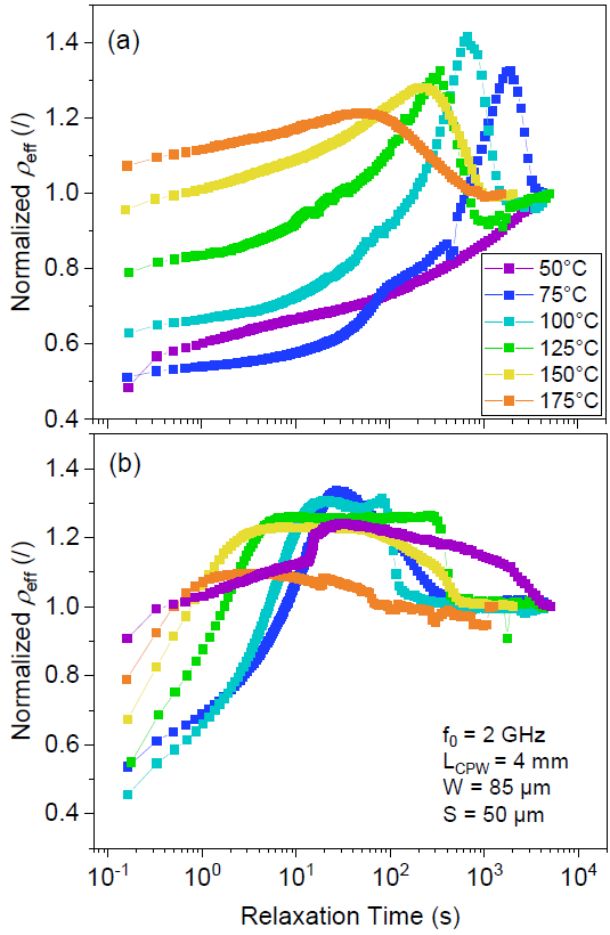


Fig. 3.26 Experimental normalized ρ_{eff} relaxation transients after a 300 s stress at V_{stress} = + 50 V (a) and -50 V (b). Relaxation times can exceed 1,000 s, and curve features are temperature dependent. Reproduced from [112]. ©2022 IEEE.

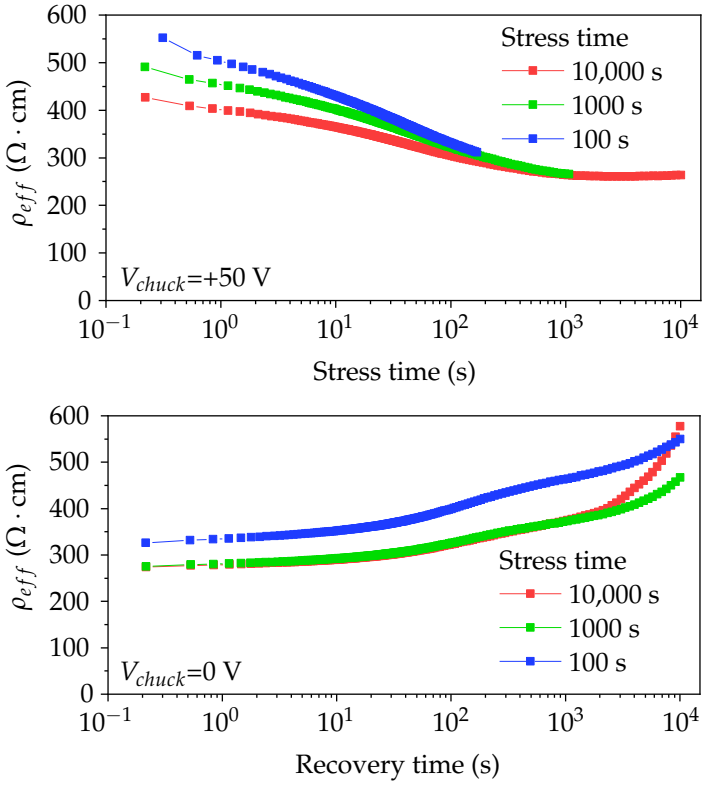


Fig. 3.27 Different stress times can lead to different initial conditions for the relaxation phase. Successive stress-relaxation sequences for sample A1 at $V_{chuck} = +50$ V and 50 °C. The CPW line used has signal line width of 85 µm and slot width of 50 µm, with a length of 4 mm.

3.6 Chapter summary

In this chapter, the bottom-up evaluation of substrate parasitic effects in GaN-on-Si stacks was continued with the study of the second part of the epitaxial stack: the C-doped buffer. An important reliability concern for GaN-on-Si RF substrates was presented: the time dependence of ρ_{eff} and HD when the substrate is stressed. This effect arises for low-loss substrates (i.e., substrates where the parasitic doping and interface charge is kept under control) and can significantly degrade their performance. It was experimentally demonstrated and successfully reproduced using a simple TCAD model, identifying buffer charge redistribution as the underlying cause. The main contributions of the chapter are summarized below.

Characterization

The evidence of buffer charge redistribution was first observed in the form of hysteresis in the $\rho_{eff} - V_{chuck}$ curves. By comparing samples with gradual inclusion of the III-N stack, the hysteresis was found to originate in the upper III-N layers.

Then, a custom experimental setup was developed to track the evolution of ρ_{eff} and HD with time, in response to a bias step. Long (> 1000 s) time constants were observed for ρ_{eff}, along with a temperature dependence indicating a thermally activated process at play. ρ_{eff} can vary by a factor of 2 when subjected to a bias step, which potentially affects the active structures lying on top of such a drifting substrate, as will be seen in Chapter 4. HD showed similar trends but the measurement here is made more complex by noise and longer acquisition times.

For implanted stacks, lying under passive structures in GaN-on-Si circuits, the issue is less pronounced. It is suspected that a certain degree of Fermi level pinning takes place in the III-N layers where a large quantity of N-induced defects exist.

Modelling

A description of the interplay between charge redistribution and change in ρ_{eff} was presented. Starting with a 1-D structure and important MOS theory, the model was then complexified to a 2-D model also including C doping. It was shown that when a movement of charge takes place in the buffer, the V_{FB} seen by Si is modified. The Si surface, which reacts instantaneously the the V_{FB} change, responds to the slow charge redistribution in the buffer by

a slow change of ρ_{eff}.

Importantly, to reproduce the experimental time constants and extracted activation energies, it is necessary to include a Poole-Frenkel transport model in the cGaN layer (and not in the superlattice). This modifies the activation energies, making them match the experiment. A qualitative match of the ρ_{eff} evolution with time is finally achieved.

Mitigation solutions

The validated model could finally be used to examine potential solutions to the substrate performance drift. It was found that C doping reduction and buffer thinning had little influence on the slow movement of charge. The bottleneck appears to be the transport of charge across the buffer. Indeed, by increasing the amount of vertical leakage paths in the cGaN, the time constants significantly decrease. This is consistent with existing literature on the dynamic R_{ON} effect in GaN-on-Si HEMTs.

4

Impact of the GaN-on-Si substrate on RF circuit performance

4.1 Introduction

The GaN channel and eventually the HEMT constitute the final step in the GaN-on-Si epitaxial layer. Ultimately, the device finds itself at the core of each of the functional blocks of the front end module such as the low noise amplifier, the power amplifier or the RF switch. Important effort is spent by different research groups to improve the architecture of the transistor in order to reach competitive high-frequency and high-power performance. Their goal is to obtain better figures of merit for these blocks (efficiency, linearity, power handling) [26]–[28].

While RF circuit performance is indeed improved by technology optimization, which is out of the scope of this thesis, it can be hindered by poor substrate characteristics. In this chapter, two of the important functional blocks of the RF FEM will be analyzed from the angle of substrate-related parasitic effects.

The RF switch is typically regarded as a substrate-sensitive component [113]. In Section 4.2, the contribution from the harmonics generated in the

substrate to the overall linearity of the switch will be investigated. The aim of this section is to reach a substrate performance specification for highly linear GaN-on-Si switches.

In Section 4.3, the power amplifier is tackled. As the key target functional block for GaN-on-Si technology, this component drives most of the process development. It will be shown that power loss in the substrate can degrade the efficiency of the PA. A physics-based modelling approach to estimate this degradation is presented, which is validated against experimental data.

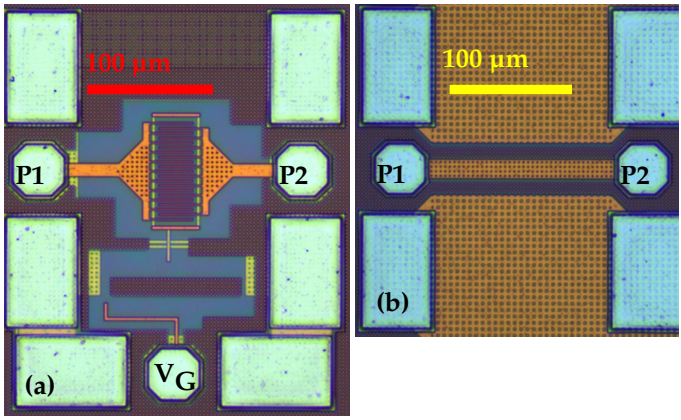


Fig. 4.1 (a) Optical micrograph of the SPST RF switch discussed here, with L_g = 150 nm and W_{tot} = 0.5 mm. (b) A 150-µm-long CPW line of similar dimensions to the switch access lines (Thru line) is used to analyze the relative contribution of the substrate to non-linearities. Port 1 (P1), Port 2 (P2) and DC gate bias pad (VG) are indicated where applicable. Reproduced from [114]. ©2024 IEEE.

4.2 Contribution of substrate harmonic distortion on GaN-on-Si RF switch linearity

4.2.1 Devices under test and DC characteristics

The HEMT stacks considered here were grown using MOCVD on 200 mm, HR-Si wafers (3-6 kΩ · cm). They consist of an AlN nucleation layer, a strain relief III-N superlattice buffer, a C-doped GaN buffer layer, and finally a 50 nm-thick GaN channel. Apart from the GaN channel, the stack is identical to sample A1 in Fig. 3.11. Two wafers with different device architectures are chosen because of their different intrinsic linearity.

A. HEMTs comprising 1 nm AlN spacer and 5 nm AlGaN barrier. Equivalent oxide thickness (EOT) is 4.0 nm.

B. MOS-HEMTs with 1 nm AlN spacer and 2 nm AlGaN barrier. A 2.5 nm high-K (HfO_2) dielectric layer is used as gate oxide. Equivalent oxide thickness, calculated from capacitance measurements is 2.4 nm

MOS-HEMTs using high-K gate dielectrics are of interest as they enable enhancement-mode operation together with low gate leakage, off-state current and improved drain induced barrier lowering (DIBL) [24], [115].

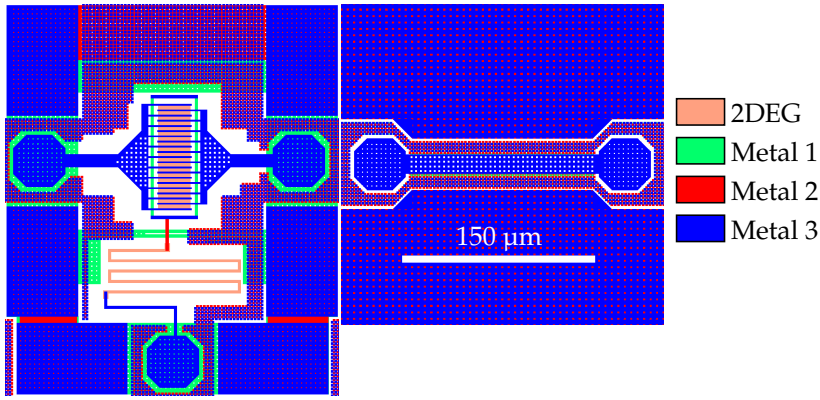


Fig. 4.2 Layout schematic of the considered common-gate HEMT and Thru line. For clarity, only the three metal levels and the 2DEG constituting the transistor and gate resistor are shown. The full structures are on top of implanted material with the exception of 2DEG regions.

A 3-layer Cu back end of line (BEOL) is used in both wafers, with the distribution of the different metal levels as displayed in Fig. 4.2. The devices under test have a gate length L_g = 150 nm and total width of 0.5 mm. A single pole, single throw (SPST) switch with a bias resistor using 2DEG as the resistive material at the gate terminal is shown in Fig. 4.1a. Its value, estimated with help of the 2DEG sheet resistance ($\sim$ 340 Ω/sq), is $\sim$ 113 kΩ (see Fig. 4.8a). Switches were embedded in GSG pads using a $\sim$10 µm-wide access line, with a total pad-to-pad distance of $\sim$145 µm.

Methodology for substrate HD evaluation from CPW lines

The HD measured at the output of the switch is contributed by (i) the intrinsic device and (ii) the substrate-induced non-linearities. It is assumed these contributions add up, as the effect of interference is at most 3 dB. Substrate HD is measured using CPW lines as described in Chapter 1. Two different CPW lines were fabricated on both wafers:

- A 2 mm-long CPW line, with pitch S $\cong$ 12 µm and central conductor width W $\cong$ 15 µm. Dimensions were chosen to fairly compare it with other RF substrate technologies in terms of HD and ρ_{eff} [116], [117].
- A 150 µm-long Thru line (Fig. 4.1b), with same S and W as the 2 mm-long CPW line.

The layout of the Thru line is similar to the switch access line (Fig. 4.1). It

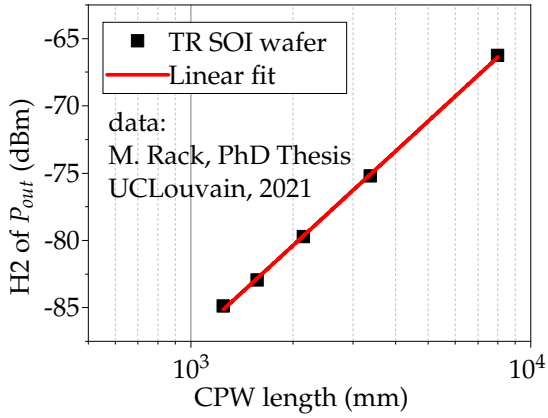


Fig. 4.3 Dependence of second harmonic power on the length of the CPW line, measured on a trap-rich SOI wafer. The linear fit presents a ∼ 23 dB/dec slope.

is then possible to use it to isolate the substrate contribution to switch HD from intrinsic device non-linearities, assuming substrate HD is captured by the Thru line measurement. Importantly, the length of the CPW line used to isolate substrate non-linearities should be close to the total pad-to-pad length of the switch structure. Indeed, H2 at the CPW output depends quadratically on its length, as illustrated experimentally by Fig. 4.3. The extracted slope of 23 dB_{H2}/dec indicates that for a 10x increase in CPW length, H2 power increases by 23 dB or ∼200x.

Substrate performance

To evaluate substrate losses, the substrate ρ_{eff}, extracted for the 2 mm-long CPW line, is shown for the entire 200 mm substrate in Fig. 4.4. Interestingly, ρ_{eff} shows non-uniformity across the wafer. For both wafers, while the median ρ_{eff} is high, it can drop to values below 1 kΩ · cm in some parts of the wafer. A left-right or diagonal pattern can even be observed. Different hypothesis could explain such non-uniformity:

- Non-homogeneous conditions in the MOCVD reactor;
- Spacial non-uniformity of doping in the CZ-Si wafer;
- Uneven distribution of the oxygen interstitials.

These hypothesis could not be verified as characterizing the Si wafer alone, before processing and without perturbing it is impossible. Indeed, the

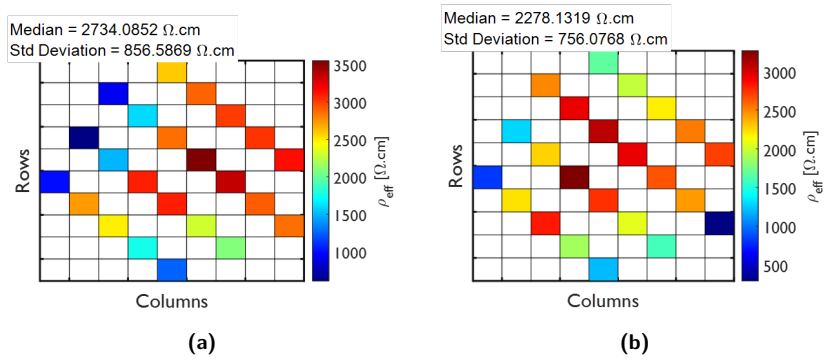


Fig. 4.4 Effective resistivity shows non-uniformity in the fully-processed wafers under study. (a) HEMT wafer and (b) MOS HEMT wafer. Data is averaged from 0.9 GHz to 5 GHz. CPW line cross-section: central conductor width W = 15 µm, pitch S = 12 µm.

deposition of a dielectric layer such as SiO_2 or Al_2O_3 prior to the CPW line would lead to the formation of a PSC layer that would dominate over the non-uniform effects. It should be noted that such non-uniform effects, although leading to a difference of ρ_{eff} of a factor of 2, are quite subtle: the corresponding B doping difference is only $\sim 1 \times 10^{13}\,\mathrm{cm}^{-3}$. In the following, a representative die with ρ_{eff} close to the median value is selected on both wafers and further studied. Results are shown in Fig. 4.5 for these representative dies.

Wafer-wide median ρ_{eff} averaged over the frequency range 0.9 GHz - 5 GHz are reported in Table 4.1. These high ρ_{eff} (> 2 kΩ · cm) mean that total RF losses are dominated by series metallic losses over shunt substrate losses [7], as shown in the inset of Fig. 4.5. This is the case for both wafers.

The HD measured on the same CPW lines on the selected dies is represented in Fig. 4.6. As is commonly observed for GaN-on-Si and more generally Si-based substrates, substrate HD is dominated by H2. At 15 dBm of H1, values of -84 dBm and -87 dBm are measured for wafer A and B, respectively. Such high substrate linearity is competitive with state-of-the art trap-rich SOI substrates. It also offers a relevant template to study RF switch linearity.

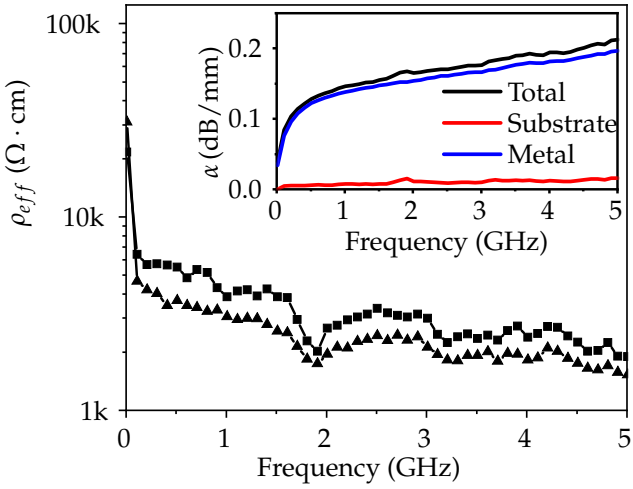


Fig. 4.5 Effective resistivity higher than 2 k$\Omega \cdot$ cm until 5 GHz extracted for a typical die on wafers A (squares) and B (triangles). Inset: series metallic losses are dominating over substrate losses. CPW line cross-section: central conductor width W = 15 µm, pitch S = 12 µm. Reproduced from [114]. ©2024 IEEE.

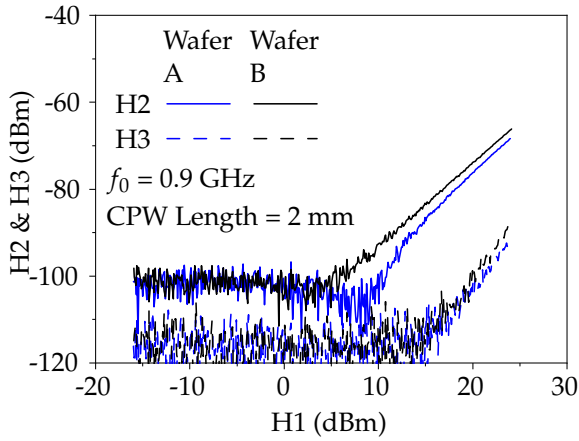


Fig. 4.6 Second and third harmonic power measured at the output of a 2-mm long CPW line on a representative die of Wafers A and B (same die as in Fig. 4.5). CPW line cross-section: central conductor width W = 15 µm, pitch S = 12 µm. Reproduced from [114]. ©2024 IEEE.

4.2.2 DC and Small-signal characterization

DC characterization and gate leakage

The $I_D - V_G$ and $I_G - V_G$ characteristics for the common-gate Devices A and B are shown in Fig. 4.7. Both devices are similar in terms of threshold voltage and peak drain current, but a significant difference is observed in gate leakage. Where Device A presents significant gate current, a substantial reduction of I_G is enabled by the use of a high-K gate dielectric in Device B. The lower EOT of Device B also leads to a 38% lower R_{ON} (Fig. 4.7).

The significant gate leakage can be problematic in the RF switch operation, more specifically its power handling. Indeed, the HEMT gate (hereafter named "intrinsic gate") is connected to the DC gate pad ("extrinsic gate") through a resistor. If I_G is high, a large proportion of the applied voltage can be dropped on this gate resistor (R_G). The value of R_G (113 kΩ), extracted in Fig. 4.8a, is close to the theoretically calculated value of 108 kΩ. The intrinsic V_G is given by:

$$V_{G,i} = V_{G,e} - R_G I_G. \tag{4.1}$$

The result of Eq. 4.1 is shown in Fig. 4.8b for Device A and B. For Device A, the intrinsic V_G saturates in the on-state because of the large voltage drop

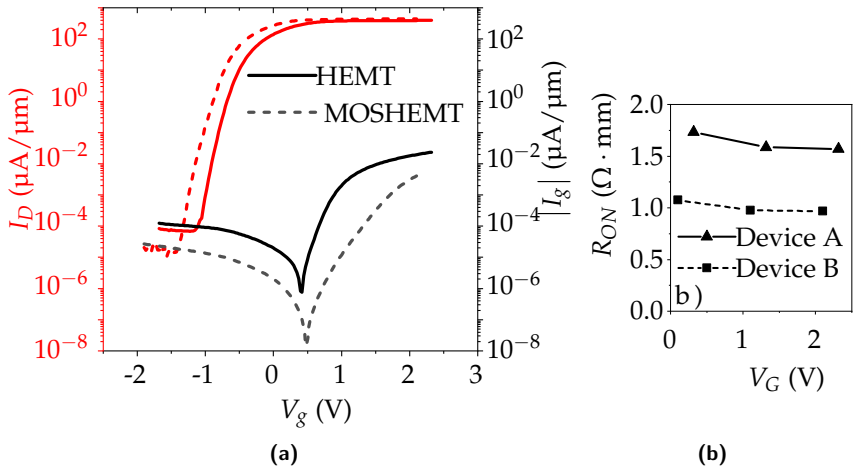


Fig. 4.7 (a) Addition of a gate oxide in Device B leads to one order of magnitude lower gate leakage. (b) R_{ON} as function of gate bias with a lower value for the Device B due to smaller EOT as compared to Device A. L_g ~150 nm. Reproduced from [114]. ©2024 IEEE.

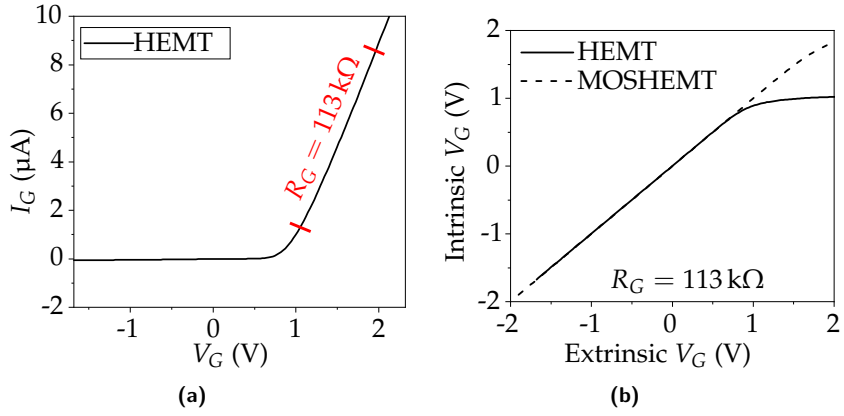


Fig. 4.8 The issue of a large gate leakage for a GaN-on-Si RF switch. (a) Gate current as a function of extrinsic gate voltage. The slope of the curve in on-state (largest I_G) allows calculation of the value of the gate resistor. (b) The intrinic gate voltage can saturate at values lower than the extrinsic gate voltage when the gate leakage is high, such as in the HEMT case.

Device	R_{ON} ($\Omega \cdot$ mm)	C_{OFF} (fF/mm)	$R_{ON} \times C_{OFF}$(fs)	IL (dB)
A	1.47	286	420	0.22
B	0.97	320	310	0.19

Table 4.1 Summary of important figures-of-merit extracted from small-signal measurements of the common-gate HEMTs

on R_G. During operation of the RF Switch, a large voltage swing on the drain or source terminal can then turn off the transistor if the peak voltage is above $V_{G,i,sat} - V_T$ and it is impossible to bias the HEMT further in on-state to prevent this issue. A similar problem occurs in the off state, although at larger $|V_{G,e}|$ owing to the lower I_G in off state. For device B exhibiting lower I_G, the saturation in $V_{G,i}$ is visible but less pronounced.

Small-signal characterization

The insertion loss and isolation were extracted from small-signal RF measurements (Fig. 4.9). Relatively low bias values for on-state ($V_t + 3$ V) and off-state ($V_t - 1$ V) are chosen to limit leakage. Insertion loss is ∼-0.2 dB at 5 GHz and remains below 0.6 dB for both switches until 30 GHz. This is in line with the state-of-the-art in GaN switches [118]–[120]. Both device architectures show similar insertion losses although a slight improvement is achieved for device B thanks to its lower R_{ON}. The off-state capacitances and corresponding $R_{ON} \times C_{OFF}$ figures-of-merit are reported in Table 4.1. They are extracted at low frequency (see Fig. 4.10) as follows:

$$R_{ON} = Re\left(-\frac{1}{Y_{12}}\right) \tag{4.2}$$

$$C_{OFF} = \frac{-Im(-Y_{12})}{2\pi f} \tag{4.3}$$

While device architecture and switch layout need to be optimized to further reduce $R_{ON} \times C_{OFF}$, these switches provide a relevant framework to study the impact of substrate non-linearity on overall HD. It should be noted that limited substrate impact is expected on the small-signal characteristics in this study. In [113], an identical RF switch fabricated on three different RF SOI substrates showed no difference in the extracted R_{ON} and C_{OFF}. A study of FD SOI switches in [33] showed that shunt losses through the conductive substrate could lead to increased insertion loss (independently of R_{ON}, which is determined by the device architecture). However, the ∼ 2

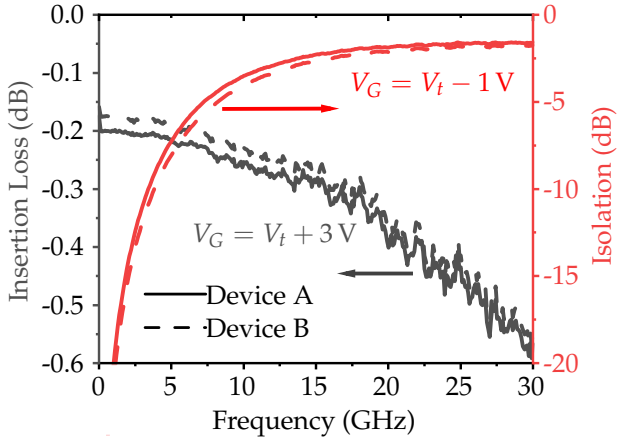


Fig. 4.9 Insertion loss (at $V_G = V_t + 3$ V) and isolation (at $V_G = V_t - 1$ V) for the two device architectures with L_g = 150 nm. Reproduced from [114]. ©2024 IEEE.

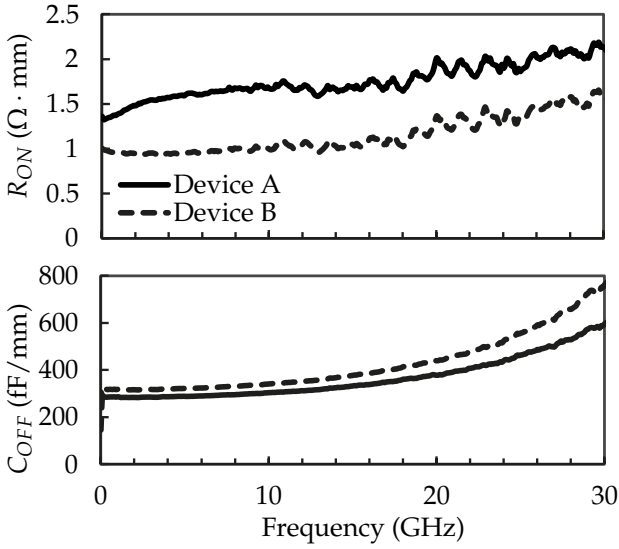


Fig. 4.10 (top) on-state resistance extracted from RF measurements at $V_{ON} = V_T + 3$ V. (bottom) off-state capacitance extracted from RF measurements at $V_{OFF} = V_T - 1$ V. No de-embedding is used.

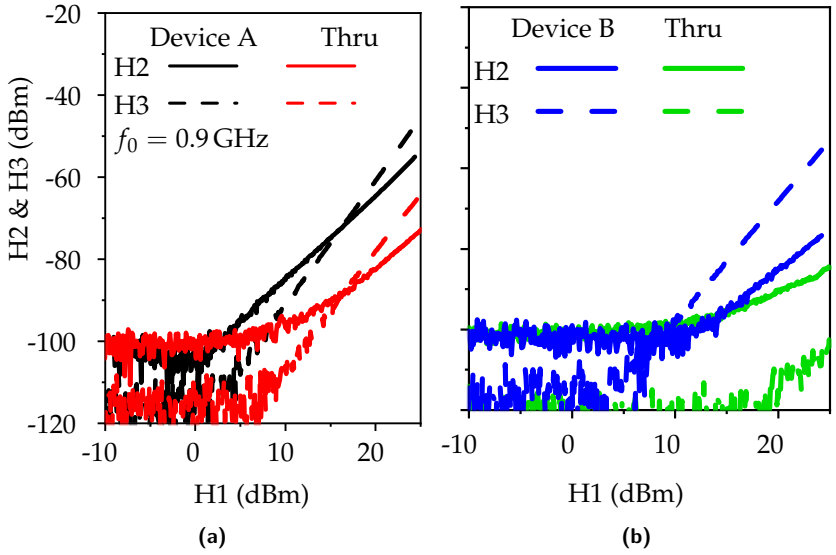


Fig. 4.11 Large-signal performance of the switch with Device A (a) and Device B (b) in on-state ($V_G = V_t + 3$ V) with Lg = 150 nm, compared with the Thru line on each wafer. 2-mm-long CPW data is reported in Table 1 for both wafers. Reproduced from [114]. ©2024 IEEE.

µm-thick buffer in GaN-on-Si is hundred times thicker than the 20 nm BOX in FD SOI processes, reducing the device-substrate coupling.

4.2.3 Harmonic distortion of CPW lines and RF switches at 0.9 GHz

In this section, single tone HD data are reported at fundamental frequency of 0.9 GHz, which is a widely used frequency to quantify and benchmark substrate non-linearity. The dc gate bias was set to V_T + 3 V. H2 and H3 are measured at the DUT output and plotted in Fig. 4.11 against the fundamental (H1). H2 is discussed in more details since it dominates total harmonic distortion (THD) for CPW lines (see Fig. 4.6) and thus represents most of the substrate contribution for switch non-linearity.

A Thru line and switch in on-state are compared on Wafer A (Fig. 4.11a). For Device A, H2 ≅ -90 dBc, which lies above the Thru line H2 by 16-20 dB at H1 levels of 15-20 dBm. This implies that for such a highly linear III-N/Si stack, switch non-linearities are dominated by the channel by a 16-20 dB margin. The same analysis can be made for H3. Device B is significantly more linear than Device A (Fig. 4.11b): H2 ≅ -110 dBc, a

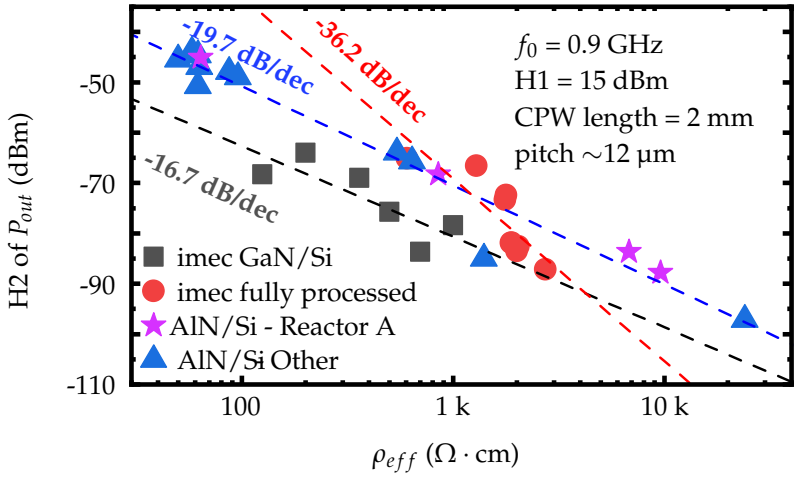


Fig. 4.12 Benchmark plot for small- and large-signal performance of GaN-on-Si substrates and AlN/Si stacks. A correlation is observed between ρ_{eff} and harmonic distortion, with a different slope for the fully processed HEMT stacks and the stacks grown until the GaN channel. Reproduced from [114]. ©2024 IEEE.

~19 dB reduction compared with Device A. It is presumed that this is mostly due to the larger I_G (and thus lower intrinsic V_G) in Device A, although gate dielectric is known to also affect linearity [121]. Because of the intrinsic gate voltage saturation and the large voltage swing reaching non-linear operating regions of the device, the intrisic device non-linearities are increased compared with higher intrinsic VG allowed by lower Ig in Device B. For Device B, H2 levels for the Thru line and the switch are very similar (Fig. 4.11b), implying that for a more linear device, substrate contribution to distortion can be high.

Advanced GaN-on-Si substrates are reaching performance comparable to trap-rich SOI substrates, with H2 levels reaching close to -90 dBm (Fig. 4.12).

Correlation between HD and effective resistivity

In addition, H2 power (measured on a 2-mm-long CPW line at f_0 = 0.9 GHz) and ρ_{eff} are strongly correlated. Indeed, by increasing ρ_{eff} the conductivity of the PSC layer (G_{PSC}) is reduced. Furthermore, the relaxation time of free carriers constituting the PSC layer is increased, which increases linearity due to reduced modulation of G_{PSC} [100]. For a variety of fully processed (i.e., device processing and BEOL) GaN-on-Si stacks, an increase of ρ_{eff} by

10× leads to a reduction of H2 levels by ∼36 dB.

The correlation also exists for samples were growth has been stopped after the GaN channel, but with a different slope. This could be linked to a different distance between the CPW line and the Si substrate, or to a different electromagnetic environment in the fully-processed stack (dummies, back-end-of-line layers). However, it can be seen on Fig. 4.12 that AlN/Si structures (distance to CPW line: 175 nm) follow a slope close to the GaN/Si stacks (distance to CPW line: 2.5 µm) despite the large difference in distance from the substrate. An electromagnetic environment cause seems more likely but should be confirmed in the future with the fabrication of fully processed wafers with lower ρ_{eff}.

Effective resistivity specification

The switch non-linearity is dominated by device non-linearity if the following is true:

$$H2_{Thru\ Line} \leq H2_{RF\ switch} \tag{4.4}$$

This condition holds for Wafer A, where we have (at H1 = 15 dBm):

$$H2_{Thru\ line\ A,\ dBm} = H2_{RF\ switch\ A,\ dBm} - 16\,\mathrm{dB} \tag{4.5}$$

Eq. 4.5 implies that the substrate for Wafer A would need to generate ∼16 dB more distortion until it would contribute significantly to the switch distortion. To obtain an estimate of the corresponding ρ_{eff} decrease, consider the 2-mm-long CPW line on Wafer A. This line showed H2 = -84 dBm (see Table 4.1). From Fig. 4.12 and small-signal data in Fig. 4.5, the corresponding ρ_{eff} is $\sim 2\,\mathrm{k\Omega \cdot cm}$. Following the ∼36 dB/dec trend line, a 16 dB increased H2 would represent a ρ_{eff} of $\sim 700\,\Omega \cdot \mathrm{cm}$. For device A , this corresponds to the lowest possible ρ_{eff} for which Eq. 4.5 is still respected.

It is noted that this lower bound is specific to a particular device performance, requiring a co-optimization of substrate and device linearity. Indeed, for the significantly more linear switch with Device B, this ρ_{eff} requirement is higher: at 0.9 GHz we have $H2_{Thru\ line\ B} \approx H2_{RF\ Switch\ B}$, making the above exercise impractical. If further linearity improvement was required for Device B, a co-optimisation of the device together with the substrate would be needed. However, it is likely less relevant provided that $H2_{RF\ Switch\ B}$ is as low as -110 dB , a level comparable with state-of-the-art commercially available products.

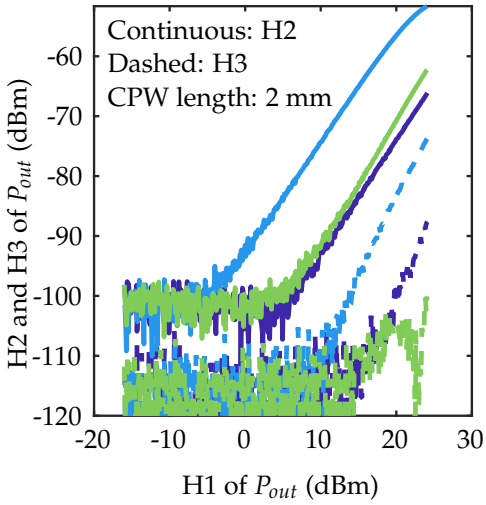


Fig. 4.13 Second and third harmonic power measured on 2 mm-long CPW lines for different dies on Wafer A. H3 consistently lies more than 20 dB lower than H2. The different levels of distortion can be correlated to the non-homogeneous substrate performance of this wafer.

4.2.4 Limitations of the proposed approach

Third harmonic level

For 2 mm-long CPW lines, the second harmonic lies several tens of dB higher than the third harmonic in the entire explored power range (Fig. 4.6). This trend is validated for several CPW lines on different dies in Fig. 4.13, indicating that the substrate's most significant contribution to distortion is by H2 generation rather than H3. Also for the more widely studied SOI technology where HD also originates in the Si substrate, H2 is generally dominating the substrate-induced distortion [54], [122]. On the other hand, third-order harmonics are perhaps more critical for RF applications where linearity figures of merit such as the output and input third-order intercept points (OIP3 and IIP3) are based on third-order intermodulation products [36]. In this work, it is assumed that H3 originates mostly from the intrinsic HEMT device. However, from Fig. 4.11 it seems that for shorter CPW lines such as the Thru line considered here H3 can contribute equally or even more than H2. While this can question the validity of the conclusions obtained from analyzing H2, several aspects should be clarified regarding H3.

- H3 does not seem to scale with CPW length. As discussed in Fig. 4.3 the power of the generated harmonics under a CPW line should be proportional to its length. The unnaturally high H3 in Thru line measurements might then be caused by an external factor.

- H3 is frequently omitted in discussions on substrate-induced HD because it appears to be highly dependent on the contact quality, in contrast with H2 [90]. The physical reason for this sensitivity is still unclear.

Future work is required to elucidate the peculiarities of H3 measurement on CPW lines. Still, the characterization of H2 is well established and can be considered to be the main contribution from the substrate to the distortion of the RF switch.

Test structure design

From Fig. 4.1 and Fig. 4.2, it can be seen that the spacing between the signal line and the ground plane is slightly different for the Thru line or the switch structure. It was shown in Chapter 1 that the substrate performance measured on CPW lines is dependent on the spacing (see Fig. 1.7). Consequently, for a given substrate, the HD measured on the Thru line and the substrate contribution measured on the switch structure can differ. As was demonstrated in Fig. 1.7, this effect is more significant for strongly non-homogeneous (and thus, lossy) substrates. For highly-resistive substrates such as those encountered in this study and spacings above $\sim 10\,\mu m$, a CPW spacing difference of a few micrometres or even tens of micrometres will only lead to a minor difference in measured substrate performance. For additional insights on the impact of CPW spacing on measured substrate FOM, references [85] and [90] can be consulted.

Furthermore, the tapering region from the switch access to the source and drain fingers is not accounted for by the simple Thru line. For a more straightforward one-to-one comparison, it would be possible to design the Thru line as an exact copy of the RF switch structure, with the intrinsic device replaced by a rectangular piece of Metal 1. The gate electrodes would also not be included. This better test structure is schematically represented in Fig. 4.14.

Specificity to a single device

The methodology introduced here proposes to specify the substrate performance with respect to a given intrinsic device non-linearity. The ρ_{eff} lower

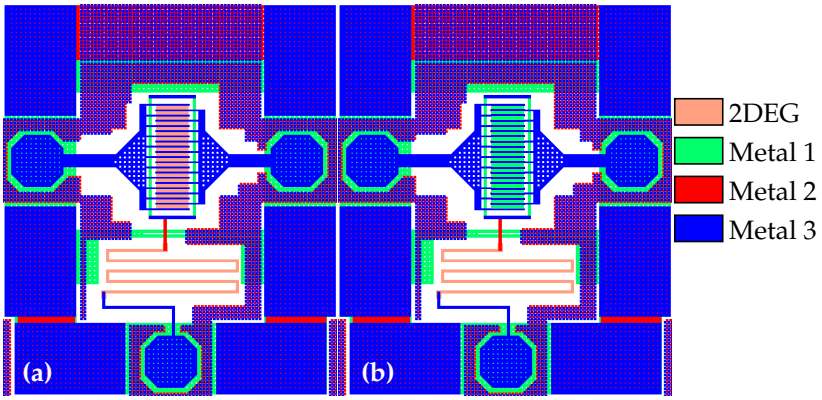


Fig. 4.14 (a) Layout view of the switch structure. (b) Schematic of a hypothetical better-suited Thru line structure, in which the active intrinsic device is replaced by a rectangular piece of Metal 1.

boundary obtained in Section 4.2.3 cannot be applied to any RF switch, or even to any GaN-on-Si switch: it is specific to the particular switch under study. This is a significant drawback of the approach as any optimization to the linearity of the device must be followed by a re-evaluation of the substrate specification. Also, if improvements of linearity are obtained by circuit design techniques or if multiple transistors are stacked, thereby modifying the switch structure, the substrate linearity specifications might not be valid [123], [124].

4.2.5 Power Handling

In this section, a different GaN-on-Si HEMT RF switch device, presenting less gate leakage, is briefly considered. This device has a treshold voltage of $V_T =\sim -2$ V. A wider bias range can be reached with the lower I_G. The results of the large-signal measurements are shown in Fig. 4.15. The progressive turn-on of the transistor in off-state can be clearly seen for weakly negative bias values in Fig. 4.15a. At -4 V, the HEMT turns on for part of the large-signal cycle starting from $P_{in} = 13$ dBm. At -10 V, the turn-on power is increased to 22 dBm. This highlights the interest of biasing the HEMT as far as possible in the off-state for the best large-signal isolation.

In Fig. 4.15b, H2 is seen to improve as the on-state bias is increased, eventhough the insertion loss is not affected (i.e., all on-state curves of Fig. 4.15a are superposed on each other). This can be attributed to a bias point

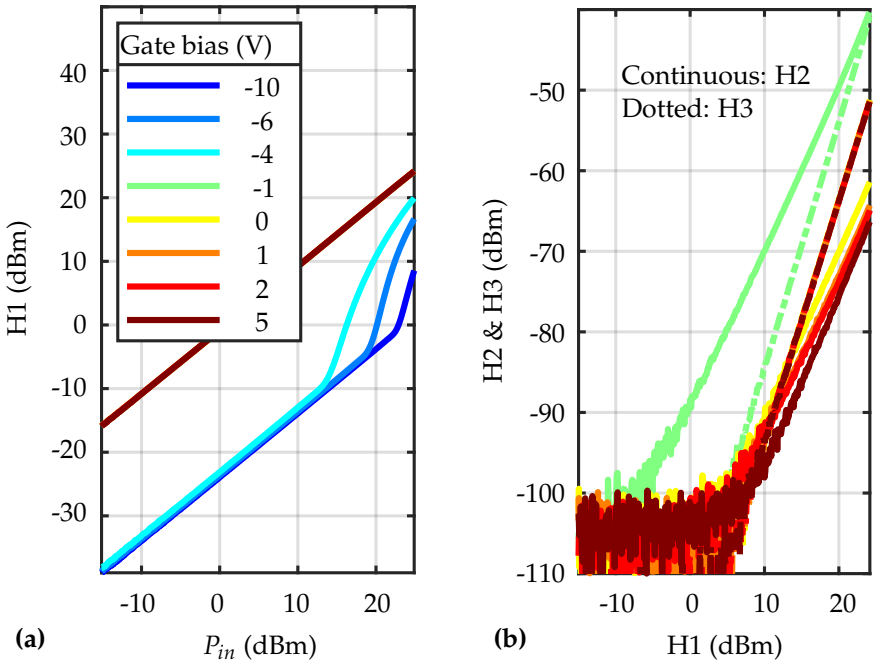


Fig. 4.15 (left) Evolution of first harmonic power at the output of the switch as a function of input power, for different values of gate bias. (right) Second and third harmonic power against H1 for different values of gate bias in on-state.

that is further away from the non-linear region around V_T.

4.3 Power dissipation and PAE degradation

Under high-frequency operation, the GaN-on-Si PA can be coupled to the conductive Si substrate as the impedance of the insulating buffer decreases. Then, if the PSC layer is conductive enough, RF power can be dissipated in it. This power is not transmitted to the load and thus leads to a decrease in the PA's efficiency.

The issue of power dissipation in the substrate has first been pointed out in [125] where an decrease in Si resistivity with temperature was associated with increase loss. In [126], a first modelling approach comprising a so-called buffer resistance showed a link to efficiency, but did not link its value to physical arguments. A detailed study of the interplay between temperature, substrate resistance and loss was presented in [127]. However, the substrate resistance has to be extracted from measurements. Very recently, the carrier distribution in the Si substrate was taken into account [128].

In this section, a more general approach is proposed to obtain a clear physical understanding of the effect of a lossy substrate on the PA performance. First, a simple waveform analysis of the PA shows how the presence of a finite substrate resistance can impact the power added efficiency (PAE), an important figure-of-merit for a PA. Then, the correlation between substrate loss and PAE is demonstrated experimentally on a variety of substrates. The core of the work consists in a physics-based model of the substrate resistance and capacitance, taking into account the doping profile giving rise to the PSC, the dimensions of the transistor and the operating frequency. Important physical insights are gained from this model. A predicition of the PAE penalty associated with the the substrate is achieved and, importantly, matches the experimental data. Finally, the effect of the operating temperature is discussed.

4.3.1 Waveform analysis and inclusion of a substrate resistance

Fig. 4.16 shows a simplified large-signal equivalent circuit of the drain side of a power amplifier. In this circuit, the equivalent substrate network has been added between source and drain nodes. While the capacitance C_{sub} can be compensated for by matching networks, R_{sub} will lead to a shunt power loss and consequently efficiency degradation [33]. For this simplified circuit, it is possible to reach an analytical formulation of the PA's PAE in the case study of class B bias. The derivation is based on what is done in [129]. The final expression can then straightforwardly generalized to class

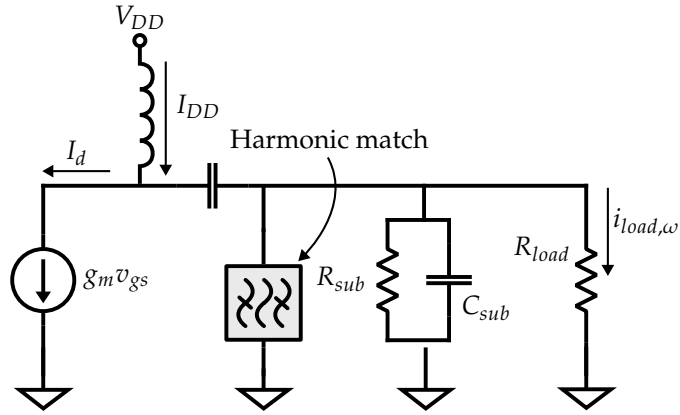


Fig. 4.16 Simplified circuit of the drain side of a power amplifier including substrate resistance and capacitance.

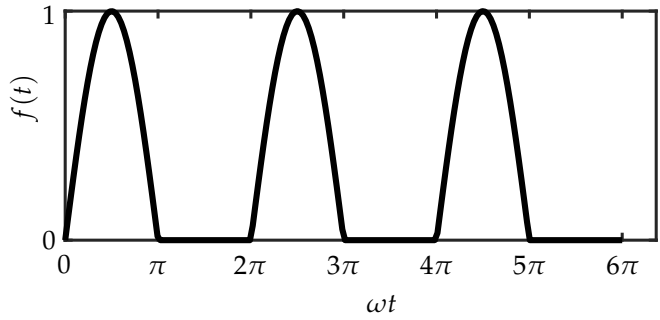


Fig. 4.17 Representation of the current waveform in B-class operation.

AB.

Power amplifier in class B

A B-Class Power Amplifier is considered in an ideal case with infinite substrate impedance. The drain current of the transistor is given by:

$$i_D(t) = g_m V_{GS} f(t), \tag{4.6}$$

where $f(t)$ is shown in 4.17 and given by:

$$f(t) = \frac{1}{2}\left(\sin(\omega t) + |\sin(\omega t)|\right) \tag{4.7}$$

The load current is obtained by assuming that no DC enters the load branch:

$$i_l(t) = I_{DD} - i_D(t) \tag{4.8}$$

$$I_{DD} = mean(i_D(t)) = \frac{\omega g_m V_{GS}}{2\pi} \int_0^{\frac{2\pi}{\omega}} f(t)dt = \frac{g_m V_{GS}}{\pi} \tag{4.9}$$

$$i_l(t) = \frac{g_m V_{GS}}{\pi}(1 - \pi f(t)) \tag{4.10}$$

Next, the harmonics of the load current are removed by harmonic matching. $f(t)$ is replaced by its Fourier transform:

$$i_{l,tot}(t) = \frac{g_m V_{GS}}{\pi}\left(1 - \pi\left(\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - (\cdots)\right)\right) \tag{4.11}$$

$$i_{l,fund} = -\frac{g_m V_{GS}}{2}\sin\omega t \tag{4.12}$$

The load voltage is given by the load line:

$$v_L = \frac{2V_{DD} - V_k}{2}\sin\omega t, \tag{4.13}$$

in which V_k is the transistor knee voltage. The RMS power delivered to the load is thus:

$$P_{load,RMS} = \frac{1}{8} g_m V_G S(2V_{DD} - V_k) = \frac{1}{8} I_{Dmax}(2V_{DD} - V_k), \tag{4.14}$$

where I_{Dmax} is the transistor maximum drain current. Here, the load resistance is assumed to be $R_{load} = \frac{2V_{DD} - V_k}{I_{Dmax}}$. The DC power is given by

$$P_{DC} = \frac{V_{DD} g_m V_{GS}}{\pi} = \frac{V_{DD} I_{Dmax}}{\pi} \tag{4.15}$$

To obtain the Power Added Efficiency, the gate side is considered. The input powered is delivered through the gate resistance (R_g) to C_{gs}

$$\begin{aligned} P_{in,RMS} = \frac{1}{2} R_g I_{Gmax}^2 &= \frac{1}{2} R_g \omega^2 C_{gs}^2 V_{gs}^2 \\ &= \frac{1}{2} R_g (2\pi)^2 f^2 C_{gs}^2 \frac{I_{Dmax}^2}{g_m^2} \\ &= \frac{1}{2} R_g I_{Dmax}^2 \left(\frac{f}{f_t}\right)^2 \end{aligned} \tag{4.16}$$

It is now possible to compute PAE:

$$PAE = \frac{P_{load,RMS} - P_{in,RMS}}{P_{DC}} = \frac{\pi}{4}\left(1 - \frac{V_k}{2V_{DD}} - 2\frac{R_g I_{Dmax}}{V_{DD}}\left(\frac{f}{f_t}\right)^2\right) \quad (4.17)$$

For the ideal case of $V_k = 0, R_g = 0$, the limit of $\frac{\pi}{4}$ is found. The substrate resistance is now included. The DC power consumption which depends only on supply voltage and transistor maximum current is not affected by R_{sub}. Similarly, no term in the expression for $P_{in,RMS}$ depends on R_{sub}. However, the load current is now divided into the R_{load} branch and the R_{sub} branch. $i_{L,effective}$ is defined as the current flowing through R_{load}:

$$i_{l,effective}(t) = i_l(t)\frac{R_{sub}}{R_{sub} + R_{load}} = \theta i_l(t) \quad (4.18)$$

$$P_{load,effective} = \theta P_{load} \quad (4.19)$$

The expression for PAE is then reached:

$$PAE = \frac{\pi}{4}\left(\theta\left(1 - \frac{V_k}{2V_{DD}}\right) - 2\frac{R_g I_{Dmax}}{V_{DD}}\left(\frac{f}{f_t}\right)^2\right) \quad (4.20)$$

Assuming that the small-signal R_{sub} causes power dissipation during large-signal operation, the finite substrate resistivity will lead to a PAE penalty that increases as R_{sub} decreases. The PAE penalty is defined as the difference, in percentage points, between the PAE value for $\theta = 1$ and for $0 < \theta < 1$.

Power amplifier in class AB

The class AB is defined by a conduction angle α between π and 2π, with $\alpha = \pi$ being the limiting case of class B. Class AB is a frequently used bias condition as it constitutes a tradeoff between class A (best linearity) and class B (best efficiency) [130]. The drain current in class AB is given by a slightly more complex expression [130]:

$$i_D(t) = g_m V_{GS}\frac{\cos\omega t - \cos\frac{\alpha}{2}}{1 - \cos\frac{\alpha}{2}}. \quad (4.21)$$

The same analysis as performed above for class B can be followed. The integral in eq. 4.9 now depends on α. The power delivered to the load will

Wafer	Si thickness	III-N thickness	ρ_{eff}
A	1 mm	1.85 µm	$60\,\Omega\cdot$cm
B	725 µm	1.8 µm	$>3\,\mathrm{k}\Omega\cdot$cm

Table 4.2 Description of the two wafers considered to study the impact of substrate loss on the power amplifier.

be given by:

$$P_{load,effective} = \theta\frac{1}{8\pi}I_{Dmax}(2V_{DD}-V_k)\frac{\alpha-\sin\alpha}{1-\cos\frac{\alpha}{2}}. \tag{4.22}$$

Similarly, the DC power consumption also depends on the conduction angle:

$$P_{DC} = \frac{V_{DD}I_{Dmax}}{\pi}\frac{2\sin\frac{\alpha}{2}-\alpha\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}}. \tag{4.23}$$

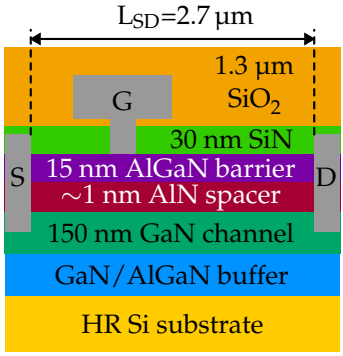
Finally, the PAE generalized for class AB is given by:

$$PAE = \frac{1}{4\left(2\sin\frac{\alpha}{2}-\alpha\cos\frac{\alpha}{2}\right)} \left(\theta\left(1-\frac{V_k}{2V_{DD}}\right)(\alpha-\sin\alpha)-2\frac{R_g I_{Dmax}}{V_{DD}}\left(\frac{f}{f_t}\right)^2\left(1-\cos\frac{\alpha}{2}\right)\right) \tag{4.24}$$

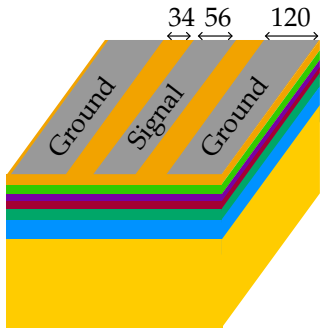
In comparison with the result obtained for a class B operation, the coefficient θ is multiplied by a factor $\frac{\alpha-\sin\alpha}{\pi\left(2\sin\frac{\alpha}{2}-\alpha\cos\frac{\alpha}{2}\right)}$. Because this factor is smaller than 1 for conduction angles between π and 2π, the PAE penalty (in percentage points as defined above) will be lower for the lower-efficiency bias class AB.

4.3.2 Devices under test

In contrast with the previous parts of this thesis, the devices in this section are provided by CEA-leti. Two different 200 mm GaN-on-Si wafers with different substrate effective resistivities are considered and their main characteristics are given in Table 4.2 The III-N layers were grown using metalorganic chemical vapor deposition (MOCVD). The epitaxial structure is represented in Fig. 4.18a. Both wafers have a channel thickness of 150 nm and a 15 nm $Al_{0.28}Ga_{0.72}N$ barrier thickness with AlN spacer. The devices being characterized, similar on both wafers, consist of two 50 µm-wide



(a) Epitaxial structure. The GaN/AlGaN buffer consists of an AlN nucleation layer, a strain relief buffer and a C-doped GaN buffer.



(b) CPW line. The dimensions are given in micrometres.

Fig. 4.18 Schematic representation of the experimental devices considered for the impact of substrate loss on the RF power HEMT efficiency.

fingers with a gate length L_g = 150 nm. 1.4 µm-thick Al:Cu CPW lines were fabricated, together with the HEMT devices, on top of SiN passivation and ∼1.3 µm-thick SiO_2 layer. The CPW line geometry is shown in Fig. 4.18b. Ar-implantation was used instead of N to suppress the 2DEG underneath.

4.3.3 RF characterization

Effective resistivity extracted from CPW lines

CPW lines were characterized and ρ_{eff} was extracted following the procedure described in Chapter 1. The results are shown in Fig. 4.19. For Wafer A, $\rho_{eff} = \sim 60\,\Omega \cdot$ cm, which is significantly lower than the nominal Si substrate resistivity ($> 3\,k\Omega \cdot$ cm) owing to the formation of a PSC layer during the MOCVD growth of III-N layers. In most cases, the PSC layer is due to Al and Ga atoms diffusing into Si and doping the surface region (p-type), but can also be contributed to by a high interface charge at the AlN/Si interface, as demonstated in Chapter 2. This PSC layer is significantly mitigated by improving the epitaxy in Wafer B. Consequently, its ρ_{eff} stays high at values higher than $1\,k\Omega \cdot$ cm, which is competitive with state-of-the art GaN-on-Si substrates such as presented in Chapter 1. No further investigation on the origin of the ρ_{eff} difference between the two wafers is done here due to a lack of material information and no AlN/Si stacks available.

It should be noted that neither wafers present a strong bias dependence of their ρ_{eff} (see Fig. 4.20). This is expected for implanted wafers and allows

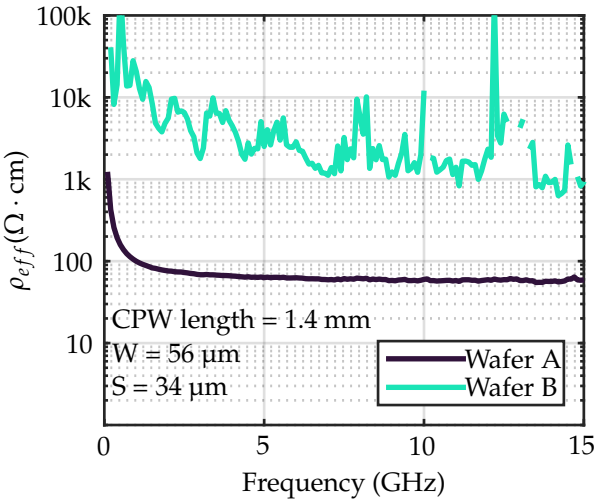


Fig. 4.19 Effective resistivity plotted against frequency for wafers A and B. Wafer A shows a relatively poor ρ_{eff} of $\sim 60\,\Omega \cdot$ cm, while Wafer B has high ρ_{eff} of $> 1\,k\Omega \cdot$ cm. CPW dimensions are designed to provide a $Z_c = 50\,\Omega$.

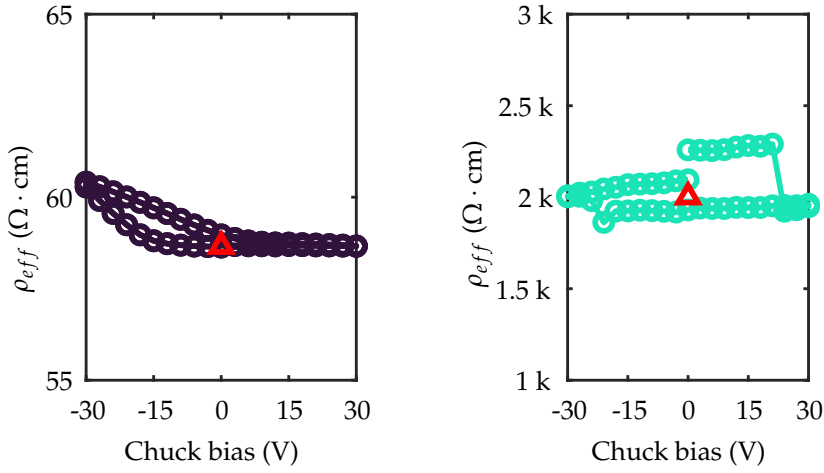
the modelling approach described in the later sections to be done at 0 V. However, it is also known that unimplanted regions can show more significant bias and time dependence. Unfortunately, the only wafers available to this study are fully processed and thus no CPW line lying on as-grown material is available.

Because of higher substrate loss in Wafer A, a strong substrate signature is expected in HEMT g_D.

Substrate signature in HEMT small-signal measurements

The lossy substrate manifests itself as a transition in the output conductance of the transistor when plotted against frequency. As frequency increases, the free carriers in the PSC layer (in this case, most probably holes which are majority carriers) cannot respond anymore to the small-signal AC voltage, causing an increase in g_D [131]. In first approximation and neglecting any dimensional effects that will be treated later, this transition frequency is proportional to the dielectric relaxation frequency of the substrate, which is given by:

$$f_{sub} \cong (2\pi\varepsilon_{Si}\rho_{Si})^{-1} \tag{4.25}$$



(a) Wafer A. **(b)** Wafer B.

Fig. 4.20 Bias dependence of effective resistivity measured for the two wafers. The ramp rate is set to 10 V/min. Effective resistivity is averaged over a frequency range where it is flat. The red triangle indicates a measurement performed 300 s after the bias sweep. No significant bias dependence or hysteresis is observed. The sweep direction is : 0 V→-30 V→+30 V→0 V.

Output conductance ($Re(Y_{22})$) and capacitance ($Im(Y_{22})/\omega$) are extracted from S-parameters measurements using an Agilent E5061B ENA available in Welcome. The devices are biased in off-state ($V_G < V_T$, $V_D = 0V$) to remove the impact of self-heating on g_D. The access lines are de-embedded using the measurement of a Thru line [132]. Results are shown for both wafers in Fig. 4.21. A transition in g_D and C_{dd} is observed at a few hundreds of MHz for Wafer A. For Wafer B, showing almost 2 orders of magnitude higher ρ_{eff} (and thus lower f_{sub}), the substrate-related transition takes place at frequencies lower than what is reachable with this measurement setup.

Experimental correlation between PAE and substrate loss

Further evidence of substrate loss can be found in a large-signal FOM such as PAE (Fig. 4.22). The on-wafer fundamental Load-Pull setup is based on DELTA tuners (Focus Microwaves) which are directly connected to the RF probes for optimal impedance coverage. The large signal performance is measured at f=28GHz for a nominal bias point (V_{DD} = 10 V, I_{Dq} = 200 mA/mm) and the load impedance is set on each device for optimal PAE. For each measurement, the small-signal parameters of a transmission line

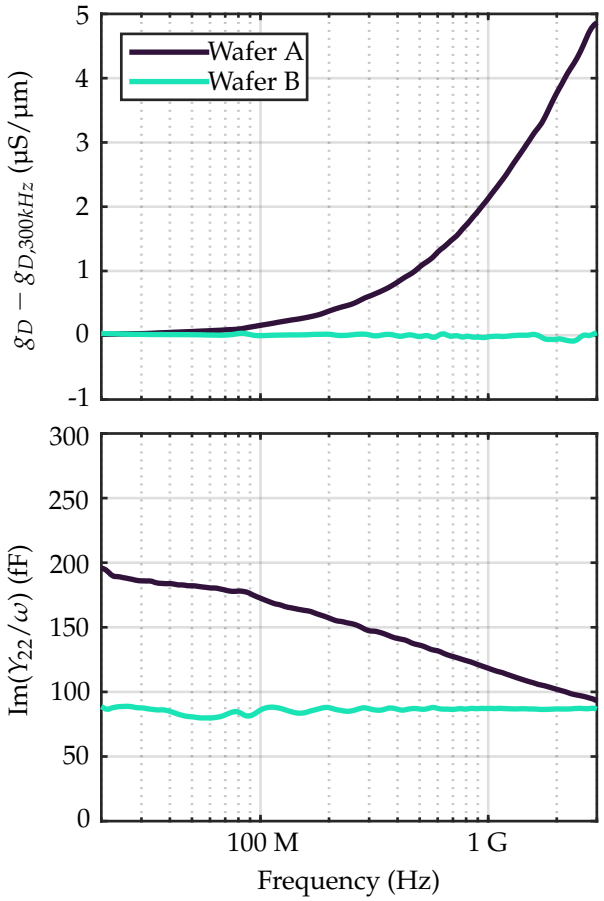


Fig. 4.21 Output conductance and capacitance extracted from small-signal measurements of HEMTs in off-state on wafers A and B. The typical substrate effect is experimentally observed for Wafer A, while the more resistive Wafer B's transition frequency is too low to be measured.

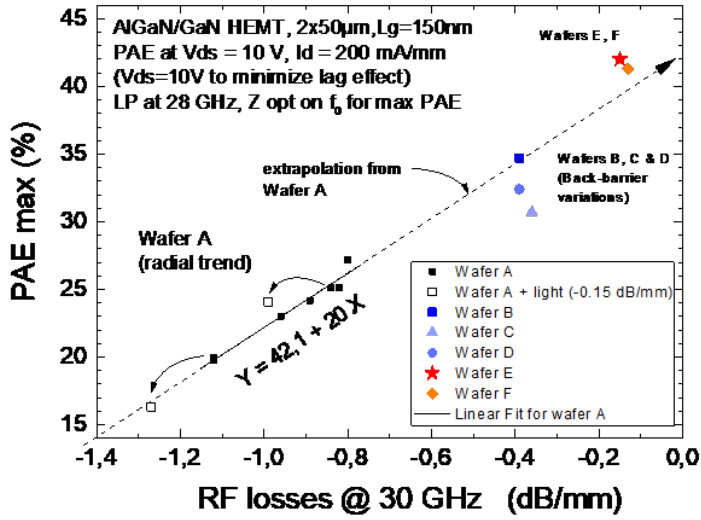


Fig. 4.22 Evidence of correlation between substrate loss and a device-level FOM: PAE. Load-pull measurements for devices fabricated on substrates with different substrate loss show a correlation between a degradation of PAE and substrate losses Note that under high intensity visible light the HEMT PAE is further degraded as well as the CPW losses (open squares). Different points for Wafer A correspond to die-to-die variation of substrate performance. The data is provided by CEA-leti.

on the same die using a PNA-X from Keysight were also extracted. It allows to extract the substrate losses as close as possible to the measured HEMT to limit the effect of die-to-die variation. Different wafers and test conditions were used in this study (Fig. 4.22), with Wafer A and B being analysed in detail in the rest of this section. The influence of lighting (using the probe station illumination) was found to affect the substrate losses due to photoelectric generation. A clear PAE dependence with substrate losses is observed with best results for losses <0.2dB/mm at 28GHz. A 17-point difference in PAE is seen between the lossy Wafer A and the more resistive Wafer B. In the following sections, a combination of TCAD and compact modelling will be used to better link the substrate properties with equivalent circuit elements and HEMT performance to reproduce the differences observed in Fig. 4.22.

4.3.4 Model description and validation

To allow frequency-dependent modelling of non-uniform substrates, this section proposes a more general approach. A graphical representation of the procedure is displayed in Fig. 4.23.

i. An experimental spreading resistance profile (SRP) is used as doping profile in a 1D TCAD simulation of the substrate. In GaN-on-Si technology, surface doping by Al and Ga is the main contribution to the PSC layer, and SRP allows extraction of the doping profile. The resulting DC simulation provides the free carrier distribution in the semiconducting substrate, from which a resistivity profile with depth is computed.

ii. In Matlab, an equivalent circuit of the substrate's cross section is built. It consists of an arbitrary number of cells (see Fig. 4.24a), where each cell comprises four elements (Fig. 4.24b). Each element contains the local electrical properties (ρ, ε) of the substrate:

$$R_h = \rho \frac{W_{cell}}{H_{cell}} \tag{4.26}$$

$$R_v = \rho \frac{H_{cell}}{W_{cell}} \tag{4.27}$$

$$C_h = \varepsilon \frac{H_{cell}}{W_{cell}} \tag{4.28}$$

$$C_v = \varepsilon \frac{W_{cell}}{H_{cell}} \tag{4.29}$$

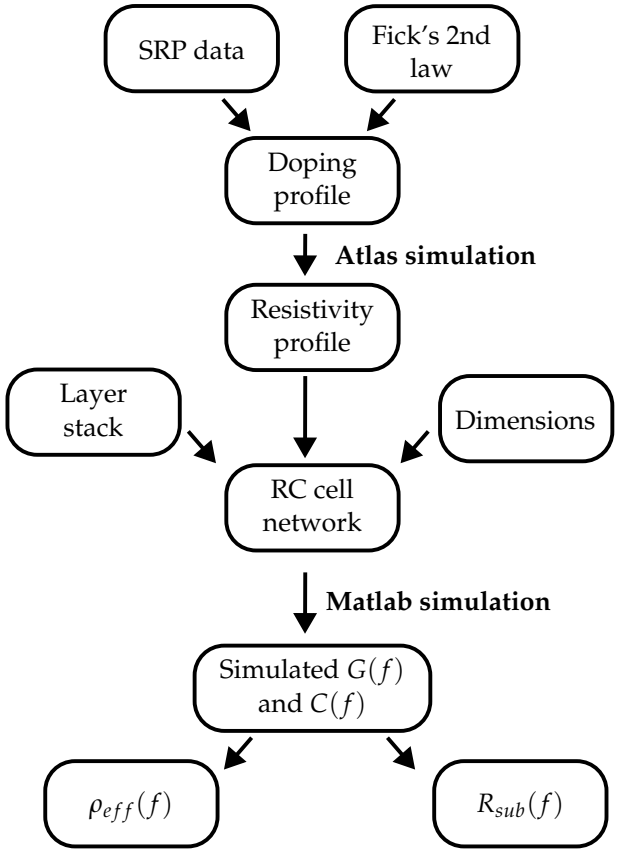


Fig. 4.23 Successive steps of the physics-based modeling approach proposed here.

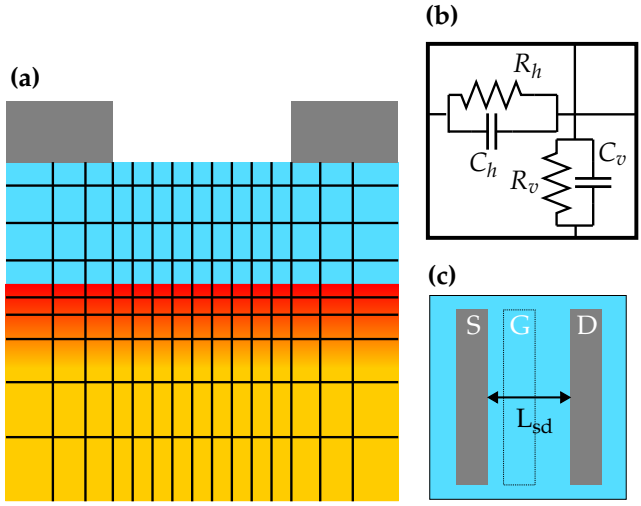


Fig. 4.24 (a) Representation of a typical RC mesh with a finer discretization in the PSC region. (b) Every cell of the RC mesh is made of one horizontal and one vertical RC element, and connected to adjacent cells. (c) Top view of a simulated HEMT, where the two electrodes represent the source and drain fingers.

where W_{cell} and H_{cell} are the width and height of the cell, respectively, and ρ is provided by the TCAD-simulated resistivity profile mentioned above. To emulate the electrodes, the relevant nodes (which depend on the contact dimensions and the mesh) are shorted together.

iii. The equivalent circuit is simulated at each frequency point to obtain the 2-port Y parameters between P1 and P2. From Y_{12} the equivalent $R_{sub}(f)$ and $C_{sub}(f)$ can be extracted.

Once the resistivity profile has been simulated in TCAD, the entire modelling stream takes place in Matlab and can be swiftly integrated with other scripts. By choosing an appropriate mesh density, the computation is significantly reduced to a few seconds.

The substrate network model is now used to reproduce CPW measurements. Because no SRP was available for the wafers in this study, a set of representative doping profiles were generated. These doping profiles are computed using the solution to Fick's second law:

$$N_A = N_{A,bulk} + n_0 \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right), \tag{4.30}$$

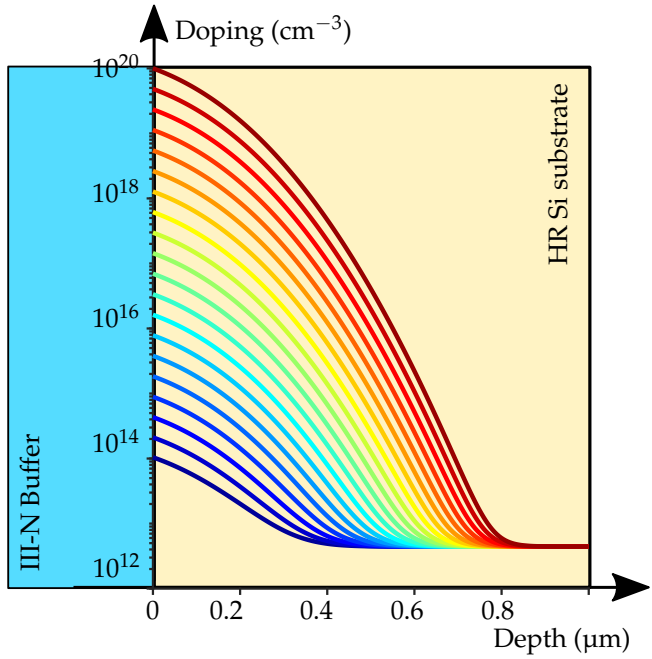


Fig. 4.25 Set of representative surface doping profiles used to represent substrates with varying resistivity (blue: limited PSC, red: significant PSC).

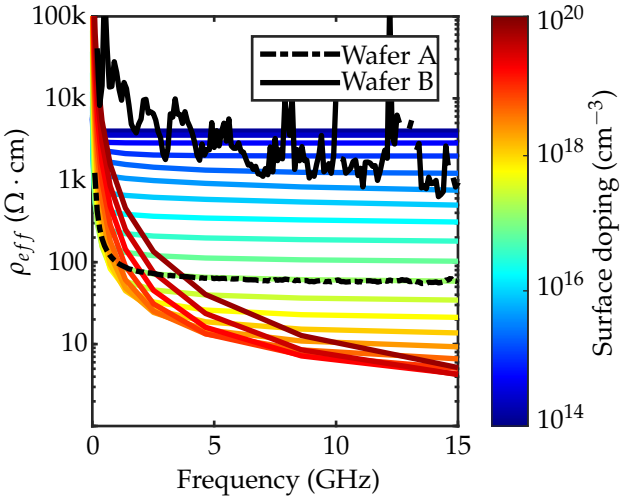


Fig. 4.26 Simulated effective resistivity as a function of frequency for the different PSC layer doping profiles shown in Fig. 4.25. The measured wafers A and B are overlaid on the simulations, allowing to find the corresponding PSC profile.

in which $N_{A,bulk}$ is the doping concentration deep into the Si substrate (corresponding to 3 k$\Omega \cdot$ cm as specified by the supplier), n_0 is the surface doping and $\sqrt{Dt}$ is the diffusion length. It is known that the doping profiles in Si respect eq. 4.30 for GaN-on-Si processes, as already shown in chapter 2 and also in [49]. The diffusion length is fixed at 100 nm, which is typical for a GaN-on-Si thermal budget. n_0 is varied from 1×10^{14} cm^{-3} (well-controlled Al diffusion) to 1×10^{20} cm^{-3} (extremely severe Al diffusion). The resulting doping profiles are represented schematically in Fig. 4.25. The geometries for P1 and P2 were adapted to the CPW dimensions (see Fig. 4.19). After Y parameter computation, the equivalent $R_{sub}(f)$ was used to extract $\rho_{eff}(f)$. Simulation results are shown in Fig. 4.26 overlaid with experimental data for wafers A and B. The frequency dependence of $\rho_{eff}(f)$ is well-captured by the model. At low frequencies, the "slow-wave mode" translates into a substrate impedance dominated by the insulating buffer. For higher frequencies (quasi-TEM mode), the buffer impedance decreases and the substrate impedance is dominated by the conductive substrate. The transition frequency between these two regimes increases with decreasing substrate resistivity, as shown in Fig. 4.27.

Each wafer can be related to a PSC surface doping by comparing its

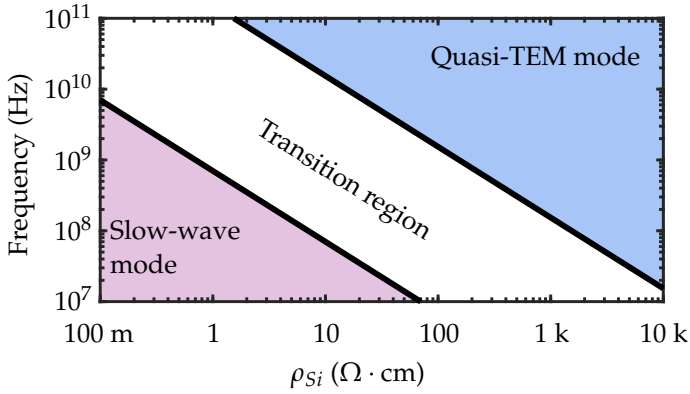


Fig. 4.27 Propagation modes in a 1.8 µm III−N/1 mm Si microstrip line as a function of frequency and Si resistivity. The transition between the slow-wave mode and the quasi-TEM mode takes place at lower frequencies as the Si resistivity increases. Transition frequencies are computed following [133].

$\rho_{eff}(f)$ curve with a simulated curve. Note that a single (f, ρ_{eff}) point can be associated to multiple surface doping values and it is thus important to consider the full frequency response. The match with experimental data is achieved for a surface doping of $\sim 1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $\sim 1 \times 10^{15}\,\mathrm{cm}^{-3}$ for Wafer A and Wafer B, respectively.

Now that CPW measurements could be reproduced and the modelling methodology validated, dimensions can be modified to match a typical HEMT device.

4.3.5 Prediction of power loss inside the GaN-on-Si substrate

The impact of a conductive substrate on the PAE is now explored using the model described earlier. The same set of PSC doping profiles is used as in Section 4.3.4 and the total dielectric thickness and permittivity is adapted for the simulation of a transistor (S/D contacts lie directly on the III-N, while CPW lines lie on an additional ∼1.3 µm of SiO_2). The lateral dimensions of a typical HEMT (L_{SD} = 2.7 µm) are then used to create the RC network. Results for R_{sub} and the resulting PAE penalty points are shown in Fig. 4.28. The PAE penalty is calculated as the difference between the maximum value ($\theta = 1$ in eq. 4.20) and the calculated value with finite R_{sub}. R_{sub} is given for a 100 µm-wide device similar to what was measured above (Fig. 4.22). The results from Fig. 4.28 are discussed in detail in the following.

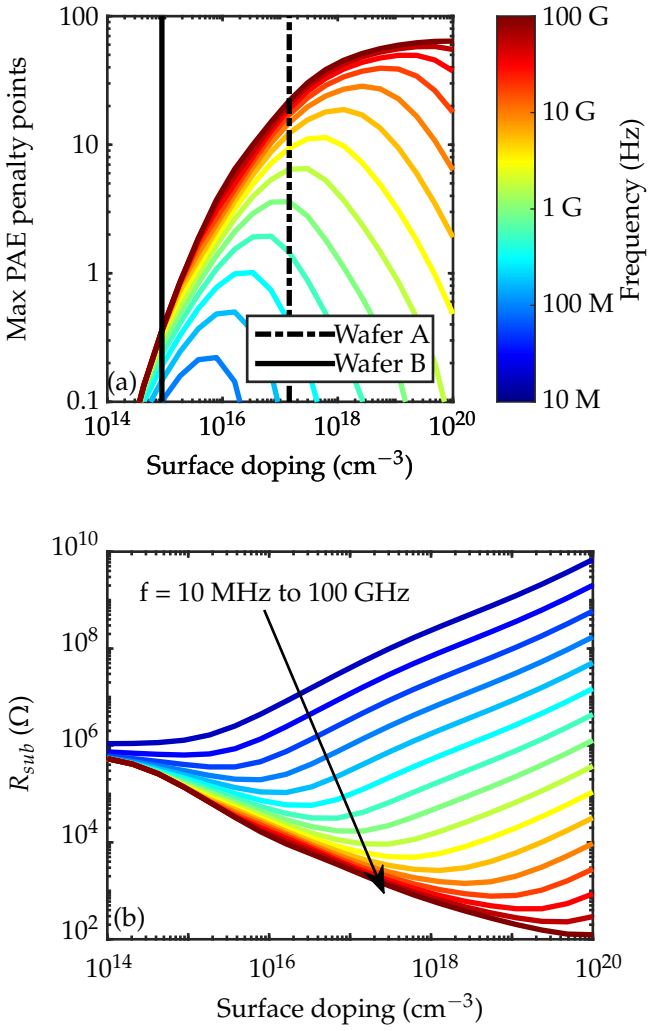


Fig. 4.28 (a) PAE penalty as a function of the simulated PSC layer surface doping for frequencies logarithmically spaced between 10 MHz to 100 GHz. The measured wafers are added in black after correlating effective resistivity with PSC surface doping. (b) Corresponding R_{sub}. The considered transistor has source-drain spacing of 2.7 µm.

For very low frequency, the insulating buffer has a very large impedance. As a result, the conductive substrate is effectively disconnected from the HEMT and R_{sub} is very high, irrespectively of the doping in the PSC layer. The resulting PAE penalty is negligible. At medium to high frequencies, the impedance of the insulating buffer decreases and the HEMT sees the conductive substrate, leading to a reduced R_{sub} and a decrease in PAE. Counterintuitively, at a given frequency there exists a PSC doping for which R_{sub} is minimal and PAE penalty maximal. Indeed, for a very conductive PSC layer, the transition frequency f_{sub} from which the substrate starts to conduct can possibly be higher than the operating frequency, and equivalent R_{sub} can be high with no PAE penalty. This regime correlates to the "slow-wave mode" in CPW line data. However, using low-resistivity Si for the realization of GaN-on-Si MMICs is not an acceptable solution, as such a circuit would suffer from increased crosstalk and the integration of low-quality factor passive elements. At the other end of the PSC layer doping spectrum (low doping), f_{sub} is well below the operating frequency but R_{sub} stays high owing to the highly resistive substrate.

Owing to more significant field penetration at high frequency, the worst-case PAE penalty increases with frequency: from less than one point at 100 MHz, a > 40 point drop in PAE is predicted at 28 GHz for a surface doping of $\sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$. Consequently, a careful engineering of the RF substrate is critical to enable high-efficiency PAs at FR2 and mm-wave bands. To keep the impact of substrate loss under control with a PAE penalty of less than 1 point regardless of the operating frequency, surface doping should be limited to $\sim 2 \times 10^{15}\,\mathrm{cm}^{-3}$. Finally, it is possible to place wafers A and B on the PAE penalty plot of Fig. 4.28a using the surface doping that fits the experimental $\rho_{eff}(f)$ (see Fig. 4.26). The predicted PAE penalty suffered when moving from Wafer B to Wafer A is ∼15 points at 28 GHz, close to the 17-point difference observed experimentally.

4.3.6 Power loss under high temperature operation

It has been demonstrated in Section 1.5 than ρ_{eff} is strongly dependent on the Si temperature, as both mobility and carrier concentration are effected by a temperature change. Because of the large power density, a considerable amount of self-heating is expected in the region near and below the PA. As the temperature in the Si substrate increases, it is important to study how the consequent change in substrate performance would modify the PAE.

The doping profiles for Wafers A and B are simulated at temperatures

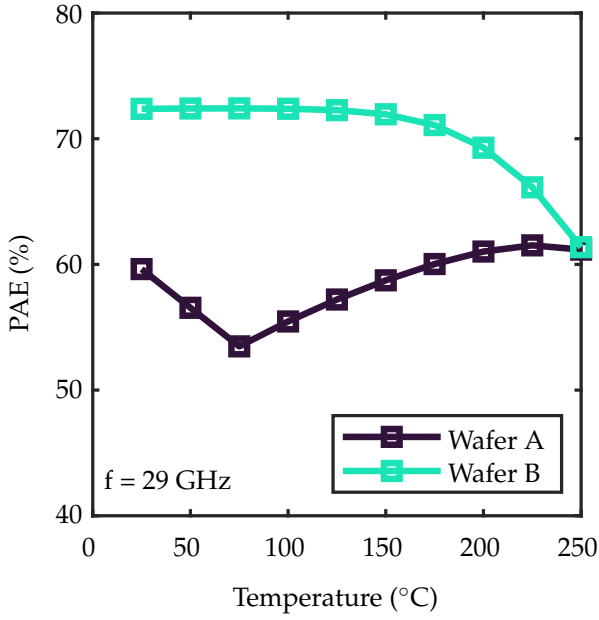


Fig. 4.29 Simulated evolution of the PAE with temperature for the doping profiles corresponding to Wafers A and B.

ranging from 25 °C to 250 °C. Then, the PA model is ran for each resulting resistivity profiles as described above. The results at 29 GHz are displayed in Fig. 4.29.

For Wafer B which shows a high ρ_{eff} (low surface doping), the PAE is stable until $\sim$ 150 °C. Then, as the intrinsic carrier number exceeds the doping in the bulk Si, the substrate becomes lossier and PAE drops. For Wafer, with higher surface doping, the PAE initially worsens with temperature before increasing as the surface mobility decreases. At 250 °C, both wafers show comparable PAE.

In conclusion, for normal operating temperatures (less than 150 °C in Si), the high-ρ_{eff} wafer is superior and leads to the lowest PAE penalty. For extreme temperatures exceeding 250 °C, the interest of a low-loss substrate is counterbalanced by the significant increase in Si conductivity. As discussed in Section 1.5, a thinning down of the superlattice strain relief buffer would lead to a higher Si surface temperature. Then, the advantage of HR Si over standard Si would become less obvious.

4.4 Chapter summary

This chapter assessed how the bottom layers of the GaN-on-Si stack, in which the substrate loss originates, can impact the uppermost layers containing the functional devices and circuit. Linking the material properties of the underlying substrate with device functioning, two important functional blocks were analyzed.

For the RF switch, is was shown that substrate-induced HD can contribute significantly the the non-linearity of a common-gate device. The relative part of the substrate compared to intrinsic device non-linearity could be estimated with help of a Thru line structure capturing only the substrate distortion. By comparing two different devices, it was then shown that a co-optimization of device and substrate non-linearity is needed to reach highly-linear switches. Finally, the correlation between ρ_{eff} and HD leads to the proposition of a specification in terms of ρ_{eff}, that is specific to a device non-linearity.

The most important application being the PA, its sensitivity to a lossy substrate was investigated. Experimentally, it was demonstrated that a correlation exists between substrate loss and PAE, suggesting that RF power dissipation in the substrate takes place. To predict the amount of dissipation, a combination of waveform analysis, TCAD simulation and custom-made Matlab modelling was employed. Finally, a model for a substrate resistance was reached and inserted into a simplified equivalent circuit to predict the PAE penalty suffered because of the substrate. The results matched the experimentally observed difference in PAE on two GaN-on-Si wafers. Finally, the model was used to predict the effect of operation temperature on the PAE drop.

5

Perspectives and conclusions

After exploring in detail the origin of substrate loss in GaN-on-Si technology, engineering the AlN/Si interface to reduce it, understanding the time dependence of substrate properties and assessing the impact they have on active circuits, this chapter takes a step back on the thesis. First, the environmental aspect is discussed. Then, an alternative route is explored and compared before drawing the conclusions percolating from this work.

The substrate performance of GaN-on-Si is approaching the state-of-the art trap-rich SOI, with ρ_{eff} above a few k$\Omega \cdot$cm and high linearity. The technological landscape for a substrate-sensitive application can thus now comprise GaN-on-Si. However, in order to help limit the consequences of the anthropocene, the choice of a certain technology must take into account its potential impact on the crossing of planetary boundaries. In Section 5.1, the environmental aspect is added as a criterion of choice besides performance and cost.

In Section 5.2, a different solution to eliminate the substrate-related issues by porosification of the Si substrate is discussed. A first successful demonstrator is presented, with its advantages and drawbacks.

Finally, Section 5.3 presents a summary of this thesis along with an outlook emerging from it.

5.1 Environmental analysis of RF substrates

The scientific content presented in this section is the result of a collaboration with Benjamin Vanhouche, PhD Student at imec and Vrije Universiteit Brussel at the date of publication of this thesis. For this reason, the study is presented in a condensed manner as an outlook. Extensive discussion on the sustainability aspects of RF substrates will be found in the PhD thesis of Benjamin Vanhouche.

5.1.1 Introduction

The sector of information and communication technologies (ICT) currently accounts for ∼4 % of the total greenhouse gases emissions [134]. This part can be expected to increase in the coming years with the predicted increase in electronic devices and connected objects. Limiting and even decreasing the impact of the sector is critical to respect the goals set by the Paris agreements. Because manufacturing accounts for a significant part (about 70 %) of the emissions associated with connected user equipment, it is particularly relevant to quantify the environmental impact of the fabrication of these devices [135]. According to [135], ∼40 % of the manufacturing impact of a smartphone can be attributed to the fabrication of the integrated circuit.

Because this thesis proposes a relatively new technology (namely, GaN-on-Si) as a relevant choice for RF FEM in terms of RF substrate performance, it is the responsibility of the development engineers to assess its potential environmental impact and compare it with other existing or potential platforms. In this way, an environmental criterion can be taken into account in addition to the performance, power, area and cost (PPAC) when performing the technological choice.

In this section, different semiconductor platforms with good RF performance (existing or foreseen) are compared in a life cycle analysis (LCA). The place of GaN-on-Si in the spectrum is discussed together with other Si-based or III-V/III-N technologies.

5.1.2 Scope of the LCA study

A LCA consists in the quantification of the impacts of an object and its corresponding inputs and outputs according to one or more indicators, during the entirety of its life cycle. It includes the production phase, the use phase and the end-of-life. As discussed above, for connected devices it appears that the production phase represents the largest chunk of the emissions.

Denomination	Starting wafer	Additional process steps
Si bulk	Si	n.a.
FD SOI	Si	Smart cut process
TR SOI	Si	Smart cut process + trap-rich layer
GaAs	GaAs	n.a.
GaN-on-SiC	SiC	GaN epitaxy
GaN-on-Si	Si	GaN epitaxy

Table 5.1 RF substrates compared in the life cycle analysis study.

This study will thus limit itself to a so-called cradle-to-gate analysis. The production phase is considered from the cradle, or the extraction of the raw materials, to the exit of the product through the gate of the factory. Because the study of the transistors themselves and their fabrication is out of the scope of this thesis, the finished product is considered to be an engineered substrate with no devices fabricated on top. It should be noted that the starting wafer significantly contributes to the overall semiconductor manufacturing chain.

The RF substrates considered in this study are listed in Table 5.1. For Si-based technologies, no difference is made between high resistivity and standard resistivity Si. Because the different technologies compared use different wafer sizes (ranging from 150 mm to 300 mm diameter), the functional unit of $1\,cm^2$ of RF substrate is considered. This takes into account the energetic advantage of processing large wafers, but assumes that a given wafer area offers the same functionality for every technology, which is not necessarily true (e.g., a GaN PA could perhaps take less area than a GaAs PA).

The technologies are compared according to two environmental indicators.

Global warming potential (GWP). It represents the amount of greenhouse gases emitted along the fabrication. GWP is expressed in $kgCO_{2,eq}$.

Abiotic depletion potential (ADP). It provides a quantification of the depletion of the material resources on the planet associated with the fabrication of the RF substrate. An extensive discussion of ADP can be found in [136]. It can be best understood by its definition:

$$ADP_i = \frac{DR_i/(R_i)^2}{DR_{ref}/(R_{ref})^2}, \tag{5.1}$$

in which DR_i is the extraction rate of resource i and R_i is the ultimate reserve of resource i. It can be seen that ADP takes into account the scarcity of each material. The reference resource is antimony, meaning that ADP is expressed in $kgSb_{eq}$. While the ADP of materials is obvious (extracting materials from the earth crust depletes their reserves), other more abstract fabrication inputs such as electricity contribute to it as well. Indeed, the electrical network also uses up scarce materials.

5.1.3 Life cycle inventory

In order to correctly quantify the GWP and ADP of each RF substrate, a breakdown of every process step in terms of energy and material consumption and greenhouse gases emission is required. The life cycle inventory (LCI) is performed for all the technologies under study. Detailed information on the LCI is available to the reader in Appendix C, and is summarized hereafter.

Si wafer

The fabrication of a Si wafer is a complex sequence of steps: material extraction, purification, doping. Here, the impact associated to a Cz-Si wafer is taken from the well-established database Ecoinvent [137].

GaAs wafer

Similarly, the GaAs wafer process flow is quite intricate. The most critical step is the vertical gradient freeze (VGF) during which the ingot is recrystallized. It is a particularly energy-intensive fabrication step. The complete flow is studied in [138].

SiC wafer

Unlike Si and GaAs, the fabrication of an SiC wafer is not based on purification and crystallization of the liquid phase material. Rather, a SiC powder is sublimated in a high-temperature reactor and transported to the ingot seed. This physical vapor transportation (PVT) step takes place at temperatures above 2000 °C. The SiC fabrication is modelled in [139].

GaN epitaxy

Consisting of a single process step, the MOCVD growth of the epitaxial III-N stack is modelled by considering a growth time of ∼3 hours for a standard, 2.5 µm-thick stack in imec's Aixtron reactor. The energy consumption of

the reactor, not directly available, is adapted from [140]. The emission of greenhouse gases such as methane is also considered. For GaN-on-SiC, the buffer thickness is assumed to be limited to 1 µm owing to the lower lattice mismatch.

Smart-cut process and Trap-rich layer deposition

The fabrication of SOI wafers relies on the smart cut process, which is described in detail in [141]. Its many individual steps are not detailed here. Following internal communications, the seed wafer is assumed to be re-used 50 times before being trashed. This recycling is an important contributor to the relatively low impact of SOI. The trap-rich layer is assumed to be a 2 µm-thick layer of polysilicon (Poly Si), as described in [9].

All cleanroom-related process steps are modelled within the virtual fab LCA tool developped at imec : imec.netzero. It includes material and energy consumption of a wide range of process flows as well as fab models. A detailed study of a complete process flow using this tool can be found in [142].

5.1.4 Results and discussion

Following the LCI, the impact of the different technologies according to GWP and ADP is presented in Fig. 5.1. The impact is split between the fabrication of the wafer itself (which, for Si bulk and GaAs, is also the end product) and the process leading to the engineered RF substrate.

GaN-on-SiC emerges as the most impactful of the considered substrates. With about one order of magnitude more GWP as the rest, it is penalized by the PVT process which is highly energy intensive. The VGF process is also the main cause of the relatively high GWP of GaAs. Si-based technologies benefit from the lower impact of the Si wafer manufacturing. The processing leading to an FD SOI wafer only slightly degrades its GWP compared to bulk Si. Indeed, the process steps show a limited thermal budget, and the extensive recycling of the seed wafer reduces its impact by a factor 50. The high-temperature deposition of the thick Poly Si increases the thermal budget and thus GWP, with the benefit of greatly improved substrate performance [7]. The p-n passivation technology, not explored here, could lead to comparable substrate performance with a limited increase in GWP [143].

The high thermal budget of III-N epitaxy makes GaN-on-Si the most impactful of all substrates using a Si wafer. Here, the additional processing dominates the GWP over the Si wafer fabrication. Note that the MOCVD-related GWP is directly proportional to the buffer thickness. Reducing the

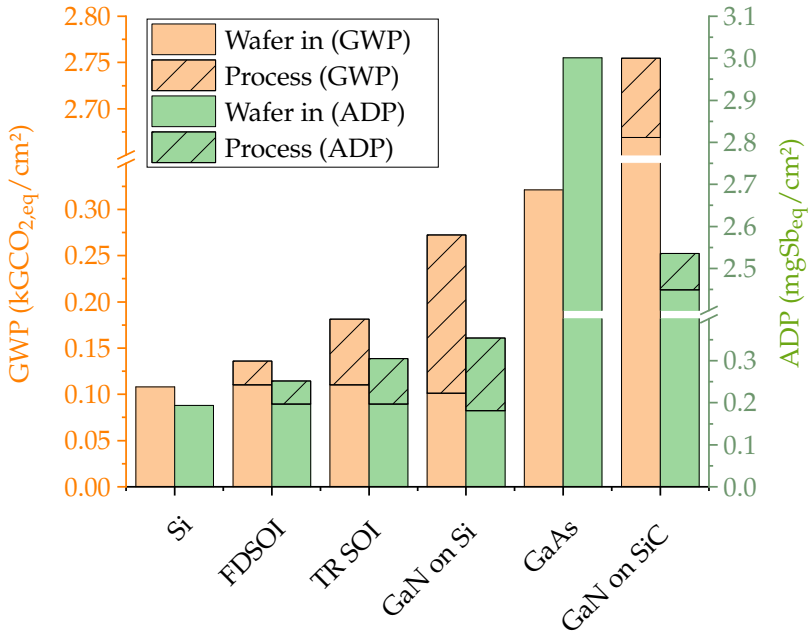
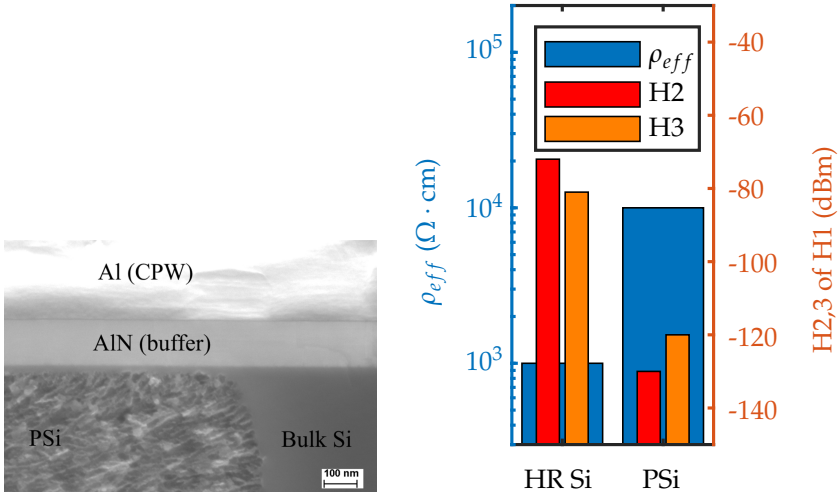


Fig. 5.1 Results of the LCA for the production of different RF substrates. GWP and ADP are indicated and split in the starting wafer fabrication and the additional processing needed to reach an engineered RF substrate.

buffer thickness by a factor of two could bring the GWP of GaN-on-Si in the vicinity of TR SOI while reducing the parasitic dopant diffusion in Si. However, doing this requires improving the buffer engineering as GaN crystal quality and vertical breakdown would be degraded.

Overall, ADP follows the GWP trends, owing to the finite ADP related to the use of electricity and the large reserves of Si material. The only exception is the GaAs wafer, where large quantities of Ga and As, relatively scarce materials, are needed. In this respect, the use of thin films of the III-N or III-V material on a Si wafer shows a clear advantage. As only a ~ 2 µm-thick layer of Ga-containing material is used for GaN-on-Si compared to the $\sim$700 µm-thick GaAs wafer, the ADP related to Ga is more than 300 times smaller.

In conclusion, from an environmental standpoint, GaN-on-SiC should be avoided for user equipment due to the highly impactful fabrication of an SiC wafer. The use of III-N or III-V materials in a bulk fashion (e.g., a GaAs wafer) is also advised against, as it leads to significant depletion of scarce materials resources. Instead, such materials should be used as thin-films, such as GaN-on-Si. However, the Si-based technologies are still superior. They seem to benefit from their relatively simple (and energy-efficient) processing, as well as from the large Si reserves. In the future, the LCA should be performed under the assumption of a telecommunication infrastructure application, in which the use phase might have a more significant impact, favoring highly-efficient technologies. Other indicators such as water usage and toxicity should also be considered.



(a) SEM image of the post-process AlN/PSi sample. Reproduced from [144]. ©2023 IEEE.

(b) Small- and large-signal performance of AlN/PSi and AlN/HR Si samples. Data taken from [144].

Fig. 5.2 Demonstration of local post-process porosification of Si in AlN/Si structures. The Si is locally porosified under CPW lines to improve the substrate performance.

5.2 Alternative substrate loss mitigation approach: GaN-on-Porous Si

While this thesis proposes understanding of the physical phenomena leading to degraded performance and solutions to mitigate them, GaN-on-Porous Si constitutes a drastic way to suppress all substrate-related issues. As a post processing step, it is possible to locally (e.g., under CPW lines) transform the monocristalline Si substrate into Porous Si (PSi) [144]. Outstanding substrate performance of PSi has been demonstrated in SOI, with $\rho_{eff} > 5\,\text{k}\Omega \cdot \text{cm}$ and H2 as low as -115 dBm (for H1=15 dBm at 0.9 GHz)[145].

A local, post-process porosification process is demonstrated by Incize on AlN-Si wafers fabricated at imec (Fig. 5.2a). The AlN layer serves as an etch stop, and GaN layers are expected to stay unaffected by the process. It should be noted that low-resistivity Si is necessary for PSi fabrication. The RF performance of this demonstrator (Fig. 5.2b) is very competitive, as expected: $\rho_{eff} \approx 10\,\text{k}\Omega \cdot \text{cm}$ and H2 is lower than -120 dBm at 15 dBm of

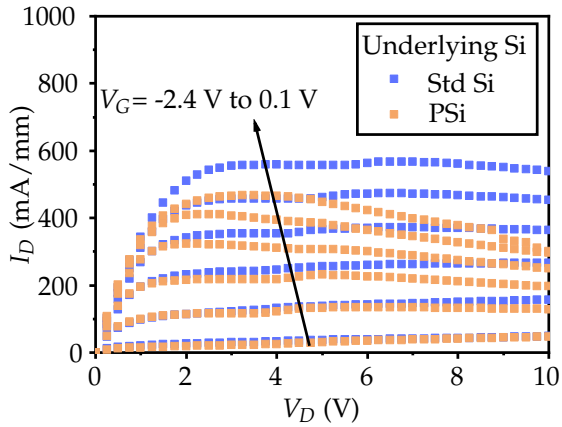


Fig. 5.3 $I_D - V_D$ characteristics for a 0.5 µm GaN device. One device is located above porous Si, one above standard resistivity crystalline Si. The two devices are on the same wafer. Significant self-heating is clearly observable in the device lying on top of porous Si.

H1 and at 0.9 GHz.

Following the successful implementation of PSi under AlN, the process could be performed under a fully processed GaN-on-Si wafer. Similarly to AlN/Si substrate performance is excellent. However, it is not possible to reliably use GaN HEMTs on PSi if they are expected to function at a high power density. Indeed, PSi is a poor thermal conductor. As a consequence, self-heating in the HEMT is severly degraded, as shown in Fig. 5.3. Some devices were even seen to fail. PSi is a promising way to suppress susbtrate-related parasitics under passive structures such as transmission lines or inductors. However, it is not possible to use PSi under active devices because of the increased self-heating. Under these regions, other substrate loss mitigation techniques such as those proposed in this thesis (in particular in Chapter 2) must be employed.

5.3 Concluding summary and outlook

5.3.1 Concluding summary

This thesis proposed an analysis of the substrate-related parasitic effects in GaN-on-Si stacks, which must be mitigated to enable high-performance circuits for future telecommunication generations. The contribution and impact of the different layers of the stack were successively investigated.

First, after presenting the RF characterization methodology, the HR Si substrate and the PSC layer were studied. The operation temperature and HEMT processing steps can significantly affect the substrate performance. Then, the AlN/Si interface and the AlN nucleation layer were characterized using a wide array of methods. A TCAD model could reproduce the contribution of this interface. The next layer of the HEMT stack is the C-doped buffer, which leads to a new phenomenon: the time dependence of substrate properties. Here also, a combination of modelling and novel characterization techniques allowed to identify the role of C traps. Finally, the active layers were considered in relation with the substrate. The impact of a lossy, non-linear substrate on the RF Switch and PA were examined.

Three important scientific questions were raised in the introduction of this work. They will now be considered in the light of the learnings emerging from this thesis.

Understanding *What are the main contributions to degraded substrate performance in GaN-on-Si and what is the role played by the complex epitaxial stack in it?*

There are two main contributions to a reduced effective resistivity and linearity in GaN-on-HR Si substrates. Firstly, the doping by Al (and Ga) atoms of the surface of the HR Si substrate can lead to the formation of a PSC layer. Secondly, the interface charge at the interface between AlN and Si can be significant and attract free carriers at the Si surface by field effect which also form a PSC layer (field-induced). Those two contributions are independent of each other.

The epitaxial stack plays a major role in the substrate performance. The phenomenon of time dependence of substrate performance (effective resistivity and distortion), unique among Si-based RF substrates, is caused by charge redistribution in the buffer. The traps created by C doping emit and capture free carriers which are able to travel across the buffer, mostly with the help of extended defects such as dislocations. This causes the

PSC layer conductivity to slowly and significantly change over time when the substrate is stressed. Also, the different steps leading to the growth of GaN layers and HEMT fabrication, by their thermal budget, can modify the n-type doping of Si.

Predicting *To what extent does the substrate affect the functioning and figures of merit of key target applications for RF GaN-on-Si and what are the substrate specifications for a limited impact?*

The harmonic distortion induced by the substrate can significantly contribute to the non-linearity of an RF switch. By measuring a Thru line with dimensions similar to a switch, it is possible to isolate the substrate part and quantify the effective resistivity that is needed for the intrinsic device non-linearities to dominate the distortion. A co-optimization of the substrate and the device is needed to reach highly-linear switches.

For the PA, the lossy substrate can couple to the HEMT and lead to RF power dissipation. This degrades the efficiency by up to 15 points, which is confirmed experimentally. With a physics-based modelling approach, it is possible to estimate the degradation as a function of frequency and substrate performance. Highly resistive substrates are preferred to limit the power dissipation, except for very high temperature operation.

Improving *Is it possible to consistently fabricate high-performance GaN-on-Si substrates, without relying on long and costly process optimization cycles?*

Once the parasitic doping has been optimized by adapting epitaxial conditions, it is important to control the interface charge between AlN and Si. This interface charge is linearly dependent on TMAl predose, which is applied before growing the AlN material. In order to cancel out the interface charge for any process window, it is sufficient to produce two samples with different TMAl predose and make use of the linear relationship that can be inferred from C-V measurements. A N isolation implant tuned to cause sufficient damage to the 2DEG region but not too much in the upper buffer layers then allows to limit the additional charge induced by the many defects.

Assessing *What is the environmental impact of GaN-on-Si compared to other competing technologies that offer state-of-the-art substrate performance?*

In terms of global warming potential and abiotic depletion potential, GaN-on-Si offers a significant improvement from GaN-on-SiC, which suffers from

an energy-intensive starting SiC wafer. Compared to Si-based technologies, in particular trap-rich SOI, GaN-on-Si is more impactful. In order to reduce its embodied emissions, the GaN-on-Si industry should aim at a reduction of the epitaxy thermal budget, either by a reduction of the epitaxial stack thickness or by a lower growth temperature.

5.3.2 Discussion

Reach of this thesis beyond GaN-on-Si

Heterogeneous integration of compound semiconductors on Si is not limited to GaN. In particular, InP and related compounds are promising materials with applications well into the mm-wave. There also, a high substrate performance will be required to meet the application requirements.

More closely related to GaN-on-Si are other integration approached presented in Section 1.2.1. For GaN-on-SOI and GaN-on-engineered substrate, a relatively thick (10 µm) Si film is still used below the III-N layers to allow successful epitaxy. This thickness is larger than the typical diffusion length for Al and Ga, which typically reach no more than a few micrometres in the Si substrate. Interface charge between AlN and Si is not avoided by these approaches, and buffer charge redistribution considerations also remain. Consequently, the findings of this thesis can fully be applied to these alternative approaches. It should be noted that the inclusion of a trap-rich layer below the buried oxide in GaN-on-SOI might only lead to a moderate improvement of substrate performance. Indeed, the 10 µm-thick Si film is expected to host the formation of a PSC layer that would not be suppressed by the trap-rich layer. One solution could be to thin down the SOI film until it is completely depleted and resistive.

GaN-on-SiC presents the significant advantage of a semi-insulating substrate, where no PSC layer can exist.

Trade-offs regarding layer thicknesses in GaN-on-Si

This thesis brings forward additional trade-offs that must be taken into account when designing GaN-on-Si stacks.

Regarding diffusion of Al (and Ga) atoms, increasing the thickness of the III-N buffer leads to additional thermal budget, which has been linked to increased diffusion in [49]. If reducing the growth temperature is possible, it might be possible to grow thicker buffers without a significant thermal budget penalty.

Modifying the buffer thickness also changes the vertical spacing between

the CPW line and the conductive Si substrate. The thickness of the epitaxial stack impacts ρ_{eff}, as shown in Fig. 1.7. However, as the CPW pitch increases beyond $\sim$ 10 µm, this effect becomes limited (a few hundred $\Omega \cdot$ cm difference between AlN only and a full buffer). For transistors with smaller pitches between source and drain, this is a more important concern.

The interface charge at AlN/Si interface is not expected to change significantly with the buffer thickness. Additional fixed charge in the upper III-N layers might be thickness-dependent, but can be compensated by appropriate TMAl predose.

Buffer charge redistribution processes were shown to be almost independent of the thickness of the C-doped layers.

Thermal simulations have demonstrated a majoritarian contribution of the superlattice strain relief buffer to the overall thermal resistance of the III-N stack. The reduction of thickness in this layer would thus lead to an increase in the temperature at the Si surface. It is known that the substrate performance is degraded at temperatures higher than 125 °C so caution is needed when adjusting this layer's thickness.

Finally, the thermal budget of III-N epitaxy is a major contributor to the environmental impact of GaN-on-Si. In order to reduce the GWP and ADP of the MOCVD growth step, a reduction of the buffer thickness is seen as a promising approach.

These trade-offs come in addition to the existing ones in terms of crystal quality and device scaling.

Third harmonic

For long CPW lines (2 mm), the substrate HD is dominated by the second harmonic. However, for shorter CPW lines and common-gate HEMT devices, the third harmonic becomes significant. The reason for this higher H3 is not entirely clear at this stage, although some hypotheses exist. Also at higher H1 power levels more relevant to GaN-on-Si, H3 can cross H2 even for long CPW lines and become dominant. There, a total HD figure of merit would perhaps contain a more relevant indication of the substrate non-linearity.

Correlation between effective resistivity and HD

Such a correlation has been demonstrated experimentally for various types of III-N stacks, but it is presently not clear why the slope of the ρ_{eff}-HD trendline is different for fully-processed HEMT stacks compared to other stacks. Also, there is currently no physical argument to explain the particu-

lar value obtained for the slope.

5.3.3 Outlook

Several future undertakings can be envisioned from this thesis, which established a solid base for the characterization and modelling of Si-based RF substrates.

Semi-vertical characterization structures These novel characterization devices constitute a promising methodology to characterize HR Si MI(O)S structures. With process development and layout optimization, it will be possible to access the electrical properties of the interface.

Non-linear effect of the substrate on the PA Linearity is a key aspect of the PA. Similarly to the RF switch, it can be expected that substrate distortion contributes to PA FOM beyond the first-order power loss considered here. The quantification of these effects will require integration of a non-linear substrate model with a large-signal model of the PA. Possibly, the R-C elements in the meshed equivalent circuit could be made non-linear.

A dimension-agnostic substrate figure of merit Clearly, a limitation of effective resistivity is its dimension-dependence. When the characteristic dimension of the substrate-sensitive device (CPW, transistor) becomes small, it cannot be used directly. Here, an evolution of the formalism could make the modelling task easier and also produce a truly CPW cross-section independent figure of merit.

Assessment of the environmental impact of RF technologies The LCA performed at the substrate-level in this thesis opens additional questions related to the sustainability of RF technologies. Additional indicators, in particular the water usage, should be included. The study could be extended to the transistor level, where significant energy consumption takes place especially for scaled devices. Finally, the functional unit can be improved and modified depending on the end application (user equipment versus base station).

Appendices

A

Poole-Frenkel mechanism

This appendix aims to provide a brief description of the Poole-Frenkel conduction mechanism, which is encountered in several charge transport phenomena in GaN-on-Si stacks.

1.1 Potential barrier lowering

The Poole-Frenkel effect originally relates to the emission or capture barrier for a trap level in the semiconductor bandgap. In the absence of electric field, the emission rate of electrons from an donor trap is given by:

$$e_n = v_n \sigma_n n_i \exp \frac{E_T - E_i}{k_B T}, \tag{A.1}$$

in which v_n is the electron thermal velocity, σ_n is the electron capture cross-section, n_i is the intrinsic carrier density and E_i is the intrinsic energy. In other words, there is a potential barrier for electron emission which is equal to $E_T - E_i$. When the material is subjected to an electric field, the potential barrier is lowered as shown schematically in Fig. A.1. As a consequence, the emission rate in eq. A.1 is modified such that:

$$\frac{e_n}{e_{n0}} = \exp \frac{\Delta E_{PF}}{k_B T}. \tag{A.2}$$

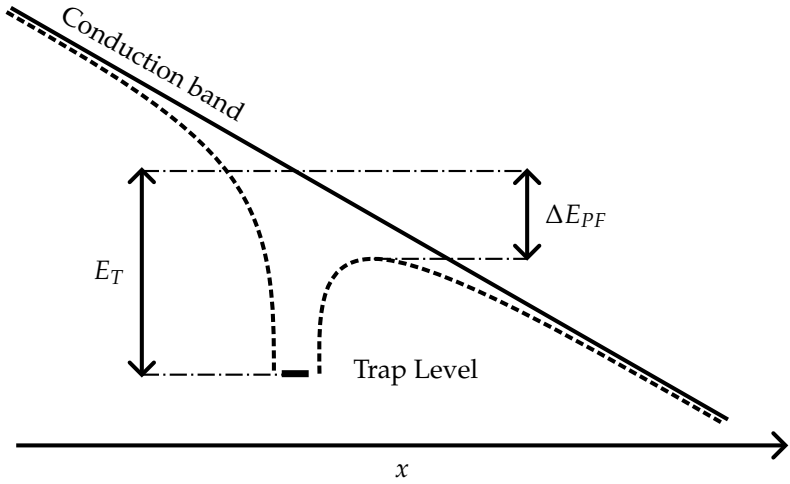


Fig. A.1 Energy diagram of a semiconductor material subjected to high electric field. The potential barrier for the emission of a free carrier from the trap level to the conduction band is decreased by ΔE_{PF}.

The potential barrier lowering, ΔE_{PF} is given by:

$$\Delta E_{PF} = \sqrt{\frac{q^3|F|}{\pi\varepsilon}}, \tag{A.3}$$

in which F is the electric field. Consequently, the emission rate increases exponentially with the square root of electric field.

1.2 Poole-Frenkel mobility

For a wide bandgap material such as GaN or AlN, the number of free carriers participating in in-band conduction is very low. Then, conduction can occur *via* different conduction mechanisms. In particular, under high electric field, charge transport can originate in emission of free carriers by the Poole-Frenkel mechanism. The resulting mobility then follows an exponential dependence on electric field similar to eq. A.2:

$$\mu = \mu_0 \exp\frac{-E_T}{k_B T} \exp\frac{\sqrt{\frac{q^3|F|}{\pi\varepsilon}}}{k_B T}. \tag{A.4}$$

The Poole-Frenkel mobility has been found to accurately describe a wide

variety of vertical transport experiments in GaN-on-Si (see Chapter 3 and also references [107], [108], [146], [147]) and AlN/Si (see Chapter 2 and references [67], [87]) stacks.

B

Conductance method for interface trap density extraction

The theoretical background behind the conductance method is described extensively in [77], [78]. Briefly, the response of interface traps to a small AC signal imposed on the MIS capacitor gate leads to a measurable loss. The resulting conductance is given by (in the ideal case of no spatial dispersion of the trap time constant):

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln\left[1 + (\omega\tau_{it})^2\right], \tag{B.1}$$

in which G_p is the real part of the admittance after subtraction of C_{AlN} and R_s (see Fig. B.1) and τ_{it} is the trap time constant. τ_{it} is defined as (in the case of an electron trap):

$$\tau_{it} = \frac{f_0}{v_{th}\sigma n_s}, \tag{B.2}$$

in which n_s is the surface electron density, v_{th} the thermal velocity, σ the capture cross-section and f_0 the trap occupation probability. Eq. B.1 is plotted against ω with DC bias as a parameter. An example theoretical curve is shown in Fig. B.2 The DC bias places the Fermi level at a certain

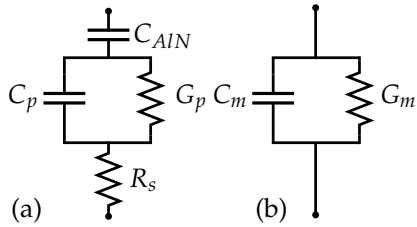


Fig. B.1 (a) Equivalent circuit of the AlN/Si MIS capacitor in depletion. The bulk Si substrate is represented by the series resistance R_s. (b) Measured admittance.

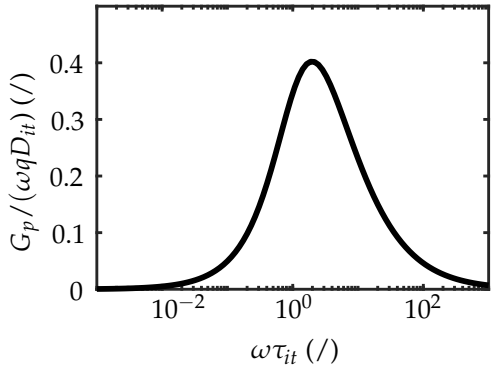


Fig. B.2 Graphical representation of Eq. B.1.

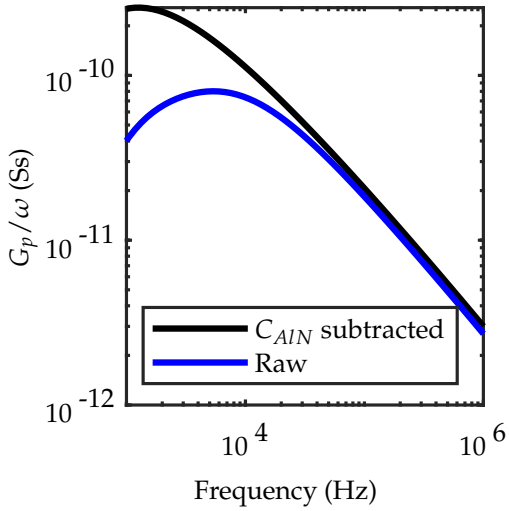


Fig. B.3 Calculated parallel conductance curves. Eq. B.1 is used to generate a theoretical G_p, which is put in series with a 175 nm-thick AlN layer capacitance. Failure to subtract the capacitance of the 175 nm-thick AlN layer before calculating G_p can shift both the location and height of the peak, sometimes even beyond the frequency range of measurement.

position in the bandgap, and only traps located close to the Fermi level contribute to loss in Eq. B.1. The graph then shows a peak at which $D_{it} \approx 2.5 G_p/(q\omega)$, which allows extraction of D_{it}. The corresponding bias point then has to be linked to the surface potential to construct the $D_{it}(\phi_s)$ distribution in the bandgap.

The subtraction of C_{AlN} is particularly critical for thick dielectrics such as the AlN nucleation layer. Failure to do so and considering directly extracting G_p as the real part of Y_m, the measured admittance, can change both the frequency and height of the G_p/ω peak, as illustrated theoretically in Fig. B.3. In Fig. B.4, this peculiarity is shown experimentally for an AlN/Si sample. While peaks in G_p/ω are seen in the raw data, they are shifted to frequencies lower than the instrument's limit after C_{AlN} removal . Subsequent extraction of D_{it} can then be severely overestimated.

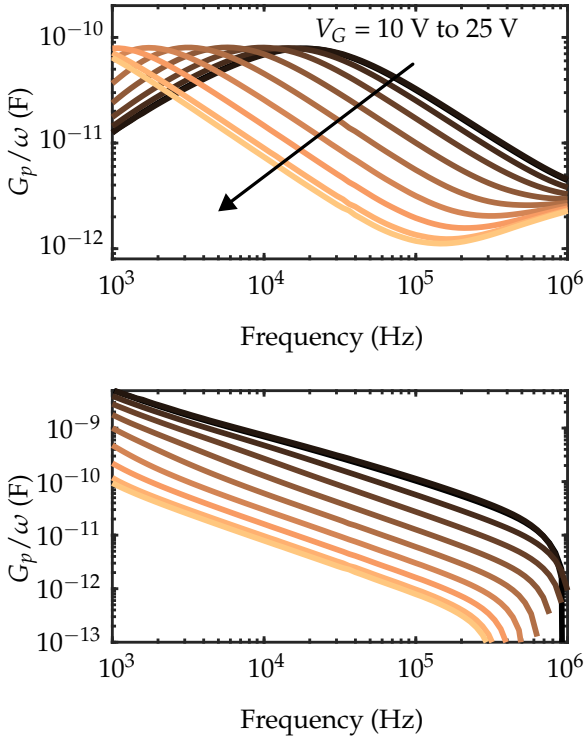


Fig. B.4 Measured G/ω-f curves for a 175 nm AlN-HR Si sample. (top) without C_{AlN} deembedding and (bottom) after C_{AlN} deembedding.

C

Supplementary information: LCA of RF substrates

This appendix contains more detailed information on the life cycle inventory (LCI) for the different RF substrates considered in Section 5.1.

3.1 Si wafer

The LCI for the fabrication of a Cz-Si wafer is taken from Ecoinvent. It comprises the extraction of raw SiO_2, its reduction and purification to electronic grade, and finally the Czochralski process and cutting of the ingot. The Czochralski process consists in the introduction of a seed crystal in the Si melt, and subsequent slow pulling of the crystal to create the ingot.

3.2 GaAs wafer

The LCI for the fabrication of a GaAs wafer is taken from [138]. Pure Ga and As are used to form a poly-GaAs ingot. Then, the ingot is crystallized using a vertical gradient freeze (VGF) process, where the material is locally heated to melt on a seed, and progressively freezes as the heated zone moves. For a single ingot, the VGF process is assumed to last one week. The ingot is then cut to obtain the GaAs wafers. It should be noted that some Ga is lost during the process but can be partially reclaimed and reused.

Due to the energy-intensive VGF process, the energy consumption for the fabrication of a GaAs wafer is higher than Si, with $\sim 265\,\text{kW}\cdot\text{h}$ per 150 mm-diameter wafer.

3.3 SiC wafer

The LCI for the fabrication of a SiC wafer is detailed in [139]. The process initiates with SiC powder, which is synthesized with the Acheson process from silica and carbon. The Acheson process consists in a carbothermal reaction, meaning that SiO_2 is reduce by carbon at high temperature to form SiC. The following steps form the so-called physical vapor transport (PVT) growth of SiC. Because liquid SiC does not exist, the powder must be sublimated. Then, the sublimated SiC is transported towards a seed, where a surface reaction takes place to allow the crystallization of a SiC boule. The sublimation temperature of SiC exceeds 2500 °C, leading to a significant thermal budget and energy consumption of the VGF step.

The study in [139] considers the growth of 150 mm-diameter SiC wafers, and takes into account the production of SiC powder ($280\,\text{kW}\cdot\text{h}$ per boule), PVT growth ($16\,250\,\text{kW}\cdot\text{h}$ per boule), and finally cutting. An energy consumption of $665\,\text{kW}\cdot\text{h}$ per wafer is obtained.

3.4 GaN epitaxy

For GaN-on-Si, the only additional process step required to reach an engineered substrate starting from a HR Si wafer is MOCVD growth. While flows of incoming and exhaust gases are available for the reactor installed at imec, the electricity consumption is unknown. It is particularly important to quantify the energy consumed for epitaxy as a high temperature is reache for a relatively long time (~ 3 hours).

In [140], an extensive LCA of III-N-on-Si photovoltaic cells is presented. From internal communication with Aixtron, an energy consumption value is presented for a typical epitaxy run. Since the reactor, wafer size and quantity, and buffer thickness are different from imec RF GaN-on-Si buffer, the energy consumption must be adapted. It is assumed that the normalized electrical energy consumption, computed in C.1, can be transferred to the epitaxial reactor at imec. This assumption probably overestimates the energy consumption for GaN-on-Si as large-area wafer reactors are expected to be more efficient. Furthermore, the reactor used in C.1 is a CCS-type reactor whereas RF GaN-on-Si is grown in a planetary-type reactor.

Wafer diameter	100 mm
Number of wafers	31
Total area	2435 cm^2
Epi thickness	3.53 µm
Electricity consumption per run	105.06 kW · h
Electricity consumption normalized with area and epi thickness	1.22×10^{-2} kW · h · $µm^{-1}$ · cm^{-2}

Table C.1 Properties of the epitaxial reactor considered in [140] used to reach a normalized electrical energy consumption.

For RF GaN-on-Si, an Aixtron G5 MOCVD reactor is considered. This reactor holds five 200 mm-diameter Si wafers. A III-N thickness of 2.505 µm is considered to reach an electrical energy consumption normalized with area of 3.06×10^{-2} kW · h/cm^2.

Regarding the impact of TMGa and TMAl, the precursors used in MOCVD growth of epitaxy, the extensive documentation found in [138] was used.

3.5 Smart cut process and trap-rich layer

The process flow used to fabricate a trap-rich SOI wafer is presented in Fig. C.1. It is detailed hereafter.

(a) A 1 µm to 2 µm-thick layer of poly-Si is deposited on the handle wafer using Low Pressure Chemical Vapor Deposition (LPCVD). This step occurs at ∼ 625 °C. Following LPCVD, a chemical mechanical polishing (CMP) step takes place.

(b) The handle wafer undergoes thermal oxidation in a dry atmosphere at ∼ 850 °C. The total oxide thickness (split between handle and seed) is of a few hundred nanometres.

(c) The seed wafer also undergoes thermal oxidation.

(d) Hydrogen ions are implanted at a shallow depth (∼ 1 µm) in the seed wafer.

(e) The handle and seed wafer are bonded together.

(f) A heat treatment at ∼ 300 °C allows to split the wafers. Then, a second heat treatment at a higher temperature (above 1000 °C for ∼ 2 hours)

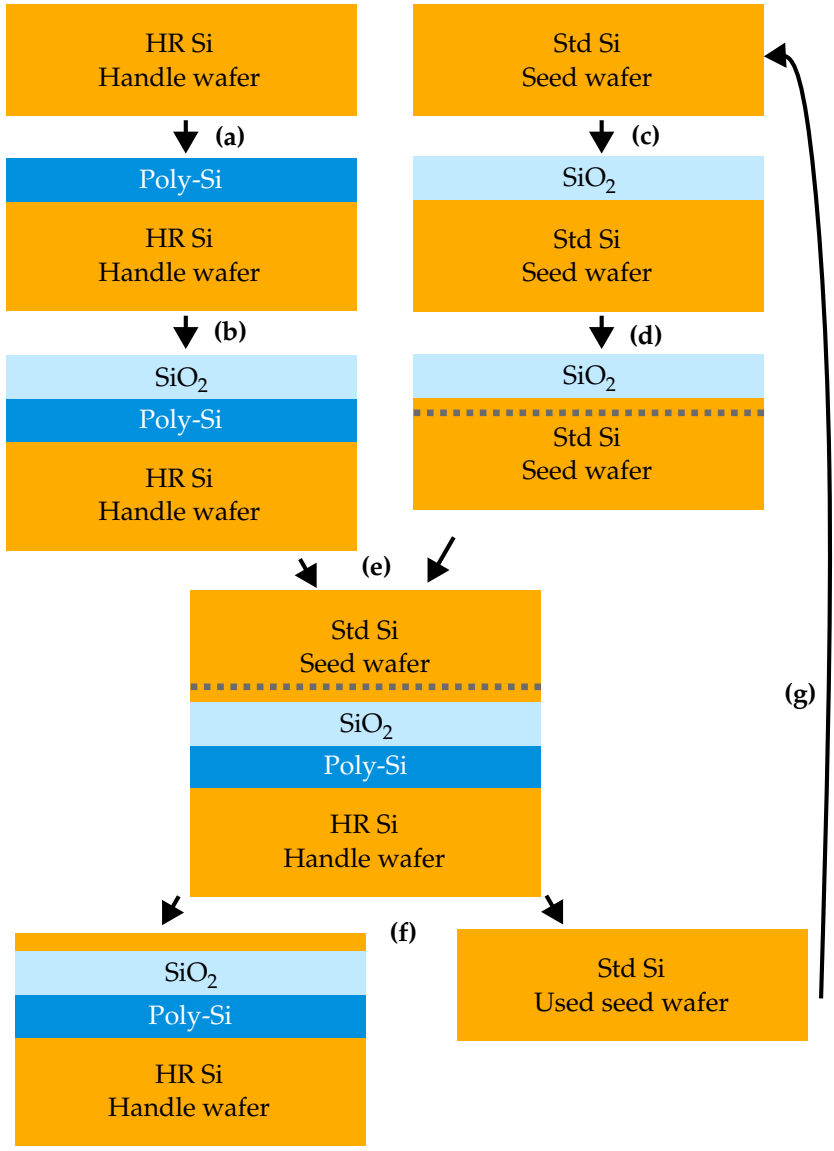


Fig. C.1 Process flow considered for the fabrication of a TR-SOI wafer.

is needed to strengthen the bond. A second CMP step allows a smooth surface of the Si film.

(g) The seed wafer is recycled. It is assumed that step **(g)** can be performed 50 times.

According to this flow, a virtual flow was defined in the imec.netzero platform (see below). When precise tools or recipes were not available, it was always possible to find a close approximation.

3.6 Electricity mix

The LCA methodology imposes the computation of the global warming potential (GWP) according to three different scopes.

Scope 1 emissionss correspond to the direct emissions of greenhouse gases during the fabrication of the RF substrates. These emissions occur directly at the fab. For instance, exhaust gases from the III-N epitaxy contribute to the scope 1 GWP.

Scope 2 emissions correspond to the emissions related to the use of electrical energy, which emits greenhouse gases at its production. These emissions take place at the electricity generation facility.

Scope 3 emissions are indirect emissions. This category takes into account e.g. the emissions linked to the extraction of raw materials, fabrication of the bulk wafer or transport of the materials.

For the cradle-to-gate LCA study performed in this thesis, scope 2 and 3 emissions are dominating over scope 1 because the different extraction and fabrication processes are highly energy-intensive. For this reason, the carbon intensity of the electricity used in the different fabrication steps is a particularly important parameter and significantly impacts the GWP results. As an example, the electricy mix in France or Belgium is less carbon-intensive than in China because of the widespread use of nuclear energy. The different substrates in this study can be produced in several different places in the world, which is why the global electricity mix is considered, with a carbon intensity of 708 $gCO_{2,eq}/kWh$.

3.7 imec.netzero platform

The life cycle analysis (LCA) was performed with imec's in-house LCA tool called imec.netzero. It functions as a virtual fab, containing a wide variety

of semiconductor fabrication tools, process steps and materials. The tool databases comprises the electrical consumption of the tools, their capacity and their emission (i.e. exhaust gases). A process step is characterized by a processing time and the use of a certain amount of materials (i.e. precursors), the embodied impacts of which are also taken into account.

A process flow consisting of several successive process steps can then be defined. A model of the fab is finally also included, which comprises the abatement and yield, among other things. The overall impact of a given product (in this case, a cm^2 of semiconductor substrate) can then be computed.

Bibliography

[1] R. L. Coffie, "High power high frequency transistors: A material's perspective," in *High-Frequency GaN Electronic Devices*, P. Fay, D. Jena, and P. Maki, Eds., Cham: Springer International Publishing, 2020, pp. 5–41.

[2] L. Cao, H. Ye, J. Wang, H. Marchand, W. Johnson, and P. Fay, "RF harmonic distortion of coplanar waveguides on GaN-on-Si and GaN-on-SiC substrates," in *CS MANTECH*, Virtual, 2020.

[3] H. Wang, T.-Y. Huang, N. Sasikanth Mannem, J. Lee, E. Garay, D. Munzer, E. Liu, Y. Liu, B. Lin, M. Eleraky, H. Jalili, J. Park, S. Li, F. Wang, A. S. Ahmed, C. Snyder, S. Lee, H. T. Nguyen, and M. E. D. Smith. "Power amplifiers performance survey 2000-present." (), [Online]. Available: https://ideas.ethz.ch/Surveys/pa-survey.html.

[4] J. Raskin, A. Viviani, D. Flandre, and J. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Transactions on Electron Devices*, vol. 44, no. 12, pp. 2252–2261, Dec. 1997.

[5] A. Reyes, S. El-Ghazaly, S. Dorn, M. Dydyk, D. Schroder, and H. Patterson, "Coplanar waveguides and microwave inductors on silicon substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 9, pp. 2016–2022, Sep. 1995.

[6] Y. Wu, S. Gamble, B. Armstrong, V. Fusco, and J. Stewart, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 1, pp. 10–12, Jan. 1999.

[7] Lederer, D., Desrumeaux, C., Brunier, F., and Raskin, J.-P., "High resistivity SOI substrates: How high should we go?" In *2003 IEEE International Conference on SOI*, Oct. 2003, pp. 50–51.

[8] H. Gamble, B. Armstrong, S. Mitchell, Y. Wu, V. Fusco, and J. Stewart, "Low-loss CPW lines on surface stabilized high-resistivity silicon," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 10, pp. 395–397, Oct. 1999.

[9] D. Lederer and J. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 805–807, Nov. 2005.

[10] S. Laurent and E. Desbonnets, *Rf substrate technologies for mobile communications (soitec white paper)*, 2011.

[11] L. Liu and J. H. Edgar, "Substrates for gallium nitride epitaxy," *Materials Science and Engineering: R: Reports*, vol. 37, no. 3, pp. 61–127, Apr. 30, 2002.

[12] Y.-F. Wu, B. Keller, S. Keller, D. Kapolnek, S. Denbaars, and U. Mishra, "Measured microwave power performance of AlGaN/GaN MODFET," *IEEE Electron Device Letters*, vol. 17, no. 9, pp. 455–457, Sep. 1996.

[13] L. T. Hieu, H.-T. Hsu, D. Panda, C.-T. Lee, C.-H. Lin, and E. Y. Chang, "Improved off-state leakage current and cutoff frequency for AlGaN/GaN HEMT by using silicon-on-insulator," *ECS Journal of Solid State Science and Technology*, vol. 12, no. 2, p. 025 001, Feb. 2023, Publisher: IOP Publishing.

[14] L. T. Hieu, C.-H. Chiang, D. Anandan, C.-F. Dee, A. A. Hamzah, C.-T. Lee, C.-H. Lin, and E. Y. Chang, "Improvements of electrical and thermal characteristics for AlGaN/GaN HEMT grown by metal-organic chemical vapor deposition on silicon-on-insulator (SOI) substrate," *Semiconductor Science and Technology*, vol. 37, no. 7, p. 075 012, Jun. 2022, Publisher: IOP Publishing.

[15] A. Magnani, T. Cosnier, N. Amirifar, U. Chatterjee, M. Zhao, X. Li, K. Geens, and S. Decoutere, "Thermal characterization of GaN lateral power HEMTs on Si, SOI, and poly-AlN substrates," *Microelectronics Reliability*, vol. 118, p. 114 061, Mar. 1, 2021.

[16] J.-S. Moon, B. Grabar, J. Wong, C. Dao, E. Arkun, H. Tai, D. Fanning, N. C. Miller, M. Elliott, R. Gilbert, N. Venkatesan, and P. Fay, "W-band graded-channel GaN HEMTs with record 45% power-added-efficiency at 94 GHz," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 2, pp. 161–164, Feb. 2023.

[17] B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, "Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave n-polar GaN MISHEMTs," *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 45–50, Jan. 2018.

[18] D. Nirmal and J. Ajayan, Eds., *Handbook for III-V High Electron Mobility Transistor Technologies*, Boca Raton: CRC Press, May 31, 2019, 442 pp.

[19] Z. Zhang, Z. Liu, and H. Fang, "Influences of growth parameters on the reaction pathway during GaN synthesis," *Journal of Crystal Growth*, vol. 482, pp. 44–55, Jan. 15, 2018.

[20] M. Zhao and W. Guo, "Formation of a III-N semiconductor structure," U.S. Patent 10818491B2, Oct. 27, 2020.

[21] M. Zhao, "Method for forming a semiconductor structure for a gallium nitride channel device," European pat. 3486939A1, May 22, 2019.

[22] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 87, no. 1, pp. 334–344, Dec. 15, 1999.

[23] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. 77, no. 2, pp. 250–252, Jun. 30, 2000.

[24] H. W. Then, L. A. Chow, S. Dasgupta, S. Gardner, M. Radosavljevic, V. R. Rao, S. H. Sung, G. Yang, and P. Fischer, "High-k gate dielectric depletion-mode and enhancement-mode GaN MOS-HEMTs for improved OFF-state leakage and DIBL for power electronics and RF applications," in *2015 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2015, pp. 16.3.1–16.3.4.

[25] M. Micovic, D. F. Brown, D. Regan, J. Wong, Y. Tang, F. Herrault, D. Santos, S. D. Burnham, J. Tai, E. Prophet, I. Khalaf, C. McGuire, H. Bracamontes, H. Fung, A. K. Kurdoghlian, and A. Schmitz, "High frequency GaN HEMTs for RF MMIC applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2016, pp. 3.3.1–3.3.4.

[26] S. Yadav, A. Alian, R. ElKashlan, B. J. O'Sullivan, A. Khaled, B. Kazemi, U. Peralagu, S. Banerjee, B. Parvais, and N. Collaert, "High performance mm wave AlN/GaN MISHEMTs on 200 mm Si substrate," in *2023 International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2023, pp. 1–4.

[27] E. Morvan, Y. Gobil, F. Morisot, J. Biscarat, M. Charles, J. Lugo, A. Divay, M. Medbouhi, I. Charlet, J. Delprato, P. Scheiblin, B. Rrustemi, A. Giry, A. Serhan, S. Ruel, P. Pimenta-Barros, F. Laulagnet, S. Minoret, A. Anotta, T. Billon, and B. Duriez, "6.6W/mm 200mm CMOS compatible AlN/GaN/Si MIS-HEMT with in-situ SiN gate dielectric and low temperature ohmic contacts," in *2023 International Electron Devices Meeting (IEDM)*, Dec. 2023, pp. 1–4.

[28] H. W. Then, M. Radosavljevic, Q. Yu, A. Latorre-Rey, H. Vora, S. Bader, I. Momson, D. Thomson, M. Beumer, P. Koirala, J. Peck, A. Oni, T. Hoff, R. Jordan, T. Michaelos, N. Nair, P. Nordeen, A. Vyatskikh, I. Ban, A. Zubair, S. Rami, and P. Fischer, "Enhancement-mode 300-mm GaN-on-Si(111) with integrated Si CMOS for future mm-wave RF applications," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 6, pp. 835–838, Jun. 2023, Conference Name: IEEE Microwave and Wireless Technology Letters.

[29] A. Ghorbel, P. Chiu, E. Dogmus, C. Malaquin, C. Buey, and C. Troadec, "Accelerated adoption of GaN RF in telecom infrastructure as opportunities for GaN-on-Si," in *CS MANTECH*, Orlando, FL, 2023.

[30] B. Debaillie, F. Brunier, D. Morche, E. N. Isa, and J. Craninckx, Eds., *Technologies Enabling Future Mobile Connectivity & Sensing*, New York: River Publishers, Jan. 9, 2024, 194 pp.

[31] Q. Yu, A. A. Farid, I. Momson, J. Garrett, H. Vora, S. Bader, A. Zubair, P. Koirala, M. Beumer, A. Vyatskikh, P. Nordeen, T. Hoff, M. Radosavljevic, S. Rami, F. O'Mahony, and H. W. Then, "Advancements in 300 mm GaN-on-Si technology with industry's first circuit demon-

stration of monolithically integrated GaN and Si transistors," *IEEE Microwave and Wireless Technology Letters*, 2024, Early access.

[32] A. Inoue, "Millimeter-wave GaN devices for 5g: Massive MIMO antenna arrays for sub-6-GHz and mm-wave bandwidth," *IEEE Microwave Magazine*, vol. 22, no. 5, pp. 100–110, May 2021, Conference Name: IEEE Microwave Magazine.

[33] M. Rack, L. Nyssens, Q. Courte, D. Lederer, and J.-P. Raskin, "Impact of device shunt loss on DC-80 GHz SPDT in 22 nm FD-SOI," in *ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC)*, Sep. 2021, pp. 195–198.

[34] M. Rack, L. Nyssens, and J.-P. Raskin, "Silicon-substrate enhancement technique enabling high quality integrated RF passives," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA: IEEE, Jun. 2019, pp. 1295–1298.

[35] S. Marsh, *Practical MMIC design*. Artech, 2006.

[36] D. M. Pozar, *Microwave Engineering*. Wiley, Apr. 13, 2012, 756 pp.

[37] D. Lederer and J.-P. Raskin, "Effective resistivity of fully-processed SOI substrates," *Solid-State Electronics*, vol. 49, no. 3, pp. 491–496, Mar. 2005.

[38] L. Nyssens, M. Rack, and J.-P. Raskin, "Effective resistivity extraction of low-loss silicon substrates at millimeter-wave frequencies," *International Journal of Microwave and Wireless Technologies*, vol. 12, no. 7, pp. 615–628, Sep. 2020, Publisher: Cambridge University Press.

[39] W. Heinrich, "Quasi-TEM description of MMIC coplanar lines including conductor-loss effects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 1, pp. 45–52, Jan. 1993.

[40] S. Yadav, **P. Cardinael**, M. Zhao, K. Vondkar, A. Khaled, R. Rodriguez, B. Vermeersch, S. Makovejev, E. Ekoga, A. Pottrain, N. Waldron, J.-P. Raskin, B. Parvais, and N. Collaert, "Substrate RF losses and non-linearities in GaN-on-Si HEMT technology," in *2020 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2020, pp. 8.2.1–8.2.4.

[41] "1. RF technology roadmap for 5g and 6g RF front end systems," in *Technologies Enabling Future Mobile Connectivity and Sensing*, River Publishers, 2023, pp. 1–10.

[42] C. Roda Neve, "Small- and large-signal characterization of trap-rich HR-Si/HR-SOI wafers for SoC applications," Ph.D. dissertation, UCL - Université Catholique de Louvain, 2012.

[43] D. Marti, M. Vetter, A. R. Alt, H. Benedickter, and C. R. Bolognesi, "110 GHz characterization of coplanar waveguides on GaN-on-Si substrates," *Applied Physics Express*, vol. 3, no. 12, p. 124 101, Dec. 3, 2010.

[44] T. T. Luong, F. Lumbantoruan, Y.-Y. Chen, Y.-T. Ho, Y.-C. Weng, Y.-C. Lin, S. Chang, and E.-Y. Chang, "RF loss mechanisms in GaN-based high-electron-mobility-transistor on silicon: Role of an inversion channel at the AlN/Si interface," *physica status solidi (a)*, vol. 214, no. 7, p. 1 600 944, 2017.

[45] Z. Liu, W. Xing, G. I. Ng, and E. A. Fitzgerald, "RF and power GaN HEMTs on 200 mm-diameter 725 um-thick p-Si substrates," in *2019 Electron Devices Technology and Manufacturing Conference (EDTM)*, Mar. 2019, pp. 100–102.

[46] U. Gösele, E. Schroer, P. Werner, and T. Y. Tan, "Low-temperature diffusion and agglomeration of oxygen in silicon," in *Early Stages of Oxygen Precipitation in Silicon*, R. Jones, Ed., Dordrecht: Springer Netherlands, 1996, pp. 243–261.

[47] C. A. Londos, M. J. Binns, A. R. Brown, S. A. McQuaid, and R. C. Newman, "Effect of oxygen concentration on the kinetics of thermal donor formation in silicon at temperatures between 350 and 500 °c," *Applied Physics Letters*, vol. 62, no. 13, pp. 1525–1526, Mar. 29, 1993.

[48] J. Paloheimo, "Chapter 3 - properties of silicon crystals," in *Handbook of Silicon Based MEMS Materials and Technologies (Second Edition)*, ser. Micro and Nano Technologies, M. Tilli, T. Motooka, V.-M. Airaksinen, S. Franssila, M. Paulasto-Kröckel, and V. Lindroos, Eds., Boston: William Andrew Publishing, Jan. 1, 2015, pp. 56–85.

[49] C. Mauder, H. Hahn, M. Marx, Z. Gao, R. Oligschlaeger, T. Zweipfennig, A. Noculak, R. Negra, H. Kalisch, A. Vescan, and M. Heuken, "Investigation and reduction of RF loss induced by al diffusion at the AlN/Si(111) interface in GaN-based HEMT buffer stacks," *Semiconductor Science and Technology*, vol. 36, no. 7, p. 075 008, Jun. 2021.

[50] H. Yu, U. Peralagu, A. Alian, M. Zhao, B. Parvais, and N. Collaert, "Parasitic side channel formation due to ion implantation isolation of GaN HEMT," *MRS Advances*, Dec. 12, 2022.

[51] H. Yu, V. Putcha, U. Peralagu, M. Zhao, S. Yadav, A. Alian, B. Parvais, and N. Collaert, "Leakage mechanism in ion implantation isolated AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 131, no. 3, p. 035 701, Jan. 18, 2022.

[52] "James ziegler - SRIM & TRIM." (), [Online]. Available: http://www.srim.org/index.htm.

[53] U. Peralagu, A. Alian, V. Putcha, A. Khaled, R. Rodriguez, A. Sibaja-Hernandez, S. Chang, E. Simoen, S. E. Zhao, B. De Jaeger, D. M. Fleetwood, P. Wambacq, M. Zhao, B. Parvais, N. Waldron, and N. Collaert, "CMOS-compatible GaN-based devices on 200mm-Si for RF applications: Integration and performance," in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, pp. 17.2.1–17.2.4.

[54] C. Roda Neve and J.-P. Raskin, "RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 924–932, Apr. 2012.

[55] B. Kazemi Esfeh, M. Rack, K. Ben Ali, F. Allibert, and J.-P. Raskin, "RF small- and large-signal characteristics of CPW and TFMS lines on trap-rich HR-SOI substrates," *IEEE Transactions on Electron Devices*, vol. 65, no. 8, pp. 3120–3126, Aug. 2018.

[56] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[57] *Atlas User's Manual*. Santa Clara, CA: Silvaco, Inc., Aug. 26, 2016.

[58] J. Carrete, B. Vermeersch, A. Katre, A. van Roekeghem, T. Wang, G. K. H. Madsen, and N. Mingo, "almaBTE : A solver of the space–time dependent boltzmann transport equation for phonons in structured materials," *Computer Physics Communications*, vol. 220, pp. 351–362, Nov. 1, 2017.

[59] B. Vermeersch, R. Rodriguez, A. Sibaja-Hernandez, A. Vais, S. Yadav, B. Parvais, and N. Collaert, "Thermal modelling of GaN & InP RF devices with intrinsic account for nanoscale transport effects," in *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA: IEEE, Dec. 3, 2022, pp. 15.3.1–15.3.4.

[60] H. Ishikawa, G. Y. Zhao, N. Nakada, T. Egawa, T. Soga, T. Jimbo, and M. Umeno, "High-quality GaN on Si substrate using AlGaN/AlN intermediate layer," *physica status solidi (a)*, vol. 176, no. 1, pp. 599–603, 1999.

[61] H. Ishikawa, K. Yamamoto, T. Egawa, T. Soga, T. Jimbo, and M. Umeno, "Thermal stability of GaN on (1 1 1) Si substrate," *Journal of Crystal Growth*, vol. 189-190, pp. 178–182, Jun. 15, 1998.

[62] L. Pan, X. Dong, Z. Li, W. Luo, and J. Ni, "Influence of the AlN nucleation layer on the properties of AlGaN/GaN heterostructure on Si (111) substrates," *Applied Surface Science*, vol. 447, pp. 512–517, Jul. 31, 2018.

[63] T. Novák, P. Kostelník, M. Konečný, J. Čechal, M. Kolíbal, and T. Šikola, "Temperature effect on al predose and AlN nucleation affecting the buffer layer performance for the GaN-on-Si based high-voltage devices," *Japanese Journal of Applied Physics*, vol. 58, SC1018, SC May 2019.

[64] Y. Cordier, R. Comyn, E. Frayssinet, M. Khoury, M. Lesecq, N. Defrance, and J.-C. D. Jaeger, "Influence of AlN growth temperature on the electrical properties of buffer layers for GaN HEMTs on silicon," *physica status solidi (a)*, vol. 215, no. 9, p. 1 700 637, 2018.

[65] J. J. Freedsman, A. Watanabe, Y. Yamaoka, T. Kubo, and T. Egawa, "Influence of AlN nucleation layer on vertical breakdown characteristics for GaN-on-Si," *physica status solidi (a)*, vol. 213, no. 2, pp. 424–428, 2016.

[66] F. Lumbantoruan, Y.-Y. Wong, Y.-H. Wu, W.-C. Huang, N. M. Shrestra, T. T. Luong, T. B. Tinh, and E. Y. Chang, "Investigation of TMAl preflow to the properties of AlN and GaN film grown on Si(111) by MOCVD," in *2014 IEEE International Conference on Semiconductor Electronics (ICSE2014)*, Aug. 2014, pp. 20–23.

[67] H. Yacoub, D. Fahle, M. Finken, H. Hahn, C. Blumberg, W. Prost, H. Kalisch, M. Heuken, and A. Vescan, "The effect of the inversion channel at the AlN/Si interface on the vertical breakdown characteristics of GaN-based devices," *Semiconductor Science and Technology*, vol. 29, no. 11, p. 115 012, Nov. 1, 2014.

[68] X. Li, M. Van Hove, M. Zhao, B. Bakeroot, S. You, G. Groeseneken, and S. Decoutere, "Investigation on carrier transport through AlN nucleation layer from differently doped Si(111) substrates," *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 1721–1727, May 2018.

[69] S. Chang, M. Zhao, V. Spampinato, A. Franquet, T.-H. Do, A. Uedono, T. T. Luong, T.-H. Wang, and L. Chang, "The influence of AlN nucleation layer on radio frequency transmission loss of AlN-on-Si heterostructure," *physica status solidi (a)*, vol. 217, no. 7, p. 1 900 755, 2020.

[70] H. Chandrasekar, K. N. Bhat, M. Rangarajan, S. Raghavan, and N. Bhat, "Thickness dependent parasitic channel formation at AlN/Si interfaces," *Scientific Reports*, vol. 7, no. 1, p. 15 749, Nov. 16, 2017.

[71] Y. Zhang, S. Liu, J. Ma, Y. Yao, B. Wang, S. Xu, B. Hou, Z. Liu, J. Zhang, and Y. Hao, "More than 60% RF loss reduction and improved crystal quality of GaN-on-Si achieved by in-situ doping tert-butylphosphorus," *Journal of Crystal Growth*, vol. 625, p. 127 443, Jan. 1, 2024.

[72] P. Lin, J. Liu, H. Lin, Z. Chuang, W. Hsu, Y. Chen, P. Liu, and R. Horng, "Suppression of p-type parasitic channel formation at the interface between the aluminum nitride nucleation layer and the high-resistivity silicon substrate," *Surfaces and Interfaces*, vol. 36, p. 102 590, Feb. 1, 2023.

[73] L. Wei, X. Yang, J. Shen, D. Liu, Z. Cai, C. Ma, X. He, J. Tang, S. Qi, F. Xu, X. Wang, W. Ge, and B. Shen, "Al diffusion at AlN/Si interface and its suppression through substrate nitridation," *Applied Physics Letters*, vol. 116, no. 23, p. 232 105, Jun. 9, 2020.

[74] C. Ma, X. Yang, J. Shen, D. Liu, Z. Cai, Z. Chen, J. Tang, L. Sang, F. Xu, X. Wang, W. Ge, and B. Shen, "Low RF loss and low dislocation density of GaN grown on high-resistivity Si substrates," *Applied Physics Express*, vol. 15, no. 3, p. 031 003, Feb. 2022.

[75] Z. Cai, X. Yang, Z. Shen, C. Ma, Z. Chen, D. Liu, F. Xu, N. Tang, X. Wang, W. Ge, and B. Shen, "RF loss reduction by a carbon-regulated Si substrate engineering in GaN-based HEMT buffer stacks," *Applied Physics Letters*, vol. 123, no. 4, p. 042 102, Jul. 24, 2023.

[76] S. Chang, M. Zhao, V. Spampinato, A. Franquet, and L. Chang, "The influence of AlN nucleation layer on RF transmission loss of GaN buffer on high resistivity Si (111) substrate," *Semiconductor Science and Technology*, vol. 35, no. 3, p. 035 029, Feb. 2020.

[77] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. John Wiley & Sons, Nov. 21, 2002, 928 pp., Google-Books-ID: 4PZiQgAACAAJ.

[78] D. K. Schroder, *Semiconductor Material and Device Characterization*. John Wiley & Sons, Inc., 2006.

[79] I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual work function metal gate CMOS technology using metal interdiffusion," *IEEE Electron Device Letters*, vol. 22, no. 9, pp. 444–446, Sep. 2001.

[80] X. Zhang, D. Walker, A. Saxler, P. Kung, J. Xu, and M. Razeghi, "Demonstration of an electronic grade ti/AlN/Si metal-insulator-semiconductor capacitor," presented at the The Japan Society of Applied Physics, 1996.

[81] L. M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electronics*, vol. 5, no. 5, pp. 285–299, Sep. 1, 1962.

[82] E. M. Vogel and G. A. Brown, "Challenges of electrical measurements of advanced gate dielectrics in metal-oxide-semiconductor devices," *AIP Conference Proceedings*, vol. 683, no. 1, pp. 771–781, Sep. 30, 2003.

[83] S. Ghosh, A. Hinz, S. M. Fairclough, B. F. Spiridon, A. Eblabla, M. A. Casbon, M. J. Kappers, K. Elgaid, S. Alam, R. A. Oliver, and D. J. Wallis, "Origin(s) of anomalous substrate conduction in MOVPE-grown GaN HEMTs on highly resistive silicon," *ACS Applied Electronic Materials*, vol. 3, no. 2, pp. 813–824, Feb. 23, 2021.

[84] H. Hahn, C. Mauder, M. Marx, Z. Gao, P. Lauffer, O. Schön, P. T. John, S. Yadav, S. Banerjee, **P. Cardinael**, J. .-. Raskin, B. Parvais, and D. Fahle, presented at the CS Mantech, Tucson, AZ, May 2024.

[85] M. Rack, L. Nyssens, J. .-. Raskin, D. Lederer, A. Paganini, M. B. Shinde, and A. Beganovic, "Device layout dimension impact on substrate effective resistivity," in *2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Burlingame, CA, USA: IEEE, Oct. 2018, pp. 1–2.

[86] P. P. Maiti, A. Dash, S. Guhathakurata, S. Das, A. BAG, T. P. Dash, G. Ahmad, C. K. MAITI, and S. Mallik, "Experimental and simulation study of charge transport mechanism in HfTiOx high-k gate dielectric on SiGe heterolayers," *Bulletin of Materials Science*, vol. 45, no. 1, p. 39, Feb. 20, 2022.

[87] M. Placidi, A. Pérez-Tomás, J. C. Moreno, E. Frayssinet, F. Semond, A. Constant, P. Godignon, N. Mestres, A. Crespi, and J. Millán, "Interfacial properties of AlN and oxidized AlN on Si," *Surface Science*, vol. 604, no. 1, pp. 63–67, Jan. 1, 2010.

[88] V. W. L. Chin, T. L. Tansley, and T. Osotchan, "Electron mobilities in gallium, indium, and aluminum nitrides," *Journal of Applied Physics*, vol. 75, no. 11, pp. 7365–7372, Jun. 1, 1994.

[89] C. Berglund, "Surface states at steam-grown silicon-silicon dioxide interfaces," *IEEE Transactions on Electron Devices*, vol. ED-13, no. 10, pp. 701–705, Oct. 1966, Conference Name: IEEE Transactions on Electron Devices.

[90] M. Rack, "Modelling of advanced silicon-based substrates for RF and mm-wave applications," Ph.D. dissertation, UCL - Université Catholique de Louvain, 2021.

[91] S. Raghavan and J. Redwing, "Growth stresses and cracking in GaN films on (111) Si grown by metalorganic chemical vapor deposition. II. graded AlGaN buffer layers," *Journal of Applied Physics*, vol. 98, no. 2, p. 023 515, Jul. 22, 2005.

[92] E. Feltin, B. Beaumont, M. Laügt, P. de Mierry, P. Vennéguès, H. Lahrèche, M. Leroux, and P. Gibart, "Stress control in GaN grown on silicon (111) by metalorganic vapor phase epitaxy," *Applied Physics Letters*, vol. 79, no. 20, pp. 3230–3232, Nov. 12, 2001.

[93] S. L. Selvaraj, A. Watanabe, A. Wakejima, and T. Egawa, "1.4-kV breakdown voltage for AlGaN/GaN high-electron-mobility transistors on silicon substrate," *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1375–1377, Oct. 2012.

[94] Y. Sun, K. Zhou, Q. Sun, J. Liu, M. Feng, Z. Li, Y. Zhou, L. Zhang, D. Li, S. Zhang, M. Ikeda, S. Liu, and H. Yang, "Room-temperature continuous-wave electrically injected InGaN-based laser directly grown on Si," *Nature Photonics*, vol. 10, no. 9, pp. 595–599, Sep. 2016.

[95] S. Kato, Y. Satoh, H. Sasaki, I. Masayuki, and S. Yoshida, "C-doped GaN buffer layers with high breakdown voltages for high-power operation AlGaN/GaN HFETs on 4-in Si substrates by MOVPE," *Journal of Crystal Growth*, Thirteenth International Conference on Metal Organic Vapor Phase Epitaxy (ICMOVPE XIII), vol. 298, pp. 831–834, Jan. 1, 2007.

[96] R. ElKashlan, H. Yu, A. Khaled, S. Yadav, U. Peralagu, A. Alian, N. Collaert, P. Wambacq, and B. Parvais, "A composite AlGaN/cGaN back barrier for mm-wave GaN-on-Si HEMTs," in *ESSDERC 2023 - IEEE 53rd European Solid-State Device Research Conference (ESSDERC)*, ISSN: 2378-6558, Sep. 2023, pp. 152–155.

[97] M. J. Uren, M. Silvestri, M. Cäsar, G. A. M. Hurkx, J. A. Croon, J. Šonský, and M. Kuball, "Intentionally carbon-doped AlGaN/GaN HEMTs: Necessity for vertical leakage paths," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 327–329, Mar. 2014.

[98] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee, and M. Kuball, ""leaky dielectric" model for the suppression of dynamic RON in carbon-doped AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2826–2834, Jul. 2017.

[99] N. Zagni, A. Chini, F. M. Puglisi, M. Meneghini, G. Meneghesso, E. Zanoni, P. Pavan, and G. Verzellesi, ""hole redistribution" model explaining the thermally activated RON stress/recovery transients in carbon-doped AlGaN/GaN power MIS-HEMTs," *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 697–703, Feb. 2021, Conference Name: IEEE Transactions on Electron Devices.

[100] M. Rack, F. Allibert, and J.-P. Raskin, "Modeling of semiconductor substrates for RF applications: Part II—parameter impact on harmonic distortion," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4606–4613, Sep. 2021.

[101] S. Rathkanthiwar, A. Kalra, N. Remesh, A. Bardhan, R. Muralidharan, D. N. Nath, and S. Raghavan, "Impact of pits formed in the AlN nucleation layer on buffer leakage in GaN/AlGaN high electron mobility transistor structures on Si (111)," *Journal of Applied Physics*, vol. 127, no. 21, p. 215 705, Jun. 4, 2020.

[102] **P. Cardinael**, S. Yadav, M. Zhao, M. Rack, D. Lederer, N. Collaert, B. Parvais, and J.-P. Raskin, "Impact of III-N buffer layers on RF losses and harmonic distortion of GaN-on-Si substrates," in *ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC)*, Grenoble, France: IEEE, Sep. 13, 2021, pp. 303–306.

[103] A. Y. Polyakov, S. J. Pearton, P. Frenzer, F. Ren, L. Liu, and J. Kim, "Radiation effects in GaN materials and devices," *Journal of Materials Chemistry C*, vol. 1, no. 5, pp. 877–887, Jan. 4, 2013.

[104] C. Koller, G. Pobegen, C. Ostermaier, and D. Pogany, "Effect of carbon doping on charging/discharging dynamics and leakage behavior of carbon-doped GaN," *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5314–5321, Dec. 2018.

[105] V. Putcha, H. Yu, J. Franco, S. Yadav, A. Alian, U. Peralagu, B. Parvais, and N. Collaert, "Interpretation and modelling of dynamic-RON kinetics in GaN-on-Si HEMTs for mm-wave applications," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, 11B.2–1–11B.2–8.

[106] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Brückner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in GaN HEMTs-part i: Advantages and limitations of drain current transient measurements," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013.

[107] A. Nardo, C. De Santi, C. Koller, C. Ostermaier, I. Daumiller, G. Meneghesso, E. Zanoni, and M. Meneghini, "Positive and negative charge trapping GaN HEMTs: Interplay between thermal emission and transport-limited processes," *Microelectronics Reliability*, Proceedings of ESREF 2021, 32nd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, vol. 126, p. 114 255, Nov. 1, 2021.

[108] H. Yu, J. Fang, B. Vermeersch, U. Peralagu, H. Han, O. Richard, A. Alian, N. De Almeida Braga, B. Kazemi Esfeh, S. Banerjee, E. Bury, B. Parvais, and N. Collaert, "Charge movement in back barrier induced time-dependent on-state breakdown of GaN HEMT," in *2023 International Electron Devices Meeting (IEDM)*, Dec. 2023.

[109] N. Zagni, M. Cioni, F. Iucolano, M. Moschetti, G. Verzellesi, and A. Chini, "Experimental and numerical investigation of poole–frenkel effect on dynamic RON transients in C-doped p-GaN HEMTs," *Semiconductor Science and Technology*, vol. 37, no. 2, p. 025 006, Dec. 2021, Publisher: IOP Publishing.

[110] V. Moroz, H. Y. Wong, M. Choi, N. Braga, R. V. Mickevicius, Y. Zhang, and T. Palacios, "The impact of defects on GaN device behavior: Modeling dislocations, traps, and pits," *ECS Journal of Solid State Science and Technology*, vol. 5, no. 4, P3142, Jan. 22, 2016, Publisher: IOP Publishing.

[111] S. Dalcanale, M. J. Uren, and M. Kuball, "TCAD simulation of leakage through threading dislocations in GaN-based pn-diodes," *Silvaco Simulation Standard*, pp. 7–8, Jul. 2018.

[112] **P. Cardinael**, S. Yadav, M. Zhao, M. Rack, D. Lederer, N. Collaert, B. Parvais, and J.-P. Raskin, "Time dependence of RF losses in GaN-on-Si substrates," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 688–691, Jun. 2022.

[113] B. Kazemi Esfeh, M. Rack, S. Makovejev, F. Allibert, and J.-P. Raskin, "A SPDT RF switch small- and large-signal characteristics on TR-HR SOI substrates," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 543–550, 2018.

[114] **P. Cardinael**, S. Yadav, M. Rack, U. Peralagu, A. Alian, B. Parvais, N. Collaert, and J.-P. Raskin, "Contribution of substrate harmonic distortion to GaN-on-Si RF switches linearity," *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 3, pp. 298–301, Mar. 2024.

[115] H. W. Then, C. Y. Huang, B. Krist, K. Jun, K. Lin, N. Nidhi, T. Michaelos, B. Mueller, R. Paul, J. Peck, W. Rachmady, S. Dasgupta, D. Staines, T. Talukdar, N. Thomas, T. Tronic, P. Fischer, W. Hafez, M. Radosavljevic, P. Agababov, I. Ban, R. Bristol, M. Chandhok, S. Chouksey, and B. Holybee, "3d heterogeneous integration of high performance high-k metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5g and beyond) and SoC applications," in *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA: IEEE, Dec. 2019, pp. 17.3.1–17.3.4.

[116] L. Zhu, S. Liu, F. Allibert, I. Radu, X. Zhu, Y. Lu, and X. Wang, "RF characteristics of two generations of RFeSI HR-SOI substrates over temperature," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 5, pp. 377–379, May 2018.

[117] M. Rack, F. Allibert, and J.-P. Raskin, "Modeling of semiconductor substrates for RF applications: Part i—static and dynamic physics of carriers and traps," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4598–4605, Sep. 2021.

[118] F. Drillet, J. Loraine, H. Saleh, I. Lahbib, B. Grandchamp, L. Iogna-Prat, I. Lahbib, O. Sow, and G. Uren, "RF SPST switch based on innovative heterogeneous GaN/SOI integration technique," in *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, Jan. 2021, pp. 117–120.

[119] S. Kaleem, J. Kuhn, R. Quay, and M. Hein, "A high-power Ka-band single-pole single-throw switch MMIC using 0.25 µm GaN on SiC," in *2015 IEEE Radio and Wireless Symposium (RWS)*, San Diego, CA, USA, Jan. 2015, pp. 132–134.

[120] T. Kim, H. Im, S.-H. Lee, K.-J. Kim, and C. Park, "Highly linear k-/Ka-band SPDT switch based on traveling-wave concept in a 150-nm GaN pHEMT process," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 8, pp. 987–990, Aug. 2022.

[121] K. Jena, R. Swain, and T. R. Lenka, "Effect of thin gate dielectrics on DC, radio frequency and linearity characteristics of lattice-matched AlInN/AlN/GaN metal–oxide–semiconductor high electron mobility transistor," *IET Circuits, Devices & Systems*, vol. 10, no. 5, pp. 423–432, 2016.

[122] D. C. Kerr, J. M. Gering, T. G. McKay, M. S. Carroll, C. Roda Neve, and J.-P. Raskin, "Identification of RF harmonic distortion on Si substrates and its reduction using a trap-rich layer," in *2008 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 2008, pp. 151–154.

[123] A. Tombak, M. S. Carroll, D. C. Kerr, J.-B. Pierres, and E. Spears, "Design of high-order switches for multimode applications on a silicon-on-insulator technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 10, pp. 3639–3649, Oct. 2013.

[124] P. D. Hurwitz, "RF switch branch having improved linearity," U.S. Patent 9190994B2, Nov. 17, 2015.

[125] C. Park, A. Edwards, P. Rajagopal, W. Johnson, S. Singhal, A. Hanson, Q. Martin, E. L. Piner, K. J. Linthicum, and I. C. Kizilyalli, "High-power and high-voltage AlGaN/GaN HEMTs-on-Si," in *2007 IEEE Compound Semiconductor Integrated Circuits Symposium*, ISSN: 2374-8443, Oct. 2007, pp. 1–4.

[126] L. Pattison, T. Boles, N. Tuffy, and G. Lopes, "Improving GaN on Si power amplifiers through reduction of parasitic conduction layer," in *2014 9th European Microwave Integrated Circuit Conference*, Oct. 2014, pp. 92–95.

[127] I. Takenaka, K. Ishikura, K. Asano, S. Takahashi, Y. Murase, Y. Ando, H. Takahashi, and C. Sasaoka, "High-efficiency and high-power microwave amplifier using GaN-on-Si FET with improved high-temperature operation characteristics," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 3, pp. 502–512, Mar. 2014.

[128] Y. Yamaguchi and T. Oishi, "Quasi-physical equivalent circuit model of RF leakage current in substrate including temperature dependence for GaN-HEMT on Si," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 5, pp. 1945–1956, May 2023.

[129] S. D. Kee, "The class E/F family of harmonic-tuned switching power amplifiers," Ph.D. dissertation, California Institute of Technology, 2002.

[130] S. Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition*. Artech House, 2006.

[131] S. Makovejev, J.-P. Raskin, M. K. Md Arshad, D. Flandre, S. Olsen, F. Andrieu, and V. Kilchytska, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs," *Solid-State Electronics*, Selected Papers from the ULIS 2011 Conference, vol. 71, pp. 93–100, May 1, 2012.

[132] H. Ito and K. Masuy, "A simple through-only de-embedding method for on-wafer s-parameter measurements up to 110 GHz," in *2008 IEEE MTT-S International Microwave Symposium Digest*, ISSN: 0149-645X, Jun. 2008, pp. 383–386.

[133] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line on Si-SiO_2 system," *IEEE Transactions on Microwave Theory and Techniques*, vol. 19, no. 11, pp. 869–881, Nov. 1971, Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[134] D. Bol, T. Pirson, and R. Dekimpe, "Moore's law and ICT innovation in the anthropocene," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, ISSN: 1558-1101, Feb. 2021, pp. 19–24.

[135] L.-P. P.-V. P. Clément, Q. E. S. Jacquemotte, and L. M. Hilty, "Sources of variation in life cycle assessments of smartphones and tablet computers," *Environmental Impact Assessment Review*, vol. 84, p. 106 416, Sep. 1, 2020.

[136] L. Van Oers and J. Guinée, "The abiotic depletion potential: Background, updates, and future," *Resources*, vol. 5, no. 1, p. 16, Mar. 2016.

[137] "Ecoinvent - data with purpose.," ecoinvent. (), [Online]. Available: https://ecoinvent.org/.

[138] B. L. Smith, "Development and life cycle assessment of advanced-concept III-V multijunction photovoltaics," Ph.D. dissertation, Rochester Institute of Technology, 2018.

[139] A. Diaz Triana, S. Schmidt, S. Glaser, and M. L. Makoschitz, "A "life cycle thinking" approach to assess differences in the energy use of SiC vs. Si power semiconductors," in *e-Nova 2021*, 2021.

[140] C. F. Blanco, S. Cucurachi, F. Dimroth, J. B. Guinée, W. J. G. M. Peijnenburg, and M. G. Vijver, "Environmental impacts of III–v/silicon photovoltaics: Life cycle assessment and guidance for sustainable manufacturing," *Energy & Environmental Science*, vol. 13, no. 11, 4280–4290, Nov. 12, 2020, Publisher: The Royal Society of Chemistry.

[141] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Boston, MA: Springer US, 2004.

[142] L. Boakes, M. Garcia Bardon, V. Schellekens, I.-Y. Liu, B. Vanhouche, G. Mirabelli, F. Sebaai, L. Van Winckel, E. Gallagher, C. Rolin, and L.-Å. Ragnarsson, "Cradle-to-gate life cycle assessment of CMOS logic technologies," in *2023 International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2023, pp. 1–4.

[143] M. Rack, L. Nyssens, and J. Raskin, "Low-loss Si-substrates enhanced using buried pn junctions for rf applications," *IEEE Electron Device Letters*, vol. 40, no. 5, pp. 690–693, May 2019.

[144] G. Scheen, R. Tuyaerts, **P. Cardinael**, E. Ekoga, K. Aouadi, C. Pavageau, A. Rassekh, M. Nabet, S. Yadav, J.-P. Raskin, B. Parvais, and M. Emam, "GaN-on-porous silicon for RF applications," in *2023 53rd European Microwave Conference (EuMC)*, Sep. 2023, pp. 842–845.

[145] M. Rack, Y. Belaroussi, K. Ben Ali, G. Scheen, B. Kazemi Esfeh, and J.-P. Raskin, "Small- and large-signal performance up to 175c of low-cost porous silicon substrate for RF applications," *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 1887–1895, May 2018.

[146] O. Mitrofanov and M. Manfra, "Poole-frenkel electron emission from the traps in AlGaN/GaN transistors," *Journal of Applied Physics*, vol. 95, no. 11, pp. 6414–6419, Jun. 1, 2004.

[147] H. Wang, P.-C. Hsu, M. Zhao, E. Simoen, A. Sibaja-Hernandez, and J. Wang, "Investigation of defect characteristics and carrier transport mechanisms in GaN layers with different carbon doping concentration," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4827–4833, Nov. 2020, Conference Name: IEEE Transactions on Electron Devices.