UNIVERSITÉ CATHOLIQUE DE LOUVAIN
LABORATOIRE D'HYPERFRÉQUENCES
Louvain-la-Neuve

Wideband characterization of advanced SOI material and MOS devices for high frequency applications

Dimitri Lederer

Jury

Prof. Luc Vandendorpe (Président)
Prof. J.-P. Raskin (promoteur)
Prof. D. Flandre
Prof. D. Vanhoenacker-Janvier
Prof. G. Dambrine
Prof. F. Danneville
Prof. J.-P. Colinge
Dr. B. Aspar

Thèse présentée en vue de l'obtention du grade de docteur en Sciences Appliquées

SEPTEMBER 2006

Remerciements

L'aboutissement de cette thèse de doctorat n'aurait pu être réalisé sans le support et l'aide d'un grand nombre de personnes, qui de près ou de loin, m'ont aidé et soutenu durant ces six années de recherche passées au laboratoire d'Hyperfréquences de l'UCL.

Mes sincères remerciements s'adressent en premier lieu aux membres du jury, à savoir les Professeurs Luc Vandendorpe, Danielle Vanhoenacker, Denis Flandre et Jean-Pierre Raskin de l'UCL, les Professeurs Francois Danneville et Gilles Dambrine de l'IEMN (Lille), le Professeur Jean-Pierre Colinge de UC Davis (Sacramento) ainsi que le Docteur Bernard Aspar de TraciT Technologies (Grenoble). Je les remercie vivement pour le temps consacré à la lecture de ce travail et les remarques qu'ils ont émises lors de la défense privée de cette thèse. Ces commentaires auront contribué à améliorer la qualité scientifique du texte final.

Parmi les membres du jury, je remercie en particulier le Professeur Jean-Pierre Raskin, promoteur de cette thèse, pour la manière dont il a encadré ces travaux. La profonde liberté de recherche et la grande disponibilité qu'il m'a accordées durant ces six années m'ont permis d'entièrement assouvir ma curiosité scientifique, tout en gardant un fil conducteur à cette thèse. Les nombreuses heures de discussion passées ensemble, et en particulier ses dissertations scientifiques emballantes et improvisées m'ont, chaque fois, enrichi. Sa franchise, son optimisme, son dynamisme et son humour n'ont fait qu'égayer davantage ces moments, tant dans son bureau que dans un couloir, un asenceur ou une chambre d'hôtel. Evoluer dans un tel environnement fut un régal pour l'esprit. Puissent d'autres avoir la chance d'en profiter.

Durant ces années passées à l'UCL, de nombreuses discussions scientifiques m'ont également été offertes par les Professeurs Denis Flandre, Isabelle Huynen, Danielle Vanhoenacker, Gilles Dambrine et Francois Danneville. Je les remercie vivement pour leur écoute, leur patience et l'intérêt qu'ils ont témoigné envers mes questions. A chaque occasion leurs réponses et leurs commentaires m'ont permis d'avancer et d'approfondir mes reflexions.

Dans ce même esprit, je remercie également Vincent Dessart et Pierre Delatte de Cissoid ainsi que Valeria Kilchytska du Laboratoire de Microélectronique pour leurs conseils avisés et les riches discussions scientifiques que nous avons partagées.

Parmi les techniciens qui ont activement participé à la réalisation de ce travail, je tiens à remercier tout particulièrement Pascal Simon, technicien du laboratoire

d'Hyperfréquences, pour sa disponibilité et son aide précieuse lors des campagnes de mesures effectuées durant ces années de recherche. C'est en traitant les innombrables fichiers de mesures alimentant le compte SOIDATA sur Musin que j'ai pu apprécier, à sa juste valeur, l'immense qualité de son travail. Son humilité et sa rigueur font de lui un technicien hors-pair. Il va sans dire que ce travail aurait été bien plus ardu sans son intervention et que 'un peu de lui' se trouve dans la quasi-totalité des résultats présentés ici.

Au laboratoire d'Hyperfréquences, j'aimerais remercier également Francois Hubin pour sa grande compétence informatique et la disponibilité dont il a témoigné à mon égard. La rapidité de ses interventions, toujours sans faille, lors de mes soucis informatiques m'ont procuré un gain de temps considérable. Je remercie aussi Robert Platteborze pour son aide matérielle, et notamment pour le prêt de son fer à souder qui fut solicité à maintes reprises afin de réparer les montures de mes lunettes.

Parmi les techniciens des salles blanches, je remercie tout particulièrement André Crahay et Christian Renaux pour leur écoute et la qualité de leurs conseils. Je remercie non moins chaleureusement David Spote et Nathanaël Mahieux pour la disponibilité, la compétence et la dévotion qu'ils ont manifestées à chaque fois qu'ils ont 'processé' des tranches pour moi. Je serais probablement toujours occupé à travailler en salles blanches sans leur aide précieuse.

Merci aussi aux nombreux étudiants qui, en venant me poser des questions à l'improviste dans mon bureau, ont fait de ces nombreuses heures de travail personnel un métier plus sociable et humain.

Merci également tous ceux qui ont assuré un support matériel, direct ou indirect, à ce travail. Ces remerciements s'adressent à Brigitte et Pascal pour leur disponibilité lors de mes ennuis informatiques sur PC ou stations UNIX, à Annette, Marie-Christine et Christel pour leur soutien logistique.

Merci aussi à tous ces potes doctorants émiciens, Ides, Bruno, Bertrand, Morin, Francois, Ming, Aimad, Mehdi, Judith, Majid, Llukasj, Vikram et Benoit, tous embarqués sur le même navire (si si, Benoit). Leur humour aura largement contribué à la bonne humeur et la bonne entente règnant au 'labo'. Merci en particulier à Ides, pour les innombrables discussions, dans le doute comme dans l'euphorie mutuelle, pour tous les 'capu' servis à même mon bureau et toutes les parties de tennis.

Merci aussi à mon entourage proche. A mes parents pour l'éducation, l'esprit critique et l'ouverture d'esprit qu'ils m'ont inculqués. A mes parents, mes beaux-parents, frère et soeur, beaux-frères et belles soeurs, eux qui ont suivi l'évolution de ce travail et l'ont appuyé jusqu'à son terme.

Enfin, j'adresse ma plus profonde reconnaissance à Anne-Catherine, elle qui n'a jamais réellement compris l'objet de ces recherches mais qui en a bien saisi la finalité: me permettre d'exprimer mon intérêt pour la recherche scientifique et m'épanouir davantage. Elle fut la première à me le rappeler dans les périodes creuses. Elle m'a encouragé et supporté durant toutes ces années, même si cela signifiait pour elle de nombreuses heures 'sup', de voyages à l'étranger, et donc, d'absence. Cela ne l'a pas empêché, pendant que je mettais tout en oeuvre pour accoucher de cette unique thèse, de couver et mettre au monde quatre enfants. Merci, mille fois merci pour Valentine, Louis, Eliott et Diego. Eux aussi, à leur manière, ont donné un sens à ce travail.

TABLE OF CONTENTS

Scientific Publications

Articles in periodicals

[1] M. Si Moussa, C. Pavageau, D. Lederer, L. Picheta, F. Danneville, N. Fel, J. Russat, J.-P. Raskin and D. Vanhoenacker-Janvier, "Behaviour of TFMS and CPW Line on SOI Substrate versus High Temperature for RF Applications", *Solid State Electron. (accepted)*, October 2006.

[2] J.-P. Raskin, T. M. Chung, V. Kilchytska, D. Lederer and D. Flandre,"Analog/RF Performance of Multiple-gate SOI Devices: Wideband Simulations and Characterization", *IEEE Trans. Electron Dev.*, vol. 53, pp. 1088–1095, May 2006.

[3] D. Lederer and J.-P. Raskin,"New Substrate Passivation Technique Dedicated to High Resistivity SOI Wafer Fabrication", *IEEE Electron Dev. Lett.*, vol. 26, pp. 805–807, November 2005.

[4] V. Kilchytska, D. Lederer, P. Simon, N. Collaert, J.-P. Raskin and D. Flandre,"Accurate effective mobility extraction by split C-V technique in SOI MOSFETs: suppression of the influence of floating-body effects", *IEEE Electron Dev. Lett.*, vol. 26, pp. 749–752, October 2005.

[5] D. Lederer, V. Kilchytska, T. Rudenko, N. Collaert, D. Flandre, A. Dixit, K. De Meyer and J. P. Raskin ,"FinFET analogue characterization from DC to 110 GHz", *Solid State Electronics*, vol. 49, pp. 1488–1496, September 2005.

[6] D. Lederer, D. Flandre and J.-P. Raskin,"Frequency degradation of SOI MOS device output conductance", *Semiconductor and Science Technology*, vol. 20, pp. 469–472, May 2005.

[7] D. Lederer and J.-P. Raskin,"Effective resistivity of fully-processed SOI substrates", *Solid State Electronics*, vol. 49, pp. 491–496, March 2005.

[8] D. Lederer and J.-P. Raskin, AC analysis of floating body effects in PD SOI MOSFETs", *Belgian Journal of Electronics & Communications HF*, vol. 2, pp. 46–47, 2004.

[9] D. Lederer, D. Flandre and J.-P. Raskin, "AC behavior of gate-induced floating body effects in ultra-thin oxide PD SOI MOSFETs", *IEEE Electron Dev. Lett.*, vol. 25, pp. 104–106, February 2004.

[10] D. Lederer and J. P. Raskin, "Substrate Loss Mechanisms for Microstrip and CPW Transmission Lines on Lossy Silicon Wafers" *Solid State Electronics*, vol 47, pp. 1927–1936, 2003.

[11] G. Dambrine, C. Raynaud, D. Lederer, M. Dehan, O. Rozeaux, M. Vanmackelberg, F. Danneville, S. Lepilliet and J. P. Raskin, "What are the limiting parameters of deep submicron MOSFET's for high frequency applications?", *IEEE Electron Dev. Lett.*, vol. 24, pp. 189–191, March 2003.

[12] V. Kilchytska, D. Levacq, D. Lederer, J.-P.Raskin, and D. Flandre, "Floating Effective Back-Gate Effect on the Small-Signal Output conductance of SOI MOSFETs", *IEEE Electron Dev. Lett.*, vol. 24, pp. 414–416, June 2003.

Articles in Books

[1] D. Lederer and J.-P. Raskin, "Temperature dependence of RF losses in HR SOI substrates", in *Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment*, Eds.: D. Flandre A.N. Nazarov and P.L.F. Hemment P.L.F., Kluwer Academic Publisher, NATO Science Series Elsevier, pp. 192–196, 2005.

[2] D. Lederer and J.-P. Raskin, "Performance of RF passive structures on oxidized High-Resistivity substrates", to be published in *Focus on Semiconductor Research*, Novapublishers, 2007.

Conference Proceedings

[1] D. Lederer and J.-P. Raskin, "Characterization of body resistance in PD SOI MOSFETs using 4-port VNA measurements", *Proceedings of the 6th Topical Meeting on Silicon Microwave Integrated Circuits for RF Systems (Accepted)*, January 2007.

[2] D. Lederer, B. Aspar, C. Laghae-Blanchar and J.-P. Raskin, "Performance of SOI devices transferred onto passivated HR SOI substrates using a layer transfer technique", *Proc. of 2006 IEEE International SOI Conf. (Accepted)*, October 2006.

[3] J.-P. Raskin, G. Pailloncy and D. Lederer, "On-wafer wideband characterization: from technology improvements to compact models for advanced MOS devices", *Microwave Technology and Techniques Workshop Enabling Future Space Systems*, European Space Agency (ESA), Estec, Noordwijk, The Netherlands, May 2006.

[4] D. Lederer and J.-P. Raskin, "On-wafer wideband electrical characterization: a powerful tool for improving the IC technologies", (invited paper), *7th Diagnostics & Yield Symposium*, Warsaw, Poland, June 2006.

[5] D. Lederer and J.-P. Raskin, "Bias effects on RF passive structures in HR Si substrates", *Proceedings of the 6th Topical Meeting on Silicon Microwave Integrated Circuits for RF Systems*, San Diego, pp. 8–11, January 2006.

[6] D. Lederer, B. Parvais, K. Mercha, N. Collaert, J.-P. Raskin and S. Decoutere, "Fin Width dependence of FinFET RF performance", *Proceedings of the 6th Topical Meeting on Silicon Microwave Integrated Circuits for RF Systems*, San Diego, pp. 334–337, January 2006.

[7] V. Passi, D. Lederer and J.-P. Raskin, "Wideband characteristics of multigates MOS devices", *The Thirteenth International Workshop on the Physics of Semiconductor Devices*, (invited paper), New Delhi, India, December 2005.

[8] D. Lederer, O. Rozeau and J.-P. Raskin, "Wideband characterization of body-accessed PD SOI MOSFETs with multiport measurements", *Proc. of 2005 IEEE International SOI Conf.*, Honolulu, pp. 65–66, October 2005.

[9] M. Si Moussa, C. Pavageau, D. Lederer, L. Picheta, F. Danneville, J. Russat, N. Fel, J.-P. Raskin and D. Vanhoenacker-Janvier, "An investigation of Temperature Effects on CPW and MSL on SOI Substrate", *Proc. of 2005 IEEE International SOI Conf.*, Honolulu, pp. 70–71, October 2005.

[10] V. Kilchytska, D. Lederer, P. Simon, N. Collaert, J.-P. Raskin and D. Flandre, "Revised split C-V technique for mobility investigation in advanced devices", *Proc. of 2005 IEEE International SOI Conf.*, Honolulu, pp. 110–111, October 2005.

[11] J.-P. Raskin, T.M. Chung, V. Kilchytska, D. Lederer, A. Dixit, N. Collaert, T. Rudenko and D. Flandre, "FinFET: a mature multigate MOS technology? A wideband transistor simulation and characterization approach", *Network of Excellence – SINANO Workshop*, Grenoble, France, September 2005.

[12] D. Lederer and J.-P. Raskin, "Couplage de surface dans les substrats de silicium à haute résistivité", *Proc. of XIVèmes Journées Nationales Microondes*, Nantes, France, May 2005.

[13] D. Lederer, V. Kilchytska, T. Rudenko, N. Collaert, D. Flandre, A. Dixit, K. De Meyer and J.-P. Raskin, "FinFET analog characterization from DC to 110 GHz", *EUROSOI Workshop*, Grenada, Spain, pp. 99–100, January 2005.

[14] D. Vanhoenacker-Janvier, D. Lederer, J.-P. Raskin and M. Dehan, "Characterisation and optimisation of passive microwave devices integrated on Silicon-on-Insulator", (invited paper), *Asia Pacific Microwave Conference*, New Delhi, India, 2004.

[15] D. Lederer, N. Collaert and J. P. Raskin, "FinFET analog characterization up to 110 GHz", *Proceedings of URSI Forum*, Brussels, Belgium, December 2004.

[16] D. Lederer, P. Delatte, M. Si Moussa, D. Vanhoenacker-Janvier and J.-P. Raskin, "Crosstalk, line and RF MOSFETs", *MEDEA+T206 SOI Project 2004 Workshop*,

Crolles, November 2004.

[17] D. Lederer, R. Lobet and J.-P. Raskin, "Enhanced High resistivity SOI wafers for RF applications", *Proc. of IEEE International SOI Conference*, Charleston (SC), pp. 46–47, October 2004.

[18] V. Kilchytska, N. Collaert, R. Rooyackers, D. Lederer, J.-P. Raskin and D. Flandre, "Perspective of FinFETs for analog applications", *Proc. of ESSDERC*, Leuven, Belgium, pp. 65–68, September 2004.

[19] D. Lederer and J.-P. Raskin, "Temperature dependence of RF losses in HR SOI substrates", *Proc. of NATO Advanced Research Workshop on science and technology of SOI structures and devices operating in harsh environment*, Kiev, April 2004.

[20] D. Lederer and J.-P. Raskin, "AC analysis of floating body-effects in PD SOI MOSFETs", *Proc. of URSI Forum*, Brussels, Belgium, pp. 58–59, December 2003.

[21] D. Lederer, C. Desrumeaux, F. Brunier and J.-P. Raskin, "High Resistivity SOI substrates: how high should we go?", *Proc. of IEEE International SOI Conf.*, Newport Beach (CA), pp. 50–51, September 2003.

[22] D. Lederer, M. Dehan, D. Vanhoenacker, D. Flandre and J.-P. Raskin, "Frequency degradation of SOI MOS device output conductance", *Proc. of IEEE International SOI Conf..*, Newport Beach (CA), pp. 76–77, September 2003.

[23] G. Laurent, L.M. Hagelsieb, D. Lederer, P.-E. Lobert, D. Flandre, J. Remacle and J.-P. Raskin, "DNA Electrical detection Based on Inductor Resonance Frequency in Standard CMOS Technology", *Proc. of ESSCIRC*, Estoril, Portugal, September 2003.

[24] D. Lederer, D. Vanhoenacker, T. Lemoine, J.P. Ghesquiers et J.P. Raskin, "Analyse des pertes diélectriques et conducteur dans les guides d'onde coplanaires réalisés sur substrat de silicium haute résistivité", *XIIIémes Journées Nationales Microondes*, Lille, France, June 2003.

[25] D. Lederer and J.-P. Raskin, "Analysis of Shunt and Series Substrate Losses for CPW Transmission Lines made on Lossy Silicon Wafers", *Proceedings of URSI Forum*, Brussels, Belgium, December 2002.

[26] M. J. Azanza, R. N. Pérez Bruzón, D. Lederer, A. C. Calvo, A. Del Moral and A. Vander Vorst, "Reversibility of the effects induced on the spontaneous bioelectric activity of neurons under exposure to 8.3 and 217.0 Hz low intensity magnetic fields", *2nd Intern. Workshop on Biological Effects of EMFs*, Rhodes, pp. 651–659, October 2002.

[27] V. Kilchytska, D. Levacq, D. Lederer, J.-P.Raskin, and D. Flandre, "Substrate effects on the small-signal characteristics of SOI MOSFETs", *Proc. of ESSDERC*, Florence, Italy, pp. 519–522, September 2002.

[28] D. Lederer and J.P. Raskin, "Substrate Loss Mechanisms for Microstrip and CPW Transmission Lines on Lossy Silicon Wafers", *Proc. of IMS*, Seattle, Oregon, pp. 685–688, June 2002.

[29] D. Lederer and J.P. Raskin, "Substrate Loss Mechanisms for Microstrip and CPW Transmission Lines on Lossy Silicon Wafers", *Proc. of URSI Forum*, Louvain-la-Neuve Belgium, December 2001.

[30] D. Lederer, M. J. Azanza, A. C. Calvo, R. N. Pérez Bruzón, A. del Moral and A. Vander Vorst, "Effects associated with the ELF of GSM signals on the spontaneous bioelectric activity of neurons", *Proc. of 5th International Congress of the European Bioelectromagnetic Association*, Rhodes, Greece, pp. 194–195, October 2001.

[31] D. Lederer, "Biological Effects Induced by Low Intensity EMF", *Proc. of URSI Forum*, Brussels, Belgium, pp. 55, December 2000.

Patents

[1] J.-P. Raskin, D. Lederer and F. Brunier, "Procédé de fabrication de structure multicouche à pertes diminuées", Patent application n^o: 240578/D21249, filed in September 2003.

[2] J.-P. Raskin and D. Lederer, "Method of manufacturing a multilayer semiconductor structure with reduced ohmic losses", Patent application n^o: PCT/BE2004/000137, filed in October 2004.

Glossary

AC: Alternative current
AFM: Atomic force microscopy
APCVD: Atmospheric pressure chemical vapor deposition
AZE: Active zone extension
BESOI: Bonded and etched back SOI
BCB: Benzocyclobutene
BEOL: Back-end of line
BOX: Buried oxide
BC: Body-contacted
BT: Body-tied
CAD: Computer-aided design
CMOS: Complementary metal-oxide-semiconductor
CMP: Chemo-mechanical polishing
CPW: Coplanar waveguide
CVD: Chemical vapor deposition
DC: Direct current
DECT: Digital European cordless telephony
DELTA: Depleted lean-channel transistor
DIBL: Drain-induced barrier lowering
DT: Dynamic threshold
DUT: Device under test
ECB: Electrons (from the) conduction band
EVB: Electrons (from the) valence band
FB: Floating body
FBE: Floating body effect
FD: Fully-depleted
FUSI: Full gate silicidation
GAA: Gate-all-around
GIFBE: Gate-induced floating body effect
GPS: Ground positioning system
HBT: Heterojunction bipolar transistor
HDD: Highly doped drain
HF: High frequency
HP: High performance
HR: High resistivity
HRS: High resistivity silicon

HVB: Holes (from the) valence band
IC: Integrated circuit
IMD: Intermetal dielectric
IR: Infrared
ITRS: International Technology Roadmap for Semiconductors
LKE: Linear kink effect
LNA: Low noise amplifier
LPCVD: Low pressure chemical vapor deposition
LSB: Low Schottky barrier
MAG: Maximum available gain
MEMS: Micro-electro-mechanical systems
MIS: Metal-insulator-semiconductor
MMIC: Monolithic microwave integrated circuit
MOSFET: Metal-oxide-semiconductor field effect transistor
MOCVD:
MS: Microstrip line
MSG: Maximum stable gain
MUGFET: Multiple gate MOSFET
OSE: Outside spacer extension
PD: Partially-depleted
PECVD: Plasma-enhanced chemical vapor deposition
PMA: Post-metalization anneal
PMD: Primary metal dielectric
PSC: Parasitic surface conduction
RF: Radiofrequency
RFIC: Radiofrequency integrated circuit
RFID: RF identification
RMS: Root mean square
RTA: Rapid thermal anneal
RTAC: RTA-crystallized
SCE: Short channel effects
S/D: Source and drain
SEG: Selective epitaxial growth
SEM: Scanning electron microscopy
SG: Single gate
SIMOX: Separation by implanted oxygen
SoC: System-on-chip
SoG: Spin-on-glass

SOI: Silicon-on-insulator
SOQ: Silicon-on-quartz
SOS: Silicon-on-sapphire
sSOI: Strained silicon-on-insulator
SSOI: SiGe-on-SOI
STI: Shallow trench isolation
TA: Thermal anneal
TEM: Transverse electromagnetic *or* Transmission electron microscopy
TFT: Thin film transistors
TG: Triple gate
TLR: Thru-Line-reflect
TFMS: Thin film microstrip line
UCL: Université catholique de Louvain
UTB: Ultra-thin body
VCO: Voltage-controlled oscillator
VNA: Vector network analyzer
WLAN: Wireless local area network

CHAPTER 1
INTRODUCTION

1.1 SOI: the future of CMOS

In 1965 Gordon Moore was the first to notice that the number of devices inside chips could be increased at a constant exponential pace, essentially because engineers were able to reduce the size of transistors. Over the years and for more than four decades Moore's axiom has held true and is now widely considered as a "law", gradually shifting from a mere observation to the driving force of the semiconductor industry.

The fantastic evolution of microelectronics has thus been made possible by continuously shrinking the size of the transistors and successively overcoming the challenges encountered at each transistor generations. In this context, the silicon-based planar bulk CMOS technology has been the technology of choice by microprocessor manufacturers due to its low cost and excellent scalability. Figure 1.1 shows the evolution of the gate length of bulk CMOS transistors fabricated at Intel for the past 25 years. The figure highlights the discrete technological steps, or *nodes*, that have been achieved and indicates that 30 nm-long devices are now being produced. The figure also shows the predictions made by the International Technology Roadmap for Semiconductors (ITRS) for the coming 15 years.

According to the 2005 ITRS Roadmap [1], the downscaling of planar bulk CMOS devices has now reached a point where further scaling is to face significant challenges. The main issue arises from the high-channel doping required to control short-channel effects (SCE), which significantly degrades carrier mobility and reduces the drain current. It also increases band-to-band tunneling across the junctions, leading to an increase of the parasitic leakage current. In addition, the statistical fluctuation of channel dopants is to cause increasing variations of the threshold voltage.

As a consequence, the implementation of new structures such as *ultra-thin body* (UTB) *fully depleted* (FD) *Silicon-on-Insulator* (SOI) and *multiple gate* MOSFETs (MUGFETs), which both require lower doping levels, appears as the only viable alternative in silicon-based technologies to replace planar bulk CMOS devices in microprocessors within a few years. As illustrated in Figure 1.1 the introduction of UTB FD SOI and multiple gate MOSFETs on the industrial stage should occur no later than in 2008 and 2011, respectively. Nevertheless, the tremendous challenges faced by the implementation of FD SOI devices (such as a precise control

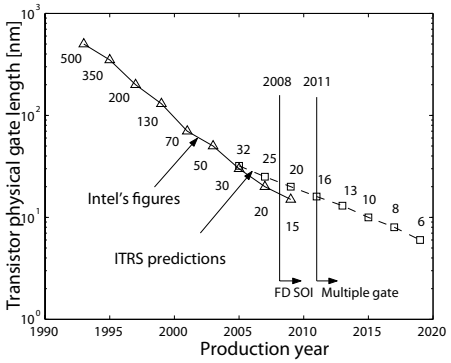


Figure 1.1: Evolution of the physical gate length in microprocessors fabricated at Intel and future ITRS predictions.

of the silicon film thickness, the reduction of source and drain resistances to tolerable values, ...) has driven some major IC manufacturers to directly target the fabrication and production of multiple gate transistors. In this context, the most likely-to-emerge MUGFETs consist in the triple gate and the FinFET structures due to their high compatibility with planar CMOS processing. At the present time, these SOI-based devices have already been subjected to intense investigation in major IC foundries such as Intel [2] or IBM [3].

SOI therefore appears as a necessary option for future silicon-based devices. Yet it must be pointed out that the introduction of SOI into production lines has actually been achieved much earlier than what was planned by the 2005 ITRS for the *fully depleted* UTB MOSFETs or SOI MUGFETs. Leading IC manufacturers, such as IBM, AMD and Freescale, have been producing *partially depleted* SOI chips for half a decade by now. This is because the improvements gained by using SOI instead of bulk devices have considerably boosted chip performance. The first SOI product, a 64-bit PowerPC microprocessor from IBM, was already shipped in the summer of 1998 [4].

The continuous and long term efforts that have been devoted to developing and producing SOI by many independent and private research groups have grown SOI into a mature technology. The use of SOI in the *digital* microprocessor world is now globally spread. However, as SOI is especially well suited for low power applications, the SOI technology has also recently penetrated the *analogue* market. As described at the end of this chapter, the SOI technology constitutes a serious option for low cost analogue/RF products, such as front-end receivers of mobile phones.

SOI is thus mature, worldwide and application rich.

The coming paragraphs offer an introductive view of the SOI technology as opposed to the bulk technology and briefly expose the reasons why it has gradually become a major actor in the IC industry. The scope of this thesis is detailed at the end of this chapter.

1.2 The SOI material

The first silicon-on-insulator wafers were developed more than 30 years ago, and initially consisted in SOS (silicon-on-sapphire) wafers which were first commercialized in 1971 [5]. These wafers presented low carrier mobility and a high cost of fabrication, which has pushed scientists to develop other types of silicon-on-insulator materials such as silicon-on-insulator-on-silicon (SOI). The first commercially available SOI wafers were the SIMOX substrates, already in 1987.

1.2.1 Fabrication of SOI wafers

A variety of different methods have been developed to fabricate high quality SOI wafers, which distinguish themselves from bulk wafers by the presence of a thin insulating layer at a certain depth of the top silicon surface. An exhaustive overview of these methods, which can be classified into three main families, can be found in [5] and [6]:

- The first category comprises SOI wafers obtained by *deposition* of either crystalline silicon (using epitaxial growth) or polysilicon on an insulator-covered wafer. In the latter case, the recrystallization of polysilicon into single crystal silicon can be obtained by laser or zone melting methods [5].

- In a second approach, the SOI wafers are fabricated by *isolating* a thin silicon layer from the substrate. This layer is then oxidized and forms the buried oxide of the final structure. The most successful technique of this category has been the Separation-by-Implanted-Oxygen (SIMOX) approach, in which the BOX is fabricated by implanting oxygen at a certain distance from the surface of the starting bulk wafer. The implanted wafer is then annealed to form SiO_2 at the desired depth.

- In the last category, the SOI wafers are built by *bonding* two wafers together. A variety of bonding approaches have been proposed, such as the Bonded-and-Etched-back SOI (BESOI) and the Smart-Cut process. BESOI wafers are obtained by thinning a silicon wafer that has been bonded onto an oxidized wafer. Though

this method provides high quality SOI wafers, it is expensive since it consumes two Si wafers per SOI wafer produced. Another approach, called Smart-Cut, solves this issue. This successful technique is widely considered in the 3^{rd} chapter of this work and is further described in the coming section.

1.2.2 The Smart-Cut process: a technical and commercial success

SOI wafers fabricated using the Smart-Cut technique are called UNIBOND wafers. The fabrication of UNIBOND wafers is illustrated in Figure 1.2. The method consists in the following basic steps [7]: (a) thermal oxidation of a Si bulk substrate called "donor substrate", (b) implantation of hydrogen through the oxide into the donor substrate, which forms microcavities and microbubbles in the implanted substrate at a depth equal to the implantation range, (c) bonding of the oxidized substrate with a HR Si substrate called "handle substrate" (d) thermal processing of the bonded structure in order to split the donor substrate and leave a silicon film on the oxide, (e) chemo-mechanical polishing (CMP) of the Si film to obtain the desired surface roughness and layer thickness.

The Smart-Cut technique provides numerous advantages over other methods used to build SOI wafers, which are summarized here [5, 6]:

- it yields a much better uniformity of the silicon surface (0.15 nm) than other methods,

- since only a small proportion of the donor wafer is used per fabrication cycle, the donor wafer is almost entirely recyclable,

- unlimited combinations of BOX and film thicknesses can be achieved, targeting a variety of different applications (high power, MEMS, optoelectronics...),

- this method can potentially be used to transfer a thin layer of any semiconductor material on top of an insulator,

- it relies on existing standard microelectronic manufacturing equipment.

These advantages have largely contributed to its popularity among the scientific community and has lead to an undeniable industrial success. Large volume production was achieved around the year 2000. SOI wafers fabricated using the Smart-Cut process currently represent 80 % of the total SOI wafer market.

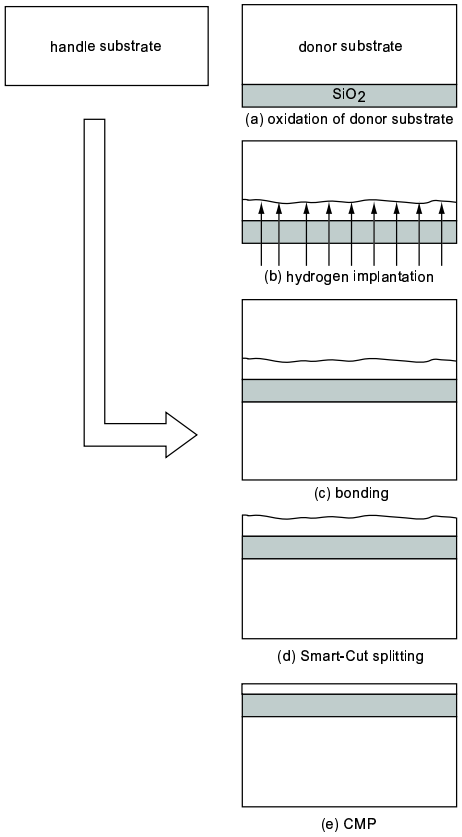


Figure 1.2: Fabrication of UNIBOND SOI wafers using the Smart-Cut process.

1.3 Advantages of SOI over bulk

At a device or circuit level, the advantages of SOI over bulk CMOS technologies are well known [5,6,8] and can be summarized as follows:

- *substrate isolation*: as the BOX isolates the source/drain extensions from the substrate, junctions capacitances and leakage current are reduced. This yields increased speed and reduced power consumption compared to the bulk technology. The isolation from the substrate also provides immunity to latchup.
- *reliability*: SOI circuits are highly insensitive to radiation effects, since electron-hole pairs are generated in the thick silicon substrate instead of inside the thin active film.
- *top material*: since the Smart-Cut process can be adapted to transfer any semiconductor material on top of the buried oxides, strained silicon-on-insulator (sSOI) and SiGe-on-insulator (SGOI) wafers can be easily fabricated. This type of wafers have already been demonstrated to increase device performance by carrier mobility enhancement [9,10], and are almost ready for production.
- *HR substrates*: The use of high resistivity (HR) substrates (with resistivity higher than 1 k$\Omega.cm$) is hardly compatible with bulk CMOS when digital circuitry is required (due to latchup issues [11,12]) unless patterned implants of deep boron doses are used to locally reduce the substrate resistivity [13]. In SOI, low loss HR substrates can be easily fabricated and boost the performance of Si-based RF circuits.

At a process level, other main benefits of SOI are:

- *increased layout density*: unlike in bulk technology neither wells nor deep trenches are needed to isolate the devices from one another, allowing flexibility for more compact designs and offering a simplified technology.
- *new device architectures*: the use of SOI substrates facilitates the fabrication of SCE-free multiple gate devices at nanoscale dimensions, which form the future of the CMOS roadmap.

Because of these significant advantages, it is often considered that the SOI technology is one node ahead than its bulk rival: at node n it performs comparably with the bulk technology at node $n+1$ [6].

SOI currently represents some 3-4 % of the total wafer market. This figure is even expected to rise to 10 % by the end of the decade. Recent market research made by Gartner Dataquest and Semicon Research Corp. indicates that the total

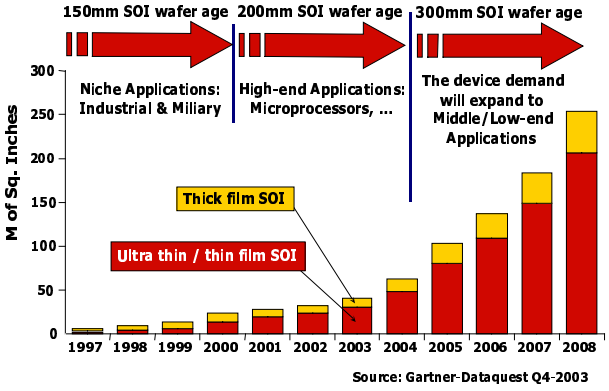


Figure 1.3: Time evolution of the SOI wafer market.

SOI wafer market is expected to approach US$1 billion by 2009. Figure 1.3 shows the fantastic evolution of the SOI wafer market over the last decade. The figure also highlights the relative contribution of thin (with a top film thickness (t_{Si}) lower than 1 μm) and thick ($t_{Si} > 1\ \mu m$) SOI products and indicates the market penetration time of the different wafer sizes. 300 mm-wide SOI wafers are currently being manufactured and processed. The size of the wafers should further increase in future years (450 mm in 2012 [14]). The maturity and benefits of SOI combined with the increased availability of SOI wafers have charmed some major IC chip builders into the fabrication and commercialization of SOI-based products, as described below.

1.4 *Fully vs partially depleted devices: distinct advantages, different applications*

In planar SOI technology two distinct families of devices are classically considered. In *fully-depleted* (FD) MOSFETs, the thickness of the silicon film is reduced in such a way that the depletion region below the inversion channel extends down to the buried oxide. In this case the entire Si film is depleted from free carriers. When the film is made thicker the depletion region can stop at a certain depth within the silicon film, leaving an un-depleted region above the buried oxide called the *body*. For this reason such devices are referred to as *partially depleted* (PD) MOSFETs. The floating potential of the body region in PD SOI MOSFETs is responsible of

floating body effects, which affect the device electrical behaviour.

The electrical characteristics of fully and partially depleted transistors are distinct and confer different advantages to both types of devices:

- *Fully depleted MOSFETs*: FD devices present nearly ideal subthreshold slopes, enabling the reduction of the threshold voltage and of the power consumption. Junction capacitances are the lowest and the FD technology is therefore particularly well suited for ultra low power analog applications [15, 16]. This was demonstrated by a Japanese company, OKI, which fabricated an IC in 0.35 μm Fully-Depleted (FD) SOI consuming 150 nA at 0.7 V for a CASIO solar watch [17]. OKI also successfully built AC receivers for time code signals (transmitted at frequencies ranging from 40 KHz to 100 KHz) with a power consumption of 17 μW, one third to one tenth lower than using bipolar-based technologies.

- *Partially depleted MOSFETs*: PD transistors present a reduced process complexity compared to FD devices [4]. They also present other advantages such as a dynamic threshold voltage (V_T) (which can boost the drain current and reduce switching times [6]), an easier processing of multiple V_T circuits, and the possibility of connecting the body (thereby enabling to completely suppress floating body effects under DC conditions [4]). The characteristics of PD devices make them very attracting for high speed, high performance digital applications. Companies like IBM, Freescale, AMD and Toshiba-Sony have all adopted PD SOI for their microprocessor products. Examples of upcoming high end applications are the graphic processors of game consoles (Play Stations and Xbox).

Other niche applications of SOI include radiation-hard circuits for the space and military industry, high temperature circuits for the automotive industry as well as for oil drilling equipment, and more recently, MEMS [18] and optoelectronics components [19]. The status of SOI for mixed signal/RF applications is discussed in the next paragraph.

1.5 Future use of SOI, a promising contender for mixed signal and RF applications

The mainstream of RF applications currently relies on III-V (GaAs, GaN) and silicon-germanium (SiGe) bipolar silicon (BiCMOS) technologies due to their superior noise and high frequency performance [20]. The availability of wide bandgap materials (such as GaN) has also made III-V technologies more suitable for RF applications in which high power amplification is needed [21]. However, as device dimensions have continued to scale down silicon-germanium (SiGe) heterojunction

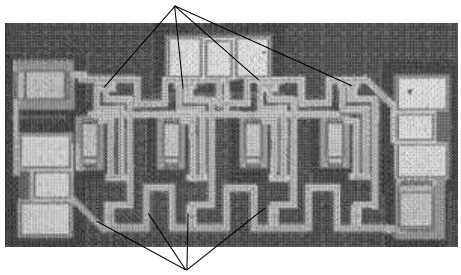
bipolar (HBT) and RF CMOS technologies are now able to seriously compete with compound semiconductors. For instance, 90 nm gate length nMOS devices were recently reported with f_t and f_{max} values of 243 and 208 GHz respectively and a minimum noise figure of 1.1 dB at 26 GHz [22]. The rapid improvement of the RF capability of silicon has been such that silicon is now widely considered as a viable option to replace GaAs in some applications [20, 23, 24].

Clearly, the main motivator for the use of CMOS over BiCMOS or III-V technologies is its lower cost. As explained in [25] similar or even lower cost can be obtained using BiCMOS or III-V technologies when *purely* RF functions are considered. Indeed in that case the chip area is dominated by passive devices and I/O pads. However, when even small amounts of digital logic are to be integrated CMOS has a clear advantage as circuit density and chip size scale with the square of the minimum lithographic dimension [25]. For this reason most successful commercializations of RF bulk CMOS products have been realized with systems-on-chip (SoCs), in which a high level of (mixed: digital/analog) integration could be achieved: radio transceivers for wireless local area network (WLAN), Bluetooth and Zigbee standards [24, 26], GPS receivers, transceivers for DECT (Digital European Cordless Telephony) cordless and GSM cellular phones [24].

Because of the recent advances in CMOS technology, the current limitations of CMOS are no longer related to the intrinsic performance of the active devices but to the quality of the passive components [27]. The performance of RF circuits is indeed determined to a large extent by the quality factors of the passive devices, which reflects their ability to store electrical energy and their propensity to dissipate power. Power dissipation is mainly associated with substrate and conductor losses, and to a lesser extent electromagnetic radiation. A reduction of substrate as well as conductor losses is therefore crucial. Another important issue in mixed signal RF CMOS applications is the amount of noise injected into the substrate by the digital logic and crosstalk which can affect sensitive RF functions. Proper design is thus essential in reducing substrate noise generation and parasitic crosstalk.

In this context, SOI appears as a technology of choice for mixed signal RF CMOS applications. Due to its lower junction capacitance and reduced leakage current, SOI provides reduced static and dynamic power consumption of the digital logic (by a factor close to 30-40 % [8]) combined with increased cut off frequencies [28]. Crosstalk in SOI is also reduced since the buried oxide (BOX) provides better electrical insulation [29]. In terms of passive device integration the major benefit of SOI is the possibility of using high resistivity (HR) substrates, as mentioned earlier. Though there is still some concern from parasitic surface conduction below the BOX in HR SOI wafers, typical effective resistivity values lie in the several hundreds

Active devices:
Floating body effects and body node characterization in **Chapter 4**
RF properties of triple gate MOSFETs in **Chapter 5**



Transmission lines and passive devices:
substrate losses in **Chapter 2**
improvement of substrate quality in **Chapter 3**

Figure 1.4: Top picture of a travelling wave amplifier highlighting the use of both passive (transmission lines) and active (MOSFETs) devices. The figure also outlines the different aspects investigated in this work.

of Ω.cm range, which provides substantial loss reduction over standard (20 Ω.cm) resistivity wafers. The reduction of substrate losses in the case of HR SOI also relaxes the design of passive devices, allowing a further decrease in conductor losses. Optimized passive designs for HR substrates was demonstrated to allow up to 60 % reduction of power consumption for RF blocks such as VCO's [30].

Examples of successful realizations of mixed signal RF circuits using SOI are the 10 Gbps ethernet transceiver from Mitsubishi [31], which was already commercialized in 2002, or more recently the RFID tags designed by Hitachi on a 0.130 μm technology [32]. It is believed that these are only the first examples of SOI-based RF applications, as SOI is likely to become a major contender for the low power mixed signal/RF industry.

1.6 Scope of this work

The scope of this work is to assess the present status of the RF performance of HR SOI substrates and SOI devices for analogue and RF applications. For such applications it is often desired that passive and active components are integrated on the same chip to reduce fabrication costs. Passive devices typically consist in transmission lines, varactors and inductors, which are distributed amongst and connected to the nodes of active devices such as bipolar transistors or MOSFETs. This is illustrated in Figure 1.4 for the particular case of a travelling wave amplifier, a widely used RF circuit block.

In order to achieve high speed performance and low power consumption it is also desirable that passive devices with the lowest losses and active devices with the highest cut-off frequencies are built on the same chip.

As losses of passive devices are intimately related to losses in the substrate itself, the first part of this work (Chapter 2) deals with the RF performance of *high resistivity SOI substrates*, with a nominal resistivity (ρ_{Si}) value typically higher than 3 $k\Omega.cm$. It is well known that HR SOI wafers exhibit a substantial loss reduction over standard ($\rho_{Si} \simeq 20\ \Omega.cm$) resistivity substrates. However it is shown in Chapter 2 that currently manufactured HR SOI wafers suffer from a resistivity degradation at the substrate surface, which considerably reduces the RF performance expected by this kind of wafers. In Chapter 3 we propose a HR SOI wafer fabrication technique that successfully overcomes this issue.

While Chapters 2 and 3 focus on the performance of *passive* devices on HR SOI substrates, Chapters 4 and 5 deal with the analogue/RF behaviour of *active* devices. In Chapter 4, a frequency analysis of floating body effects in partially-depleted SOI devices is presented. This analysis includes the gate-induced floating body effect caused by gate tunneling in advanced CMOS technologies. It is shown that its frequency behaviour exhibits strong similarities with that of the well know kink effect, both being dictated by time variations of the body potential. An accurate AC modeling of these floating body effects therefore requires a complete characterization of the body node in PD devices, which can be accomplished by using a multiport measurements set up. The use of multiport measurements to characterize multiple access PD SOI devices is illustrated for the first time in that chapter. Finally, the RF properties of sub-100 nm triple gate FD SOI devices are analyzed in Chapter 5. The main sources of parasitics in these devices are highlighted and technological approaches to reduce these parasitics are proposed. Despite unoptimized device geometry and technological process steps, the investigated devices outline cut off frequencies on the order of 100 GHz, supporting their possible use for future RF applications.

References

[1] "Executive summary." [Online]. Available: http://www.itrs.net/Common/2005ITRS/ExecSum2005.pdf

[2] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," *VLSI Symp.*, 2006.

[3] J. Kedzierski, M. Ieong, E. J. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, "Extension and source/drain design for high performance FinFET devices," *IEEE Trans. Electron Dev.*, vol. 50, no. 4, pp. 942–957, 2003.

[4] G. G. Shahidi, "SOI technology for the GHz era," *IBM Journal of Research and Development*, vol. 46, pp. 121–131, 2002.

[5] J.-P. Colinge, *Silicon-On-Insulator technology: Material to VLSI.* USA: Springer, 2004.

[6] S. Cristoloveanu, "Silicon-on-insulator technologies and devices: from present to the future," *Solid State Electronics*, vol. 45, pp. 1403–1411, 2001.

[7] M. Bruel, "Smart cut: A promising new SOI material technology," *Proceedings of 1995 IEEE International SOI Conference*, pp. 178–179, Tucson, AZ, 1995.

[8] D. Flandre, J.-P. Raskin, and D. Vanhoenacker, "SOI CMOS transistors for RF and microwave applications," *International Journal of High Speed Electronics and Systems*, vol. 11, no. 4, pp. 1159–1248, 2001.

[9] Z.-Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Electron mobility enhancement in strained-si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *IEEE Electron Dev. Lett.*, vol. 22, pp. 321–323, 2001.

[10] C. Mazure and I. Cayrefourcq, "Status of device mobility enhancement through strained silicon engineering," *IEEE Int. SOI Conf.*, pp. 1–6, 2005.

[11] C. C. Huang, M. D. Hartranftand, N. F. Pu, C. Yue, C. Rahnand, J. Schrankler, G. D. Kirchner, F. L. Hampton, and T. E. Hendrickson, "Characterization of CMOS latch-up," *Digest of International Electron Device Meeting*, pp. 454–457, 1982.

[12] T. Yamaguchi, S. Morimoto, G. H. Kawamoto, and J. C. D. Lacy, "Process and device performance of 1 μm-channel n-well CMOS technology," *IEEE Trans. Electron Dev.*, vol. 31, pp. 205–214, 1984.

[13] K. Benaissa, J.-T. Yuan, D. Crenshaw, B. Williams, S. Sridhar, J. Ai, G. Boselli, S. Zhao, S. Tang, S. Ashbun, P. MAdhani, T. Blythe, N. Mahalingam, and H. Schichijo, "RF CMOS high-resistivity substrates for systems-on-chip applications," *IEEE Trans. Electron Dev.*, vol. 50, no. 3, pp. 567–576, 2003.

[14] "Front end processes." [Online]. Available: http://www.itrs.net/Common/2005ITRS/FEP2005.pdf

[15] M. Vanmackelberg, C. Raynaud, O. Faynot, J.-L. Pelloie, C. Tabone, A. Grouillet, F. Martin, G. Dambrine, L. Picheta, E. Mackowiak, P. Llinares, J. Sevenhans, E. Compagne, G. Fletcher, D. Flandre, V. Dessard, D. Vanhoenacker, and J.-P. Raskin, "0.25 μm fully depleted SOI MOSFETs for RF mixed analog-digital circuits,including a comparison with partially depleted devices with relation to high frequency noise parameters," *Solid State Electronics*, vol. 46, pp. 379–386, 2002.

[16] F. Ichikawa, Y. Nagatomo, Y. Katakura, M. Itoh, S. Itoh, H. Matsuhashi, T. Ichimori, N. Hirashita, and S. Baba, "Fully depleted SOI process and device technology for digital and RF applications," *Solid State Electronics*, vol. 48, pp. 999–1006, 2004.

[17] M. Nagaya, "Fully-depleted type SOI device enabling an ultra low-power solar radio wristwatch," *OKI Technical Review*, vol. 70, no. 1, pp. 48–51, 2003.

[18] V. Gaff, "SOI-MEMS in oil exploration," *Advanced Substrate News*, vol. 1, April 2005.

[19] C. Gunn, "CMOS photonics^{TM} - SOI learns a new trick," *Proc. of IEEE Int. SOI Conf.*, pp. 7–13, 2005.

[20] A. R. Barnes, A. Boetti, L. Marchand, and J. Hopkins, "An overview of microwave component requirements for future space applications," *Proc. of 13th GAAS Symposium*, pp. 5–9, Paris, 2005.

[21] J. Palmour, S. T. Sheppard, R. P. Smith, S. T. Allen, W. L. Pribble, T. J. Smith, Z. Ring, J. J. Sumakaris, A. W., Saxler, and J. W. Milligan, "Wide bandgap semiconductor devices and MMICs," *Digest of International Electron Device Meetings*, pp. 17.4.1–17.4.4, 2001.

[22] N. Zamdmer, J. Kim, R. Trzcinski, J.-O. Plouchart, S. Narasimha, M. Khare, L. Wagner, and S. Chaloux, "A 243-ghz f_t and 208-ghz f_{max}, 90nm SOI CMOS SoC technology with low-power millimeter-wave digital and RF circuit capability," *Symposium on VLSI Technology Digest of Papers*, pp. 98–99, 2004.

[23] J. J. Liou and F. Schwierz, "RF MOSFET: recent advances, current status and future trends," *Solid State Electronics*, vol. 47, no. 11, pp. 1881–1895, 2003.

[24] A. A. Abidi, “RF CMOS comes of age,” *IEEE Journal of Solid State Circuits*, vol. 39, no. 4, pp. 549–561, 2004.

[25] J. J. Pekarik, D. D. Coolbaugh, P. E. Cottrell, S. M. Csutak, D. R. Greenberg, B. Jagannathan, D. I. Sanderson, L. Wagner, J. Walko, X. Wang, and J. Watts, “Enabling RFCMOS solutions for emerging advanced applications,” *Proc. of 13th GAAS Symposium*, pp. 36–43, Paris, 2005.

[26] K. T. Le, “Designing a ZigBee-ready IEEE 802.15.4-compliant radio transceiver,” *RF Design*, vol. 11, 2001.

[27] “RF and A/MS technologies for wireless communications.” [Online]. Available: http://www.itrs.net/Common/2005ITRS/Wireless2005.pdf

[28] R. Huang, H. Liao, and G. Zhang, “SOI CMOS technology for RF/MMIC applications: yes or no?” *Proc. of 35th European Solid-State Device Research Conf.*, pp. 244–247, 2005.

[29] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, “Substrate crosstalk reduction using SOI technology,” *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2252–2261, 1997.

[30] P. Delatte, G. Picun, L. Demeus, P. Simon, and D. Flandre, “Low-power 5 GHz CMOS LC-VCO optimized for high-resistivity SOI substrates,” *Proc. of ESSCIRC*, pp. 395–398, Grenoble, 2005.

[31] “Mitsubishi electric launches world’s first SOI-CMOS single-chip 10-Gbit ethernet physical-layer transceiver LSI,” 2002. [Online]. Available: http://www.mitsubishielectric.com/news/2002/Ethernet_Physical-Layer_Transceiver_8-13-02.html

[32] E. Times, “Hitachi advances paper-thin RFID chip,” 2006. [Online]. Available: http://www.eetimes.com/news/semi/showArticle.jhtml?articleID=179100286

CHAPTER 2
RF PERFORMANCE OF HIGH RESISTIVITY SOI SUBSTRATES

2.1 Introduction

With the rapid boom of mobile communication systems and the recent explosion of the telecommunication market, much pressure has been set on the microelectronics industry to produce low cost, high performance RF and mixed mode circuits. The integration of both RF analogue and digital circuits on a single chip requires that substrate issues are fully addressed, since substrate losses and crosstalk noise are known to be major factors limiting the performance of Systems-on-a-Chips (SoCs) [1], [2]. Selecting the appropriate material for the substrate is therefore crucial. In this context High Resistivity Silicon (HRS) appears as a promising medium for radio frequency integrated circuits (RFIC) [3,4] and mixed signal applications [2] due to its low cost and full compatibility with CMOS processing. Besides, nominal values of resistivity as high as 10 kΩ.cm can readily be achieved. However, due to the semiconductor nature of silicon, oxidized HR silicon substrates (such as in HR SOI wafers) are usually characterized by space charge effects at the SiO_2/Si interface, which can lead to a local reduction of the substrate resistivity and parasitic conduction at the substrate surface [3–6].

The aim of the present chapter is therefore to provide the reader with a view of the difficulties encountered when intending to obtain *truly high* resistivity substrates. It is also to assess the RF performance of oxidized HR silicon or HR SOI substrates. Since an extensive use of transmission lines is made for characterization purposes, this chapter starts with a brief overview of the fundamental properties of such structures on the SiO_2/Si system, as presented in [7]. In that section, two different structures are investigated: the microstrip (MS) line and the coplanar waveguide (CPW). It is shown that due to different electrical configuration inside the two structures, both types of lines exhibit distinct electrical behavior and substrate loss mechanisms. In particular, the coplanar structure is particularly sensitive to variations of the electrical properties at the substrate surface. This structure then proves itself as a very convenient tool to characterize the properties of oxidized HR silicon substrates and is used to analyze the effect of parasitic conduction below the oxide. A new factor of merit is developed for this purpose, called *effective resistivity*, which enables a fair performance comparison between

wafers having differently processed CPW lines. The impact on the substrate effective resistivity of various technological (fixed charges in the oxide, traps at the SiO_2/Si interface, oxide thickness ...) and external (DC bias and temperature) parameters is then extensively investigated, constituting the core of this chapter. It is shown that a very effective way to remove free carriers from the substrate surface consists in introducing a large density of traps at the SiO_2/Si interface. This method enables to completely eradicate substrate losses and to realize low loss CPW lines on oxidized HR silicon. The performance of such structure is then compared with those obtained using other technologies, such as purely dielectric substrates (fused silica) or other line topologies. The line topology that is investigated is the thin film microstrip (TFMS) line, which presents the advantage of being insensitive to the substrate electrical behavior since it is completely screened by a metallic ground plane. The last section of this chapter is finally devoted to further illustrate the negative impact of parasitic surface conduction (PSC) in oxidized HR substrates for two other types of passive structures: crosstalk structures and inductors. Combining measured data and small signal equivalent circuits of the structures, it is shown that better RF performance (lower crosstalk, higher quality factor of inductors) can be obtained by removing free carriers from the substrate surface.

2.2 MIS lines in silicon-based MMICs

Ever since the early years of silicon-based technologies, device interconnections have been a major source of concern. It was indeed already understood during the late sixties, when fast switching semiconductor devices started becoming available and very large scale integration appeared feasible, that the interconnection delay was going to set a severe constraint limiting the ultimate speed of logic circuits [8]. With the increase of circuit operating frequencies interconnections could not be considered as equipotential wires and their transmission line behavior needed to be fully addressed.

At that time, and for more than two decades, the only line structures available for the fabrication of Monolithic Microwave Integrated Circuits (MMICs) consisted in microstrip lines and several coplanar structures such as slotlines and coplanar waveguides. Among those structures, it appeared that *microstrip lines* (MS) and *coplanar waveguides* (CPW) were the most attractive for use in MMICs due to the convenient field configuration and superior electrical characteristics of those two line topologies [9]. Schematic views of a MS line and a CPW line with finite ground planes on a silicon-based technology are provided in Figures 2.1a and b,

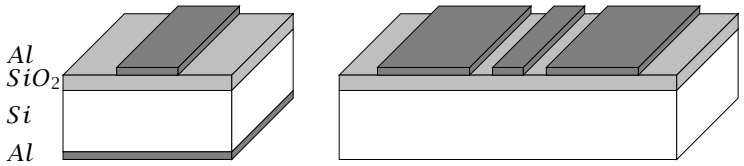


Figure 2.1: Schematic representation of a MIS microstrip line (a) and a MIS coplanar waveguide with finite ground planes (b).

respectively. The use of MS and CPW lines in silicon technologies was also largely supported by the easiness and low cost of their fabrication process, which simply consists in depositing a layer of aluminium on an oxidized silicon substrate for CPW lines, with an additional wafer backside metalization in the case of MS lines. The insulating oxide (SiO_2) layer sandwiched between the metal strips and the substrate was - and is still - intended to electrically isolate the lines from the silicon, thus avoiding parasitic DC current injection into the substrate. For this reason these structures are often referred to as Metal-Insulator-Silicon (MIS) lines.

Nowadays MIS lines and to a larger extent MIS CPW lines are still of great interest for silicon-based MMICs. They are typically used in passive structures such as matching circuits, filters, transformers and inductive elements in distributed amplifiers [10–12]. However, the presence of an insulating oxide that is 2 to 3 orders of magnitude thinner than its lossy silicon counterpart confers very specific characteristics to lines fabricated on the $SiO_2 - Si$ system. Over the past 4 decades, those properties have attracted a considerable interest among the scientific community and have been extensively investigated through a variety of methods: experimental approaches [7], rigorous analytical and numerical techniques [13–17] and also using closed-form expressions [18,19]. While all those studies largely led to a better knowledge of MIS line physical properties, a significant contribution was already provided in the early seventies by the pioneering work of Hasegawa and his co-workers [7]. This contribution is summarized below.

2.2.1 The $SiO_2 - Si$ system and its propagation modes

In his fundamental work, Hasegawa *et al.* identified three possible modes of signal propagation in MIS MS lines [7]:

- the *quasi-TEM* mode,
- the *slow wave* mode,

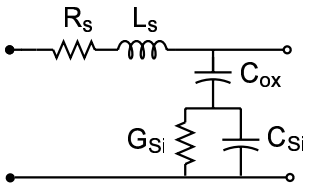


Figure 2.2: General distributed equivalent circuit of a MIS line.

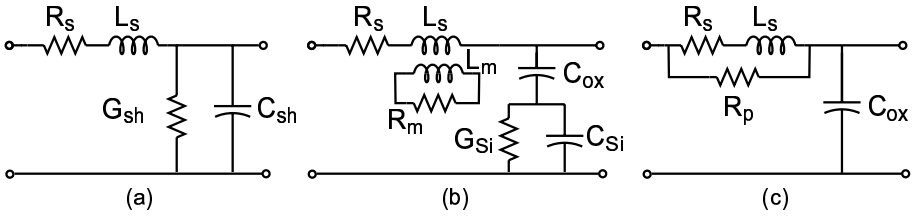


Figure 2.3: Distributed circuit associated with the (a) Quasi-TEM, (b) skin effect and (c) slow-wave propagation modes in a MIS line.

· the *skin effect* mode.

For a given substrate, the presence or not of one propagation mode is largely dependent on the frequency of the applied signal and the resistivity of the silicon substrate. This is briefly described in the following sections, in which, for a better view of the physics behind each mode, a distributed model is proposed and derived from the general, intuitive model of the MIS MS line presented in 2.2 [19].

2.2.1.1 Quasi-TEM mode

The Quasi-TEM mode appears when the product of the frequency by the resistivity (ρ_{Si}) of the Si substrate is large enough so as to produce a small loss angle [7]. For a given silicon substrate, this occurs when the frequency is higher than the Si dielectric relaxation frequency (f_e):

$$f_e = \frac{1}{2\pi\rho_{Si}\epsilon_{Si}} \tag{2.1}$$

where ϵ_{Si} is the dielectric permittivity of silicon. In that case, displacement currents dominate over conduction currents inside the substrate, which behaves like a homogeneous lossy dielectric [20]. The line distributed circuit becomes the one presented in Figure 2.3a, with $G_{sh} = G_{Si}$ and $C_{sh}^{-1} = C_{Si}^{-1} + C_{ox}^{-1} \simeq C_{Si}^{-1}$.

2.2.1.2 *Skin effect mode*

When the product of the frequency by the Si conductivity (σ_{Si}) is large, the skin depth inside the Si substrate may become smaller than the substrate thickness. In that case the substrate behaves like a lossy conductor suffering from the well known *skin effect*. That is, longitudinal electric fields exponentially decay across the Si substrate.

A major characteristic of this mode is its highly dispersive behavior, the skin depth (δ) being inversely proportional to the square root of f:

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma_{Si}}} \tag{2.2}$$

in which μ represents the magnetic permeability of the metal. Thus, as the frequency increases the effective thickness (δ) of the lossy substrate is reduced and its proximity to the metallic conductors is augmented. This leads to an increase of the series resistance associated with longitudinal currents inside the substrate. Besides, the presence of a ground plane close to the metallic strip prevents magnetic fields from penetrating inside the substrate [13], thereby producing a mirror inductor which reduces the value of the total lineic inductor. To account for these effects, the equivalent distributed circuit proposed in [21] and reproduced in Figure 2.3b includes a coupled mirror (L_m) inductor in series with an additional substrate resistance (R_m).

2.2.1.3 *Slow wave mode*

According to [7], the third mode appears when f is not so large and ρ_{Si} is moderate. In that case, conduction currents dominate over displacement currents inside the Si substrate and a strong Maxwell-Wagner interfacial polarization occurs at the SiO_2/Si interface [22]. The total line capacitance becomes equal to C_{ox} (Figure 2.3c), thereby significantly increasing the effective permittivity of the structure and reducing the wave velocity. For this reason, this propagation mode is referred to as the *slow wave* mode. For such mode, the skin effect is usually unimportant and the magnetic field freely penetrates inside the substrate. The field distribution is therefore similar to the one found in non magnetic insulating substrates [23] and so is the line series inductor. However, longitudinal currents in the lossy substrate must still be considered for an accurate description of the mode. These currents are commonly represented by a parallel resistance (R_p) in the series element of the distributed equivalent circuit [13, 19, 24] (Figure 2.3c).

Over the past four decades, the slow wave mode has attracted a significant

interest among MMICs designers [13, 15, 24, 25] because it can be easily obtained, exhibit relatively low losses with large slowing factors and demonstrate little dispersion over a broad range of microwave frequencies [13]. A typical application of the slow wave mode is the delay line. It can also be used as an electronically controllable variable phase shifter if the insulator is replaced by a Schottky contact, in which the depletion capacitance is tuned by the application of a DC bias on the line [25, 26].

2.2.2 *The frequency* vs *Si resistivity chart*

As explained in [7], each propagation mode defines a specific region in the f *vs* ρ_{Si} chart. These regions are given in Figure 2.4a in the case of a MIS MS lines for two values of oxide thickness (0.1 and 1 μm) and a 750 μm-thick silicon substrate. They were defined in the graph according to Equation 2.1 and the following expressions:

.

$$f_s = \frac{1}{2\pi}\frac{t_{ox}}{t_{sub}}\frac{1}{\epsilon_{SiO_2}\rho_{Si}} \tag{2.3}$$

where f_s corresponds to the relaxation frequency of the interfacial polarization and coincides with the point where the AC voltage drop across the oxide (v_{ox}) is equal to the one across the silicon (v_{Si}),

.

$$f_\delta = \frac{\rho_{Si}}{\pi\mu_0 t_{sub}^2} \tag{2.4}$$

where f_δ corresponds to the frequency point where the skin depth is equal to the thickness of the silicon substrate. The lower frequency limit of the skin effect mode is however defined as 4 times f_δ, or $\delta = t_{sub}/2$ [7],

.

$$f_{s\delta} = \frac{f_s^2}{f_\delta} \tag{2.5}$$

where $f_{s\delta}$ defines the upper limit of the skin effect mode. Using an additional 0.01 factor ensures that the vertical electric field inside the skin layer can be neglected in comparison with the field across the oxide [7].

To relate this chart with the present status of advanced SOI technologies, an additional region was defined in Figure 2.4a representing the area inside which current analogue SOI applications would typically lie. A ρ_{Si} range from 10 Ω.cm to 10 kΩ.cm and a frequency range from 100 MHz to 100 GHz were simultaneously

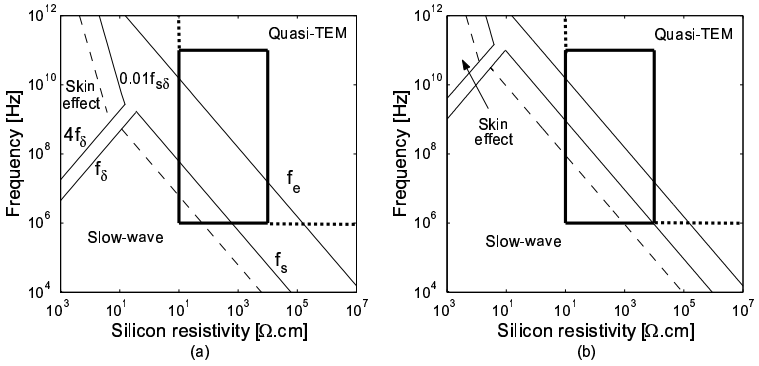


Figure 2.4: Frequency νs resistivity chart outlining the different regions of operation for a MIS MS (a) and CPW (b) lines with t_{ox} = 0.1 (dashed) or 1 (solid lines) μm and t_{sub} = 750 μm.

considered. This region of interest is also included in Figure 2.4b, which is identical to Figure 2.4a but which was adapted to CPW lines by analytically assuming a closer proximity of the ground plane to the signal line. For a typical CPW line with a 20 μm spacing between the central and and ground conductors an average 50 μm t_{sub} was considered in Eqs. 2.3 and 2.4.

On the basis of Figures 2.4a and b, several observations can be made:

- The figures clearly indicate that in current applications of SOI for MMICs, the skin effect propagation mode should not be encountered. This is true, regardless of the line topology, the oxide thickness and the substrate resistivity.

- For MMICs operating in the several GHz region on standard resistivity substrates, the propagation mode lies in the transition region between the slow-wave mode and the Quasi-TEM mode. As shown later in this work, this region presents high losses and is very dispersive.

- However, MMICs working in the same frequency range on high resistivity substrates (10 kΩ.cm) already operate in quasi-TEM mode and do not suffer from dispersion issues.

It therefore appears that the use of high resistivity silicon substrates for RF applications presents the major advantage, besides the well-known strong loss reduction, of only generating the Quasi-TEM propagation mode. It is worth recalling at this point that for such mode the composite SiO_2/Si double layer behaves like a purely homogenous substrate, thereby strongly simplifying substrate modeling

issues as well as the work of circuit designers [27]. However, the use of high resistivity silicon as a microwave substrate also raises other issues, which are be discussed in the next paragraph.

2.2.3 Main issues occurring when using HR SOI substrates in MMICs

HR Si substrates have now been considered to be suitable for MMIC applications for approximately two decades, due essentially to their low loss behavior [3, 4]. However, in SOI CMOS technology a major source of concern with regards to the use of HR silicon substrates is to maintain a high value of ρ_{Si}, which is not so trivial due to the semiconductor nature of such substrate. Indeed, when HR SOI wafers are used the resistivity of the Si substrate can be largely affected by:

- the CMOS process endured by the wafer: nominal values of substrate resistivity close to 10 kΩ.cm are now commonly achieved, which corresponds to a level of p-type impurities of 1.3x10^{13} $/cm^3$ or lower (Figure 2.5). This is at least 4 orders of magnitude lower than typical MOSFETs doping levels, which are fabricated above the covering oxide. As a consequence, a particular care must be provided while processing the devices in order to prevent contamination with doping impurities at the substrate surface. In the case of passive structures, one may reasonably expect some specific process steps other than dopant implantation to be also a source of direct substrate contamination, such as for instance plasma etching. This possible source of resistivity degradation, though of primary concern for chip makers on HR silicon substrates, will not be investigated in this work.

- the surface potential of the silicon substrate (ϕ_S), corresponding to the electrostatic potential at the SiO_2/Si interface: assuming a uniformly (low) doped Si substrate, this potential is null under flatband condition and so is the electric field. In that case only, the substrate surface is neutral and free carriers are equally distributed inside the substrate. However, when the substrate potential is shifted to either positive or negative values, a space charge region is formed near the substrate surface. According to the nature of the substrate doping and the sign of ϕ_S, either an accumulation, a depletion and/or an inversion layer can be formed underneath the oxide layer [28]. While a depletion layer tends to locally increase the substrate resistivity, this parameter behaves very differently when the substrate surface is either inverted or accumulated. Indeed, apart from turning the Si into a highly inhomogeneous substrate, an inversion or accumulation layer underneath the oxide can also drastically reduce the value of resistivity near the substrate surface.

The effects of surface potential and space charges on the RF properties of MIS lines have been investigated by several authors [29], [30, 31], who all proposed an analytical model based on the combination of semiconductor transport and Maxwell's field equations. However, mainly for simplicity reasons, the authors were forced to restrict their analysis to the simpler case of MS line geometries. Besides, in those works only moderate (or high) substrate doping levels (i.e. $>1\text{x}10^{15}\ /cm^3$) were considered, corresponding to resistivity values lower than 10 Ω.cm. Yet, when a thin, highly conductive layer is formed at the top of a HR substrate one may expect that its influence on substrate losses largely differ from the MS to the CPW structure for one essential reason: electric field lines are mostly vertical (i.e., perpendicular to the SiO_2/Si interface) inside the MS line while they run mostly horizontally (i.e., parallel to the SiO_2/Si interface) inside the coplanar waveguide. This particular point is addressed in the coming section, in which we propose to investigate and compare the effect of ϕ_S and the impact of a low resistivity layer underneath the oxide on substrate losses for the two line topologies of interest. It is shown that, due mainly to their different electric field configurations, both structures exhibit substantially different behaviors.

2.2.4 Loss mechanisms: CPW vs *MS*

2.2.4.1 Electric field distributions - IE3D simulations

In order to assess the impact of parasitic surface conduction below the oxide in both MS and CPW MIS structures, numerical simulations were first performed with a field solver. As shown below, these simulations provide an accurate tool to describe the electric field distribution inside the silicon substrate for the two line topologies. The IE3D software from Zeeland was used and the simulations were made for two values of substrate resistivity (20 Ω.cm and 2 kΩ.cm) and two different frequencies (1 and 21 GHz).

For the standard resistivity substrate (20 Ω.cm) it is known from the frequency-resistivity chart presented in Section 2.2.2 that the propagation mode is not clearly defined. The operation point lies indeed in the transition region between the slow-wave and the quasi-TEM dielectric mode, i.e., when interfacial polarization is still present. In that case the most adequate equivalent circuit to model the substrate behavior consists in the shunt elements of Figure 2.3b: C_{ox} in series with the parallel combination of G_{Si} and C_{Si}. This circuit indeed considers the Maxwell-Wagner interfacial polarization effect [22], which turns the equivalent shunt capacitance (G_{sh}, Figure 2.6) and conductance (C_{sh}) into highly frequency-dependent parameters, as shown in Figure 2.7 for the case of the MS line and two values of ρ_{Si}. In

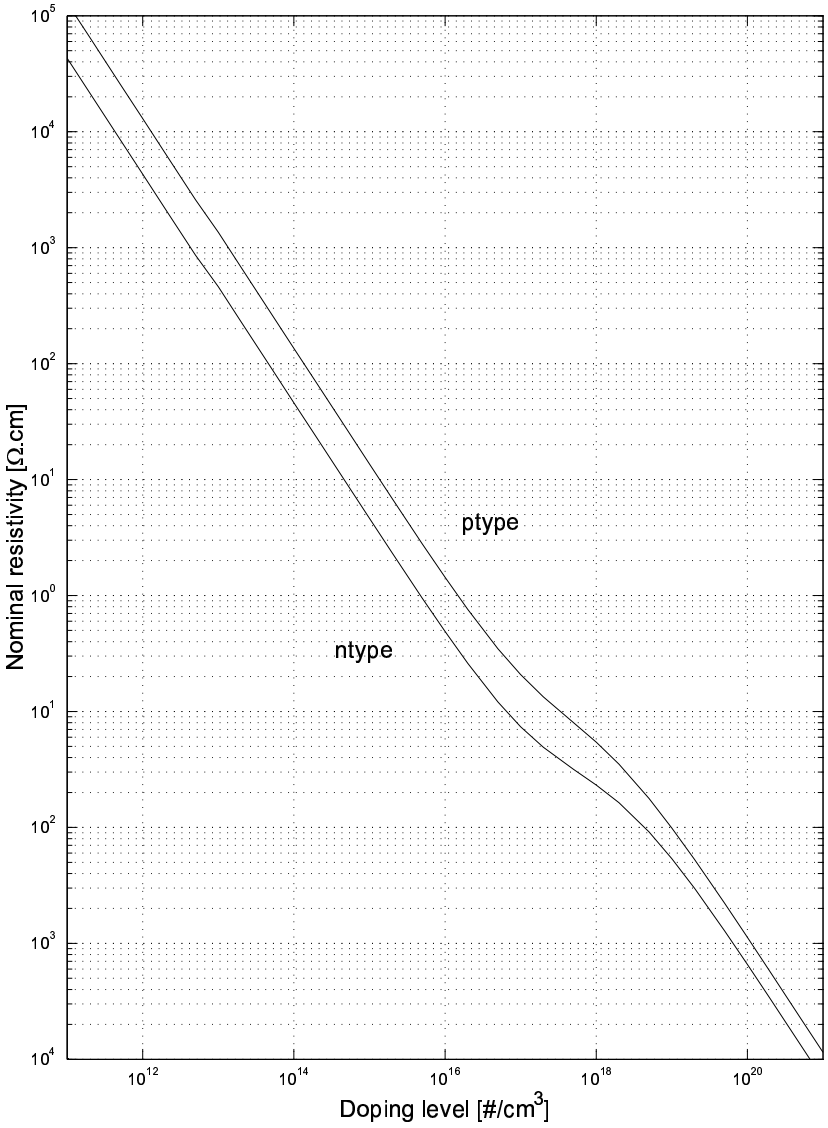


Figure 2.5: Silicon resistivity as a function of dopant concentration [32].

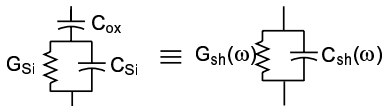


Figure 2.6: Shunt elements of the distributed equivalent circuit of MIS structures considering the Maxwell-Wagner effect.

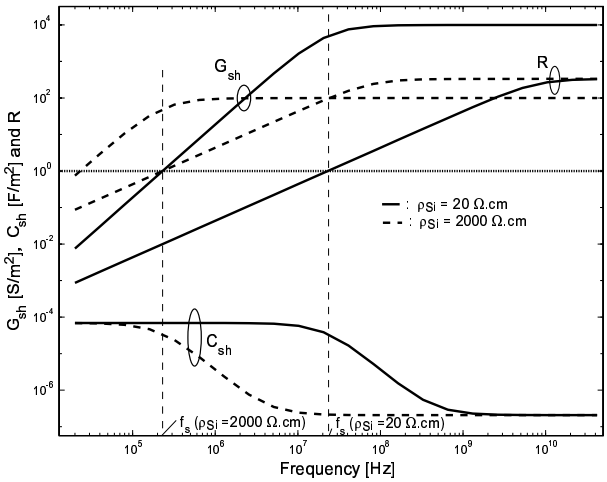


Figure 2.7: Frequency behavior of C_{sh}, G_{sh} and $R = \nu_{Si}/\nu_{ox}$ in the case of a MIS MS structure for two different values of substrate resistivity.

this figure, the effect of space charge at the Si/SiO_2 interface was voluntarily and momentarily ignored. It is to be noted that the shape of these curves are expected to be identical in the case of CPW lines (though not displayed) because the CPW distributed equivalent circuit is similar to that of MS lines.

Figure 2.7 also displays the variations of the ratio $R = \nu_{Si}/\nu_{ox}$ versus frequency for the MS structure, where ν_{Si} and ν_{ox} are the voltage across the silicon substrate and the oxide layer, respectively. R is therefore directly related to the Maxwell-Wagner effect. As explained earlier, R becomes equal to unity when f is equal to f_s, the relaxation frequency of interfacial polarization. In more physical terms, this means that for $f \geq f_s$ electrical fields present inside the structure do not remain confined inside the oxide layer but start spreading across the substrate.

Simulation results obtained with IE3D agree quite well with the predictions made by Figure 2.7 as illustrated in Figure 2.8, which compares the electric field

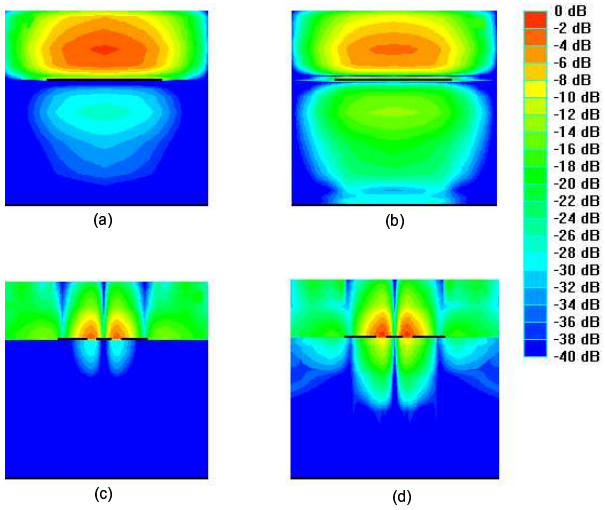


Figure 2.8: Field distribution for both MS ((a) and (b)) and CPW ((c) and (d)) lines at 1 ((a) and (c)) and 21 ((b) and (d)) GHz and for a standard value of substrate resistivity.

intensities in a MS and a CPW structure for a Si resistivity of 20 Ω.cm at 1 and 21 GHz. For the studied MS line the central conductor width is W=430 μm. For the CPW line the central conductor width (W_s), the lateral ground plane width (W_g) and the spacing between the conductors (S) are respectively 24, 106 and 40 μm. For both structures the thickness of the silicon substrate is 500 μm. In Figure 2.8 the vertical and horizontal components of the transverse fields are represented in the MS and CPW figures, respectively. Fig. 2.9 pictures the same simulation results in the case of the high-resistivity substrate. The combination of the two figures indicates that the electric fields penetrate deeper in the substrate at 21 GHz than at 1 GHz when its resistivity is low. This is true for both structures and is due to the fact that the value of R is much smaller at 1 than at 21 GHz for ρ = 20 Ω.cm (Figure 2.7).

On the other hand, the distribution of the field lines is more or less identical for the two frequencies of interest in the case of the high resistivity substrate because the value of R does not change between both frequencies. However, the most important feature of the field distribution is the following: regardless of the frequency and the substrate resistivity, it appears from a simple comparison of the

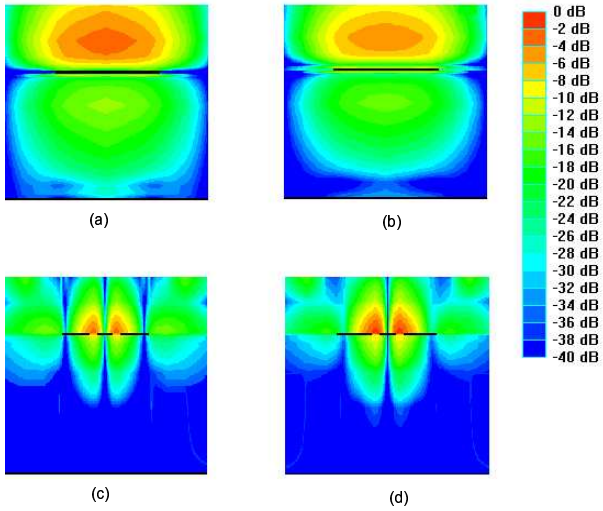


Figure 2.9: Field distribution for both MS ((a) and (b)) and CPW ((c) and (d)) lines at 1 ((a) and (c)) and 21 ((b) and (d)) GHz and for a high value of substrate resistivity.

figures that the electric fields penetrate much deeper into the substrate of the MS than of the CPW structure. In other words, these simulation data suggest that the field distribution in MS structures is more affected by volume phenomena inside the substrate while they are primarily sensitive to surface changes in the case of CPW structures.

This observation is further supported by additional IE3D simulations, presented in Figure 2.10. In that case, the structures were simulated with an additional low resistivity (ρ = 0.2 Ω.cm) 2 μm-thick layer sandwiched between the SiO_2 layer and the HR Si substrate. The introduction of this layer simulates for instance the presence of an inversion layer induced by fixed oxide charges (Q_f) at zero bias. The thickness and resistivity of this layer were roughly deduced from Atlas simulation, for an arbitrary Q_f value of 3x10$^{10}/cm^2$. The figure clearly demonstrates that at 21 GHz this inversion layer has no effect on the field distribution inside the MS structure: the layer is more or less transparent to the fields. In opposition, the CPW structure appears highly sensitive to this surface layer, which prevents all field penetration inside the substrate even at high (21 GHz) frequency.

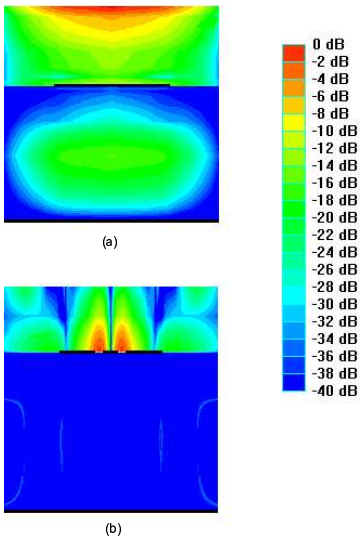


Figure 2.10: Field distribution for both MS and CPW lines at two different frequencies and for HR substrate with an additional low resistive layer underneath the oxide.

2.2.4.2 *Quantitative effect of* V_a *and* Q_f - Atlas simulations

As already pointed out, the main physical parameters contributing to the creation of a low resistivity free carrier layer at the surface in HR substrates are the DC bias applied on the line metallic conductors and the charges inside the oxide. As shown in Figure 2.11 for the CPW line both parameters impact differently on the charge distribution below the oxide, which is simply due to the different location of their field of influence inside the structure. Indeed, applying a DC bias on the conductors can only locally modify the charge distribution below the oxide, i.e. in proximity of the conductors (Figure 2.11a). On the other hand, fixed charges inside the oxide are usually distributed all across the wafer. Significant Q_f values can therefore contribute to create a uniform charge layer at the substrate surface of the entire wafer (Figure 2.11b).

To simulate structures with a discontinuous low resistivity layer below the oxide a full 3-D field solver must be used, at the cost of larger time consumption and higher use of computer resources. An alternate solution consists in using a semiconductor and space charge solver, such as Atlas. This software presents the advantages of requiring only 2D simulations and of performing accurate computations of the charge distribution inside the structure for a given V_a and Q_f set

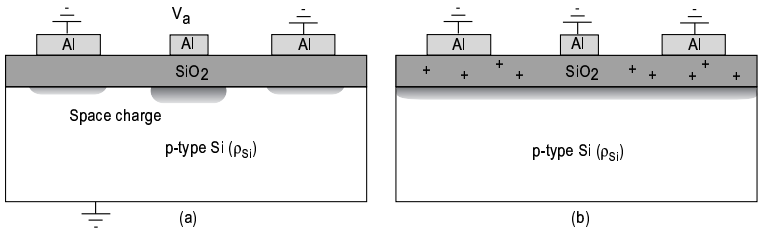


Figure 2.11: Illustration of the inversion layer distribution in the case of a CPW structure fabricated on an oxidized, p-type HR Si substrate with (a) no fixed charges in the oxide and a positive or null DC bias applied on each conductor, and (b) fixed charges in the oxide and a null bias applied on the conductors.

of values. Furthermore, it also computes the small signal AC admittance between each pair of electrodes of the simulated device, thereby providing a direct access to the total shunt conductance (G_{sh}) of our structures. This parameter can be directly related to substrate losses since it is known that for low loss transmission lines we can write:

$$\alpha_{sub} \simeq \frac{G_{sh}}{2}\sqrt{\frac{L_s}{C_{sh}}} \tag{2.6}$$

(where L_s is the line series inductance). In other words, RF substrate losses are directly proportional to G_{sh}.

The simulations were thus performed by considering the simultaneous effect of V_a and Q_f on a p-type substrate. The simulation results are displayed in Figure 2.12a and b for the CPW and the MS structures, respectively, and for f = 10 GHz. The data are plotted as a function of the applied bias as well as for varying Q_f values. Percentage variations are shown to outline the sensitivity of both structures to the studied parameters. In all cases the reference point was considered as the value of G_{sh} at $V_a = 0\ V$ and $Q_f = 0\ /cm^2$.

From this figure, several observations can be made:

- First, it is interesting to notice that the V_a dependence of G_{sh} in both MS and CPW structures exhibits the same trend. For a null value of Q_f (thick lines), losses are largely increased when a strong negative or positive bias is applied. Indeed in those two cases, the surface potential is either highly negative ($V_a < 0$) or positive ($V_a > 0$), thereby attracting a low resistivity accumulation ($V_a < 0$) or inversion ($V_a > 0$) layer at the substrate surface. The increase is however slightly higher when the surface is inverted, probably due to the higher mobility of electrons. Substrate losses reach a minimum value for an applied bias ($V_{a,min}$) corresponding to deep depletion underneath the central line.

- For positive Q_f values, losses become much more pronounced when the surface

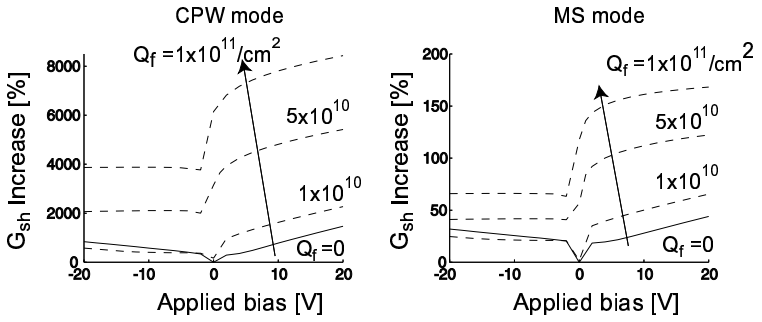


Figure 2.12: Simulated effect of bias and fixed charge densities on G_{sh} for the (a) CPW and (b) MS structures.

is inverted ($V_a > 0$), while their increase is almost insignificant when it is accumulated ($V_a < 0$). This effect is attributed to the impact of Q_f and V_a on the discontinuity of the inversion layer below the oxide. When V_a is positive, the inversion layer covers the entire substrate surface, even below the ground conductors for which the applied bias is 0 V. When V_a is negative, an accumulation layer is formed below the central (or top) conductor, which disrupts the inversion layer and creates a depletion region between the accumulated and inverted zones, i.e., at the conductor edges. This reduces the size of the inversion layer, and also creates highly resistive regions below the oxide. Both effects contribute to a reduction of substrate losses, both in CPW and MS structures. For the latter, the large impact of the inversion layer discontinuity on G_{sh} is probably related to the horizontal electric field components associated with edge and field line curving effects.

- The figure also clearly outlines the much higher impact of space charge distributions below the oxide in the case of the CPW structure than in the case of the MS structure. This could be expected from the results of field distribution computed with the field solver, which highlighted a higher sensitivity of the CPW line to surface resistivity variations. It is seen in Figure 2.12 that applying a highly positive bias (20 V) on the top conductor of the MS line leads to a substrate loss increase close to 40 % while applying the same bias on the central conductor of the CPW structure multiplies losses by a factor close to 10.

- Finally, Figure 2.12a indicates that G_{sh} increases (and so does α) when fixed charges are present inside the insulating oxide layer since, as already discussed, these charges lead to create an inversion layer everywhere below the oxide. As

the thickness of this inverted layer is an increasing function of the oxide charge density; G_{sh} is an increasing function Q_f for a given value of V_a. Again, it is interesting to notice that the influence of Q_f is much heavier on the shunt conductance of the CPW than on the MS structure. It is also seen in the figure that the value of $V_{a,min}$ is reduced when Q_f is increased, which further contributes to increase substrate losses at $V_a = 0$V. This effect is simply related to a reduction of the threshold voltage as Q_f is increased [33].

2.2.4.3 Experimental results

In order to confirm the trends and observations outlined by the simulated data, the comparison between the MS and the CPW structures was also performed using experimental structures that were fabricated on four distinct HR wafers, two of which carrying the CPW lines and the other two supporting the MS structures. Both the CPW and MS lines had the same cross dimensions as the structures simulated in the previous section. In the case of CPW1 and CPW2, the lines were made on thermally oxidized HR SOI and HR bulk wafers, respectively. The backside BOX/Si interface of the SOI wafer presenting a very high (industrial level) quality, Q_f is therefore expected to be higher for the home-oxidized bulk wafer. In the case of the MS lines, both wafers were HR bulk wafers. A Q_f-rich, 300 nm-thick oxide was deposited by Atmospheric Pressure Chemical Vapor Deposition (APCVD) for MS3 and the oxide layer was thermally grown in the case of MS4.

For all wafers, the lines were measured from 40 MHz to 40 GHz by applying a DC bias (V_a) on the central (CPW) or top (MS) conductor and grounding the substrate in order to sweep the surface potential from negative to positive values. The line propagation constant (γ) was extracted from the measured S-parameters with a classical Thru-Line-Reflect (TLR) method. Total losses inside the structures (α) were then simply obtained by $\alpha = Re(\gamma)$.

Figure 2.13a displays the losses as a function of the applied voltage at an arbitrary frequency of 10 GHz for CPW1-2. The curves exhibit the same trend in all the measured frequency range. Not surprisingly, it is seen that losses are dramatically increased when a strongly positive bias is applied on the line central conductor. However, a significant loss increase is also outlined for highly negative values of V_a. Though not as important as for positive V_a values, this increase is much higher than the one observed in Figure 2.12a and may be due to an underestimation by Atlas of the contribution of the accumulation layer to substrate losses. Figure 2.13a also indicates that the value of $V_{a,min}$ is lower for CPW2 than for CPW1. As explained earlier, this is simply due to the more important Q_f value in the case of

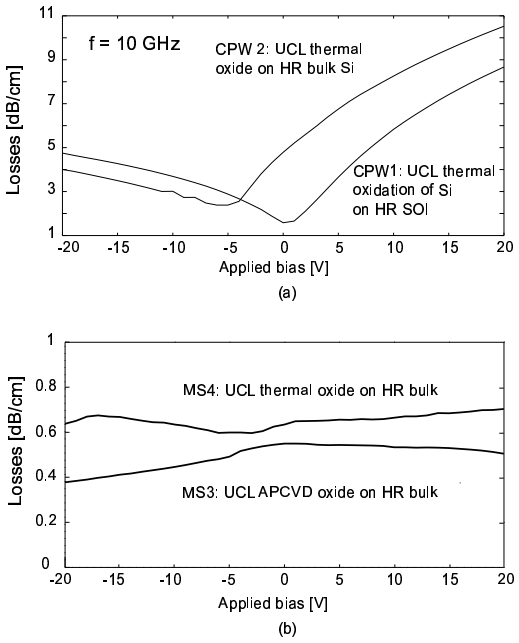


Figure 2.13: Effect of DC bias on RF losses of a MIS CPW (a) and MIS MS (b) lines for two types of oxide quality.

CPW2, which resulted here in three times higher losses at 0 V compared to CPW1.

The measurements performed on the MS lines are presented in Figure 2.13b and we can see in that case that the attenuation constant only slightly varies with respect to the applied bias for both types of oxide layers. This is in very good agreement with the simulation results presented in Figure 2.12b, which outline a much smaller V_a dependence in the case of the MS lines. The relative variations of α remain lower than 0.2 dB for both MS3 and MS4 throughout the entire bias range while CPW1-2 measurements exhibit loss variations higher than 7 dB at 10 GHz.

2.2.4.4 Conclusion

CPW losses are much more sensitive to the presence of a thin, poorly resistive layer underneath the oxide than MS lines. As shown by numerical field computation, this is because electric fields are primarily tangent to the SiO_2/Si interface in CPW structures while they are perpendicular to the same interface in MS lines.

Table 2.1: Published experimental data of CPW losses measured at 20 GHz on HR substrates. Data are provided for classical MIS CPW configurations in the upper part of the table and for improved structures in the lower part of the table (*NA stands for "not available").

Ref.	classical	improved	ρ_{Si} [Ω.cm]	Metal	T_{met} $[\mu m]$	W_s $[\mu m]$	S $[\mu m]$	α_{tot} **[dB/cm]**
[35]	⊠	□	10k	Al	1.3	70	40	**17.2**
[34]	⊠	□	10k	Al	1	20	10	**3.5**
[36]	⊠	□	3k	NA*	4	50	25	**8**
[35]	□	⊠	10k	Al	1.3	70	40	**2.8**
[35]	□	⊠	10k	Al	1.3	70	40	**0.8**
[34]	□	⊠	10k	Al	1	20	10	**2.25**
[36]	□	⊠	3k	NA	4	50	25	**1.9**
[36]	□	⊠	3k	NA	4	50	25	**1.4**

This observation can therefore be extended to any type of coplanar devices, having essentially horizontal field lines. This particular feature of coplanar devices also means that CPW lines appear as convenient structures to characterize the insulator/semiconductor interface in multilayer substrates. This point has actually been exploited by previous authors ([34]), who have used CPW structures to measure the dielectric constant of thin layer materials. In our case, the sensitivity of CPW losses to the presence of free charges at the buried SiO_2/Si interface of HR SOI substrates indicates that CPW could provide a handy tool to characterize the quality of that interface, and thus the quality of the substrate itself. As explained in the coming section, this is performed in this work by defining a new quantity called *effective resistivity*.

2.3 CPW as a tool to characterize HR oxidized Si and HR SOI substrates

2.3.1 The need for an effective resistivity

The influence of parasitic surface conduction at the substrate surface in oxidized HR bulk or HR SOI substrates has already been outlined in several works [4–6, 27, 34–36]. In some of the works the authors proposed innovative solutions to suppress the influence of surface charges and reduce RF losses. Those substrate-based solutions are described and discussed in the next chapter. Table 2.1 reports the loss reduction obtained using several of those techniques.

The point developed in this section is based on the following observation: even if a clear improvement can be obtained by reducing parasitic surface conduction,

assessing and comparing the efficiency of the proposed technological solutions between one work and another is not so trivial. Indeed, for all works reported in Table 2.1 the authors quantify the improvements provided by their novel concepts through a comparison of total RF losses (α_{tot}) obtained on CPW lines. Those data therefore include conductor losses (α_{cond}), which become dominant when dealing with high resistivity silicon substrates. The contribution of substrate (α_{sub}) losses to total losses may therefore be sometimes substantially masked by conductor losses. Besides, conductor losses critically depend on the type of metal used and the geometry of the CPW structure, which as shown in Table 2.1, can significantly vary from one paper to the other. As a consequence, it is not possible to directly extract the RF characteristics of the substrates in the innovative works of [34–36] and, thus, to fully qualify the efficiency of their method.

This is why we propose here a newly developed technique to characterize the performance of the substrate only, based on RF CPW measurements. The method relies on the definition of a new factor of merit called *effective resistivity* (ρ_{eff}), which represents the "equivalent" resistivity of a particular substrate and which includes the effect of charge distribution at the substrate surface. A technical definition as well as a method of extraction from both experimental and simulated CPW structures are given in the following section.

2.3.2 Effective resistivity extraction from CPW measurements and simulation data

The shunt distributed elements of the CPW structure on an oxidized Si substrate including surface charges are presented in Figure 2.14a. They classically consist in a combination of C_{oxGND}, C_{oxSIG}, C_{air}, C_{Si} and G_{Si}. For the case of very thick oxides, the transverse oxide capacitance becomes non negligible and must therefore also be considered (C_{oxTRAN}). The effect of surface charges on the structure is assumed to be included in Y_{surf}. The presence of surface charges might for instance be related to a DC bias applied on the metallic conductors.

It is clear that the silicon substrate presented in Figure 2.14a is highly inhomogeneous, due partly to the insulating oxide but also due to the surface charges. For this reason the equivalent shunt capacitance (C_{sh}) and conductance (G_{sh}) presented in the inset of Figure 2.14a are frequency dependent.

In order to compare the substrate properties of distinctly processed wafers or wafers biased under different conditions, we decided to model the passivated, *inhomogeneous* Si substrate with an effective *homogeneous* Si substrate (Figure 2.14b) characterized by a uniform dielectric constant ($\epsilon_{r,Si}$=11.7) and uniform re-

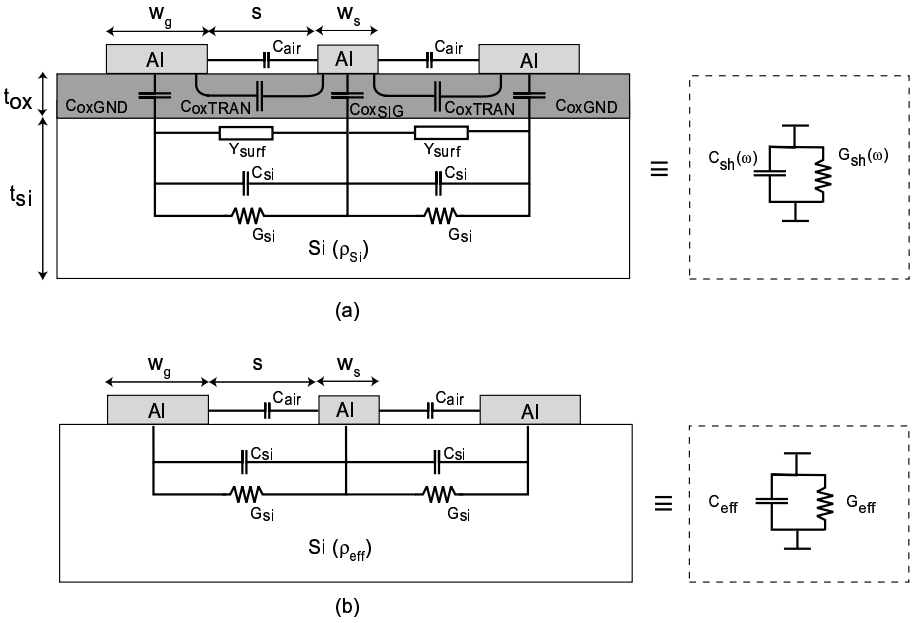


Figure 2.14: CPW structure on (a) an oxidized substrate including surface charges and (b) effective homogeneous substrate used for ρ_{eff} modeling.

sistivity (i.e., with no space charge effects), called *effective resistivity* (ρ_{eff}). In this structure, the value of ρ_{eff} is such that *the effective substrate has identical RF losses as the inhomogeneous, oxidized wafer* (i.e., $\alpha_{inh} = \alpha_{eff}$). Its extraction is based on the simplified model of the physical substrate presented in the inset of Figure 2.14a (C_{sh} // G_{sh}).

For frequencies higher than several tens of MHz and for CPW lines made on oxidzed HR Si substrates the quasi-TEM mode is dominant (Figure 2.4b). As explained earlier, RF substrate losses can then accurately be estimated using :

$$\alpha_{inh} \approx \frac{G_{sh}}{2}\sqrt{\frac{L}{C_{sh}}} \tag{2.7}$$

Obviously, this is also true for the effective structure which propagates the quasi-TEM mode only. We can therefore write:

$$\alpha_{eff} \approx \frac{G_{eff}}{2}\sqrt{\frac{L}{C_{eff}}} \tag{2.8}$$

As both structures are composed of non magnetic materials and made with metallic conductors of similar geometry, the values of their lineic inductance (L_s) are assumed to be equal. Considering that substrate losses are also equal in both structures, 2.7 and 2.8 yield:

$$G_{eff} = G_{sh}\sqrt{\frac{C_{eff}}{C_{sh}}} \tag{2.9}$$

where C_{eff} and G_{eff} are associated with the homogeneous substrate, and are therefore given by:

$$C_{eff} = \epsilon_{r,eff}C_0 = (1 + q(\epsilon_{r,Si} - 1))C_0 \tag{2.10}$$

$$G_{eff} = q\frac{C_0}{\epsilon_0\rho_{eff}} = \left(\frac{\epsilon_{r,eff} - 1}{\epsilon_{r,Si} - 1}\right)\frac{C_0}{\epsilon_0\rho_{eff}} \tag{2.11}$$

In these equations q, $\epsilon_{r,eff}$ and C_0 are the filling factor, the relative dielectric constant and the air-filled capacitance of the effective structure, respectively. Accurate close-forms analytical expressions that include metal thickness and finite ground plane width dependence are given by Heinrich in [37] for $\epsilon_{r,eff}$ and C_0. The effective resistivity of the substrate can now be extracted by combining (2.9) and (2.11):

$$\rho_{eff} = \frac{1}{\sqrt{\epsilon_{r,eff}}}\left(\frac{\epsilon_{r,eff} - 1}{\epsilon_{r,Si} - 1}\right)\frac{\sqrt{C_0}}{\epsilon_0}\frac{\sqrt{C_{sh}}}{G_{sh}} \tag{2.12}$$

In this last expression, G_{sh} and C_{sh} refer to the inhomogeneous structure and can

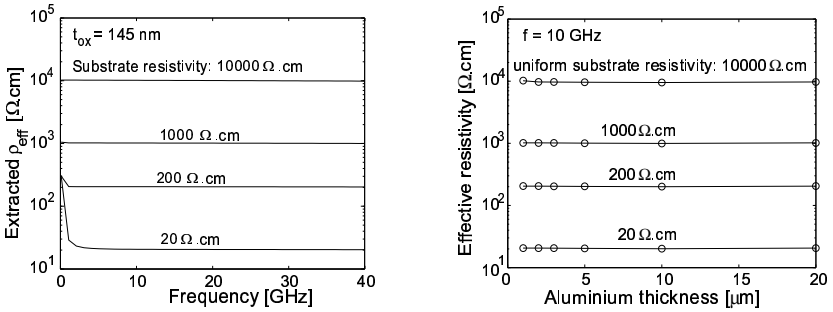


Figure 2.15: Effective resistivity values extracted from simulated data obtained with the variational principles-based method developed in [38] as a function of f (a) and as a function of t_{Al} (b) for various ρ_{Si} values. The physical parameters of the CPW structure are $W_s = 40\ \mu m$, $S = 24\ \mu m$, $W_g = 206\ \mu m$ and $t_{ox} = 150\ nm$.

be obtained from either simulation or measurements. Simulated data obtained on a quasi homogeneous structure used next to demonstrate the validity and the accuracy of the extraction method. The method is then be applied on measurement and additional simulation results to extract the effective resistivity as a function of various technological and geometrical parameters.

2.3.3 Accuracy of the method

In order to test the validity of the proposed ρ_{eff} extraction method, simulations were first performed on simple CPW structures made on oxidized silicon substrates with uniform resistivity, i.e. excluding space charge effects. The substrate resistivity and the thickness of the metal conductors were both varied. The oxide layer thickness was set to a negligible value (i.e., $t_{ox} \ll W_s$ and $t_{ox} \ll S$), so that its effect on the substrate conductance (G_{sh}) could be ignored. The simulated data were obtained with a variational principles-based technique, which offers a fast and convenient method to simulate multilayer coplanar structures [38]. The method indeed provides a direct access to the frequency-dependent *RLCG* parameters of the line.

The ρ_{eff} data extracted from the simulated structure are presented in Figure 2.15a for a CPW line with $W_s = 40\ \mu m$, $S = 24\ \mu m$, $W_g = 206\ \mu m$, $t_{Al} = 1\ \mu m$ and $t_{ox} = 150\ nm$. In this first set of simulations, the substrate resistivity (ρ_{Si}) was varied from 20 Ω.cm to 10 kΩ.cm. It is seen that all curves start from a high value in the low frequency range and reach a plateau level at higher frequencies. This particular trend is simply due to the polarization of the SiO_2/Si interface,

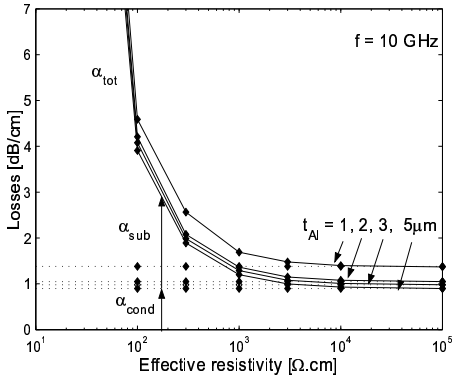


Figure 2.16: Total, conductor and substrate losses of a CPW line with a nominal geometry of $t_{Al} \simeq 1\ \mu m$, $\sigma_{Al} \simeq 3.5\text{x}10^7\ S/m$, $W_c = 40\ \mu m$, $S = 24\ \mu m$ and $W_g = 206\ \mu m$ as a function of the silicon substrate effective resistivity.

which tends to increase the effective dielectric constant of the structure at lower frequencies. This effect gradually disappears as f increases and is completely gone when $f > f_e$. It is therefore substrate resistivity-dependent, as the figure shows.

An important feature outlined by Figure 2.15a is that regardless of the substrate resistivity, the extracted ρ_{eff} closely agrees with the specified ρ_{Si} values. A closer look at the data indeed reveals that the accuracy range lies between 1 and 2 %, supporting the statement that the method is fairly accurate. Additional simulations were also performed by varying the thickness of the CPW line Aluminium conductors (t_{Al}) for different ρ_{Si} values. The results are plotted in Figure 2.15b at an arbitrary frequency of 10 GHz. Barely no variations (within 5 %) of the extracted ρ_{eff} values are observed with respect to t_{Al}, for all values of ρ_{Si}. These results correspond to what should be expected since G_{sh} is physically unaffected by a change in conductor thickness. This further demonstrates the validity and the reliability of the proposed extraction method. It can therefore be safely applied on real or modeled structures in which space charges effects near the SiO_2/Si interface are included.

2.4 Effective resistivity targets

Before analyzing the different factors that can affect the effective resistivity of high resistivity substrates it is important to have an idea of the target value required for the effective resistivity, above which substrate losses can be considered as

insignificant. In the case of CPW lines, that analysis must be performed by dissociating the relative contributions of the substrate and of the metallic conductors to total losses. These contributions are outlined in Figure 2.16 for our nominal geometry, i.e. with $t_{Al} \simeq 1\ \mu m$, $\sigma_{Al} \simeq$3.5x10^7 S/m, $W_c = 40\ \mu m$, $S = 24\ \mu m$ and $W_g = 206\ \mu m$. In this figure, conductor (α_{cond}) and substrate losses (α_{sub}) were respectively computed using analytical formulas developed in [37] and the variation principle method developed in [38]. The figure represents α_{cond}, α_{sub} and total losses ($\alpha_{tot} = \alpha_{sub} + \alpha_{cond}$) as a function of the substrate resistivity for our nominal line geometry. The simulation results indicate that substrate losses are significantly reduced for ρ_{eff} values higher than 1 kΩ.cm. However, they still amount to 23 % of total losses at ρ_{eff} = 1 kΩ.cm and are reduced to less than 8 % of α_{tot} when ρ_{eff} is higher or equal to 3 kΩ.cm. This number is further reduced for higher ρ_{eff} and becomes clearly insignificant when ρ_{eff} reaches 10 kΩ.cm. As experimentally demonstrated in [39] on the basis of CPW loss measurements, Si substrates behave as quasi-lossless if their resistivity is close to 3 kΩ.cm. The present analysis fully agrees with this anterior result. It will therefore be arbitrarily considered in the rest of this work that a given HR substrate is *quasi-lossless* if its effective resistivity obeys 3 kΩ.cm≤ ρ_{eff} <10 kΩ.cm and is *lossless* if ρ_{eff} ≥10 kΩ.cm.

2.5 Factors affecting the effective resistivity of HR SOI substrates

As explained earlier, the RF losses of CPW lines made on HR Si substrates are expected to be largely influenced by the surface potential of the silicon substrate, which governs the charge distribution at the SiO_2/Si interface. From this observation it can be anticipated that all factors affecting the surface potential in HR SOI wafers might be considered as a possible source of resistivity degradation near the substrate surface. The surface potential in MIS structures is governed by the potential balance equation [28]:

$$V_a = \phi_S + \frac{W_{MS}}{q} - \frac{Q_f}{C_{ox}} - \frac{Q_s(\phi_S)}{C_{ox}} - \frac{Q_{it}(\phi_S)}{C_{ox}} \tag{2.13}$$

in which W_{MS} is the metal-semiconductor work function difference, Q_s [$/cm^2$] is the charges in the silicon and Q_{it} [$/eV/cm^2$] is the interface trapped charge. Those two last entities are respectively given by:

$$Q_s(\phi_S) = \pm\sqrt{2\epsilon_s q N_A}\Big\{\frac{kT}{q}e^{-q\phi_S/kT} + \phi_S - \frac{kT}{q} + e^{-2q\phi_F/kT}\left(\frac{kT}{q}e^{q\phi_S/kT} - \phi_S - \frac{kT}{q}\right)\Big\}^{0.5} \tag{2.14}$$

and

$$Q_{it}(\phi_S) = q\int_{E_v}^{E_c}\Big\{\left[1 - f_0(E - q\phi_S - q\phi_F)\right]D_{it}^d(E - q\phi_S) - f_0(E - q\phi_S - q\phi_F)D_{it}^a(E - q\phi_S)\Big\}\,dE \tag{2.15}$$

in which E_c and E_v are respectively the conduction and valence band edges, $f_0(E)$ is the Fermi function, D_{it}^a and D_{it}^d are respectively the acceptor and donor traps and ϕ_F is the Fermi potential inside the substrate. It can be seen from those expressions that the main factors affecting the value of ϕ_s are

1. W_{MS}: the difference between the metal (W_M) and the silicon substrate (W_S) work functions, the latter depending on its doping level,
2. Q_f: fixed charges in the oxide layer,
3. V_a: the applied bias,
4. t_{ox}: the oxide thickness,
5. Q_{it}: the amount of trapped charges at the SiO_2/Si interface, which is itself largely dependent on the interface trap densities D_{it}^a and D_{it}^d,
6. T: the substrate temperature, which affects the substrate Fermi potential.

The impact of each factor on the value of ρ_{eff} is separately quantified and discussed in the coming sections. The analysis is based on experimental and simulated data obtained with Atlas. As explained earlier, this software first performs a static analysis of the charge distribution, thereby accounting for the simultaneous effects of all technological (N_a, t_{ox}, W_{MS}, Q_f, D_{it}) and external (V_a, T) parameters on the charge distribution inside the MIS structure. It then goes on with an AC computation of the small signal conductance and capacitance between each pair of electrode in the structure by linearizing the DC solution. It therefore provides a convenient tool to simulate the effects of those parameters on the shunt elements (G_{sh} and C_{sh}) of the CPW line, and thus on ρ_{eff}. Unless otherwise stated, the dimensions of the investigated CPW structures correspond to those of the line

studied in the previous sections, i.e. with $t_{Al} = 1\ \mu m$, $W_s = 40\ \mu m$, $S = 24\ \mu m$ and $W_g = 206\ \mu m$. These dimensions correspond to those of Set b. When mentioned in later sections, Set a, Set c, Set d and Set e refer to the geometries given in Table 2.2.

Table 2.2: Dimensions (in μm) of the CPW lines studied in this work.

	W_s	S	W_g	t_{Al}
Set a	18	38	206	1
Set b	24	40	206	1
Set c	12	26	206	1
Set d	36	56	206	1
Set e	5	10	206	1

2.5.1 Work function difference

2.5.1.1 Effect of work function difference on surface charges

The effect of metal work function on the charge distribution at or near the insulator/substrate interface in a MIS structure is usually analyzed using the concept of *band diagrams* [28, 32, 33]. Classically, a band diagram presents energy levels for electrons as a function of x, the direction perpendicular to the substrate surface. Such a diagram is shown in Figure 2.17a for the case of a metal/p-type Si system in which both materials are completely isolated from each other. It can be seen in this figure that the material *work functions* have been represented. For a given material, the work function is defined as the energy that must be provided to an electron to set it free in vacuum. It is therefore given by:

$$W_M = E_0 - E_{FM} \tag{2.16}$$

where E_0 denotes the vacuum energy level, and E_{FM} the average energy of electrons inside the metal electrode. For the Si substrate, we similarly have:

$$W_S = E_0 - E_{FS} \tag{2.17}$$

In CMOS technologies, the metals that are the most commonly used to form interconnects (and thus RF circuitry) are aluminium (Al) and copper (Cu). However both materials are usually not used as such, and are surrounded by a barrier layer of titanium (Ti), tantalum (Ta) or, more classically, one of their nitrides (TiN and TaN). This additional layer is necessary to prevent aluminium spiking into the Si substrate or the drifting of copper atoms into interlayer dielectrics. It also

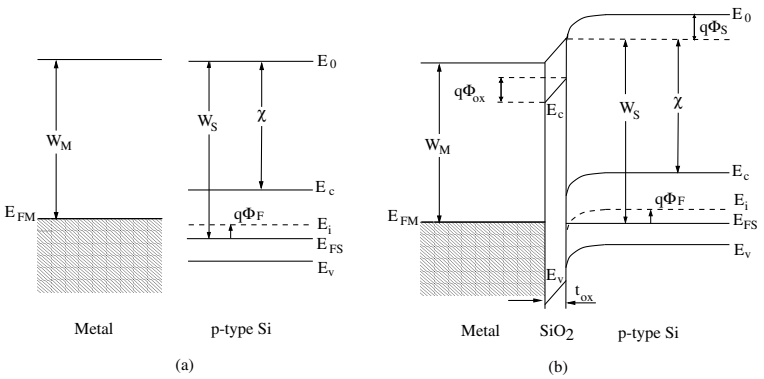


Figure 2.17: Band diagrams for a metal and a p-type silicon substrate when they are (a) separated from each other and (b) assembled to form a MIS structure.

serves as a promoter to facilitate metal adhesion on the dielectrics [40]. The work functions of Ti and Ta are respectively 4.33 and 4.25 eV. It was shown in [41] that the work function of TiN may vary from 4.2 eV to 4.9 eV according to its nitrogen content. The work function of the deposited barrier may therefore be expected to significantly vary from one interconnect technology to the other. For the sake of simplicity, and in order to illustrate the effect of work function on the substrate resistivity in separate cases, we consider here three distinct values of metal work function in the forthcoming discussion: 4.1, 4.7 and 5 eV. These values respectively correspond to the work functions of aluminium, copper and gold.

In the case of p-type substrates, E_{FS} is directly dependent on the doping level (N_a) and is given by ([28]):

$$E_{FS} = E_i - kTln\left(\frac{N_a}{n_i}\right) = E_i - q\phi_F \tag{2.18}$$

In this expression, E_i is the mid gap energy level for silicon, n_i is the silicon intrinsic free carrier concentration ($n_i = 1.45\text{x}10^{10}/cm^3$ at room temperature) and ϕ_F is called the *Fermi potential* (Figure 2.17a). In this work, ϕ_F is considered positive for p-type silicon and negative for n-type silicon, as in [28]. The work function of the Si substrate (W_S) is then simply obtained by combining 2.17 and 2.18:

$$W_S = E_0 - E_i + q\phi_F = \chi + \frac{E_c - E_v}{2} + q\phi_F \tag{2.19}$$

in which χ is the silicon *electron affinity* ($\chi = 4.17\ eV$) and $E_c - E_v$ is the depth of the silicon band gap ($E_c - E_v = 1.1\ eV$).

In the practical case of a MIS structure the metal electrode is separated from the Si substrate by an insulating oxide layer and a 0V DC contact is usually formed at the back of the substrate. This physical contact enables electrons to leave the material where their average energy is the highest and penetrate into the material where the energy is the lowest. This movement of charges occurs until it is completely balanced by an opposing electric field, which is itself created by the charge redistribution. In that case, the Fermi level of both materials line up with each other, forming a *bending* of the Si conduction (E_c) and valence (E_v) bands, as illustrated in Figure 2.17b. The amount by which the bands are bended is usually noted $q\phi_S$, where ϕ_S corresponds to the electrostatic potential at the silicon surface. In this work, the null reference for the potential is taken deep into the substrate.

The sign of the charges flowing into the Si substrate is then directly conditioned by the differences in work function: when $W_M - W_S$ is positive (resp. negative), electrons (resp. holes) leave the silicon and holes (resp. electrons) concentrate at the Si surface. In that case, ϕ_S is negative (resp. positive).

For the three W_M values of interest, we can therefore expect different behaviors in terms of band bending and charge distributions. Indeed, if we clearly have $W_{Al} - W_S < 0$ and $W_{Cu} - W_S < 0$ regardless of the doping level, the work function difference is mostly positive in the case of gold electrodes.

The impact of W_{MS} on the electron concentration at the substrate surface (n_s) is illustrated in Figure 2.18a for a t_{ox} value of 142 nm, which corresponds to the current BOX thickness of commercially available SOI wafers. The dashed lines in the figure define different regions, each corresponding to a specific regime of charge distribution, i.e. accumulation, depletion, weak inversion and strong inversion. The calculations were performed by integrating twice Poisson's equation inside the substrate (as in [33]) and the data are presented as a function of the doping (p-type) level.

The results clearly indicate that due to the different W_{MS} values, the three types of metal induce completely different behaviors of the Si substrate. In particular, it appears that in the case of a 20 Ω.cm-substrate ($N_a = 6.5\text{x}10^{14}\ /cm^3$) with aluminium the Si surface is weakly inverted. On the other hand, it is depleted or weakly accumulated in the case of copper or gold, respectively. When HR substrates ($\rho_{Si} > 3\ k\Omega$.cm) are used, different features are outlined: strong inversion is reached in the case of aluminium, while for copper and gold, respectively, the surface remains either at the onset of weak inversion or is strongly accumulated. However, it must be kept in mind that RF metal interconnects are usually not directly deposited on the BOX of SOI substrates. Additional shallow trench isolation

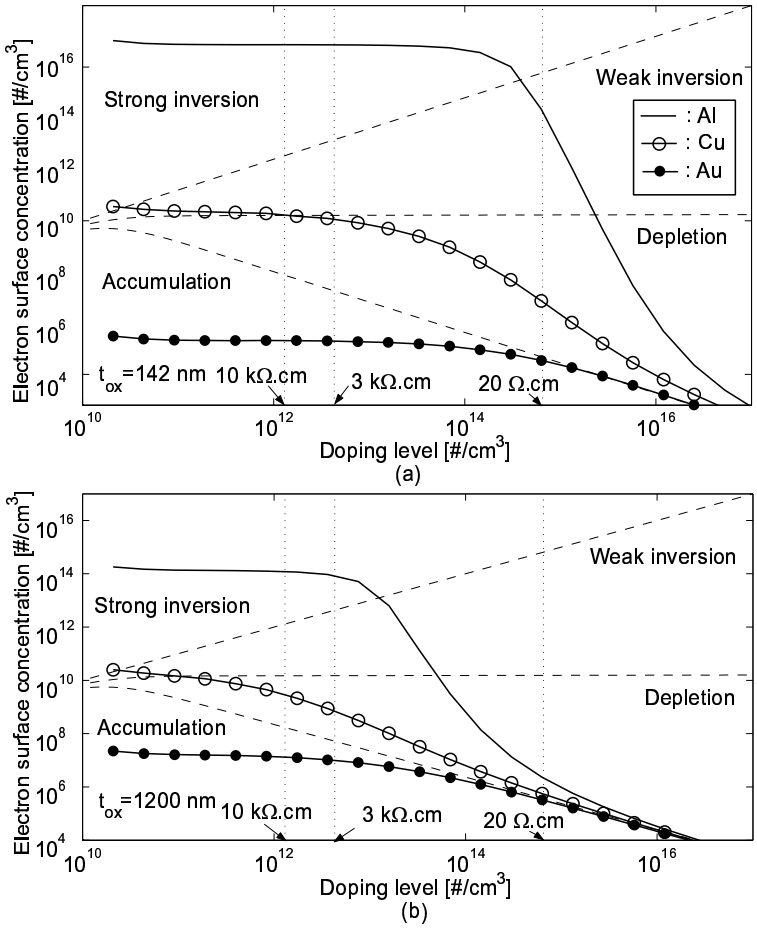


Figure 2.18: Electron surface concentration as a function of the substrate doping for (a) $t_{ox} = 142\ nm$, for (b) $t_{ox} = 1200\ nm$ and for aluminium, copper and gold electrodes. These data were computed assuming 0 V bias applied on the electrode.

(STI), polysilicon, nitride and primary metal dielectric (PMD) layers usually contribute to further isolate the first metal layer from the silicon substrate, resulting in a typical M1 distance from the substrate of 1.2 μm. Figure 2.18b shows that for such an oxide thickness value, the concentration of minority carriers at the silicon surface is reduced in the case of Al and Cu while it is increased in the case of Au. Yet these changes are not significant and the same regimes of charge distribution still prevail for the three types of metal considered.

Thus, knowing that a high level of free carriers at the Si surface is synonym of

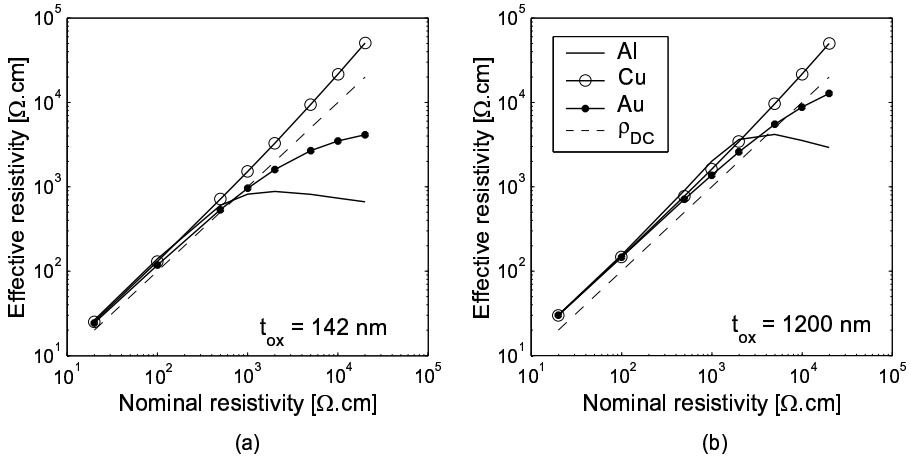


Figure 2.19: Effect of substrate doping and metal work function on the effective resistivity of a CPW MIS structure with (a) t_{ox} = 142 nm and (b) t_{ox} = 1200 nm.

reduced surface resistivity, one can expect from these data that the highest effective resistivity values will be obtained when using copper interconnects instead of gold or aluminium. This is confirmed in the next section.

2.5.1.2 Effect on substrate effective resistivity

The effect the work function difference on the substrate effective resistivity was analyzed with Atlas for a CPW structure directly deposited on the BOX of a SOI substrate (t_{ox} = 142 nm) or using the M1 of a multilayer technology (t_{ox} = 1200 nm). The simulations were made for the three metal types of interest and considering a 0 V bias applied on the top and back electrodes. In addition, a perfect oxide was assumed (i.e., with neither oxide charges nor surface states). The results are shown in Figures 2.19a and b as a function of the substrate nominal resistivity value (ρ_{DC}). The value of ρ_{DC} was varied by changing the dopant concentration inside the substrate, according to Figure 2.5.

The simulation results displayed in Figure 2.19a and b outline for both values of oxide thickness that two separate regions may be distinguished in the curves: when the doping is high and ρ_{DC} kept at lower value than 700~800 Ω.cm, the effective resistivity remains close to the nominal value and follows the dashed lines in the graphs. For higher ρ_{DC} values, a split occurs in the curves according to the metal work functions and thus, according to the free carrier concentration at the silicon surface. This can be easily interpreted by considering that conductive effects inside the Si substrate may be roughly modeled by two parallel conductances,

as illustrated in Figure 2.20. In this figure one conductance is associated with *surface* conduction ($G_{surf} = Re(Y_{surf})$) while the other with *volume* conduction ($G_{vol} = Re(Y_{vol})$) inside the bulk. (This approach is similar to the one presented in [6], in which substrate *surface* losses are dissociated from *bulk* losses). In the case of HR Si substrates, volume conduction is very low and surface conduction largely dominates, making HR Si substrates very sensitive to changes in G_{surf}. When ρ_{DC} gradually decreases, G_{vol} starts increasing and competing with G_{surf}, down to a certain limit below which G_{vol} becomes much higher than G_{surf}. In that case, the effective resistivity is dominated by volume conduction and becomes insensitive to free carrier densities at the substrate surface.

For low doping and thus high ρ_{DC} values, the best results are then clearly obtained in the case of copper interconnects ρ_{eff}, for which it was shown that the Si surface is depleted regardless of the doping level. In that case, the depletion region underneath the oxide helps increasing further the value of ρ_{eff} (slopes higher than 1 in Figures 2.19a and b). On the other hand, the effective resistivity becomes clearly degraded by either an accumulation or an inversion layer in the case of Al or Au interconnects for high ρ_{DC} values. It is seen that the effect is worse when the Si surface is inverted, which, as already discussed, is probably due to the higher mobility of electrons than holes. In that case, the effective resistivity remains lower than 1 kΩ.cm and outlines this surprising feature: it becomes a decreasing function of ρ_{DC}. This observation is related to the slight increase of surface carrier concentration when the doping level is reduced. Figure 2.19b shows that similar trends are observed when thicker oxides are used. However in that case, the effective resistivity exhibits higher values due to a combinations of 2 separate effects:

- free carrier concentration at the Si surface is lower for thicker oxides (as shown in Figure 2.18,
- the total substrate conductance (G_{sh}) is reduced for thicker oxides, thus increasing ρ_{eff} by 2.12.

As in many practical cases RF interconnects are located on higher metal levels than on M1 (and thus further away from the lossy silicon), the total oxide thickness underneath the lines is very often higher than 1.2 μm. The effect of t_{ox} on the substrate effective resistivity therefore deserves further investigation, which is performed in Section 2.5.4.

Meanwhile, these preliminary data already provide some quantitative insights on the very high sensitivity of CPW MIS structures on surface inversion or accumulation layers. In particular, it is seen that in the case of very low doped substrates

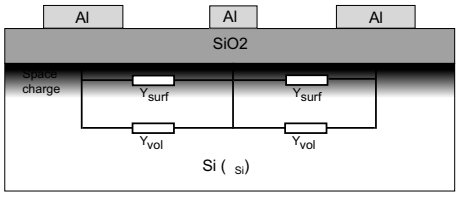


Figure 2.20: Illustration of surface (Y_{surf}) and volume (Y_{vol}) contribution to the total substrate admittance.

the effective resistivity may become more than 2 orders of magnitude lower than ρ_{DC} when aluminium is used. This, by itself, may be a serious source of concern when fabricating RF circuits on HR silicon with aluminium. The simulation results indicate that much better results may be obtained by using copper, and to a lesser extent, by using gold. However, it must be kept in mind that real interconnects are by far more complex than the CPW MIS structure considered up to now: fixed charges in the oxide, the bias applied on the line conductors as well as surface states at the SiO_2/Si interface may indeed have an even higher impact on space charge distribution underneath the insulating oxide, and thus on ρ_{eff}. The effects of Q_f and V_a are investigated next.

2.5.2 Fixed oxide charges

2.5.2.1 Different types of oxide charges

Oxide layers fabricated on silicon substrates are prone to contamination by charged impurities, which are usually referred to as *oxide charges* (Q_f). These charges affect the normal operation of MOSFET devices by shifting their threshold voltage causing sometimes severe yield and reliability issues. It is commonly accepted that that four types of charges are associated with the $Si/Si0_2$ system, differing by their electric behavior [42]:

1. *Fixed oxide charges (Q_f).* These charges are usually positive and are primarily due to structural defects in the oxide layer close to (within 2.5 nm) $Si0_2/Si$ interface. In practical cases, this type of charge is usually considered to form a sheet precisely located at the interface. Its density depends on oxidation process, oxidation ambient and temperature, cooling conditions, and on silicon orientation. This type of charge is not in electrical communication with the underlying silicon.

2. *Mobile ionic charges (Q_m).* Commonly caused by small ionic impurities such

as Li^+, Na^+, K^+ and H^+. These ions are usually located either at the metal-oxide interface (where they originally entered the oxide layer) or at the SiO_2/Si interface where they have drifted due to the application of an external bias. Drift can occur because such ions are mobile in SiO_2 at relatively low temperatures [33]. Negative ions and heavy metals may contribute to this charge even though they are not mobile below 500 °C [42].

3. *Oxide trapped charges* Q_{ot}. Are due to holes or electrons trapped in the bulk of the oxide and may therefore be either positive or negative. Trapping is commonly produced by ionizing radiation, avalanche injection, or other similar processes. Oxide trapped charges are generally annealed out by low temperature (<500 °C) treatment, although neutral traps may remain.

4. Interface trapped charges Q_{it}. These charges may be distinguished from the other three because they are exclusively located at the SiO_2/Si interface, where they are related to *surface traps*. They are therefore in direct electrical communication with the silicon substrate and may be either positive or negative, depending on the nature of the traps. Their density is also depending on the bias, unlike Q_f, Q_m and Q_{ot}. Interface traps are typically formed by 1) structural, oxidation-induced defects 2) metal impurities, or 3) other defects caused by radiation or similar bond breaking processes [42].

In this work, our attention will remain focused on the most commonly investigated entities: fixed and interface trapped charges. It is indeed assumed that for all physical wafers measured in the frame of this work oxide trapped charges were removed by the post-metalization anneal (PMA) made directly after Al deposition. Besides, no evidence for the presence of mobile charges was outlined during all static C-V measurements performed in the frame of this work.

At this point, it is important to point out a fundamental difference that exists between fixed and interface trapped charges. Fixed charges are external elements introduced into the oxide during the oxidation step. They provide an additional source of electric field into the MIS structure and therefore contribute to the parameters that condition the charge distribution at the substrate surface. In other words, free carriers must build up at the SiO_2/Si interface to compensate those charges and ensure the electrostatic neutrality of the structure:

$$Q_g + Q_f + Q_s = 0 \tag{2.20}$$

where Q_g is the charge on the gate ($[/cm^2]$) and Q_s is the total charge in the silicon ($[/cm^2]$). On the other hand, trapped charges originate from the silicon substrate

and are captured by surface traps that are considered to be neutral if empty [33]. When traps are present, the condition of electrostatic neutrality yields:

$$Q_g + Q_f + (Q_{it} + Q_s) = 0 \tag{2.21}$$

The bracketed term in this last expression outlines the charge contribution from the silicon substrate. Since Q_{it} is usually considered to be proportional to the interface trap density (D_{it}) [33],

$$Q_{it} = qD_{it} \tag{2.22}$$

2.21 shows that when D_{it} is high, the charge neutrality in the structure may be mostly assured by trapped charges, thereby strongly decreasing the free carrier density into the substrate. This can in turn have a positive impact on RF losses because trapped charges are unable to react to small signal at frequencies higher than 1 MHz [33]. The impact of interface traps and trapped charges on the effective resistivity of HR Si substrates is discussed in Section 2.5.5. The rest of this section therefore solely focuses on the effect of fixed charges (Q_f) on ρ_{eff}.

2.5.2.2 Effect of fixed oxide charges on the substrate effective resistivity

In the case of oxidized HR Si substrates, the presence of fixed oxide charges was previously shown to provide a significant contribution to RF losses because positive oxide charges attract a low resistivity layer of free carriers near the substrate surface. Though other authors also reported clear evidence of this effect ([4,5,34,43]), the impact of oxide charges on the effective resistivity of HR wafers was never quantified. This is what is proposed here.

Atlas simulations were first performed by considering varying values of Q_f for the three metal types of interest and by applying a 0 V bias on all electrodes of the structure. The results are plotted in figure 2.21a and b for an oxide thickness of 142 nm and 1.2 μm, respectively. In both figures the extracted value of ρ_{eff} is plotted as a function of Q_f.

It is seen in both figures that the Q_f dependence exhibits a maximum value for ρ_{eff}, which depends on the metal work function and on the oxide thickness. This indicates that for a given substrate, there exists an optimum value of Q_f ($Q_{f,opt}$) which guarantees the highest value for the effective resistivity and thus, the lowest substrate losses. The reason for this is that for low values of Q_f (i.e., $Q_f < Q_{f,opt}$), the thickness of the depletion layer below the oxide in the spacing between the conductors is an increasing function of Q_f. Therefore, raising Q_f

to higher values increases the size of the depletion region, thereby increasing the substrate resistivity at the surface, and thus also ρ_{eff}. When Q_f increases further, an inversion layer is formed in that region, thereby reducing ρ_{eff} despite the presence of the depletion layer.

However, as shown in the previous section, the value of ρ_{eff} is also sensitive to the surface resistivity *below* the metallic conductors (i.e., the central AND ground conductors). This is why it is seen from Figures 2.21a and b that, for low Q_f values results are largely dependent on W_{MS}. Indeed in that case, the value of Q_f is too small to have a significant impact on ϕ_S and it is therefore mostly governed by other parameters, such as W_{MS}, V_a and t_{ox}. As it was shown that for copper the substrate surface lies in a state of depletion it is not surprising that the best results are obtained using copper interconnects. The substrate surface is on the other hand accumulated in the case of Au and strongly inverted in the case Al. Using aluminium interconnects is shown once more to yield the lowest value of effective resistivity.

For a fixed oxide charge density higher than $Q_{f,opt}$, the figure shows that the effective resistivity becomes independent on the metal work function. This is because in that case the size of the inversion layer becomes more affected by Q_f than W_{MS} below the conductors, but mostly because most of the losses is attributed to the inversion layer produced in the spacing between the conductors. Surface conduction therefore largely dominates over bulk conduction and the effective resistivity rapidly decreases with Q_f, independently of W_{MS}. The simulated data indicate that Q_f values as low as 1x10^{10} $/cm^2$ can lead to a ρ_{eff} reduction higher than one order of magnitude, regardless of the metal work function. Such low value of Q_f is even lower than what can be obtained with either thermal or deposited oxides. This indicates that in similar physical structures, such as a CPW lines fabricated on the BOX of a HR SOI substrate, fixed oxide charges in the oxide are found in sufficiently large quantities so as to reduce the effective resistivity of the wafer by more than one order of magnitude.

2.5.3 DC bias

The effect of a DC bias applied on the central conductor of the CPW structure was also investigated. The influence of V_a on ρ_{eff} was first studied in the absence of fixed oxide charges. The data are plotted in Figures 2.22a and b as a function of V_a and W_{MS} for an oxide thickness of 142 nm. It is seen in Figure 2.22a that for such value of t_{ox} the impact of V_a on ρ_{eff} is very large. This is of course related to the space charge region that is formed underneath the central conductor for

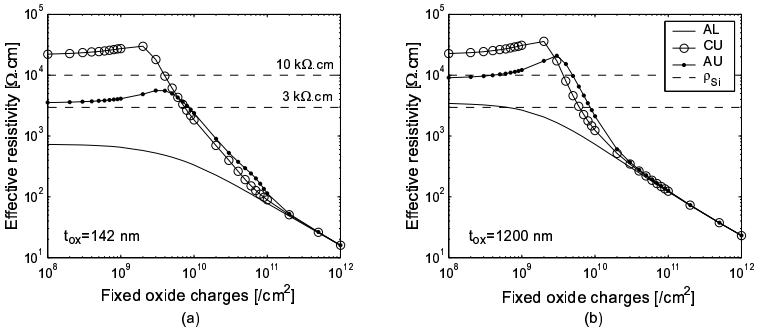


Figure 2.21: Effect of oxide fixed charges on the effective resistivity of oxidized HR Si substrates for three different types of metal and for t_{ox} = 142 nm (a) and t_{ox} = 1200 nm (b).

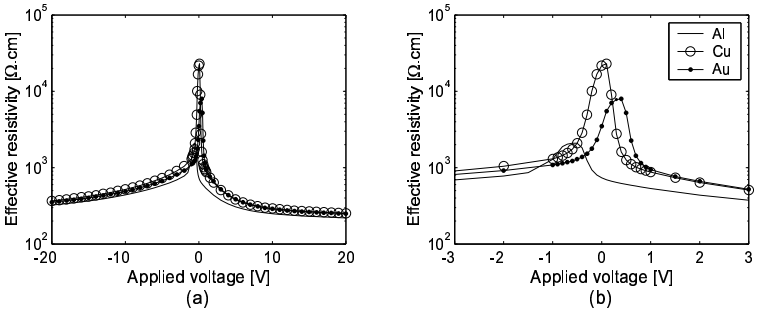


Figure 2.22: Effect of the applied voltage on the effective resistivity of oxidized HR Si substrates for three different types of metal and for t_{ox} = 142 nm.

strong values of $|V_a|$. The maximum value of ρ_{eff} ($\rho_{eff,max}$) is obtained for a V_a value ($V_{a,max}$) corresponding to deep depletion below the central conductor. It is seen that the value of ρ_{eff} very rapidly decreases for bias values slightly higher or lower than $V_{a,max}$. As expected, the value of $\rho_{eff,max}$ depends on the metal work function and is the highest in the case of copper (Figure 2.22b). This is because space charges underneath the 0 V-biased ground conductors also have an impact on the effective resistivity.

In real structures, the presence of fixed charges inside the oxide must however be considered. Figure 2.23(a), (b) and (c) illustrates the combined effect of applied bias and fixed charges on the effective resistivity for an oxide thickness of 142 nm and for the three metal types of interest. The impact of V_a and Q_f for thicker oxides is analyzed in the next section. It is seen in the three figures that the position of $V_{a,max}$ is shifted leftwards for increasing values of Q_f, due its lowering effect on the flatband voltage ([28]), regardless of W_{MS}. It is also seen that Q_f has

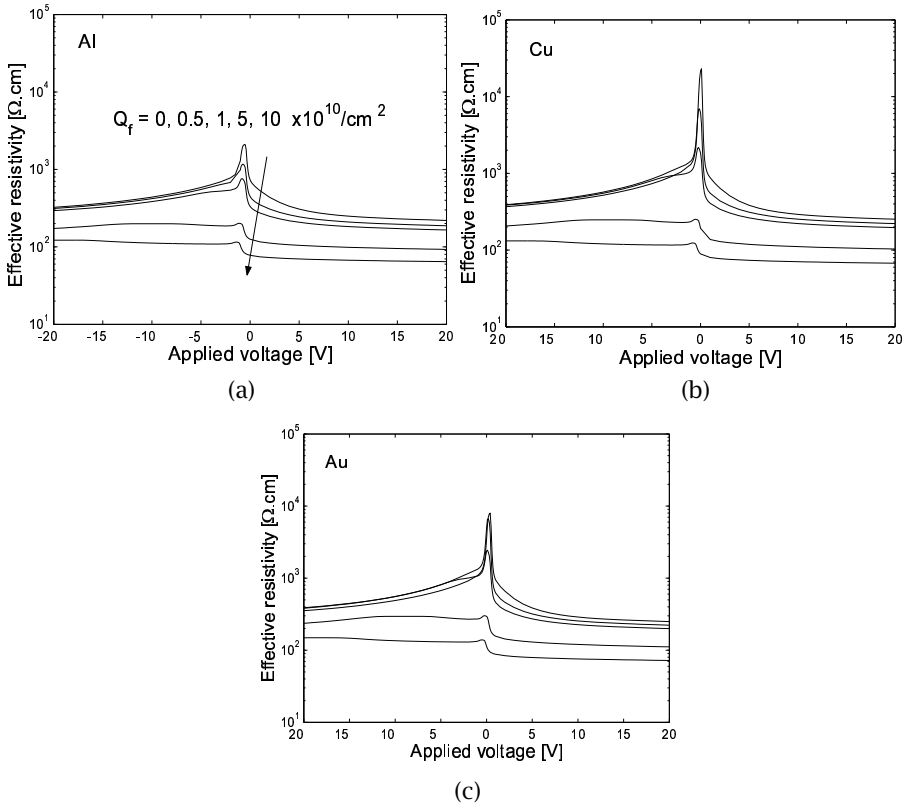


Figure 2.23: Effect of the applied voltage and Q_f on the effective resistivity of oxidized HR Si substrates for three different types of metal and for t_{ox} = 142 nm.

a very large impact on $\rho_{eff,max}$, since oxide charges contribute to degrade the surface resistivity between the conductors, independently of V_a.

The effects of Q_f and V_a on ρ_{eff} were also verified on experimental structures processed at UCL. In the case of wafer SH1, the top silicon film of a HR SOI wafer was etched in order to deposit the metallic structures directly on the 142 nm-thick BOX (dry oxide processed at SOITEC). For wafer BHR2, a HR bulk substrate was thermally oxidized in a wet ambient at UCL. The resulting oxide was thicker ($\sim$ 300 nm). In the case of wafer BH3, a 145 nm-thick oxide was deposited by APCVD on a bulk HR Si substrate too. For all wafers, the metallic structures were patterned using a 1 μm-thick Al metalization.

The experimental ρ_{eff} vs V_a curves are plotted in Figure 2.24 for the three distinct wafers. Only one die was measured on each wafer, but it is expected that a dispersion of the substrate losses should occur across the wafers in relation with

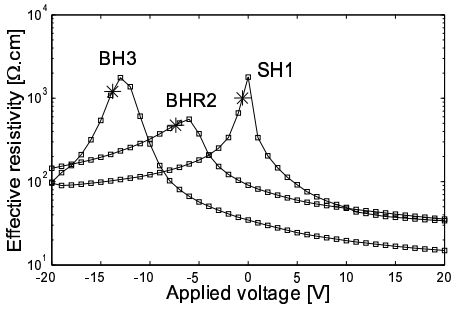


Figure 2.24: Combined effect of V_a and Q_f on the substrate effective resistivity of oxidized HR Si wafers with $t_{ox} = 145\ nm$ (BH3 and SH1) and $t_{ox} = 305\ nm$ (BHR2). Experimental data.

fixed charge densities. This was not studied here but was recently demonstrated in [44].

It is seen in the figure that due to the different methods used to form the oxide, the fixed charge densities appear to be substantially different on the three wafers, which is observable by the position of their corresponding $V_{a,max}$ value.

The values of Q_f could be estimated from quasi-static C-V measurements performed on MIS capacitors available on the wafers. Under this method Q_f is obtained by measuring the shift in flatband voltage (ΔV_{FB}) between an ideal (i.e. with $Q_f = 0$) simulated curve and the physical curve:

$$\Delta V_{FB} = \frac{Q_f}{C_{ox}} \tag{2.23}$$

where the oxide capacitance (C_{ox}) is known from the measured capacitance value in accumulation. This method is illustrated in Figure 2.25.

A less accurate method was also used in the case of large Q_f values, such as for wafers BHR2 and BH3. In those two cases, the flatband potential of the structure was roughly estimated from the ρ_{eff} vs V_a curves (stars in Figure 2.24). Neglecting the work function difference the flatband voltage is approximately given by [28]:

$$V_{FB} \approx \frac{Q_f}{C_{ox}} \tag{2.24}$$

The Q_f values obtained on wafers SH1, BHR2 and BH3 were respectively -1.1x10^{11}, 5x10^{11} and 2x10^{12} $/cm^2$. The presence of negative charges in the case of wafer SH1 might be associated with non bridging oxygen atoms near the SiO_2/Si interface inside the buried oxide [45]. It is however unclear whether those negative charges are related to the thermal oxidation during the fabrication of the UNIBOND

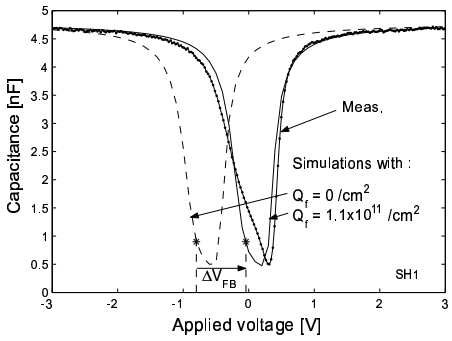


Figure 2.25: Experimental C-V curve obtained on a MIS capacitor from wafer SH1. The figure outlines the positive flatband voltage shift caused by negative Q_f. This shift is referred to a theoretical curve with $Q_f = 0\ /cm^2$.

wafers (at SOITEC) or if they were created during the wet etching of the silicon film (at UCL).

The measured data presented in Figure 2.24 exhibit a severe dependence with respect to V_a and a stronger decrease when the structures are biased in inversion (i.e., for highly positive values of V_a). Both trend agree with the simulation results presented in Figure 2.21a. However, it must be noted that the impact of V_a (sharpness of the $\rho_{eff,max}$ peak) and of Q_f (reduction of $\rho_{eff,max}$) on ρ_{eff} is much more pronounced for the simulated structures. In particular, the value of $\rho_{eff,max}$ obtained for a fixed charge density of $2\text{x}10^{11}\ /cm^2$ is well below 100 Ω.cm in the simulated structure, while it is found much higher than 1 kΩ.cm in the measured CPW lines. This can be interpreted by the presence of traps at the SiO_2/Si interface in the physical structures which is investigated later in this work.

The large impact of Q_f and V_a on ρ_{eff} in HR oxidized substrate and, thus, on substrate losses, may be detrimental in applications where biasing metallic conductors is required. This is the case for most RF analogue applications, in which the AC signal usually propagates from one biased transistor to another on the same interconnects as the ones providing the DC supply. Time varying values of substrate resistivity can be a critical issues, especially in circuits containing loss compensation, such as low noise cascode amplifiers.

Neglecting the effect of V_a on substrate losses can also lead to inaccuracies in on wafer TLR de-embedding procedures, as explained in [46]. Indeed, as this kind of method requires the on wafer measurement of standards (open, short, thru, line, load) to de-embed the device under test (DUT) from its access lines, the standards must be measured under the same bias conditions as the DUT for a

correct estimation of the access line characteristics.

Two methods can however be used at a wafer or circuit fabrication level in order to reduce the parasitic effect of the metal work function, the applied bias and oxide charges on ρ_{eff}: (1) increasing the oxide thickness (as long as this increase does not imply a similar increase of Q_f) to further isolate the metal interconnects from the lossy SiO_2/Si interface and (2) increasing the density of traps at the same interface in order to absorb free carriers from the substrate surface. These two methods are investigated in the following sections.

2.5.4 Oxide thickness

Increasing the total thickness of the insulating dielectrics between interconnects carrying high speed signals and the underlying silicon is usually foreseen as a reliable solution to reduce substrate losses. At the current stage of microelectronics, this can be achieved by different methods:

- In the case of SOI wafers, the most straightforward technique consists in forming the wafers with thicker buried oxides. Standard resistivity SOI wafers with a BOX thickness in the several μm range have been recently made available.
- In multilevel technologies, the cheapest approach is to design the passive structures on the highest metal levels available. In that case, the total oxide thickness therefore corresponds to that of the entire stack inserted between the silicon and the first metal level used. The stack is formed here by the superposition of all intermetal dielectric (IMD) layers. In the case of standard resistivity substrates, this approach can increase the quality factor of inductors by more than 20 % [47] and significantly reduce substrate coupling [48]. In current multilevel technologies, this technique allows for a maximum t_{ox} value ranging typically between 5 and 10 μm.
- Another technological approach can solve this issue by using specific post-backend modules, such as thin-film post-processing techniques [49]. In this case additional, cost effective processing is used to fabricate the passive elements above the passivation layer (i.e., above back end) using other dielectric materials, such as polymide [50] or BCB (benzocyclobutene) [51]. Additional dielectric layers of thickness up to 15∼20 μm can be reached [52], [53].

2.5.4.1 Standard resistivity substrates

As explained in Section 2.2.4.1, the RF electric field distribution near the SiO_2/Si interface in the case of CPW lines is a function of the substrate resistivity: the

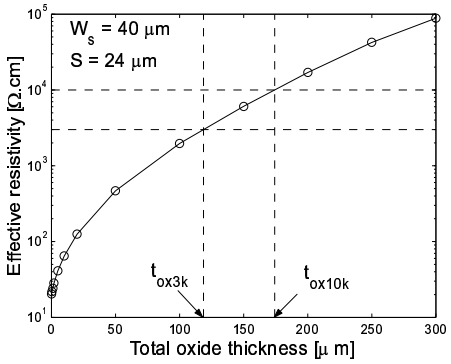


Figure 2.26: Illustration of the effect of t_{ox} on ρ_{eff} for a line geometry corresponding to set b and for a substrate resistivity of 20 Ω.cm. The dashed lines outline the definition of t_{ox3k} and t_{ox10k}, which respectively represent the minimum values of oxide thickness required to obtain effective resistivity values higher than 3 and 10 kΩ.cm.

maximum depth reached inside the substrate by the electric fields depends on the substrate doping. Other factors affecting this parameter are of course, the oxide thickness, but also the geometry of the line.

2.5.4.2 Impact of t_{ox} on ρ_{eff} for a given geometry

The impact of the oxide thickness on the effective resistivity of a CPW line is illustrated in Figure 2.26 for the studied geometry and for a standard resistivity substrate (ρ_{DC} = 20 Ω.cm). In this case, the lines on the SiO_2/Si system were simulated using the variational principles developed in [38]. The oxide relative permittivity was set to 3.9. As could be expected, the value of ρ_{eff} is an increasing function of t_{ox}. It is close to 20 Ω.cm for low values of t_{ox} (which corresponds to the specified Si substrate resistivity) and then rapidly increases with t_{ox}. This increase is related to the higher concentration of electric field inside the oxide and the consequent reduction of the substrate conductance G_{sh}. These simulation data also indicate that for such line geometry, the total oxide layer must be as thick as 118 μm (t_{ox3k}) and 174 μm (t_{ox10k}) to yield ρ_{eff} values higher than 3 and 10 kΩ.cm, respectively. Such large values of t_{ox} can not be achieved by either increasing the BOX thickness, stacking IMD layers (even in advanced technologies with up to 11 metal levels) or by using overIC technologies. If the use of standard resistivity substrates is required (as in bulk technologies), alternative solutions must then be considered to completely suppress substrate losses. However, it is to be noted that the beneficial impact of a t_{ox} increase on substrate loss reduction

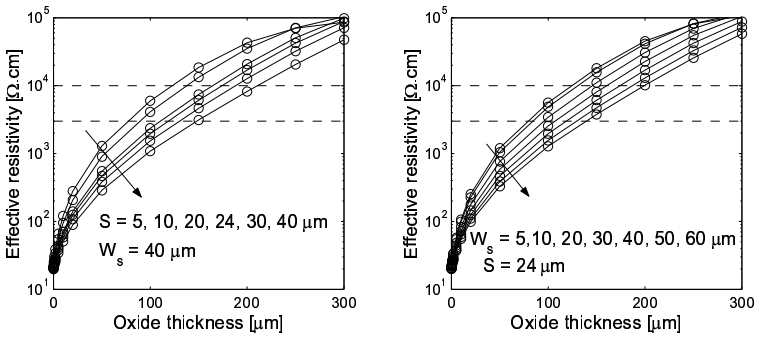


Figure 2.27: Effect of t_{ox} on ρ_{eff} and for varying (a) spacing (with W_s=40 μm) or (b) central conductor width (with S=24 μm) values.

should be expected to depend on the geometry of the conductors, since the penetration depth of field lines inside the Si substrate is also a function of W_s and S. This is investigated below.

2.5.4.3 Combined effect of t_{ox} and line geometry on ρ_{eff}

The effect of a t_{ox} increase was investigated for a large set of central conductor width and conductor spacing values, and for a constant ground plane width of 206 μm. The selected ranges for W_s and S were respectively 5-60 and 5-40 μm, corresponding to values of characteristic impedance varying between 28 and 83 Ω on silicon. In all cases, the metal thickness was set to 1 μm. The combined effects of t_{ox} and S are displayed in Figure 2.27a. It is seen that increasing the spacing between the conductors has a detrimental effect on ρ_{eff}. This is because a larger physical separation of the metallic conductors forces the electric field lines to penetrate more deeply inside the $SiO_2 - Si$ stack, and thus also inside the silicon. It is seen in Figure 2.27b that the effect of the central conductor width on ρ_{eff} is similar to that of S, essentially for the same reason.

From those two figures, it is possible to extract t_{ox3k} and t_{ox10k} curves *vs* W_s and S, providing that identical definitions are used for t_{ox3k} and t_{ox10k} as the ones given in the previous section. The curves are plotted in Figures 2.28a and b, as a function of W_s and S, respectively. It is seen that both t_{ox3k} and t_{ox10k} linearly increase with W_s and S, which provides easy-to-use rules of thumb in order to evaluate the impact of oxide thickness on ρ_{eff} (and thus on substrate losses) in the case of standard resistivity substrates. Indeed, it appears for example from Figures 2.28a and b that the value of t_{ox3k} obeys to the following laws (in which

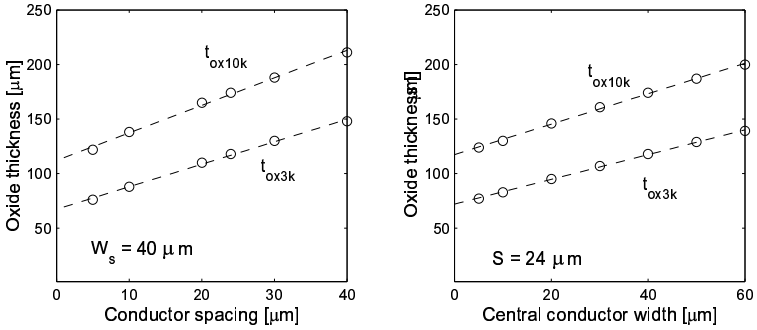


Figure 2.28: Evolution of t_{ox3k} and t_{ox10k} as a function of (a) S and as a function of (b) W_s for CPW lines on a oxidized 20 Ω.cm silicon substrate.

all data are written in μm):

$$t_{ox3k} = 2.1S + 67.3\ [\mu m] \tag{2.25}$$

$$t_{ox3k} = 1.1W_s + 72.0\ [\mu m] \tag{2.26}$$

It must be kept in mind that these two expressions are respectively valid only for a W_s value of 40 μm (Equation 2.25) and for a S value of 24 μm (Equation 2.26). Their use is therefore limited and does not provide very broad informations to anyone interested in evaluating substrate losses for *any* line geometry. Similar comments also apply to the linear trends depicted by the t_{ox10k} *vs* S and *vs* W_s curves in Figures 2.28a and b, respectively.

As a consequence, an attempt was made to evaluate the simultaneous effects of W_s and S on t_{ox3k} and t_{ox10k}, which have thus been plotted in Figures 2.29 and 2.30, respectively. The dots in these figures correspond to the simulated values, while the other mesh points were obtained by using interpolation. Both figures show that the W_s and S dependences of t_{ox3k} and t_{ox10k} can be roughly approximated by plane-like equations. A least square error-based optimization yielded the following expressions:

$$t_{ox3k} \simeq 1.12W_s + 2.07S + 21.6\ [\mu m] \tag{2.27}$$

$$t_{ox10k} \simeq 1.39W_s + 2.56S + 54.3\ [\mu m] \tag{2.28}$$

for which the maximum relative errors were estimated to be around 15 % when 5 $\mu m < W_s$ and 10 $\mu m < S$ (Figure 2.31, smallest simulation number). These

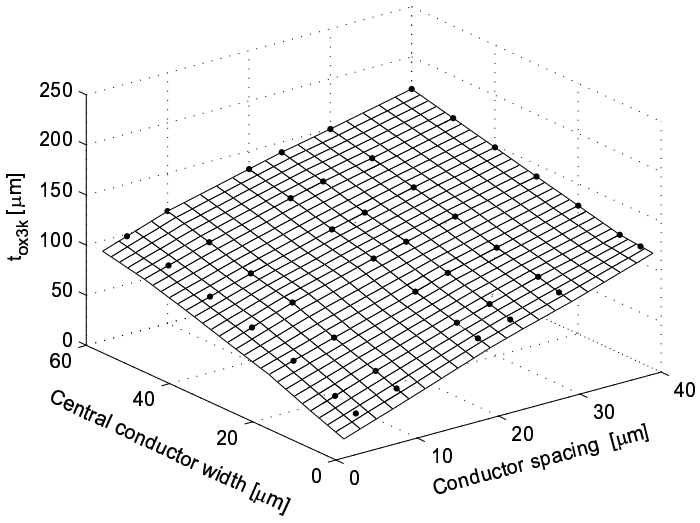


Figure 2.29: 3-D graph showing the combined effect of W_s and S on t_{ox3k} for a 20 Ω.cm Si substrate.

errors were found close to 40 % for S values lower than 10 μm, which is probably related to the non negligible effect of the metal thickness (1 μm) in those cases. The coefficients in Equations 2.27 and 2.28 are assumed to be dependent on the substrate doping.

Though the accuracy of these expressions is clearly limited, they still can be used as practical rules of thumb to roughly evaluate oxide thickness requirements. Please note that they are only valid for applications on 20 Ω.cm resistivity substrates, even if the method could easily be extended for substrates with other values of resistivity.

These expressions clearly indicate that the values of t_{ox3k} or t_{ox10k} must be very large (i.e., higher than 50 μm) to reduce substrate losses to negligible values, even for CPW lines with small geometries. For the practical case of a small line with $W_s = 10\ \mu m$ and $S = 5\ \mu m$, the values of t_{ox3k} and t_{ox10k} reported in Figures 2.29 and 2.30 are respectively 32.6 and 60.8 μm. This, again, can not be reached by stacking dielectrics in multilayer technologies. Alternative solutions must therefore be considered, such as using above IC circuits, other line topologies, or high resistivity substrates.

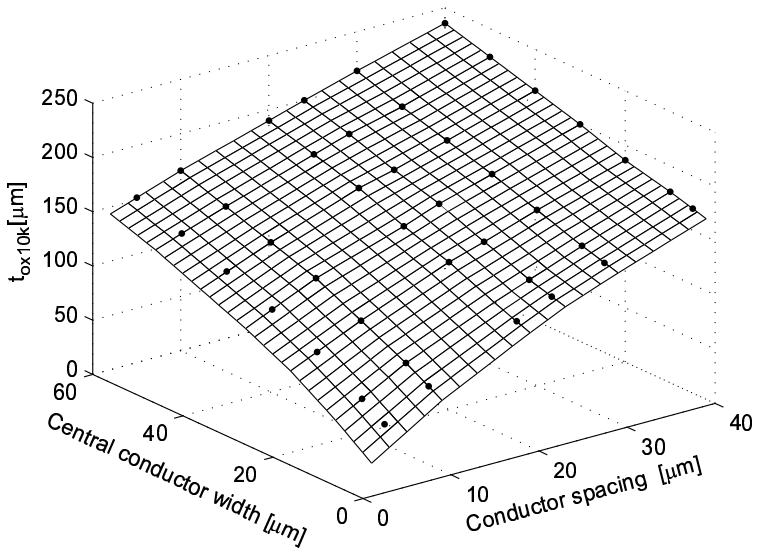


Figure 2.30: 3-D graph showing the combined effect of W_s and S on t_{ox10k} for a 20 Ω.cm Si substrate.

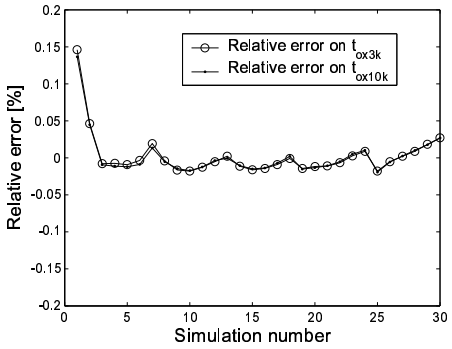


Figure 2.31: Relative error committed on t_{ox3k} and t_{ox10k} using Equations 2.27 and 2.28 for the simulated points of Figures 2.29 and 2.30. Positive errors result in overestimations of t_{ox}.

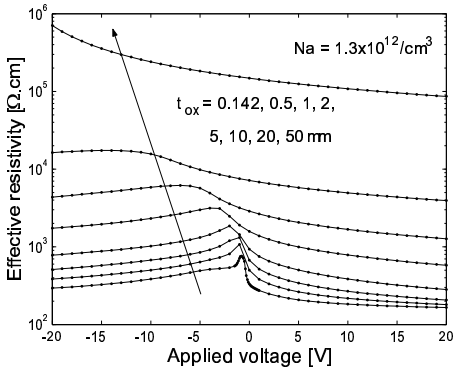


Figure 2.32: Simulated ρ_{eff} data *vs* applied voltage for HR Si substrates with varying oxide thickness values and a constant fixed charge density of 1x10^{10} $/cm^2$.

2.5.4.4 High resistivity substrates

The effect of a t_{ox} increase on the effective resistivity of HR (ρ_{Si}=10 kΩ.cm) Si substrates is illustrated in Figure 2.32 for the case of aluminium interconnects. In this case, these data were computed using Atlas since an accurate estimation of the charge distribution inside the substrate is required for a correct evaluation of ρ_{eff}. In the figure the ρ_{eff} data are plotted as a function of V_a for various t_{ox} values. The fixed charge density was set to a constant value of 1x10^{10} $/cm^2$. As expected, increasing t_{ox} has a beneficial impact on ρ_{eff} and a closer look at the data indicates that the improvement is twofold:

- first, the influence of V_a on ρ_{eff} is reduced as the oxide is made thicker. This is directly related to the fact that thicker oxide layers tend to reduce the influence of the applied bias on the surface potential (ϕ_S), thereby also reducing its control on space charges at the SiO_2/Si interface. The impact of t_{ox} on the ϕ_s *vs* V_a curves is illustrated in Figure 2.33 for the same value of Q_f and N_a as the ones used in the Atlas simulations. A reduction of the V_a influence on ρ_{eff} is beneficial for RF circuits, especially when high bias voltages are needed such as in integrated switches of front end receivers or applications using RF MEMS. Figure 2.32 also highlights a leftward shift of the flatband voltage (point corresponding to ϕ_s = 0 V in Figure 2.33) for increasing t_{ox} values. This trend is also reproduced in the Atlas simulations (Figure 2.32).

- second, significant improvements of ρ_{eff} are observed as t_{ox} is increased. This trend is similar to the one reported in the case of 20 Ω.cm resistivity substrate and is also attributed to a reduction of the line shunt conductance G_{sh}. The

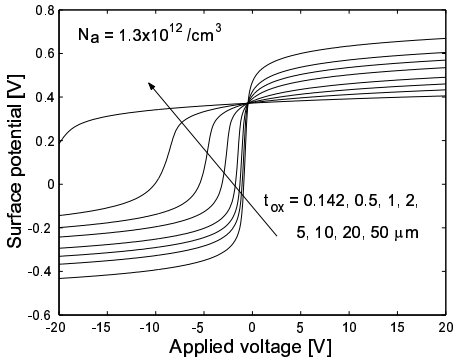


Figure 2.33: Influence of t_{ox} on the ϕ_s *vs* V_a curves for a constant Q_f value of $1\text{x}10^{10}$ $/cm^2$.

figure indicates that for such Q_f value and for the line geometry considered here, the values of t_{ox3k} and t_{ox10k} must be respectively higher than 10 and and 20 μm. These values are significantly lower than the ones required for standard resistivity substrates.

However, it must be pointed out that these simulations predict the beneficial effect of a t_{ox} increase on ρ_{eff} in the ideal case where Q_f remains constant, i.e. independently on the total oxide thickness. This, clearly, may not be expected to be the case for real structures. For instance, SOI wafers with thick buried oxides are fabricated in a different manner than wafers with thin buried oxide since a thermal oxidation is processed on both handle and donor wafers in order to achieve high t_{ox} values. Besides, the oxidation is processed in a different ambient than for classical wafers and the bonding is then achieved between the two oxide layers. It must therefore be expected that the use of different oxidation procedures results in t_{ox}-dependent Q_f values inside the buried oxide of SOI substrates. It is yet not clear whether thicker BOX should have higher or lower Q_f values.

As explained earlier, thick oxides in multilayer technologies are usually obtained by stacking a certain number of IMD layers. However, the dielectric materials used for inter-metal level filling must comply within a series of constraints, which mainly rely on their mechanical and chemical properties [54]. These materials are usually implanted with dopants (such as phosphorous, boron or florine) in order to further improve those properties and additional thin dielectric layers (such as Spin-on-Glasses (SoG)) are also introduced to solve planarization issues [55, 56]. As a result, the overall content of ionized and charges impurities in stacked dielectric layers can be expected to be very high. This was actually demon-

strated to be the case in the work of Pramanik *et al.*, in which they used a stack consisting of 2 PECVD oxide layers and 2 coats of SoG as the total IMD layer in their double metal level technology. In that work, a total Q_f value close to 8x10^{11} $/cm^2$ was found. Such high value was observed to cause parasitic conduction issues below the field oxide that is used for device isolation [57], even in the case of low resistivity wafers. Similar effects were also reported in [58].

Another consequence of using stacked dielectrics is the possibility of having distributed fixed charges across the oxide, with the expectations that the charge concentration may be higher in specific layers or at specific dielectric/dielectric interfaces. When fixed charges are not located close to the SiO_2/Si interface, their effect on space charges inside the silicon is reduced. A simple electrostatic analysis indicates that the equivalent fixed charge density ($Q_{f,equ}$) is given in that case by:

$$Q_{f,equ} = \int_0^{t_{ox}} \rho_b(x) \frac{x}{t_{ox}} dx \tag{2.29}$$

in which $\rho_b(x)$ is the bulk fixed charge concentration (in [$/cm^2/\mu m$]) and x is taken from the metal/SiO_2 interface.

In multilayer technologies using higher than 5 metal levels the total number of IMD layers is typically in the range of several tens, with layer thicknesses ranging between several tens to several hundreds of nanometers. Assuming a *homogeneous* distribution of charges across the entire stack (i.e., with $\rho_b(x) = \rho_b$), one can write:

$$Q_{f,equ} = \rho_b \frac{t_{ox}}{2} \tag{2.30}$$

This indicates that $Q_{f,equ}$ linearly increases with t_{ox}.

To obtain an empirical value of ρ_b, a simple method consists in determining the flatband potential (and, thus $Q_{f,equ}$) from either quasi-static C-V measurements or ρ_{eff} *vs* V_a curves. Knowing the total oxide thickness, ρ_b can then be estimated from 2.30. The extraction of ρ_b was performed on several technologies, all originating from commercial foundries for which details (such as the number of available metal layers, the metal layer on which the lines were processed, the total oxide thickness) are provided in Table 2.3. In the table are also included the extracted values of $Q_{f,equ}$ and ρ_b.

It is seen from the table that the ST013 and Leti025 technologies feature similar ρ_b values and that these values are both 2~3 times much smaller than for the Xfab1 technology, for which a HR SOI wafer with a thick (~ 1 μm) buried oxide was used. The higher $Q_{f,equ}$ value recorded on Xfab1 is either due to higher concentration of impurities inside the thicker BOX (and is thus inherent to the wafer fabrication process) or inside IMDs (and is thus inherent to the CMOS process). To evaluate the

Table 2.3: Technological details of investigated multilayer technologies and extracted values of bulk fixed charges densities.

Techno.	Number of metal layers	CPW metal layers	Total oxide thickness [μm]	Flatband voltage [V]	$Q_{f,equ}$ [$/cm^2$]	ρ_b [$/cm^2/\mu m$]
ST013	6	5-6	4.1	~ -22	1.2 10^{11}	5.6 10^{10}
Leti025	3	3	4.5	~ -35	1.7 10^{11}	7.5 10^{10}
Xfab1	3	1-3	2.3	< -40	>3.75 10^{11}	> 16.3 10^{10}

impact of t_{ox} in more realistic situations, additional Atlas simulations were then conducted by increasing the oxide thickness and keeping an average constant ρ_b value of 6.5x10^{10} $/cm^2/\mu m$. This level closely corresponds to the average value of ρ_b reported for the two first technologies. The results are plotted in Figure 2.34a as a function of V_a and t_{ox}. The same t_{ox} values were used as in the case of Figure 2.32, for which the data have been replotted in Figure 2.34b for an easier comparison.

It is clearly seen that the data in Figures 2.34a and b do not feature the same trends with regards to a t_{ox} increase. In the case of a constant Q_f density increasing t_{ox} appears to provide a beneficial impact on ρ_{eff}. In the case of a constant ρ_b density, it is first seen to induce a reduction of ρ_{eff} down to an oxide thicknesses corresponding to a worst case value ($t_{ox,wst}$). Above $t_{ox,wst}$, an increase of ρ_{eff} is observed.

A shown in Figure 2.35a, the presence of a minimum point in the ρ_{eff} *vs* t_{ox} curves for a constant bulk oxide charge density results from two opposite trends:

- an increase of t_{ox} is accompanied by an increase of $Q_{f,equ}$ and a resulting increase of the inverted charge below the oxide, which augments substrate losses and reduces ρ_{eff},

- an increase of t_{ox} tends to reduce the value of G_{sh}, as in the case of Figure 2.34a, and thus increase ρ_{eff}.

The figure indicates that for the investigated structure, the value of $t_{ox,wst}$ is close to 50 μm. However, as substrate losses are also a function of the penetration depth of electric fields inside the substrate, one must expect the minimum ρ_{eff} value and thus $t_{ox,wst}$ to be both a function of the line geometry. This is further illustrated in Figure 2.35b, where simulation data obtained for smaller geometries (namely, Set c and Set e from Table 2.2) are reported.

The value of ρ_{eff} was also extracted from CPW measurements on wafers from the three technologies presented in Table 2.3. The results are plotted in Figure 2.36 as a function of the applied bias. It is seen that all technologies exhibit the same behavior:

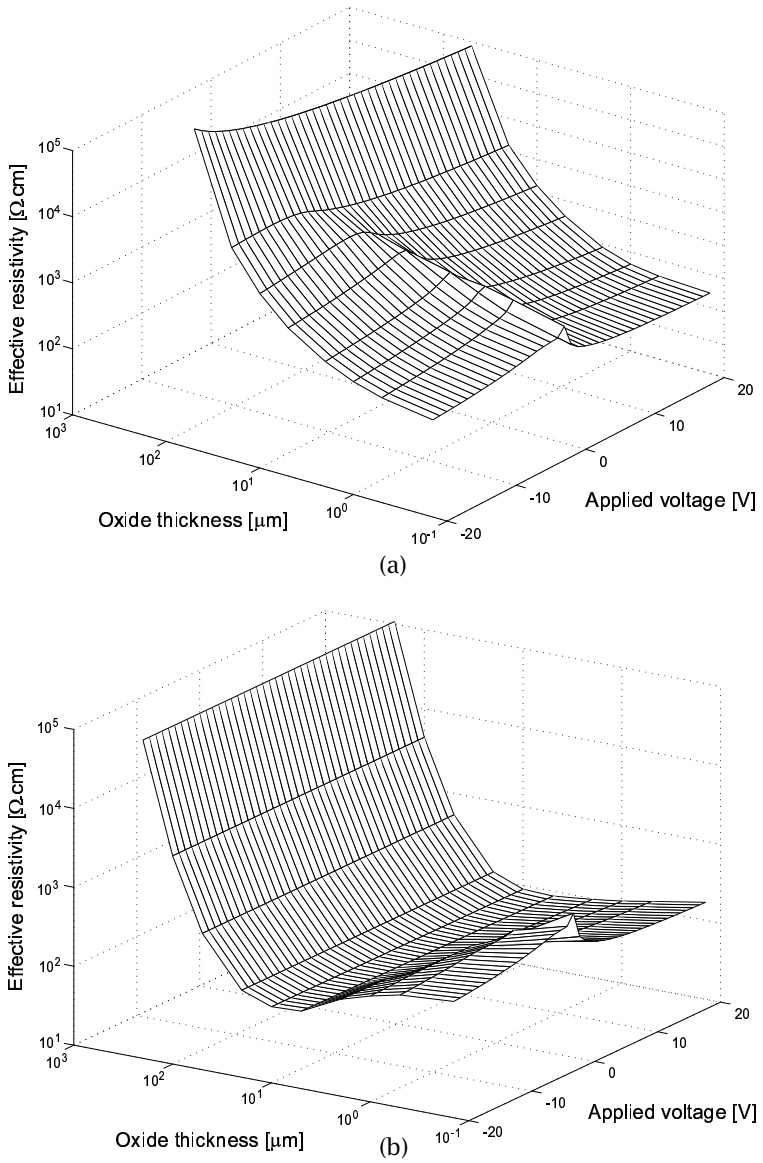


Figure 2.34: Impact of t_{ox} on the ρ_{eff} *vs* V_a curves in the case of (a) a constant Q_f value of 1x10^{10} $/cm^2$ and (b) a constant ρ_b value of 6.5x10^{10} $/cm^2/\mu m$.

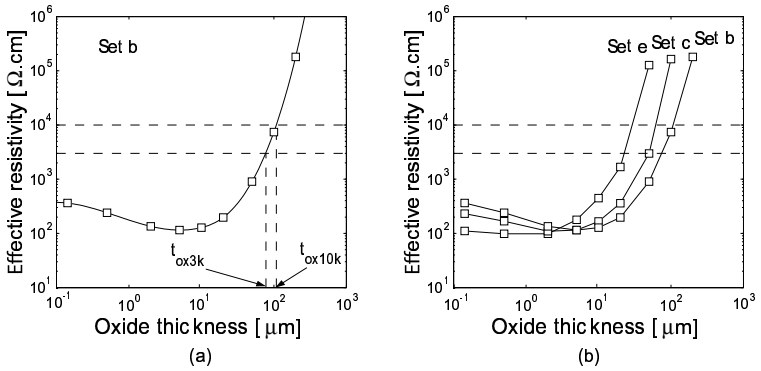


Figure 2.35: (a) Simulated ρ_{eff} *vs* t_{ox} curves in the case of set b and empirical extraction of t_{ox3k} and t_{ox10k}; (b) comparison with other CPW geometries. In all cases the metal was aluminium.

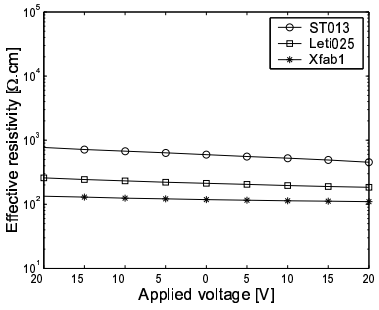


Figure 2.36: Extracted ρ_{eff} *vs* V_a curves for the three investigated multilayer technologies.

- the applied bias has hardly any effect on ρ_{eff} due to the thick oxides,
- the reported ρ_{eff} values are inversely related to the fixed charge density, i.e., the wafer with the highest fixed charge density has the lowest effective resistivity and suffers from the highest substrate losses.

Both experimental observations qualitatively agree with and confirm the simulated trends outlined in Figure 2.34. They also confirm that the values of ρ_{eff} are more than one order of magnitude lower than the nominal substrate resistivity in multilayer technologies with total t_{ox} values lower than 10~20 μm, which is

due to the important level of bulk fixed charges in IMDs. As current and future CMOS Back-End-of-Line (BEOL) technologies are doomed to stack ever increasing numbers of IMDs and metal layers, this has several negative consequences:

1. the extracted level of ρ_{eff} being much lower than several kΩ.cm, substrate losses still amount to a fair proportion of total (conductor+substrate) losses and are therefore not negligible despite what could have been initially hoped from using HR SOI substrates,

2. from a wafer manufacturer point of view, the value of the substrate effective resistivity can not be guaranteed since it merely depends on the CMOS technology that is going to be processed upon the wafers,

3. from a circuit designer point of view working on a specific technology node in a given foundry, the final value of ρ_{eff} will depend both on

   · the BEOL technology and any modification that is performed (which could be an issue in classical situations where the first metalization layers are used for characterization purposes during the early stages of product development and where the complete BEOL is used for the final products),

   · the metal levels used to design the passive structures (merely the first),

   · the geometry of the designed passive structure, as shown in Figure 2.35b,

4. from design perspectives also, the final value of ρ_{eff} could vary from one chip to another due to subtle process variations across the wafer and the large sensitivity of ρ_{eff} to Q_f or $Q_{f,equ}$.

As shown in Figure 2.34, one obvious technique to solve these issues is to use very thick oxide or insulator layers. However, this approach presents two major difficulties. First, as illustrated in Figure 2.35b, even in the case of small geometries (W_s of 10 μm and S of 5 μm for Set e), the oxide thickness values that must be reached in order to almost suppress substrate losses are more than 25 μm. Such high values of t_{ox} can only be achieved by using post-processing modules, or above IC circuits, which of course requires additional process work and know-how, thus significantly extending the price to pay. This extra cost is actually what one expects to save by using HR substrates.

Second, the total oxide thickness that should be obtained to completely suppress substrate losses (t_{ox10k}) depends on the geometry of the coplanar structure that propagates the high frequency signals, as also illustrated in Figure 2.35b. This means that if a (very) thick oxide of specific thickness is obtained and no substrate

loss is a full design constraint, there will be a limitation on the maximum geometry of the passive structures that can be implemented.

Using very thick oxides therefore does not appear as the most reliable solution to suppress substrate losses in HR SOI substrates and an alternative approach is to be considered. At this point, it is important to realize that the issues mentioned above could all be solved at once if the parasitic conduction at the SiO_2/Si interface could be suppressed. An effective approach proposed in [5] and demonstrated for the first time in [35] consists in introducing a large density of carrier traps at the substrate surface, as explained in the coming section.

2.5.5 Interface states

2.5.5.1 Origin of interface states

Interface traps are referred in this text as defects that introduce discrete energy levels (states) in the forbidden bandgap near the the SiO_2/Si interface. Those defects can behave like donors or acceptors. In the former case, the traps are neutral when filled and positive when empty. In the latter case, the traps are neutral when empty and negative when filled. The exact nature of the traps as well as the mechanisms by which they are produced are not yet fully understood but several models have been proposed to explain the physical origin of the traps. In [33], three types of models are reported:

- *The Coulombic model.* According to this model, fixed charges in the oxide induce potential wells in the silicon and quantum levels within these wells are associated with interface trap levels. For the most part, such traps are located in energy levels near the silicon band edges and result in too low midgap D_{it} density to significantly alter the electrical properties of the SiO_2/Si interface.

- *The bond models.* In these models, the distribution of interface traps in the forbidden bandgap is caused by a distribution of *bond angles* or by *stretched bonds* at the silicon surface. These bond distortions may be caused by local strain or non stoichiometry at the SiO_2/Si interface.

- *The defect models.* In these models, interface traps are caused by *defects* in the interfacial region. The origin of those defects ranges from stacking faults and micropores to atomic of molecular residues related to imperfect oxidation. In the case of thermal oxidation, the three main defect types that have been identified as *possibly* existing at the SiO_2/Si interface and as *possibly* producing interface traps are:

1. *Impurity atoms.*

2. *Excess silicon.* Probably resulting from an uncomplete oxidation process, there may be trivalent silicon atoms in the oxide at the interface. Such atoms only share three of their four valence electrons with neighboring silicon atoms and the unsatisfied valence bond (also called *dangling* bond) is known to introduce two energy levels in the silicon band gap [59, 60]: one (donor-type) at 0.25 eV and the other (acceptor-type) at ~0.85 eV above the valance band. This type of traps is commonly referred to as a P_b centers due to their paramagnetic nature in neutral state. These defects are believed to be the dominant cause of interface traps in the SiO_2/Si system [59].

3. *Non bridging oxygen.* Non bridging oxygen atoms are oxygen atoms that share only one of their two valence bonds with a silicon atom, thus interrupting the "bridge" that is formed via the oxygen between two silicon atoms. Non bridging oxygen may be caused by uncomplete oxidation (and excess of oxygen) or stress in the interfacial region. The cleavage of strained Si-O bonds result in the so-called E' centers [61]. The unsatisfied valence bond acts as an electron trap, which becomes negatively charged when filled [33].

2.5.5.2 Interface state densities

For thermal oxides, the resulting density of interface traps depends on a large set of parameters such as the oxidation temperature, the oxidation ambient (wet or dry), the oxygen pressure and also the silicon substrate orientation ((100) or (111)) [33]. Due to the three times higher density of silicon atoms at the SiO_2/Si interface for (111) substrates, interface traps densities are higher in that case than for (100) substrates. Typically, dry and low oxide layers result in D_{it} densities in the low 10^{12} $/cm^2/eV$ and in the low 10^{11} $/cm^2/eV$ near midgap, respectively, for (100) substrates [33]. However, as both P_b and E' centers are electrically active, they can react with hydrogen and capture hydrogen atoms [60, 62]. This mechanism passivates the defects and decreases the effective density of interface traps. The value of D_{it} is therefore quite sensitive to the hydrogen content of the ambient, and a reduction of D_{it} is possible by performing post oxidation anneals in hydrogen-containing ambient. Typical anneals are the Post-Metalization-Anneals (PMA) at a temperature of 430 °C in forming gas (10 % H_2 + 90%N_2). Hydrogen anneals at temperatures above 500°C can however have an opposite effect on D_{it} by depassivating the traps [62]. A reduction of trap density at the thermal oxide/silicon interface can, for instance, also be obtained by RF plasma hydrogenation of the silicon surface prior oxidation [63].

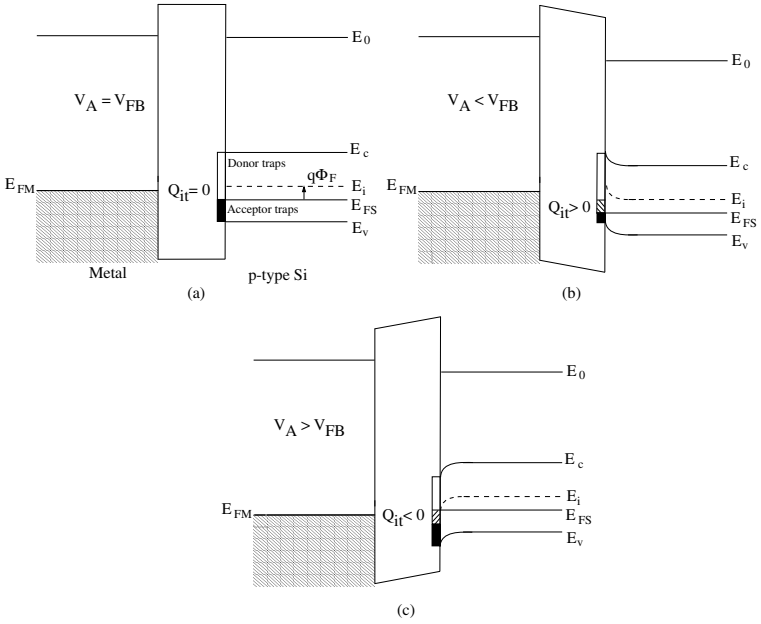


Figure 2.37: Band diagram of the simulated structures showing the simulated trap distribution at the SiO_2/Si interface as well as the sign of Q_{it} for (a) $V_a = V_{FB}$, (b) $V_a < V_{FB}$ and (c) $V_a > V_{FB}$.

In the case of SOI substrates and for the problem with which we are confronted, the relevant SiO_2/Si interface is the interface between the buried oxide layer and the silicon substrate. The nature of this interface depends on the process that is used to fabricate the SOI wafer. Mainly, the interface is either a bonded or a thermal interface. In the case of bonded wafers, the bonding process may be performed between the handle substrate and the thermally oxidized donor wafer (Smart-Cut technology) but also between the oxidized substrate and the donor wafer [64]. In the latter case, the buried oxide is not submitted to the hydrogen implant used for the splitting and different electrical properties of the interface can be expected.

Recent works have demonstrated that the trap distribution [65] as well as the trap properties [66] were significantly different from one type of interface to the other: bonded interfaces exhibit trap energies in a narrow subband between E_v+0.73 and E_c+0.93 eV, which is typical of P_b centers, while thermal interfaces are characterized by a continuous, U shape distribution of states throughout the band gap. These differences were attributed to the absence of SiO_x transition layer in the case of bonded interfaces. In those works however, the buried oxide was not subjected to H_+ implant during the wafer fabrication process.

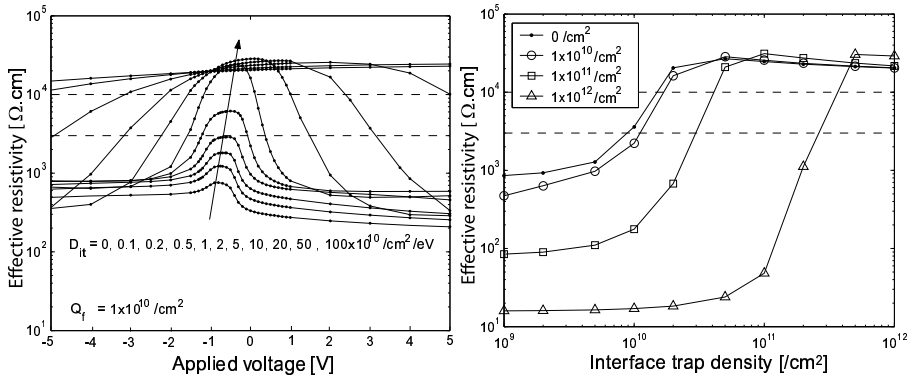


Figure 2.38: (a) Simulated ρ_{eff} *vs* V_a curves for a varying interface trap density and a constant Q_f value of 1x10^{10} $/cm^2$ and (b) bimulated ρ_{eff} values as a function of D_{it} for several Q_f densities and an applied bias value of 0 V.

To illustrate the impact of interface trap densities on the substrate effective resistivity Atlas simulations were performed. For simplicity, the trap distribution was assumed to be *continuous* and *homogeneous* throughout the band gap. Traps were considered as *donors below* and *acceptors above* the Fermi level at the substrate surface in flatband conditions (Figure 2.37) similarly to P_b centers in p-type substrates. The fixed charge density was varied and the bias was swept from -20 to 20 V.

2.5.5.3 Impact of D_{it} on ρ_{eff}: simulated data

Figure 2.38a displays the simulated ρ_{eff} *vs* V_a curves for a constant Q_f density of 1x10^{10} cm^2. It is seen from the figure that an increase of D_{it} is very beneficial on the maximum value of ρ_{eff} ($\rho_{eff,max}$) even in the case of extremely low densities (below 1x10^{10} $/cm^2/eV$). For instance, the figure shows that $\rho_{eff,max}$ reaches almost 3 kΩ.cm for a D_{it} value of 5x10^9 $/cm^2/eV$ while it is barely of 750 Ω.cm when no traps are present at the SiO_2/Si interface. For higher D_{it} levels, ρ_{eff} increases even much further and recovers the value of the nominal wafer resistivity (i.e., ρ_{DC} ~ 10 kΩ.cm) for a trap density located between 1x10^{10} and 2x10^{10} $/cm^2/eV$. Above such value, the value of $\rho_{eff,max}$ seems to saturate at a value higher than ρ_{DC} due to the presence of a depletion layer at the substrate surface.

It is also seen in Figure 2.38a that the influence of V_a on ρ_{eff} is decreased as the trap density increases. This is directly attributed to the reduced impact of V_a on the surface potential and on the charge distribution at the silicon surface

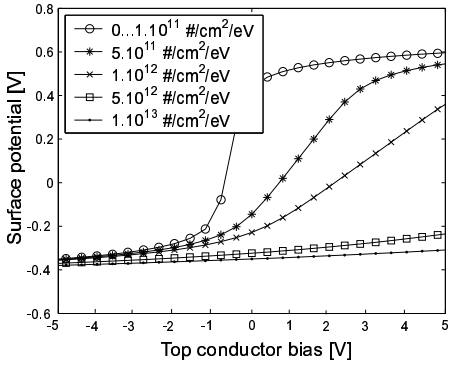


Figure 2.39: Simulated ϕ_s *vs* applied bias curves for varying D_{it} values (t_{ox} = 142 nm, W_f=4.1 eV and N_a=13x10^{11} $/cm^3$).

(Q_s) when traps are present at the SiO_2/Si interface. As explained in [33], this reduction is attributed to the ability of the traps to respond to the applied bias: any changes in Q_g (the charge on the top conductor) is balanced by both Q_s and interface trapped charges (Q_{it}). For high D_{it} values the electrostatic neutrality of the structure is thus mostly ensured by Q_{it}, thus reducing changes in Q_s and in band banding. These effects are further illustrated in Figure 2.39 in the case of a MIS capacitor with t_{ox}=142 nm, W_f=4.1 V (Al) and N_a=13x10^{11} $/cm^3$. For these additional simulations, a similar trap distribution was chosen as for the Atlas simulations. Besides, for the sake of further modeling simplification, the traps were considered as all filled below and all empty above the Fermi level for each applied bias. These simulations also show that for the trap distribution considered here, any increase of D_{it} also yields an increase of the flatband potential. This trend was confirmed by Atlas simulations.

Figure 2.38b illustrates the impact of D_{it} on the value of ρ_{eff} at 0 V for several Q_f densities. It is seen with no surprise that the minimum D_{it} level (D_{it10k}) that is required to obtain lossless substrates (i.e., ρ_{eff} = 10 kΩ.cm) is an increasing function of the fixed charge density in the oxide. This is because for higher positive Q_f densities, a higher concentration of electrons is attracted near the substrate surface and a higher density of traps is required to absorb those charges.

2.5.5.4 Impact of D_{it} on ρ_{eff}: experimental evidences

A. Different oxide qualities

Among the various wafers processed in the frame of this work, several of them exhibited strong evidences that the presence (or absence) of interface traps had a

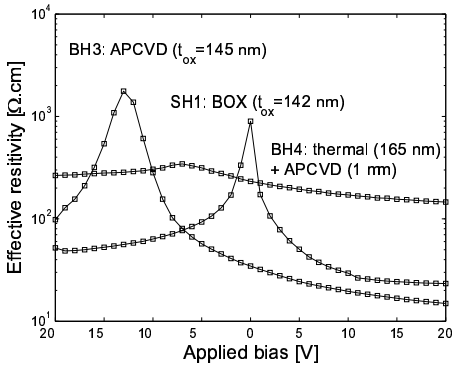


Figure 2.40: Experimental ρ_{eff} values extracted on HR wafers highlighting the positive effect of traps at the SiO_2/Si interface.

positive (or negative) impact on the value of their effective resistivity. Data from three selected wafers are reported in Figure 2.40:

- In the case of wafer SH1, the data are reported from the ones presented in Figure 2.24. For that wafer, Q_f was estimated from quasi-static C-V measurements to lie around -1x10^{11} $/cm^2$. According to simulated data performed in the absence of interface traps (Figure 2.21) such high value of Q_f should lead to much lower $\rho_{eff,max}$ values than the one reported on the experimental sample (even if Q_f is negative, because in that case a low resistivity accumulation layer is formed below the oxide between the conductors). On the other hand, the simulation data presented in Figure 2.38b indicate that for such high $|Q_f|$ value, the trap density that must be reached to obtain ρ_{eff} values in the 1 kΩ.cm range should be in the low 10^{10} $/cm^2/eV$. This is typically what can be expected in thermal or bonded oxides [65].

- For wafer BH3, a poor quality oxide layer of similar thickness was deposited by APCVD. Due to the deposition process of this oxide, higher Q_f and D_{it} values are expected. A high fixed charge density is indeed clearly seen in the figure (very low V_{FB}). It is also noticed that, despite a higher Q_f density than in the case of SH1, the value of ρ_{effmax} is even higher. This suggests that a higher trap density is present for the case of the deposited oxide, and that those traps contribute to increase $\rho_{eff,max}$ by absorbing free carriers from the substrate surface.

- For the last presented wafer (BH4), a good quality thermal oxide was first grown and then covered by a thick (1 μm) APCVD oxide. The oxide-substrate interface

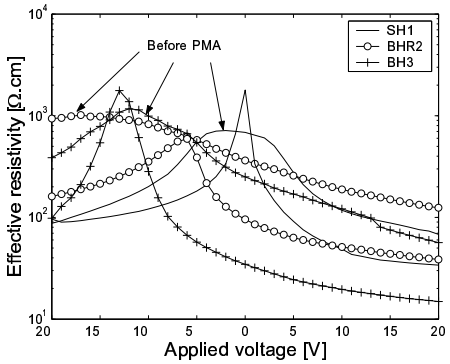


Figure 2.41: Effect of a postmetallization anneal (PMA) in forming gas on ρ_{eff} for HR wafers with different oxide qualities.

is then in that case characterized by a low D_{it} density due to the thermal oxidation and a high resulting $Q_{f,equ}$ ($\sim$ 1.8x10^{11} $/cm^2$) because of the low quality deposited oxide. Both elements contribute to a strong reduction of ρ_{eff}, similarly as for the HR SOI wafers processed with multilayer technologies (Figure 2.36).

B. Effect of postmetallization anneals

As explained earlier, hydrogen atoms are known to passivate traps at the SiO_2/Si interface during a postmetallization anneal performed in a forming gas ambient. In our case, postmetallization anneals are then expected to have a negative impact on the value of ρ_{eff} since they contribute to reduce the effective density of electrically active traps. This effect is demonstrated in Figure 2.41, which reports the effective resistivity measured on wafers SH1, BHR2 and BH3 before and after a PMA. For the three wafers, the oxide layer consisted in the BOX of a HR SOI wafer (BOX oxide), a wet thermal oxide and a APCVD oxide, respectively. It is seen that:

- for all wafers the impact of V_a is significantly lower before the PMA, which demonstrates the higher density of traps before the PMA;
- for all wafers the higher trap density before the PMA results in a higher value of ρ_{eff} at 0 V (except for wafer SH1, which has a V_{FB} close to 0 V);
- the value of $\rho_{eff,max}$ is increased after the PMA in the case of wafers SH1 and BH3, which is interpreted as being related to a reduction of Q_f during the anneal.

The simulated data presented in Figures 2.38 and the experimental data presented in Figures 2.40 and 2.41 strongly suggest that increasing the amount of

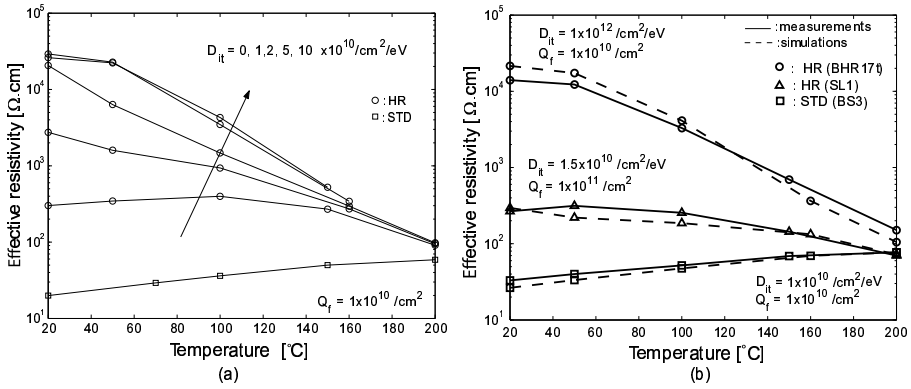


Figure 2.42: (a) Simulated impact of temperature on ρ_{eff} for a fixed 142 nm-thick t_{ox} and a fixed 1x10^{10} $/cm^2$-Q_f (HR: varying D_{it} values, STD: D_{it}=1x10^{10} $/cm^2/eV$) and (b) comparison between simulation and experimental data

traps at the SiO_2/Si interface in HR oxidized wafers might be a reliable solution to reduce the negative impact of fixed charge density and applied bias on the values of the wafer effective resistivity. This could be accomplished, for instance, by processing the oxide growth/deposition in conditions that favor the creation of those traps. According to worst case (Q_f=1x10^{12} $/cm^2$) simulated data, the D_{it} level must be at least on the order of 1x10^{12} to completely get rid of surface parasitic conduction and bias effect. It is furthermore important to keep in mind that in order to be of useful interest this value must remain stable, i.e. it may not be altered by subsequent process steps (thermal anneals, gate oxidation, PMA) endured by the wafers. Results presented in Figure 2.41 suggest that this is not going to be the case using conventional growth/deposition methods, for which D_{it} values are reduced by more than one order of magnitude [33] after a PMA. Alternate methods should therefore be considered. One of them consists in passivating the Si substrate with a layer of polysilicon. This approach is thoroughly investigated in the next chapter.

2.5.6 Temperature

This section is intended to investigate the effect of temperature (T) on the effective resistivity of HR silicon substrates and the suitability of such wafers for high temperature applications. Atlas simulations of CPW lines were performed on an oxidized HR Si substrate by varying T up to 200°C and by considering a constant oxide thickness of 142 nm, a constant Q_f density of 1x10^{10} $/cm^2$ and a varying

trap density. The simulation results are plotted in Figure 2.42a. Additional simulations were also performed in the case of a standard resistivity substrate (with Q_f=1x10^{10} $/cm^2$ and D_{it}=1x10^{10} $/cm^2/eV$ with the same trap distribution as in Section 2.5.5). The results are included in the figure for comparison.

Not surprisingly, it is seen that substrates with the highest interface trap density exhibit the highest values of effective resistivity in the lower temperature range, i.e., below ~ 150 ℃. However, as the temperature is increased the substrate resistivity is lowered and so is the impact of D_{it}. The latter effect results from a convergence of the ρ_{eff} *vs* T curves at high temperatures. This convergence is also observed for the standard resistivity substrate curve, indicating that ρ_{eff} becomes independent on the interface trap density and the substrate doping.

The decreasing impact of substrate doping and of interface trap density on ρ_{eff} can be both simply explained by an increase of majority carriers inside the silicon substrate as T is raised. This effect is due to an increase of the intrinsic carrier concentration ($n_i(T)$) [1] as shown in the following expression [33]:

$$n_i(T) = 3.3x10^{15}T^{3/2}exp\left(-\frac{E_g}{2kT}\right) \tag{2.31}$$

$$\tag{2.32}$$

where E_g is the width of the silicon band gap, k is Boltzmann's constant and q is the electron charge. The majority carrier concentration inside the silicon is then given by

$$p = n_i exp\left(\frac{q\phi_F}{kT}\right) = \frac{N_a + \sqrt{(N_a)^2 + 4n_i^2}}{2} \tag{2.33}$$

The majority carrier density obtained using the above expressions is represented in figure 2.43 as a function of T for varying doping values. These data show that for a given doping level, the majority carrier density is equal to N_a (which is independent of T) at lower temperatures and becomes equal to n_i (and thus an increasing function of T) above a certain temperature point that is N_a dependent. These trends result in an increase of p with T at high temperatures and a suppression of the doping level influence on p: at high temperatures, the silicon becomes intrinsic (i.e., n=p=n_i), which explains the trends observed in Figure 2.42a. For the standard resistivity substrate, the slight increase of ρ_{eff} with T might be explained by a reduction of the carrier mobility for increasing temperatures.

The effect of temperature on ρ_{eff} was also verified on three experimental samples, as shown in Figure 2.42b: a standard resistivity bulk wafer with a 1μm-thick

[1] The temperature effects on interface trap cross section as well as emission and capture time described in [33] is assumed to play a minor role here and is therefore not discussed.

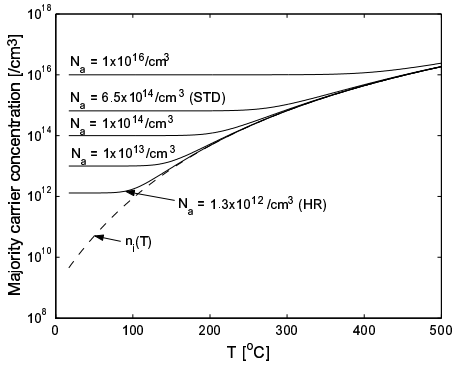


Figure 2.43: Illustration of the majority carrier concentration in the Si substrate as a function of temperature and doping level.

PECVD oxide (BS3), a silicon-etched HR SOI wafer (SL1) and a HR bulk wafer with a 3 μm-thick PECVD oxide (BHR17tb). In the latter case the trap density at the SiO_2/Si interface was increased by passivating the Si substrate with a 20 nm-thick LPCVD polysilicon layer before oxidation. The trap density was then further increased by submitting the sample to a 3h-long thermal anneal in neutral ambient (N_2) at 900°C. For the three wafers, additional simulations were performed by considering realistic values of Q_f and D_{it} (detailed in Figure 2.42b), and adjusting the substrate doping level. Both simulation and experimental results are plotted in Figure 2.42b. It is seen that a good correlation exists between the data. The figure also demonstrate both theoretically and experimentally that when the interface trap density is significant (i.e., $>1\text{x}10^{12}$ $/cm^2/eV$), the effective resistivity of oxidized HR wafers remains higher than 10 kΩ.cm (i.e., the substrate remains lossless) up to a temperature close to 60°C (T_{10k}) and remains higher than 3 kΩ.cm (i.e., the substrate remains quasi-lossless) up to a temperature close to 100°C (T_{3k}). These are much better achievements than in the case of the unpassivated HR wafer and demonstrate the possible use of HR silicon wafers for high temperature applications up to 100°C. Higher temperatures could also be targeted if non negligible substrate losses are tolerated. However, as those losses are mainly related to the free carrier concentration inside the substrate it is expected that much better performance could be achieved at higher temperature by using purely dielectric substrates, such as fused silica or sapphire. The performance of those exotic substrates and that of alternate line topologies are discussed in the next section.

2.6 CPW on HR SOI vs other technologies: who wins?

2.6.1 Proposed techniques to reduce the substrate influence

It was demonstrated in the previous sections that due to the semiconductor nature of their substrate, oxidized HR silicon wafers suffer from parasitic surface conduction below the oxide, which makes the substrate *effective* resistivity highly dependent on process-related parameters (such as the equivalent fixed charge density, the interface trap density, the total oxide thickness, the metal work function ...) or also on operation conditions (V_a). In worst case situations (high Q_f and high $|V_a|$, low D_{it} and low t_{ox}), this effect was shown to reduce the effective resistivity of the substrate by more than two orders of magnitude. It was also demonstrated that those parasitic effects could all be prevented by passivating the Si substrate with a trap-rich layer, such as polysilicon. In that case, the nominal substrate resistivity can be fully recovered.

It must be kept in mind that a variety of alternatives have also been proposed in the literature to reduce or suppress substrate losses in CMOS technologies. As already mentioned, one of them consists in using lossless dielectrics, such as sapphire and quartz. The silicon-on-sapphire (SOS) technology has been around for quite a long time [67] and is currently exploited by several renowned foundries (such as Peregrine Semiconductor and Oki Semiconductor) even if it still lacks proof of large-scale manufacturability. The limited success of this technology is essentially due to the difficulties encountered in epitaxially growing uniform, defect-free crystal silicon on the Al_2O_3 lattice, which increases the cost of SOS wafers [68, 69]. A cheaper alternative to SOS substrates consists in using fused silica (glass), commonly (and mistakenly) named quartz. The fabrication of silicon-on-quartz (SOQ) wafers has been investigated by SOITEC during these past years. The main challenge in this case is the thermal expansion coefficient mismatch between quartz and silicon [70], preventing a full compatibility of SOQ wafers with standard CMOS processing.

At a process level, many techniques have also been implemented to eradicate the parasitic influence of the substrate on the RF performance of passive devices. Such techniques typically consist in 1) local removals or thinning of the lossy silicon substrate during or after process [71], 2) substrate screening by providing a metallic shield [72] or 3) increase of the insulator thickness between the passive elements and the lossy substrates with either thicker oxide layers [73] or post-process BCB [53] and polyimide modules [74]. The main drawback of these techniques is that they qre not straightforward, which adds to the total fabrication cost. It therefore appears that in currently available multilayer technologies the

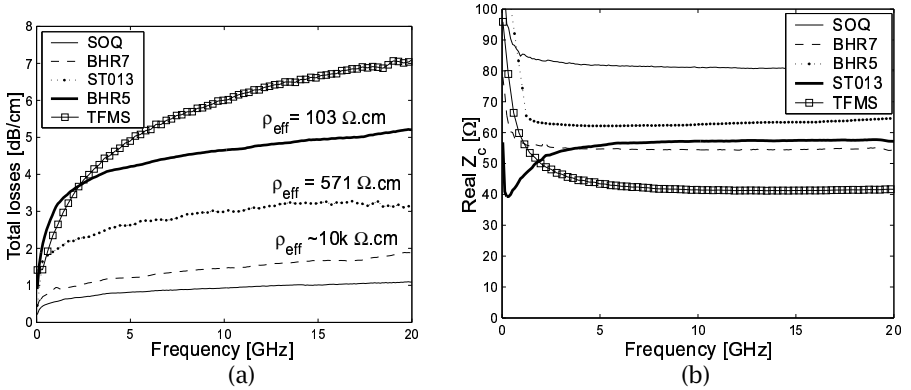


Figure 2.44: Extracted values of (a) line attenuation constant and (b) real part of characteristic impedance for CPW and TFMS lines from different technologies.

cheapest solution to eradicate substrate losses consists in using one (or two) of the metal layers to fabricate a bottom ground plane and other metal levels to propagate the signal. This configuration is particularly well suited to the microstrip line topology, commonly referred to as thin-film microstrip lines (TFMS) [75].

In the following sections, the RF performance of CPW lines on silicon wafers is compared with that of SOQ and TFMS technologies.

2.6.2 *Performance comparison between CPW lines on SOQ, on PolySi-passivated HR Si substrates and TFMS line topology*

Figure 2.44a displays the total RF losses obtained on four CPW structures of identical geometry (Set b) from distinct wafers: one fused silica substrate (SOQ), one polysilicon-passivated HR silicon substrate (BHR7), one HR SOI wafer issued from ST013 technology (ST013) and one HR bulk silicon wafer covered with a 350 nm-thick thermal oxide and a 1 μm-thick ((Q_f-rich) deposited oxide (BHR5). The CPW lines were fabricated using 1 μm-thick patterns in Al, except for the ST013 structure which was fabricated using copper on the 6th metal level (M6). In that case, additional hole patterns were included in the structures to comply with design rules (metal density), leading to a reduction of effective central line width and slightly increased conductor losses. Experimental results obtained on a TFMS line from ST013 is included in the figure too. For the TFMS line, a 7 μm-wide strip was designed on the stacked M6 (copper) and AluCap (Aluminium) layers. The ground plane was obtained using the first two metal levels, resulting in an equivalent oxide thickness of 2.9 μm. For all Si-based CPW lines the extracted value of the substrate effective resistivity is provided in the figure.

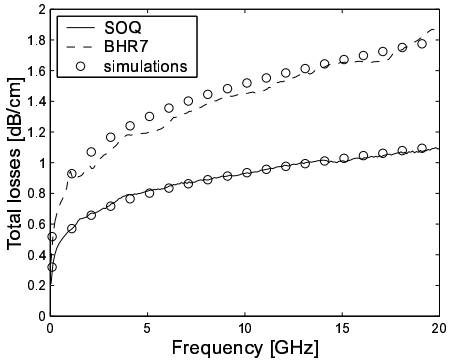


Figure 2.45: Comparison between simulated and measured data for wafers SOQ and BHR7. The simulation results were obtained using Heinrich's expressions and by considering lossless substrates.

2.6.2.1 PolySi-passivated substrates vs *SOQ wafers*

Figure 2.44a provides a clear evidence that substrate passivation significantly reduces substrate losses, since losses observed on wafer BHR7 appear to be well below those obtained on wafers BHR2 and ST013 for a similar line geometry. Even better results are observed for wafer SOQ, which must be interpreted as due to either higher substrate losses and/or conductor losses for the passivated silicon substrate. Simulation results obtained using Heinrich's closed form expressions [37] and by considering lossless substrates (for an aluminium conductivity (σ_{Al}) of 3.2x10^7 S/m and a metal thickness of 1 μm) actually demonstrate that substrate losses can be completely neglected in the case of the passivated substrate. Indeed, the results displayed in Figure 2.45 show than an excellent match is obtained between simulated and experimental data for both SOS and BHR7 wafers by solely considering conductors losses.

The loss difference observed between wafers SOQ and BHR7 can then only be explained by conductor loss variations. This fact is actually related to the much lower relative dielectric constant of fused silica ($\epsilon_{fs} = 3.8$) than that of silicon ($\epsilon_{fs} = 11.7$). Indeed, for low loss substrates total losses can be expressed by:

$$\alpha_{tot} = \alpha_{cond} + \alpha_{sub} \tag{2.34}$$

$$\approx \frac{R_s}{2}\sqrt{\frac{C_{sh}}{L_s}} + \frac{G_{sh}}{2}\sqrt{\frac{L_s}{C_{sh}}} \tag{2.35}$$

$$\approx \frac{R_s}{2Z_c} + \frac{G_{sh}}{2}Z_c \tag{2.36}$$

where R_s, L_s, G_{sh} and C_{sh} are the elements of the line distributed circuit and $Z_c = \sqrt{L_s/C_{sh}}$ is the high frequency approximation of the line characteristic impedance. For a lossless dielectric substrate ($\alpha_{sub} \approx 0$) this expression reduces to:

$$\alpha_{tot} \approx \frac{R_s}{2}\sqrt{\frac{C_{sh}}{L_s}} \tag{2.37}$$

and shows, as observed, that for a given geometry, conductor losses are a decreasing function of the line effective dielectric constant.

As illustrated in Figure 2.44b, the lower permittivity of fused silica leads to a higher characteristic impedance of the CPW line on wafer SOQ compared to that on wafers BHR2 or BHR7. The characteristic impedance value on SOQ could be made closer to that on the silicon substrate by reducing the spacing between the conductors, thus without significantly impact on the series resistance. This means that equivalent CPW lines (in terms of losses and characteristic impedance) could be obtained on SOQ and on Si substrates with smaller dimensions in the case of fused silica. This also indicates that for a given level of line losses higher integration of passives is possible on SOQ substrates.

2.6.2.2 CPW vs *TFMS lines*

The results presented in Figure 2.44a indicate that for the chosen line geometries the TFMS line outlines much higher losses than CPW lines with either passivated or unpassivated substrates. This is of course associated with the smaller geometry of the TFMS line and the higher line series resistance. For the case of the ST013 technology, the impacts of strip width and metal thickness on the conductor losses and on the line characteristic impedance are outlined in Figure 2.46. Using rough extrapolations, it is anticipated from those data that a 50 Ω-Z_c TFMS (with W_s<7 μm) line using the AluCap layer would lead to losses ranging between 6 ($W_s = 7\ \mu m$ M6+AluCap) and 7.5 dB/cm (extrapolated for $W_s = 2\ \mu m$ M6+AluCap), resulting in significantly higher losses than in the case of a Set b CPW line on the same technology.

Series losses in TFMS lines can be reduced by either increasing 1) the metal conductivity (advances in that field have been the replacement of aluminium with copper for the interconnects), 2) the conductor thickness (additional thick layers of aluminium on top of the last metal level (AluCap in ST013 technology) are now commonly used) or 3) the strip width. In this last case, one should recall that for a given insulator thickness (t_{diel}), and thus for a given technology, the strip width of the TFMS line is usually determined by characteristic impedance consid-

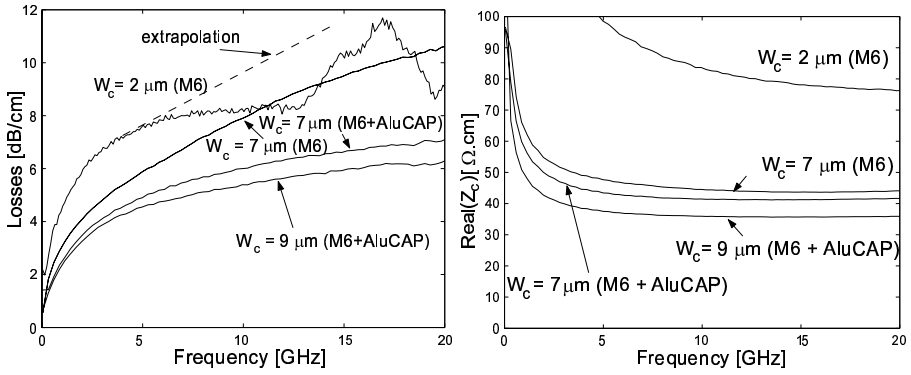


Figure 2.46: Extracted values of (a) line attenuation constant and (b) real part of characteristic impedance for TFMS lines of various geometries.

erations. Therefore, for a specified Z_c value an increase of the line width can only be achieved along with a corresponding increase of t_{diel}, and thus, by increasing the number of IMD and metal levels in the back-end of line process. It therefore appears that the properties of the TFMS lines in multilayer technologies are critically conditioned by the technology in which they are implemented. For CPW lines on Si substrates however, conductor losses are not so much constrained by technological parameters for two main reasons:

- First, both the central conductor width and the spacing between conductors (S) can be independently adjusted to achieve the desired impedance value. This provides more flexibility when designing the CPW structures and enables designers to reach higher W_s for a given Z_c target.

- Second, there is a significant difference in the number of metal levels that can be used in both structures. In a TFMS line made with a multilayer technology, the entire stack of metal levels and IMD layers must be divided to successively form the ground plane, the dielectric insulator *and* the top conductors. In the case of CPW lines, all metal levels may be stacked in order to reach the highest value of metal thickness, and thus the lowest series resistance. This point is particularly interesting at lower frequencies (i.e. below 1~2 GHz) where the skin depth is higher than several microns. For instance, the top conductors (M6+AluCap) of TFMS lines in ST013 technology is 1.8 μm and the total thickness of the M1-M6+AluCap stack is close to 5.5 μm. This indicates that for similar line cross dimensions, CPW lines can be fabricated with much lower series losses than TFMS lines, thus conferring a significant advantage of CPW lines over TFMS lines.

Figure 2.47 displays the losses *vs* ρ_{eff} chart and indicates how CPW losses vary with ρ_{eff} for two geometries (Sets b and e) and a varying aluminium (triangles) thickness. The graph is similar to the one presented in Figure 2.16 (Section 2.4 in which additional experimental data have been plotted from samples BHR5, BHR7, ST013 and TFMS. For all measured CPW lines, the effective resistivity was varied by applying a DC bias on the central conductor. A good matching is observed between the experimental and the simulated Set b data with $t_{Al} = 1\ \mu m$ (except for ST013 due to the hole patterns), supporting the accuracy of the simulations.

The figure shows that the 50 Ω-Z_c TFMS line on the multilayer technology (ST013) produces higher losses than CPW lines of Set b on silicon as long as the substrate effective resistivity is lower than approximately 100 Ω.cm. This indicates that TFMS lines offer better performance than wide CPW lines when standard resistivity substrates are used and lower performance when HR substrates are used. In the latter case the loss reduction is higher than 60 % and 80 % for unpassivated (ST013) and passivated (BHR7) substrates, respectively. For comparable structure geometries however (Set e) conductor losses drastically increase, thus reducing the benefit gained from using CPW lines. Nevertheless, in this case an increase of the conductor thickess provides a significant reduction of conductor losses, which is much more pronounced than in the case of wide structures (Set b). In particular, it is seen that for the ST013 technology, a CPW line from Set e with a 5 μm-thick stack of copper (asterisks) ($\sigma_{Cu} \sim 4\text{x}10^7\ S/m$) interconnects leads to conductor losses close to 4 dB/cm at 10 GHz on a passivated Si substrate. This represents losses that are more than 40 % lower than on the equivalent 50 Ω TFMS structures with a similar strip width.

The performance of TFMS lines could however be enhanced if the total dielectric thickness and strip width were increased, such as in post-process above IC modules [75]. Future generations are therefore expected to provide significant improvements in that field, since the 2005 ITRS Roadmap predicts that the number of metal levels should reach 14 by the year 2016 [76]. Assuming an average dielectric thickness of 1 μm per IMD layer (such as in ST013), it means that a 50 Ω-Z_c TFMS line could be made wider than 15 μm. In that case, series losses could be drastically reduced. However, as explained above, conductor losses in CPW lines will also be significantly reduced, since they will be made by stacking an even larger number of metal layers.

The results obtained in this section lead to the following conclusions regarding the design of transmission lines using a conventional (i.e., without above-IC or post-process modules) multilayer CMOS technologies:

· As surface-passivated HR Si substrates behave like lossless substrates, they com-

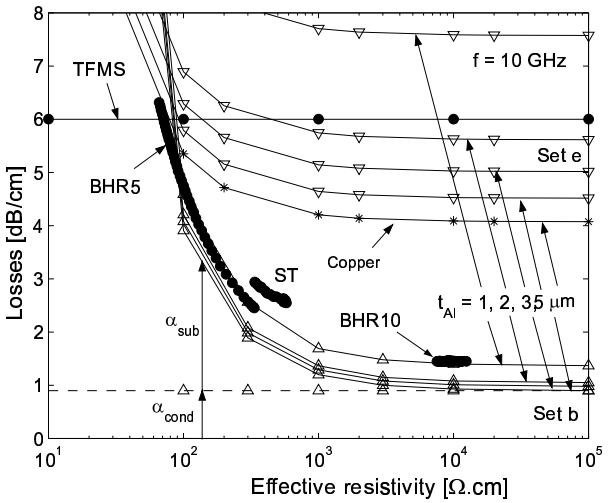


Figure 2.47: Simulated and extracted α_{tot} *vs* ρ_{eff} for CPW lines of different geometries and one TFMS line at 10 GHz.

pete in terms of RF performance with dielectric substrates such as silicon-on-quartz (fused silica) or silicon-on-sapphire (SOS) wafers. However, the lower dielectric constant of quartz and sapphire leads, for a given characteristic impedance value and loss level, to smaller line dimensions thus allowing higher integration in those technologies.

· In current multilayer technologies, TFMS lines present lower losses than similarly sized CPW lines when using standard resistivity substrates. When HR Si are used, the opposite is true even in unpassivated substrates. In that case, conductor losses in CPW lines can be significantly reduced by either stacking all available metal levels or increasing the central conductor width (to the expense of surface layout consumption). Both techniques can clearly not be applied in the case of TFMS lines, for which the strip width is the main factor determining the value of the characteristic impedance and for which a minimum number of IMD layers must be inserted between the top and ground conductors. This confers significant advantages to the CPW over the TFMS line topology, which should persist even in future technologies with higher numbers of metal layers.

2.7 Effect of parasitic substrate surface conduction on other planar devices

It was demonstrated in the previous sections that surface conduction at the substrate surface leads to a drastic reduction of the substrate effective resistivity in the case of CPW lines on oxidized HR silicon or SOI wafers, thus significantly degrading the performance of the structures in terms of RF losses. We now intend to demonstrate that this phenomenon can also deteriorate the RF performance of other types of passives, such as crosstalk structures and inductors. More precisely, the impact of parasitic conduction underneath the oxide is evaluated in the coming sections on the crosstalk properties of oxidized HR substrates and on the quality factor of inductors on such substrates. For this purpose, the structures are analyzed as a function of the bias applied on the metallic conductors. These measurements are also compared with the ones obtained on identical structures from an oxidized, polySi-passivated HR Si substrate.

The structures evaluated in the coming sections exclusively originate from the following 5 home-processed wafers:

- BHR5: 300 nm-thick thermal oxide+1 μm-thick APCVD oxide,
- BHR7: 360 nm poly LPCVD+30 nm-thick thermal oxide+1 μm-thick APCVD,
- BS3: 1μm-thick APCVD oxide on standard resistivity wafer,
- soitec1: HR SOI with oxidation of silicon film, resulting oxide thickness: 450 nm,
- SOQ: fused silica,

and the following 2 wafers processed in commercial foundries:

- Xfab: HR SOI technology with 3 metal levels,
- ST013: HR SOI technology with 6 metal levels.

All home-processed wafers received a 1 μm-thick metallization. These technological details are summarized in Table 2.4.

2.7.1 Crosstalk structures

2.7.1.1 Introduction

Substrate crosstalk reduction and isolation are critical areas of concern for SoCs applications. It is generally considered that when digital and analogue circuits are

Table 2.4: Technological details of the wafers studied in this section.

Wafer	Substrate resistivity	Passivation layer	Oxidation	Metal layer
BHR5	HR	/	300 nm thermal + 1 μm APCVD	M1: 1 μm Al
BHR7	HR	360 nm polySi	30 nm thermal + 1 μm APCVD	M1: 1 μm Al
BS3	20 Ω.cm	/	1 μm APCVD	M1: 1 μm Al
soitec1	HR SOI	/	BOX + 300 nm thermal	M1: 1 μm Al
SOQ	Fused silica	/	/	M1: 1 μm Al
Xfab	HR SOI	/	Techno Xfab with 3 metal layers	
ST013	HR SOI	/	Techno ST013 with 6 metal layers	

co-integrated, most of the noise 1) is generated by the digital parts, 2) is injected into the substrate and 3) disturbs the analogue sub-circuits [1]. Numerous studies have thus been performed to either reduce the mechanisms of noise generation [77] or substrate coupling [48], [78], [79]. The former investigations mostly rely on circuit design strategies, while studies performed to reduce substrate coupling are usually concerned with technological aspects. In that field it is interesting to notice that many authors concentrate their effort on reducing the crosstalk by introducing guard rings or grounded shields between coupling pads. The most efficient shields are therefore the ones that almost completely isolate the pads apart, forming close-to-ideal Faraday cages [79,80]. However, one should be aware that this substrate crosstalk reduction method is only efficient because it deviates the noisy signal to the ground. This is achieved by a pad-to-ground capacitance: the higher the capacitance, the better the shield. One could therefore expect that the implementation of such shields could

- have a negative impact the overall performance of circuits in which parasitic capacitances to ground are critical,
- increase load capacitances in digital subcircuits, to the cost of higher dynamic power consumption.

Similar comments also apply to those techniques that consist in reducing substrate crosstalk by inserting a ground plane below the buried oxide (BOX) of SOI wafers. This was recently achieved by introducing a metal layer [81] in the SOI structure below the BOX or by reducing the substrate resistivity at a very low level [82]. Alternate solutions that do not increase circuit-to-ground capacitance while reducing substrate crosstalk consist in improving the isolation properties of

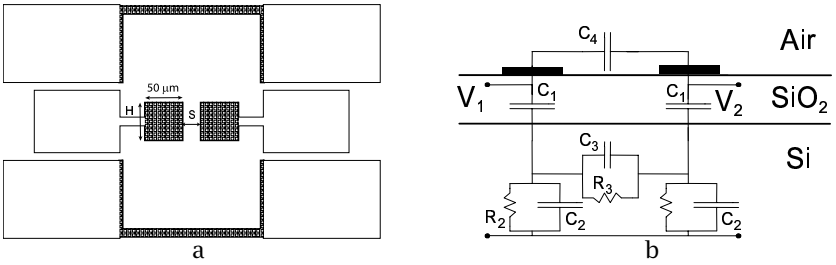


Figure 2.48: (a) Top view of the crosstalk structures analyzed in this work and (b) classical equivalent small signal circuit used to model such structure [48].

the substrate itself, which is investigated below.

2.7.1.2 Investigated structure and classical model

The crosstalk structure that is considered in this work to analyze the isolation properties of HR substrates is classically composed of two separate rectangular pieces of metal (coupling pads) that are each connected to the RF probing pads (Figure 2.48a). The spacing between the left (Port 1) and right (Port 2) coupling pads is noted S and their vertical height is noted H. All investigated structures are characterized by a constant 50 μm-width. The equivalent circuit classically used to model such structure is given in Figure 2.48b and is taken from [48], in which it was shown to accurately reproduce the frequency dependence of the substrate coupling inside oxidized *homogeneous* substrates, i.e. inside wafers with uniform values of substrate resistivity. As shown in Figure 2.49, a typical crosstalk *vs* f curve obtained with this model can be subdivided into three regions, separated by two characteristic frequencies, f_1 and f_2:

- The first region is concerned with frequency values smaller than f_1. In this frequency range, the AC potential at the substrate surface is at an intermediary value between that of the ground (0 V) and the one applied on port 1 (v_1). The pad-to-ground capacitance is in this case rather high and the signal applied on one port therefore only partly couples to the other port, resulting in a 40 dB/dec slope.

- The second region occurs for frequencies higher than f_1 and lower than f_2, which are respectively given by:

$$f_1 = \frac{1}{2\pi R_3 C_1} \tag{2.38}$$

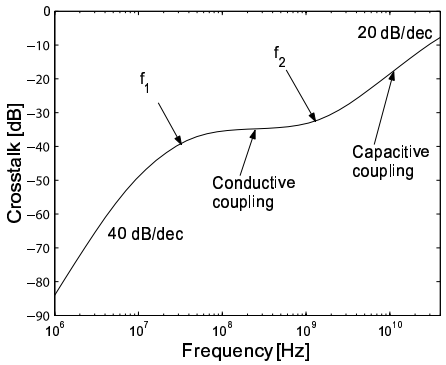


Figure 2.49: Typical crosstalk *vs* frequency curve obtained on an oxidized lossy Si substrate.

and

$$f_2 = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi \epsilon_{sub} \rho_{eff}} \tag{2.39}$$

As shown by the latter expression, f_2 corresponds to the dielectric relaxation of the substrate. For frequencies higher than f_1, the oxide becomes virtually transparent to the AC signal. The oxide capacitances (C_1) then behave as shorts in the model of Figure 2.48b. In this case the AC potential at the substrate surface is the one applied on the ports and the coupling inside the substrate is purely dictated by the substrate impedance ($R_2//C_2$). For $f < f_2$, R_2 is lower than its parallel counterpart ($1/(2\pi f C_2)$) and the coupling is therefore dominated by R_2 (conductive coupling). This results in a constant value of $|S_{21}|$ *vs* frequency dependence and a plateau level is observed between f_1 and f_2.

· In the third region, f is higher than f_2. In that case the substrate impedance ($R_2//C_2$) becomes independent on the substrate resistivity and is merely governed by C_2 since $1/(2\pi f C_2) < R_2$. The coupling between the pads is thus purely capacitive and exhibits a 20 dB/dec curve.

2.7.1.3 Impact of technological parameters on crosstalk

In order to draw some technological guidelines aimed at minimizing substrate crosstalk in real circuits, it is important to understand how technological parameters impact on the value of $|S_{21}|$. Briefly summarizing the work presented in [48], this section outlines the effect on crosstalk of three fundamental characteristics of oxidized wafers: the substrate permittivity, the substrate resistivity and the oxide thickness.

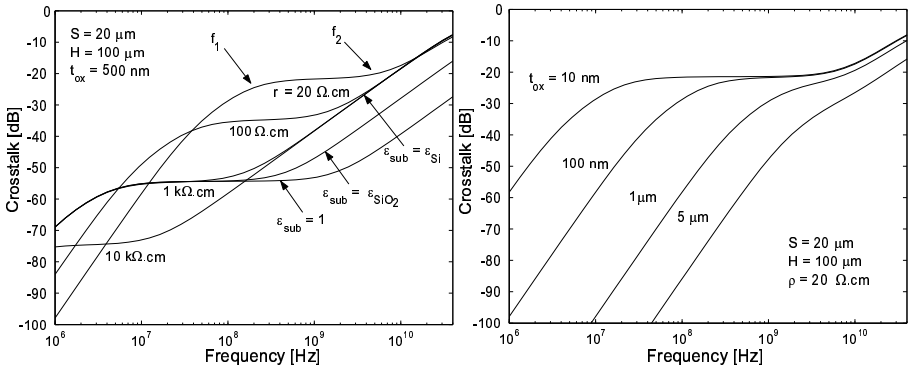


Figure 2.50: Illustration of the impacts of (a) the substrate resistivity and permittivity and (b) the oxide thickness on the crosstalk *vs* frequency curves according to the model presented in Figure 2.48b

.

· *Substrate permittivity.* The value of ϵ_{sub} dictates the value of C_2. It therefore merely impacts on f_2 and on the coupling level at frequencies higher than f_2. This is illustrated in Figure 2.50a, which displays some simulation results obtained with the model of Figure 2.48b and simple analytical formulas for pads dimensions of 100x50 μm^2, a spacing between pads of 20 μm, a substrate thickness of 750 μm, a substrate resistivity of 20 Ω.cm. No fringing fields toward the lateral ground planes were considered. The figure features some $|S_{21}|$ *vs* f curves that have been drawn for varying ϵ_{sub} values. It clearly appears that an effective way of reducing S_{21} is to use substrates with lower dielectric constant.

· *Substrate resistivity.* As shown in Eqs. 2.38 and 2.39, the value of the substrate resistivity simultaneously impacts on f_1 and f_2 (through R_3 and R_2, respectively), leading to a variation of the plateau level between f_1 and f_2. This is also highlighted in Figure2.50a, where it is seen that lower resistivity values leads to an increased coupling level. However, due to the slope difference in the regions where $f < f_1$ (40 dB/dec) and $f > f_2$ (20 dB/dec), it is also seen that a reduction of resistivity results in lower crosstalk levels below f_1. This is also observed in the experimental curves presented in Figure 2.51, which displays measured data obtained on structures from a standard (dashed lines) and HR (solid lines) SOI wafers from the multilayer ST013 technology and for two different values of oxide thickness. Once again, this occurs to the cost of higher pad-to-ground capacitances and thus of an increase of dynamic power consumption. Increasing the substrate resistivity therefore presents an interesting solution to simulta-

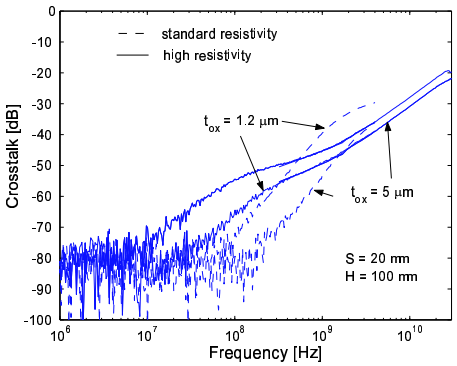


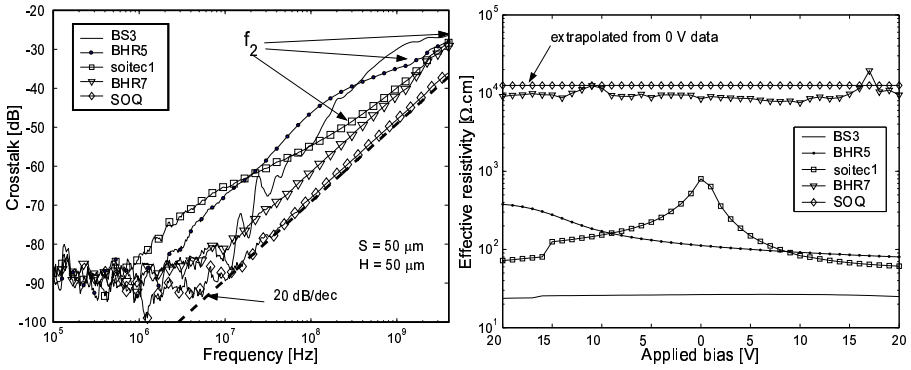
Figure 2.51: Measured crosstalk *vs* frequency curves on samples from a standard and a HR resistivity substrates from ST013 and for two values of oxide thickness.

neously reduce pad-to-ground capacitances at low frequencies and pad-to-pad coupling at high frequencies.

- *Oxide thickness.* As implicitly stated in Expression 2.38, f_1 is directly proportional to the oxide thickness, which is highlighted in Figure 2.50b. The figure clearly indicates that an increase of the oxide thickness may have a significant positive impact on the crosstalk for values below f_2. This is also outlined on the experimental data of Figure 2.51. For both wafers the structures were realized in either M1-M2 (with $t_{ox} = 1.2\ \mu m$) or M5-M6 (with $t_{ox} = 3.2\ \mu m$). It is seen that regardless of the substrate resistivity, a significant crosstalk reduction ($\simeq$ 15 dB) is obtained by increasing t_{ox} at frequencies below f_1.

2.7.1.4 Effect of inversion layer on crosstalk level in oxidized HR substrates and revised model

Figure 2.52a displays other experimental crosstalk data obtained on the 5 home-processed wafers up to 4 GHz. It is obvious from that picture that the different wafers outline very distinct values of substrate resistivity since dielectric relaxation (f_2) takes place under different frequencies on those wafers. From Eq. 2.39 it is concluded that $\rho_{eff,BS3} < \rho_{eff,BHR5} < \rho_{eff,soitec1} < \rho_{eff,BHR7}$, which is in perfect agreement with effective resistivity values extracted from CPW line measurements at 0 V (Figure 2.52b). The figure outlines the much better effective resistivity obtained on wafer BHR7, for which the value of f_2 is so low (below 10 MHz) that it corresponds to crosstalk values too small to be measured. For that wafer, an ideal 20 dB/dec curve is recorded throughout the entire measured fre-



(a) (b)

Figure 2.52: Measured (a) crosstalk *vs* frequency and (b) ρ_{eff} *vs* V_a curves on, respectively, the crosstalk structures and the CPW lines from the five home-processed samples.

quency range, similarly to the curve obtained from the lossless SOQ wafer. In this case also, the crosstalk is further reduced due to the lower dielectric constant of fused silica (3.7), and the associated lower substrate capacitance (C_3).

The relatively high value of the dielectric relaxation frequency observed on the HR wafers is obviously related to the presence of free carriers underneath the oxide, whose effect is to reduce the substrate *effective* resistivity. A closer look at Figures 2.51 (HR curves) indicates that this effect is also observed on the wafers with multilayer processing. Additional experimental data presented in Figure 2.53 further shows that this trend is independent on the geometry (H or S) of the structures. However, a reduction of f_2 is not the only effect associated with the presence of an inverted layer below the oxide. Indeed, this specific charge distribution at the substrate surface leads to a considerable inhomogeneity of the substrate RF properties, and in particular, of its resistivity. In other words, the resistivity at the substrate surface is different from the bulk resistivity, which changes the crosstalk frequency behavior for frequencies below f_1: it is indeed observed that for all structures measured on HR substrates and presented in Figures 2.51, 2.52a or 2.53, the slope of the $|S_{21}|$ *vs* f curves below f_1 is not 40 dB/dec but 20 dB/dec. The model presented in Figure 2.48b must therefore be revised to account for this effect.

We therefore propose in Figures 2.54a-c a modified version of that model, which accounts for surface charges at the SiO_2/Si interface in p-type HR substrates. In Figure 2.54a, the pads are assumed to be biased in inversion and a resistance (R_s) is added at the substrate surface to represent the effect of the inverted layer below

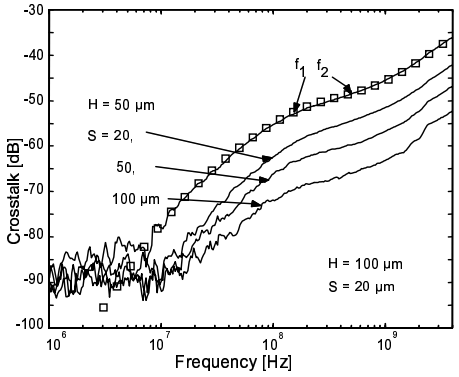


Figure 2.53: Measured crosstalk *vs* frequency curves on ST013 for structures with varying geometries.

the oxide. Two depletion capacitances (one for each pad) are also added between the inverted Si surface and the bulk. In Figure 2.54b only one pad (Port 1) is biased in inversion and the other (Port 2) is biased in accumulation. In that case the depletion region below the second pad no longer exists, but another one is formed at the pad edges (modeled by C_{d2}) between the accumulation and inverted regions below the oxide. As shown in Figure 2.55, such charge distribution was confirmed by Silvaco simulations, for a crosstalk structure with $t_{ox} = 1\ \mu m$ and a fixed charge density of 1x10^{11} $/cm^2$.

Figure 2.53 (squares) indicates that the model of Figure 2.54a can closely reproduce the experimental data obtained for $V_1 = V_2 = 0\ V$, and in particular, the 20 dB/dec frequency dependence below f_1. In this case the circuit element values were obtained by fitting the model onto the measured data and by considering a 10 kΩ.cm bulk resistivity (i.e. $R_{sub}C_{sub} = R_pC_p = \epsilon_{Si}\rho_{Si,bulk}$).

For this model, Eq. 2.39 becomes

$$f_2 = \frac{1}{2\pi R_s(C_p^{-1} + 2C_{d1}^{-1})^{-1}} = \frac{1}{2\pi\epsilon_{Si}\rho_{eff}} \tag{2.40}$$

since it is expected that for HR oxidized substrate $R_s << R_p$ and $C_{ox} >> C_p$. This indicates that a value of ρ_{eff} can be obtained once the model has been fitted onto the measurements. Using this extraction method the value of ρ_{eff} was found to be as low as 160 Ω.cm in the case of ST013 technology. This is roughly three times lower than the value obtained from CPW measurements (571 Ω.cm) on the same wafer, which is probably due to the fact that the oxide thickness was not considered in the present estimation while it is accounted for in the case of CPW lines (through $\epsilon_{r,eff}$ in Equation 2.12). However, this low ρ_{eff} value further demonstrates that

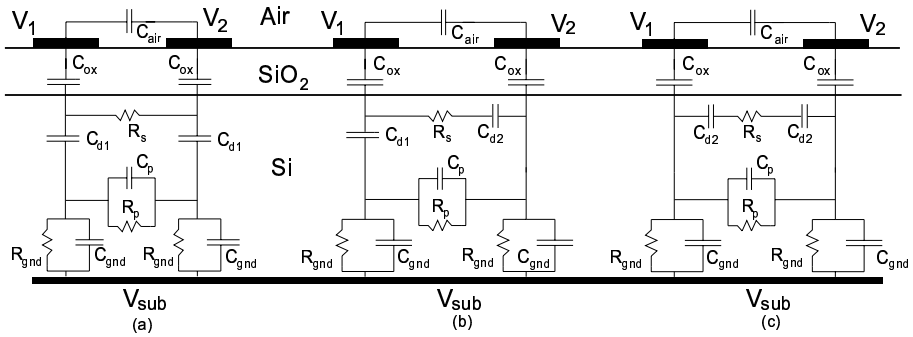


Figure 2.54: Proposed equivalent circuit of crosstalk structures to account for inhomogeneities at the substrate surface in p-type oxidized HR Si wafers when (a) the two pads are biased in inversion, (b) Port 1 is biased in inversion and Port 2 in accumulation and (c) both pads are biased in accumulation.

the inversion layer below the oxide also plays a negative impact on the isolation properties of oxidized HR p-type substrates. Figure 2.53 further indicates that this value seems to be relatively independent on the spacing between the pads, since the position of f_2 does not significantly vary with S.

To gain better insights on the effects of surface conduction on substrate coupling, additional measurements were performed by biasing the pads in the case of wafers ST013 (industrially-processed HR SOI wafer), BHR7 (polySi-passivated HR wafer) and soitec1 (home-processed HR SOI wafer). The results are plotted *vs* frequency (wafer ST013 only) and vs applied bias in Figures 2.56a and 2.56b, respectively. It is seen that applying a positive bias (i.e. $V_1 = V_2 = V_a > 0$ V) reduces ρ_{eff} to even lower values by increasing the inversion level underneath the pads, observable by the increase of the dielectric relaxation frequency in Figure 2.56b. The measurements also show that reducing the bias on both pads to negative values does not significantly impact on f_1 and f_2 but still significantly reduces $|S_{21}|$ below f_1. This can be explained by the depleted regions formed underneath the BOX between the accumulated pads and the inverted Si/SiO_2 interface. The depleted regions at the pad edges reduce the size of the inversion layer, thereby significantly decreasing its deteriorating effect on $|S_{21}|$. This charge distribution explains why an important crosstalk reduction is observed when only one of the pads is biased in accumulation (Figure 2.56b with $V_a = V_{a1} = -V_{a2} = 10$ V). Figure 2.56a indicates that these experimental data can be adequately modeled by using the equivalent circuits of Figures 2.54a, b and c and by adjusting only R_s from one model to the other.

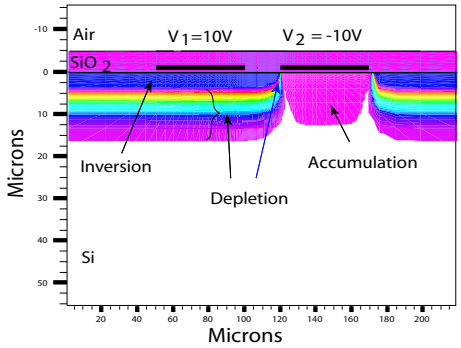


Figure 2.55: Charge distribution inside p-type HR Si substrates for a crosstalk structure with an oxide thickness of 1 μm, a Q_f density of 1x10^{11} cm^2, and one of the pads (Port 2) biased in accumulation.

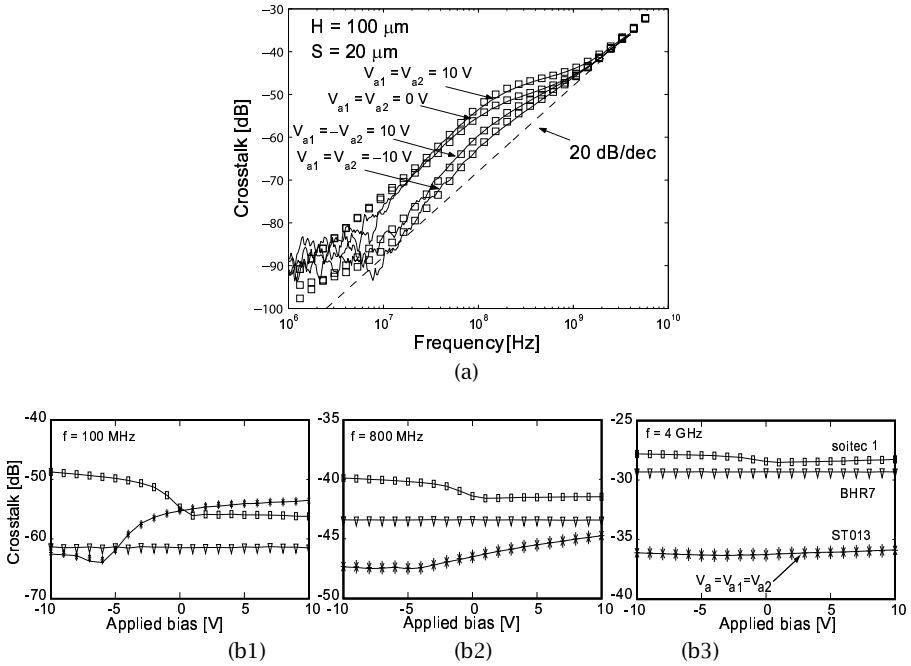


Figure 2.56: (a) Measured crosstalk *vs* frequency curves for varying bias values applied on Port 1 (V_{a1}) and Port 2 (V_{a2}). (b) Crosstalk *vs* bias curves for $V_a = V_{a1} = V_{a2}$ and for three different frequencies.

In the case of wafer ST013 Figure 2.56b also outlines crosstalk variations as high

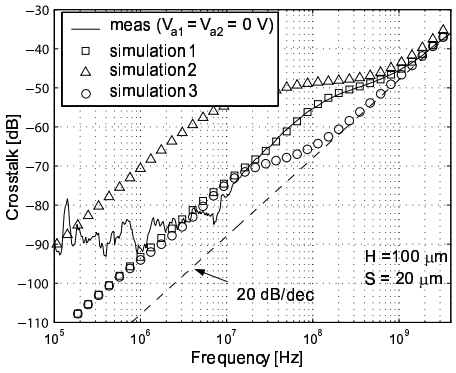


Figure 2.57: Measured and simulated crosstalk curve for wafer ST013, highlighting the significant crosstalk increase compared to a lossless substrate (20 dB/dec curve). Additional modeled data also highlight the variations of $|S_{21}|$ when t_{ox} is reduced to $t_{BOX} = 145\ nm$ (simulation 2) or when the surface resistivity is increased by a factor of 10 (simulation 3).

as 13 dB at 100 MHz as a function of V_a and indicates that for frequencies below f_1, the minimum value of $|S_{21}|$ is observed close to -6 V. This bias point corresponds to full depletion underneath the pads (as confirmed by low frequency C-V data made on the pads) and to an approximate Q_f value of 1x10^{11} $/cm^2$. The substrate surface is then strongly inverted and $|S_{21}|$ close to its maximum value when zero bias is applied on the pads. Decreasing fixed charge densities could therefore help reducing $|S_{21}|$ by shifting the threshold voltage closer to 0 V. However, as shown in the case of wafer soitec1 (for which a low negative Q_f value close to 1x10^{10} $/cm^2$ was found), this also makes the crosstalk level more sensitive to V_a around 0 V. It is interesting to notice that in the latter case, an accumulation layer is formed underneath the BOX due to the negative sign of Q_f. The crosstalk is therefore reduced when the pads are biased in inversion instead of accumulation. As shown in Figure 2.56b, the best results are clearly obtained on the polysilicon-passivated wafer, which as expected from CPW line measurements, exhibits no dependence with respect to the applied bias.

2.7.1.5 Discussion - crosstalk

As explained in [83], the main sources of substrate noise injection in digital CMOS technology consist in (i) ringing of power supply lines, (ii) capacitive coupling from switching source and drain nodes and (iii) impact ionization current. The noise generated by supply lines is directly related to the parasitic package inductance

and can therefore be strongly decreased by using proper packages (such as flip chip packages [84]). The parasitic inductance can then be reduced to values low enough (typically below 100 pH, [84], [83]) so that that the noise coupling from the active regions of MOSFETs becomes the dominant source of substrate noise, which is what is assumed in the forthcoming discussion.

In the case of SOI technology, these noise sources are expected to be reduced compared to bulk since they are capacitively coupled to the substrate through the buried oxide. However, as explained above and in [48], the oxide becomes transparent at frequencies higher than f_1 in lossy silicon substrates. In the case of ST013 technology, the value of f_1 is close to 100 MHz for coupling pads made in M1-M2 and a total 1.2 μ equivalent oxide thickness (Figure 2.57). This leads for instance to a crosstalk level at 100 MHz that is increased by 13 dB compared to the ideal case of a lossless substrate (exhibiting a 20 dB/dec in Figure 2.57).

As shown in Figure 2.50a, the value of f_1 is directly proportional to t_{ox}, and can therefore be increased by using thicker oxides. However, in real circuits having the active regions of MOSFETs as the dominant source of substrate noise injection, the isolating oxide layer is limited to the BOX of the SOI substrate, which is no more than 145 nm in current technologies. The simulation 2 curve in Figure 2.57 indicates that such a low value of t_{ox} should increase the crosstalk level below 100~200 MHz. At 100 MHz, the value of $|S_{21}|$ is 20 dB higher than in a lossless substrate. In future technologies, this trend is even expected to become worse since the ITRS Roadmap foresees a reduction of the BOX thickness to overcome short channel effects in FD devices and facilitate heat dissipation.

One possible way of solving these issues is to increase the resistivity of the substrate, which means that in the case of HR SOI wafers, parasitic conduction underneath the BOX must be avoided. This should result in a decrease of the substrate relaxation frequency (f_2). For instance in the case of ST013 technology f_2 could be made much lower than 1 GHz by simply increasing the substrate resistivity at the surface by a factor of 10. This is shown in Figure 2.57 (simulation 3 curve). In that case the value of $|S_{21}|$ is also strongly reduced between f_1 and f_2. In particular, at 100 MHz it is only 3 dB higher than the ideal case of a lossless Si substrate with the same oxide thickness.

The reduction of crosstalk level below 1 GHz is an important issue in mixed mode circuits, since it is known from previous studies that the frequency spectrum of digital circuit-generated substrate noise typically expands up to several hundreds of MHz, corresponding to multiples of the clock signal [83], [85] or circuit internal resonance frequencies [77]. As shown in Figure 2.52a, polySi-passivated HR wafers (BHR7) exhibit close-to-ideal behaviors in that frequency range.

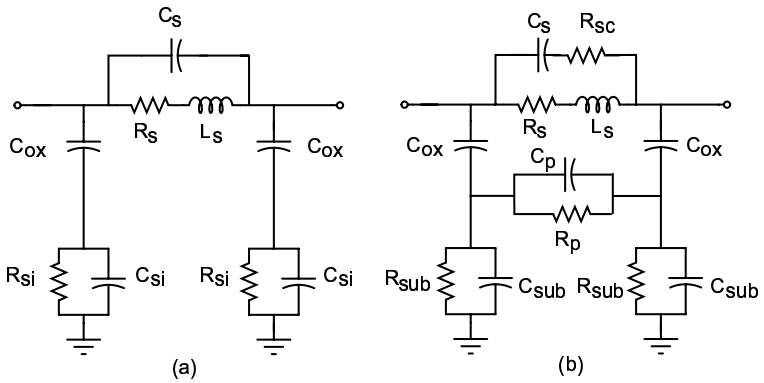


Figure 2.58: Classical small signal circuit used to model inductors on oxidized Si substrates.

2.7.2 Inductors

RF applications and circuits make an extensive use of inductors which are, for instance, especially useful to match input and output impedances in low noise amplifiers or to form the LC tank of Voltage-Controlled-Oscillators. It is known that the performance of such circuits are sometimes critically conditioned by the performance of the inductors themselves, which is quantified by the so-called *quality factor* (Q). The theoretical definition of the quality factor of an inductor is given by the following expression:

$$Q = 2\pi \frac{Peak\ Magnetic\ Energy - Peak\ Electric\ Energy}{Energy\ loss\ in\ one\ oscillation\ cycle} \tag{2.41}$$

The classical small signal equivalent circuit used to model integrated inductors is presented in Figure 2.58a [86] . On the basis of this model, it is possible to show that 2.41 can be simply rewritten as:

$$Q = -\frac{Im(Y_{11})}{Re(Y_{11})} \tag{2.42}$$

where Y_{11} is the input admittance of the equivalent circuit. This expression shows that all resistive elements in the model affect the value of the real part of Y_{11} and therefore directly contribute to a reduction of Q.

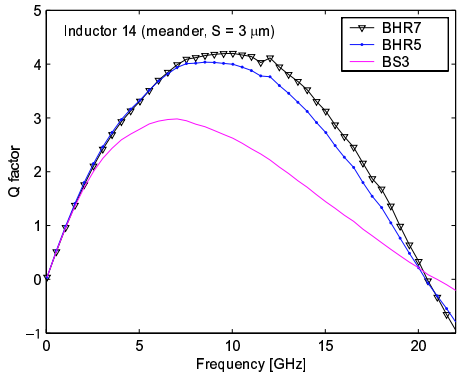


Figure 2.59: Q factor of spiral inductors measured on home-processed wafers.

2.7.2.1 *Negative impact of surface layer on the Q-factor: experimental evidences*

Figure 2.59 displays the Q factor measured on inductive elements from wafers BHR5, BHR7 and BS3, which are characterized by the same oxide thickness. As our home technology only allows one metal layer processes, the fabricated structures consist in simple meander inductors, which do not require underpasses. This kind of structure is used in distributed amplifiers where inductors are implemented into folded transmission lines in order to spare some layout space. The results shown in the figure are obtained on structures with 6 meanders and 16 μm-wide, 3 μm-spaced strips.

It is known from previous CPW and crosstalk measurement results that the inversion layer underneath the oxide causes severe parasitic conduction at the substrate surface of wafer BHR5 while it is completely absorbed by surface states in wafer BHR7. The data shown in the figure indicate that the effect of the parasitic conduction layer on the maximum value of the Q factor (Q_{max}) is very little for wafer BHR7 (a few percents). However, it is seen in Figure 2.60 that this effect becomes more pronounced when the spacing between the conductors is increased. Indeed, the differences in Q_{max} values between Wafer BHR7 and BHR5 increase with the strip spacing, showing that the inversion layer underneath the oxide plays a larger negative role in the Q factor degradation for wider spacing values. These preliminary experimental observations suggest that:

- non negligible electrical coupling takes place between adjacent strips of the inductor, inducing parasitic currents in the substrate, losses and Q_{max} degradation. To accurately take this effect into account an additional substrate im-

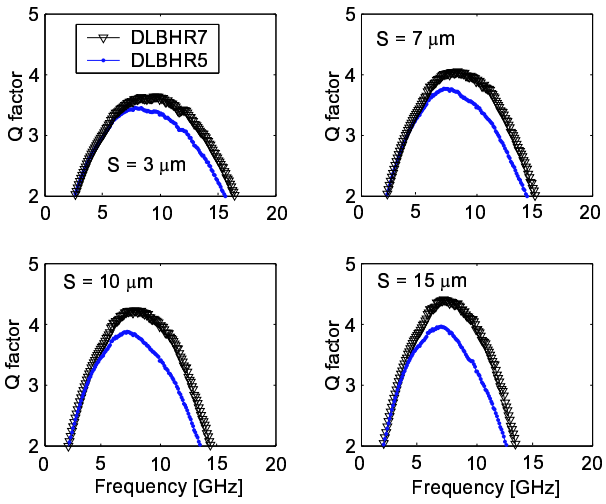


Figure 2.60: Q factor of spiral inductors measured on home-processed wafers for various inter strip spacing values.

pedance network (C_p and R_p) must be added in the model. This is illustrated in Figure 2.58b. The improvement provided by this additional substrate network is highlighted in a coming section.

- the coupling already occurs at frequencies lower than the inductor oscillation frequency, but has the worst impact at a frequency close to the one corresponding to Q_{max}.

- as the coupling generates horizontal electric field lines in the substrate, the Q factor is more sensitive to the parasitic inversion layer when the spacing between the conductors is increased. This is because a larger proportion of the field lines penetrates inside the substrate, inducing higher losses.

Additional measurements were also performed on spiral inductors from the Xfab multilayer technology. On that wafer, inductors with a variable number of turns (1, 3 and 5) were available, which were all measured as a function of the applied bias. The Q factor measured at 0 V for all inductors is presented in Figure 2.61a. It is seen that as the number of turns increase, the Q factor is severely decreased due, mainly, to increased series conductor losses. Figure 2.61b also outlines the relative variations of the Q factor as the bias is swept from -40 V to 40 V. For all curves, the normalization was performed by considering the -40 V data as the reference value, which corresponds to the bias point for which the lowest Q

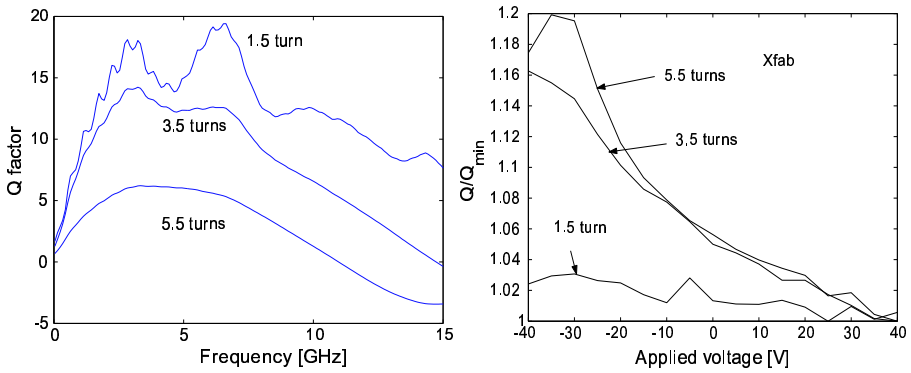


Figure 2.61: (a) Measured Q-factor of inductors with a varying number of turns on wafer XFab as a function of frequency. (b) Relative variations of Q_{max} as a function of the applied bias.

value was recorded. The figure clearly shows that as the number of turns increases the sensitivity of the inductor to the applied bias becomes more pronounced. This can be interpreted as follows: as the number of turns increases, the density of metallic strips inside the inductors increases also, which in turn raises the level of inter-strip electrical coupling and the sensitivity of the Q factor to the inversion layer. As explained in the following section, it is possible to roughly quantify the impact of the inversion layer by using the concept of an effective resistivity value.

2.7.2.2 Estimation of effective resistivity

Figure 2.62a and b display the inductance value ($-Im(1/Y_{12})\omega$) and the series resistor ($-Re(1/Y_{12})$) extracted from the measurements. The resonance effect is clearly visible in both graphs. Both parameters were also modeled using the small signal equivalent circuits presented in Figures 2.58a (model 1) and b (model 2), respectively. In the case of model 1, all elements of the circuit were directly extracted from the real and imaginary parts of the measured Y and Z parameters. The measurements were performed between 100 kHz and 40 GHz with two different VNAs. The conductor series resistance was however modeled by using the following formula:

$$R_s = \frac{R_{s,DC}.t}{\delta\left(1 - e^{\frac{-t}{\delta}}\right)} \tag{2.43}$$

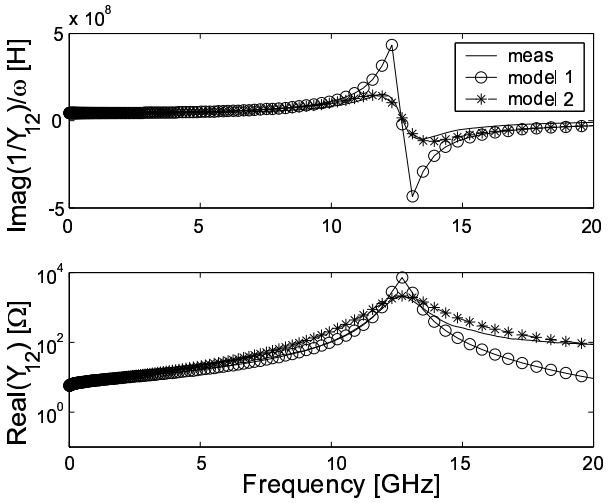


Figure 2.62: Measured and simulated Y data for an inductor from wafer XFab with 5.5 turns. The modeled data were obtained using the models of Figure 2.58a (model 1 curves) and b (model 2 curves).

which takes into account the frequency dependence of the skin effect [87]. In the case of model 2, the same parameter values were considered, except for the value of R_p which was tuned to accurately fit the modeled data on the measured curves. It was further assumed that:

- $C_s = C_{air} + C_{under}$ with C_{air} and C_{under} being respectively associated with the interstrip coupling in the air and with the underpass capacitance, which was estimated from the parallel plate capacitor expression,

- $C_{air} = C_p/\epsilon_{r,Si}$, where C_p is associated with the interstrip coupling in the Si substrate only and $\epsilon_{r,Si}$ is the relative dielectric constant of silicon.

It is seen that the resonance peaks in both figures are clearly overestimated by the model if the substrate resistance associated with inter-strip coupling is not considered. A much closer fit is indeed obtained using model 2, which is also visible on the modeled Q factor data (Figure 2.63).

By combining C_p and R_p it is possible to roughly estimate the effective resistivity of the substrate in a similar way as for crosstalk structures:

$$\rho_{eff} = \frac{C_p R_p}{\epsilon_{Si}} \tag{2.44}$$

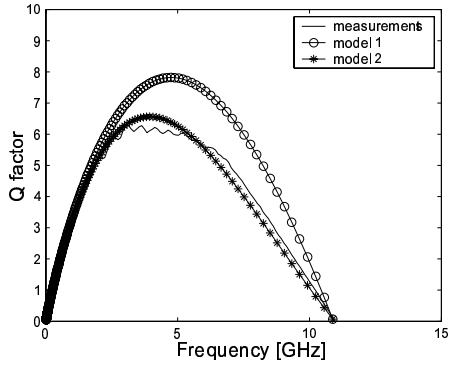


Figure 2.63: Comparison between simulated and modeled data for the Q factor of the 5.5 turn-inductor from Xfab technology. Model 1 and model 2 curves were obtained using the equivalent circuits of Figure 2.58a and b, respectively.

This method yields an approximate value of 53 Ω.cm in the case of the 5.5-turn inductor, which is consistent with the low value extracted from CPW measurements (~150 Ω.cm) and which, once more, is associated with the inversion layer underneath the oxide. A more accurate value of ρ_{eff} could be obtained by performing an electromagnetic simulation of the structure in order to precisely evaluate C_{under} and the effect of the oxide layer which also influences the interstrip coupling. Such an analysis is however out of the scope of this work.

The model can still be useful to predict the benefit obtained by a theoretical increase of the substrate resistances (R_p and R_{sub}). For a given structure, multiplying the value of R_{sub} by a factor x corresponds to an equivalent increase in effective resistivity. It is seen in Figure 2.64 that for a ρ_{eff} values close to 5 kΩ.cm (factor 100) the value of Q_{max} is increased by roughly 40 %. In that case most of the Q_{max}-limiting factors can be associated with series conductor losses. In a recent work, a factor close to 2 was reported for an inductor whose geometry was optimized for surface passivated HR Silicon substrates [27].

2.8 Conclusion

This chapter has focused on evaluating the performance of oxidized HR silicon substrates (such as HR SOI wafers) for RF applications. Both our simulation and measurements results indicated that even if substantial loss reductions can be obtained by using HR SOI wafers instead of standard resistivity substrates, space charge effects near the oxide/silicon interface can negatively affect the local value

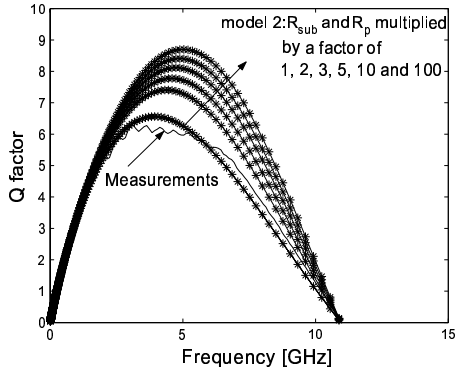


Figure 2.64: Measured and simulated Q *vs* f curves for the 5.5 turn-inductor of wafer Xfab. The modeled data were obtained using the equivalent circuit of Figure 2.58 and illustrate the increase of Q_{max} obtained by increasing R_{sub} and R_p.

of the resistivity in oxidized HR substrates. In addition, as the charge distributed near that interface typically results in poorly resistive horizontal (i.e., parallel to the interface) layers of free carriers, these layers induce substantially higher substrate losses in the case of coplanar devices (for which electric field lines are primarily horizontal) than in the case of vertical field devices. This was demonstrated both by measurements and simulations by comparing the effect of an accumulation or inversion layer at the substrate surface inside a CPW and a MS structure.

The CPW line was then identified as a very convenient structure to evaluate the contribution from the lossy SiO_2/Si interface to substrate losses in oxidized HR substrates. In this work, this contribution was quantified for the first time by extracting the *effective resistivity* of the substrates. This factor of merit represents the resistivity that a purely homogeneous (without oxide nor space charge effects) silicon substrate with the same CPW structure should have in order to sustain identical losses as the studied wafer. Using this factor of merit has the advantages of:

- focusing on the substrate performance only, thus removing the contribution of metallic losses. This is of utmost importance in the case of HR substrates for which metallic losses usually dominate over substrate losses and may significantly vary from one process to the other.
- providing the actual value of resistivity that circuit designers should consider when drawing their circuits, as substrate resistivity is usually a CAD tool input.

The CPW was then extensively used to evaluate the impact of surface charge distribution on ρ_{eff}. Similarly to what occurs inside a Metal-Insulator-Semiconductor

(MIS) structure, the distribution of charges below the oxide is primarily dictated in such device by the value of the electrostatic potential at the substrate surface (ϕ_S), which is itself conditioned by the following parameters: substrate doping, metal work function, bias applied on the metallic conductor (V_a), fixed charges in the oxide (Q_f), oxide thickness (t_{ox}), interface trap density (D_{it}) and temperature (T). A systematic study was then performed to quantify the separate impact of all those parameters on the substrate effective resistivity.

This work has enabled to finger out the parameters that play the most determinant role in the issue of parasitic surface conduction inside oxidized high resistivity substrates. The main outcomes of this investigation are:

- HR silicon substrates are characterized by a very low doping and a very low density of free carriers. As a consequence, any local increase of free carrier concentration easily leads to either an accumulated or inverted state. For the particular case of oxidized HR substrate losses can thus be drastically increased for any combination of structural and electrical parameters that lead to an increase of free carriers below the oxide. For p-type substrates with perfect oxides ($D_{it} \simeq Q_f \simeq 0$) at 0 V bias, this typically occurs when gold (accumulation) or aluminium (inversion) is used for the electrodes (or metals with similar values of work function). In non perfect thermal or deposited oxides, ρ_{eff} is a decreasing function of Q_f. Q_f values in the low $10^{10}\ /cm^2$ were shown to reduce ρ_{eff} by more than one order of magnitude. In that case also, the value of ρ_{eff} can be significantly degraded by the application of a strong negative (accumulation) or positive bias on the electrodes. This parasitic influence of the bias on the substrate effective resistivity is however significantly reduced in the case of thicker oxides ($\geq\ 1\ \mu m$).

- On the other hand, losses are significantly reduced (and ρ_{eff} increased) for a combination of parameter values that lead to a state of deep depletion at the substrate surface. For p-type substrates with perfect oxides ($D_{it} \simeq Q_f \simeq 0$) at 0 V, this occurs when copper is used for the electrodes (or a metal with a similar value of work function). In the case of non perfect or deposited thermal oxide, this can be achieved by applying an appropriate DC bias on the electrodes. However, it is important to keep in mind that ρ_{eff} is altered by PSC that occurs below the metallic conductors but also in the spacing that separates the conductors. As a consequence, optimized conditions to create depletion below the conductors (such as by properly biasing the electrodes) do not necessarily prevent PSC in the spacing between the conductors, thus leading to residual losses inside the substrate. A more efficient method consists in artificially introducing

a large density of interface traps ($\geq 10^{12}$ $/cm^2/eV$) at the SiO_2/Si interface in order to passivate the substrate surface.

· As explained above, an increase of oxide thickness (which is classically considered on CMOS or SOI technologies using standard resistivity substrates to reduce substrate losses) can reduce the influence of V_a on ρ_{eff}. However, in the case of HR silicon substrates this usually also contributes to a reduction of ρ_{eff} since the fabrication of thicker oxides usually requires deposition methods that lead to material of lower quality. This is typically what occurs in current multilevel technologies in which isolation from the substrate is usually proceeded by stacking a high number of IMD layers between the substrate and the first metal level used to design the passive structures. As those layers are not optimized for reduced charging, the equivalent fixed charge density is typically above 10^{11} $/cm^2$. Because of this issue, values of ρ_{eff} reported in this work for multilayer technologies fabricated on HR Si substrates did not exceed 600 Ω.cm.

So, both from a wafer manufacturer and a CAD designer perspectives, the problem of parasitic conduction at the surface in oxidized HR silicon substrates leads to some serious issues.

From a wafer manufacturer perspective, parasitic conduction at the substrate surface on oxidized HR Si wafers was shown to reduce the effective resistivity of the substrate by more than one order of magnitude, significantly degrading the quality of the product sold. This typically explains why companies fabricating HR bulk substrates can guarantee substrate resistivity values as high as 10 kΩ.cm (obtained by the floating zone fabrication processes), while manufacturers of HR SOI wafers can only afford to guarantee ρ_{eff} values higher than 1 kΩ.cm. Another issue faced by the wafer manufacturer is that the final, post process value of ρ_{eff} is substantially dependent on the process endured by the wafers, either bulk or SOI. This is because the substrate effective resistivity is largely dependent on the equivalent amount of fixed charged in the covering oxide layers and also on the amount of traps present at the SiO_2/Si interface. As both parameters are critically process dependent, this prevents the wafer manufacturer from specifying the effective resistivity of its wafers when they are sold to a particular foundry.

From a RFIC designer perspective, parasitic conduction leads to other issues:

· substrate losses in HR oxidized Si wafers have currently not been eradicated, despite what could have been expected from using substrates with nominal resistivity values in the 10 kΩ.cm range. In the case of CPW lines, they can not be considered as negligible compared to metallic losses. This was also shown to

increase substrate crosstalk below 1 GHz and affect the quality factor of inductors. The effects shown here are even expected to worsen for future generations of SOI wafers, which will face a decrease of the BOX thickness in order to reduce self heating and SCE in fully-depleted devices.

· besides, apart from degrading circuit performance, parasitic conduction at the silicon surface makes the modeling of substrate behavior much more complex. Indeed, as shown in this chapter the effective resistivity of the substrate depends on a variety of technological parameters and is therefore not easily predictable. This particular point is actually further exacerbated by the fact that:

  – those technological parameters can vary from one die to another (especially Q_f), possibly leading to strong dispersion in substrate losses (as shown in [44]) across a single wafer,

  – as the equivalent fixed charge density depends on the oxide thickness and the dielectric layers used for substrate insulation, it is expected that the value of ρ_{eff} depends on the metal layers that are used to design the passive structures,

  – losses (and thus ρ_{eff}) are bias dependent.

However, it was also shown in this chapter that the effective resistivity of the substrate can fully recover its nominal value when the substrate surface is passivated before oxidation, such as by introducing a large density of traps at the SiO_2/Si interface. This is because traps absorb free carriers from the interface, thereby making them unable to react to RF signals. For trap densities high enough ($\geq 10^{12}\ /cm^2/eV$), the value of ρ_{eff} no longer depends on Q_f (as long as this parameter remains within the following typical range of encountered values: $1\text{x}10^{10} < Q_f < 1\text{x}10^{12}\ /cm^2$) and therefore all of the issues mentioned above are solved. Several methods have been proposed in the literature to achieve successful substrate passivation. None of these methods were however optimized to allow an efficient and cost effective integration with the fabrication process of HR SOI wafers. Substrate passivation techniques and their compatibility with SOI wafer fabrication form the main topics of the coming chapter.

References

[1] L. E. Larson, "Silicon technology tradeoffs for radio-frequency/mixed-signal systems-on-a-chip," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 683–689, 2003.

[2] K. Benaissa, J.-T. Yuan, D. Crenshaw, B. Williams, S. Sridhar, J. Ai, G. Boselli, S. Zhao, S. Tang, S. Ashbun, P. MAdhani, T. Blythe, N. Mahalingam, and H. Schichijo, "RF CMOS high-resistivity substrates for systems-on-chip applications," *IEEE Trans. Electron Dev.*, vol. 50, no. 3, pp. 567–576, 2003.

[3] J. Buechler, E. Kasper, P. Russer, and K. Strohm, "Silicon high-resistivity-substrate for millimeter-wave technology," *IEEE Trans. Electron Devices*, vol. 33, no. 12, pp. 2047–2052, 1986.

[4] A. C. Reyes, S. M. El-Ghazaly, S. J. Dorn, M. Dydyk, D. K. Schroeder, and H. Patterson, "Coplanar waveguides and microwave inductors on silicon substrates," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 9, pp. 2016–2021, 1995.

[5] Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 1, pp. 10–12, 1999.

[6] C. Schollhorn, W. Zhao, M. Morschbach, and E. Kasper, "Attenuatation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 740–746, 2003.

[7] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line in $Si - SiO_2$ system," *IEEE Trans. Microwave Theory Tech.*, vol. 19, no. 11, pp. 869–881, 1971.

[8] I. T. Ho and S. K. Mullick, "Analysis of transmission lines on integrated-circuit chips," *IEEE J. Solid-State Circuits*, vol. 2, no. 4, pp. 201–207, 1967.

[9] R. A. Pucel, "Design considerations for monolithic microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 29, pp. 513–534, 1981.

[10] T. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge, United Kingdom: Cambridge University Press, 1998.

[11] B. Razavi, *RF Microelectronics*. Prentice Hall, 1998.

[12] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. Artech House, 2003.

[13] Y. Kwon, V. M. Hietala, and K. Champlin, "Quasi-TEM analysis of slow-wave mode propagation on coplanar microstructure MIS transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 35, no. 6, pp. 545–551, 1987.

[14] J.-S. Ko, B.-K. Kim, and K. Lee, "Simple modeling of coplanar waveguide on thick dielectric over lossy substrate," *IEEE Trans. Electron Dev.*, vol. 44, no. 5, pp. 856–861, 1997.

[15] Y. Fukuoka, Y.-C. Shih, and T. Itoh, "Analysis of slow-wave coplanar waveguide for monolithic integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 31, no. 7, pp. 567–573, 1983.

[16] T. Shibata and E. Sano, "Characterization of MIS structure coplanar transmission lines for investigation of signal propagation in integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 38, no. 7, pp. 881–890, 1990.

[17] J. Zheng, Y. C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 9, pp. 1443–1451, 2000.

[18] D. F. Williams, "Metal-insulator-semiconductor transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 2, pp. 176–181, 1999.

[19] J.-K. Wee, Y.-J. Park, H.-S. Min, D.-H. Cho, M.-H. Seung, and H.-S. Park, "Modeling the substrate effect in interconnect line characteristics of high-speed VLSI circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 10, pp. 1436–1443, 1998.

[20] J.-P. Raskin, "Modeling, characterization and optimization of passive and active microwave SOI devices," Ph.D. dissertation, Université Catholique de Louvain, 1998.

[21] J. Lescot, "Modélisation et caractérisation de composants passifs intégrés sur silicium pour applications radiofréquences," Ph.D. dissertation, Institut National Polytechnique de Grenoble, 2000.

[22] A. R. V. Hippel, *Dielectric and Waves*. New York: John Wiley & Sons, 1954.

[23] C. Seguinot, P. Kennis, and P. Pribetich, "Desktop computer appraisal of potential slow-wave propagation characteristics for Schottky coplanar lines," *Electron. Lett.*, vol. 19, no. 25, pp. 1065–1067, 1983.

[24] D. Jager, "Slow-wave propagation along variable Schottky-contact microstrip line," *IEEE Trans. Microwave Theory Tech.*, vol. 24, no. 9, pp. 566–573, 1976.

[25] J. M. Jaffe, "A high frequency variable delay line," *IEEE Trans. Electron Devices*, vol. 19, pp. 1292–1294, 1972.

[26] D. Jager and W. Rabus, "Bias dependent phase delay of Schottky-contact microstrip lines," *Electron. Lett.*, vol. 9, no. 9, pp. 201–203, 1973.

[27] M. Spirito, F. M. D. Paola, L. K. Nanver, E. Valletta, B. Rong, B. Rejaei, L. C. N. de Vreede, and J.Burghartz, "Surface-passivated high-resistivity silicon as a true microwave substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 7, pp. 2340–2347, 2005.

[28] Y. P. Tsividis, *Operation and modeling of the MOS transistor*. Mc Graw Hill, 1987.

[29] C. M. Krowne and G. B. Tait, "Propagation in layered biased semiconductor structures based on transport analysis," *IEEE Trans. Microwave Theory Tech.*, vol. 37, no. 4, pp. 711–722, 1989.

[30] K. Han and T. T. Y. Wong, "Space-charge wave considerations in MIS waveguide analysis," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 7, pp. 1126–1132, 1991.

[31] G. Wang, R. W. Dutton, and C. S. Rafferty, "Device-level simulation of wave propagation along metal-insulator-semiconductor interconnect," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 4, pp. 1127–1136, 2002.

[32] S. Sze, *Physics of Semiconductor Devices*. New York: Wiley and Sons, 1973.

[33] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: John Wiley & Sons, 1982.

[34] H.-T. Lue, T.-Y. Tseng, and G.-W. Huang, "A method to characterize the dielectric and interfacial properties of metal-insulator-semiconductor structures by microwave measurements," *J. App. Ph.*, vol. 91, no. 8, pp. 5275–5282, 2002.

[35] H. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, and J. A. C. Stewart, "Low-loss CPW lines on surface stabilized high-resistivity silicon," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 10, pp. 395–397, 1999.

[36] B. Rong, J. N. Burghartz, L. K. Nanver, B. Rejaei, and M. van der Zwan, "Surface-passivated high resistivity silicon substrates for RFICs," *IEEE Electron Dev. Letters*, vol. 25, no. 4, pp. 176–178, 2004.

[37] W. Heinrich, "Quasi-TEM description of MMIC coplanar lines including conductor-loss effects," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 45–52, 1993.

[38] I. Huynen, D. Vanhoenacker-Janvier, and A. Vander Vorst, "Spectral domain form of new variational expression for very fast calculation of lossy multi-

layered planar line parameters," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 11, pp. 2099–2106, 1994.

[39] A. C. Reyes, S. M. El-Ghazaly, S. J. Dorn, M. Dydyk, and D. K. Schroeder, "Silicon as a microwave substrate," *IEEE MTT-S Symp. Dig.*, pp. 1759–1762, May 1994.

[40] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 602–633, 2001.

[41] J. O. J. Westlinder, G. Sjoblom, "Variable work function in MOS capacitors utilizing nitrogen-controlled TiN_x gate electrodes," *Microelectronic Engineering*, vol. 75, pp. 389–396, 2004.

[42] B. E. Deal, "Standardized terminology for oxide charges associated with thermally oxidized silicon," *IEEE Trans. Electron Dev.*, vol. 27, no. 3, pp. 606–608, 1980.

[43] W. Zhao, C. Schöllhorn, and E. Kasper, "Interface loss mechanism of millimeter-wave coplanar waveguides on silicon," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 1, pp. 407–410, 2002.

[44] G. Posada, G. Carchon, P. Soussan, G. Poesen, and B. N. abd W. De Raedt, "High resistivity silicon surface passivation for the thin-film MCM-D technology," *6th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 46–49, San Diego, January 2006.

[45] B. K. Ip, K. C. Kao, and D. Thomson, "Charges and defects in SiO_2 films deposited by plasma-enhanced chemical deposition at low temperatures," *Solid State Electronics*, vol. 34, no. 2, pp. 123–129, 1991.

[46] D. Lederer and J.-P. Raskin, "Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers," *Microwave Symp. Dig.*, pp. 685–688, 2000.

[47] S. Jenei, S. Decoutere, S. Van Huylenbroeck, G. Vanhorebeek, and B. Nauwelaers, "High Q inductors and capacitors on si substrate," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 64–71, 2001.

[48] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2252–2261, 1997.

[49] G. Carchon, S. Jenei, L. Carbonell, M. V. Hove, S. Decoutere, W. D. Raedt, K. Maex, and E. Beyne, "High-Q RF inductors on standard silicon realized us-

ing wafer-level packaging techniques," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1287–1290, Philadelphia, 2003.

[50] S. Banba and H. Ogawa, "Small-sized MMIC amplifiers using thin dielectric layers," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 485–492, 1999.

[51] V. Krishnamurthy, H. Cole, and T. Sitnik-Nieters, "Use of BCB in high frequency MCM interconnect," *IEEE Trans. Comp., Packag. Manufact. Tech.*, vol. 19, no. 1, pp. 42–47, 1996.

[52] G. E. Ponchak and A. N. Downey, "Characterization of thin film microstrip lines on polyimide," *IEEE Trans. Comp., Packag. Manufact. Tech.*, vol. 21, pp. 171–176, 1998.

[53] G. Carchon, W. D. Raedt, and E. Beyne, "Wafer-level packaging technology for high-Q on-chip inductors and transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 1244–1251, 2004.

[54] T. Y. Winarski, "Dielectrics in MOS devices, DRAM capacitors, and inter-metal isolation," *IEEE Electrical Insulation Magazine*, vol. 17, pp. 34–47, 2001.

[55] D. R. Cote, S. V. Nguyen, W. J. Cote, S. L. Pennington, A. K. Stamper, and D. V. Podlesnik, "Low-temperature chemical vapor deposition processes and dielectrics for microelectronic circuit manufacturing at IBM," *IBM J. Res. Develop.*, vol. 39, pp. 437–464, 1995.

[56] D. R. Cote, S. V. Nguyen, A. K. Stamper, D. S. Armbrust, D. Tobben, R. A. Conti, and G. Y. Lee, "Plasma-assisted chemical vapor deposition of dielectric thin films for ULSI semiconductor circuits," *IBM J. Res. Develop.*, vol. 43, pp. 5–38, 1999.

[57] D. Pramanik, S. Nariani, and G. Spadini, "Field inversion in CMOS double metal circuits due to carbon-based SoGs," *VLSI Multilevel Interconnection Conference*, pp. 454–462, 1989.

[58] L. M. Liu, K. M. Lin, S. L. Yin, C. H. Fang, M. H. Liaw, J. J. Lin, L. S. Tsai, S. L. Hsu, and M. S. Lin, "Back-end induced IMO layer charging," *VLSI Multilevel Interconnection Conference*, pp. 451–453, 1991.

[59] E. H. Poindexter, G. J. Gerardi, M.-E. Rueckel, and P. J. Caplan, "Electronic traps and P_b centers at the Si/SiO_2 interface: Band-gap energy distribution," *Journal App. Phys*, vol. 56, no. 10, pp. 2844–2849, 1984.

[60] A. Edwards, "Interaction of H and H_2 with the silicon dangling orbital at the $< 111 > Si/SiO_2$ interface," *Phys. Rev. B*, vol. 44, pp. 1832–1838, 1991.

[61] F. J. Feigl, W. B. Fowler, and K. L. Yip, "Oxygen vacancy model for the e' center in Si/SiO_2," *Solid State Comm.*, vol. 14, p. 225, 1974.

[62] K. L. Brower, "Dissociation kinetics of hydrogen-passivated (111) $Si - SiO_2$ interface defects," *Phys. Rev. B*, vol. 42, no. 6, pp. 3444–3453, 1990.

[63] S. Alexandrova, A. Szekeres, E. H. adnd I. Lisovsky, V. Litovchenko, and D.Mazunov, "Oxide and interface charges in thin SiO_2 films thermally grown on RF plasma hydrogenated silicon," *Surf. Eng., Surf. Instr. and Vac. Tech.*, vol. 75, pp. 301–305, 2004.

[64] V. P. Popov, I. V. Antonova, V. F. Stas, L. V. Mironova, E. P. Neustroev, A. K. Gutakovskii, A. A. Franzusov, and G. N. Feofanov, *In: Perspectives, Science and Technologies for Novel Silicon on Insulator Devices.* Dordrecht: Kluwer, 2000.

[65] I. V. Antonova, O. V. Naumova, D. V. Nikolaev, and V. P. Popov, "Traps at the bonded interface in silicon-on-insulator structures," *Appl. Phys. Lett.*, vol. 79, no. 27, pp. 4539–4540, 2001.

[66] I. V. Antonova, O. V. Naumova, and V. P. Popov, "Modification of the bonded interface in silicon-on-insulator structures under thermal treatment in hydrogen ambient," *Journ. Appl. Phys.*, vol. 93, no. 1, pp. 426–431, 2003.

[67] F. Heiman, "Thin-film silicon-on-sapphire deep depletion MOS transistors," *IEEE Trans. Electron Dev.*, vol. 13, no. 12, pp. 855–862, 1966.

[68] T. Nakamura, H. Matsuhashi, and Y. Nagatomo, "Silicon on sapphire (SOS) device technology," *Oki Technical Review*, vol. 200, no. 71, pp. 66–69, 2004.

[69] B. C. Co, "Electronic materials industry review," *Market Research Report*, May 2004.

[70] C. Mazure, I. Cayrefourcq, B. Ghyselen, F. Letertre, and C. Maleville, "Moving from today's SOI to advanced substrate engineering," *Solid State Technology*, vol. July, p. 672, 2003.

[71] N. P. Pham, P. M. Sarro, K. T. Ng, and J. N. Burghartz, "IC-compatible two-level bulk micromachining process module for RF silicon technology," *IEEE Trans. Electr. Dev.*, vol. 48, pp. 1756–1784, 2001.

[72] I. Jeong, S.-H. Shin, J.-H. Go, J.-S. Lee, C.-M. Nam, D.-W. Kim, and Y.-S. Kwon, "High-performance air-gap transmission lines and inductors for millimeter-wave applications," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 12, pp. 2850–2855, 2002.

[73] J. A. Reynoso-Hernandes, R. Rangel-Rojo, M. Aceves, I.Zaldivar, L. E. Sanchez, and M. Herrera, "Influence of the SRO as passivation layer on the microwave attenuation losses of the CPWs fabricated on HR-Si," *IEEE Microwave Wireless Components Letter*, vol. 13, no. 12, pp. 508–510, 2003.

[74] G. Ponchak, E. Dalton, A. Bacon, J. Papapolymerou, and M. Tentzeris, "Measured propagation characteristics of finite-ground coplanar waveguide on silicon with a thick polyimide interface layer," *Proc. of the 2002 European Microwave Symposium*, vol. I, pp. 167–170, September 2002.

[75] G. Six, G. Prigent, E. Rius, G. Dambrine, and H. Happy, "Fabrication and characterization of low-loss TFMS on silicon substrate up to 220 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 1, pp. 301–305, 2005.

[76] "Process integration, devices, and structures." [Online]. Available: http://www.itrs.net/Common/2005ITRS/PIDS2005.pdf

[77] M. Badaroglu, S. Donnay, H. D. Man, Y. A. Zinzius, G. Gielen, W. Sansen, T. Fonden, and S. Signell, "Modeling and experimental verification of substrate noise generation in a 220-kgates wlan system-on-chip with multiple supplies," *IEEE J. of Solid State Circuits*, vol. 38, no. 7, pp. 1250–1260, 2003.

[78] T. Chen, C. Y. Lee, and C. H. Kao, "An efficient noise isolation technique for SOC application," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 255–260, 2004.

[79] S. Stefanou, J. Hamel, P. Baine, M. Bain, B. M. Armstrong, H. Gamble, M. Kraft, and H. Kemhadjian, "Ultralow silicon substrate noise crosstalk using metal faraday cages in an soi technology," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 486–491, 2004.

[80] J. H. Wu, J. Scholvin, and J. A. del Alamo, "A through-wafer interconnect in silicon for RFICs," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1765–1771, 2004.

[81] H. G. HS, B. Armstrong, P. Baine, M. Bain, and D. McNeill, "Silicon-on-insulator substrates with buried tungsten silicide layer," *Solid State Electronics*, vol. 45, no. 4, pp. 551–557, 2001.

[82] J. Ankarcrona, L. Vestling, K. H. Eklund, and J. Olsson, "Crosstalk reduction using low resistivity SOI," *Proceedings of EUROSOI 2005*, Grenada,2005.

[83] M. van Heijningen, J. Compiet, P. Wambacq, S. Donnay, M. Engels, and I. Bolsens, "Analysis and experimental verification of digital substrate noise generation for epi-type substrates," *IEEE J. of Solid State Circuits*, vol. 35, no. 7, pp. 1002–1008, 2000.

[84] B. Owens, S. Adluri, P. Birrer, R. Shreeve, S. Arunachalam, K. Mayaram, and T. Fiez, "Simulation and measurement of supply and substrate noise in mixed-signal ICs," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 382–391, 2005.

[85] M. van Heijningen, M. Badaroglu, S. Donnay, G. Gielen, and H. D. Man, "Substrate noise generation in complex digital systems: efficient modeling and simulation methodology and experimental verification," *IEEE J. of Solid State Circuits*, vol. 37, no. 8, pp. 1065–1072, 2002.

[86] C. Yue and S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560–568, 2000.

[87] J. Chen and J. Liou, "On-chip spiral inductors for RF applications: An overview," *Journal of Semiconductor Technology and Science*, vol. 4, no. 3, pp. 149–167, 2004.

CHAPTER 3

NEW FABRICATION METHOD FOR HR SOI WAFERS WITH INCREASED RESISTIVITY

3.1 Introduction

The investigation performed in the previous chapter has shown that oxidized HR silicon substrates suffer from parasitic surface conduction (PSC) in the substrate due, mainly, to fixed charges in the oxide. As shown in Figure 3.1 [1], this issue was first acknowledged in the mid eighties (at the early years of HR silicon) and has been attracting a growing interest amongst the scientific community during the past five years. The survey illustrates the number of papers that have *addressed* the problem of PSC (light bars) in oxidized HR Si substrates and those that have in addition attempted to technologically *solve* the issue (dark bars). It is interesting to notice that some of the proposed techniques have been recently developed in an industrial environment [3, 4], suggesting that this particular issue has become a concern at an industrial level.

In this context, the present chapter first describes the different techniques that have been proposed in the literature to suppress or reduce parasitic conduction in oxidized HR Si substrates, briefly outlining the difficulties and advantages of each method. For the particular case of HR SOI wafers this overview identifies one of those techniques as a very promising method, which consists in the insertion of an undoped polysilicon layer below the buried oxide during the fabrication process. This technique is therefore widely investigated in this chapter and is optimized for the fabrication of substrate-passivated UNIBOND SOI wafers. The effects of the polySi layer deposition parameters on the passivation efficiency is thoroughly analyzed on a quantitative basis. The morphological properties (such as texture and surface roughness) of the polysilicon layer are also investigated as they influence the quality of the bonding during wafer fabrication, and in the context of IC compatibility the analysis includes the thermal stability of the deposited layer. And last, results of preliminary bonding tests are presented at the end of this chapter.

[1] The graph reported in the figure presents the results of a survey made on the IEEE Explore [1] and Science Direct databases [2].

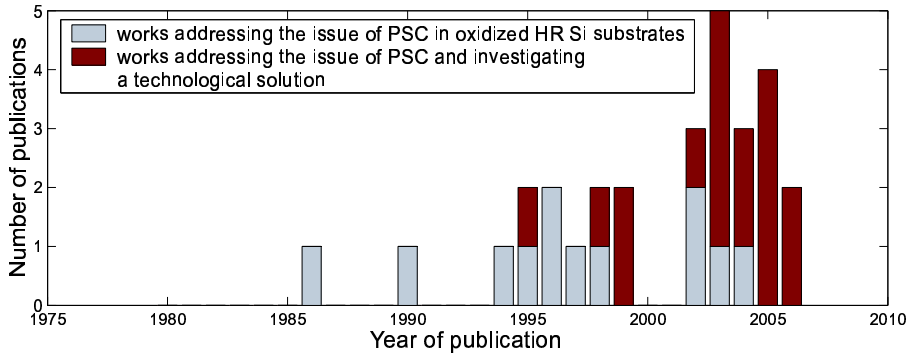


Figure 3.1: Number of publications found in IEEE Explore [1] and Science Direct [2] databases addressing the problem of parasitic conduction in oxidized HR Si substrates (light field) and proposing technological solutions to overcome that issue (dark field).

3.2 Existing methods to reduce PSC in oxidized HR Si substrates

The different techniques that have been proposed in the literature to suppress PSC in oxidized HR Si substrates are summarized in Table 3.1, along with their respective authors. In short, these techniques basically rely on three distinct approaches. One of them consists in irradiating the entire silicon substrate with protons, thereby providing a *volume* passivation method. Though not primarily intended for PSC suppression in HR substrates this technique is briefly presented because it provides a very efficient way to suppress losses in Si substrates. The second and third methods rely on *surface* processing. In the second approach the issue of PSC is (partially) solved by removing the oxide between metallic conductors, which is motivated by the observation that fixed charges inside the oxide are the main contributors to PSC. Finally, the last method consists in passivating the substrate surface (*surface* passivation) with a trap-rich layer, such as amorphous silicon ($\alpha - Si$) or polysilicon. All three techniques are discussed in the coming sections.

Table 3.1: Different techniques proposed in the literature to solve the issue of PSC in oxidized HR Si substrates along with their contributors.

	Proton irradiation	**Dielectric etching**	**Surface passivation**		
			α-Si	Ar implant	polySi
References	[5,6]	[7–9]	[10]	[4,10]	[11,12]

3.2.1 Volume passivation by proton irradiation

Proton irradiation was first proposed in 2000 by Wu et *al.* [5]. This method consists in breaking silicon atom covalent bonds by implanting protons into the bulk of the substrate, which introduces impurities into the crystal silicon and produces a large density of defects. Using high implantation energy (~ 10 MeV), it is possible to contaminate the entire substrate thickness, thereby providing a volume passivation of the substrate. This feature makes the method especially useful in the case of standard resistivity wafers: in [5] 10 Ω.cm substrates exhibited an increase of resistivity up to more than 1 MΩ.cm for a total dose of 10^{16} $/cm^2$, demonstrating the high efficiency of the technique.

The use of this method to form high resistivity substrates at an industrial scale suffers from two major limitations:

- the silicon substrate recrystallizes for temperature points higher than 600°C [5], which makes the substrate recover its initial resistivity. Avoiding this requires that the implantation is performed at an intermediary stage between the front (high thermal budget) and back (low thermal budget) end processing, allowing less flexibility;
- this further requires that hard masking must be used to protect sensitive areas on the wafer (such as active devices), adding significant cost.

To our knowledge, the full compatibility of this method within an industrial CMOS environment is still to be proved.

3.2.2 Dielectric removal

In the specific case of oxidized HR Si substrates, the most straightforward technique to get rid of parasitic surface conduction consists in removing the charged insulator in spacings between metallic conductors. This can be performed with a selective etching, as illustrated in Figure 3.2. It was demonstrated in [7] (on a Si_3N_4 dielectric layer) and in [9] (on SiO_2) that for the particular case of CPW lines, this simple method provides a substantial reduction of substrate losses (close to 14 dB/cm at 20 GHz in [9]). However, its main drawbacks are:

- it is not compatible with multilevel processing unless an alternate IC-compatible and charge-free material is provided to fill the gaps created by dielectric removal,
- it does not prevent PSC *below* the metallic conductors (as illustrated in Figure 3.2), and is therefore expected to yield residual, bias-dependent, substrate losses.

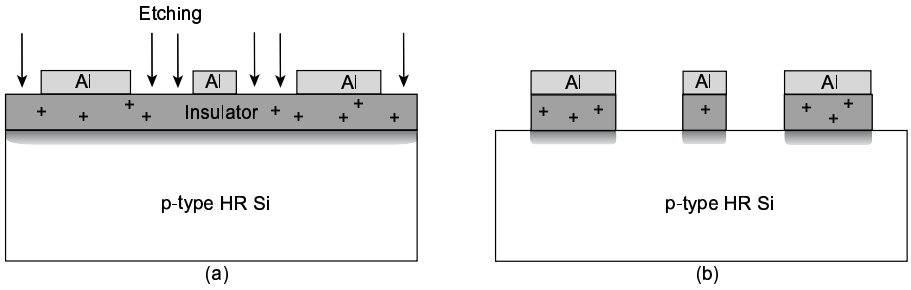


Figure 3.2: Illustration of parasitic surface layer in HR Si substrates (a) before dielectric etching and (b) after etching.

Other methods which can simultaneously overcome both difficulties consist in passivating the entire substrate surface, as discussed next.

3.2.3 Surface passivation by Ar implantation and layer deposition

In this last approach, the passivation of the substrate surface is obtained by introducing a large density of defects between the HR Si substrate and the insulating dielectric. These defects cause the formation of interface states (or traps), which capture the unwanted free carriers from the substrate surface and form a highly resistive depleted region. As indicated in Table 3.1, three different methods have been proposed to achieve successful substrate passivation.

3.2.3.1 Argon implantation

The first method consists in turning the substrate surface into an amorphous silicon layer by implanting argon within the top several microns. Argon implantation was first investigated at Philips Research Laboratories ([10, 13, 14]) and has also been more recently developed at IMEC for their thin film MCM-D technology ([4]).

Using a photolithographic process in order to prevent any deterioration of the active regions in an IC process it is possible to perform a selective implantation below the passive structures only. In this case, by creating traps in the Si substrate below the *entire* passive structures this method is expected to provide a better passivation efficiency than intermetal dielectric etching. However, it requires an additional mask and suffers from a major limitation: Ar-implanted amorphous silicon is not thermodynamically stable since for such layer recrystallization appeared to occur at temperatures higher than $\sim$ 400°C, where it started losing its passivation efficiency [10]. This passivation method might therefore not be com-

patible with the conventional thermal budgets of back end processing [15].

3.2.3.2 Layer deposition

The other method found in the literature that proposes surface passivation of oxidized HR Si substrates consists in depositing a trap-rich layer of adequate material onto the silicon surface. Different materials have been suggested: (1) amorphous silicon [10], (2) polysilicon [11, 16] and (3) oxygen-doped polysilicon [3]. In all cases two different approaches can be considered: the material is either locally deposited below the passive structure or it is deposited on the entire substrate surface before oxidation.

Using the first approach requires the passivation layer to be compatible with the entire thermal budget of a CMOS process, since the layer must be deposited at a front end level in order to reduce the number of additional process steps and photolithographic masks. To our knowledge this approach was only investigated in [3] using a 12 nm-thick passivating layer, which was shown to start loosing its passivating effect at an anneal temperature of 900°C. Despite what the paper reports, that method can therefore not be considered as compatible with *any* current Si CMOS process flow and still requires further investigation to demonstrate its full IC compatibility.

The second approach, which makes use of conventional deposition techniques (PECVD, LPCVD, ...), is much easier to implement since the trap-rich material is deposited on the entire substrate surface *before* any CMOS processing. In this case, the insulating oxide is deposited on top of the passivating layer. As such, this method can however only be considered for passive structure fabrication since it is not expected that high quality thin silicon films (for active devices) can be epitaxially grown on deposited oxides. Nevertheless, an alternate approach exists, which can fully exploit the simplicity of this passivation method: it consists in *bonding* an oxidized donor wafer onto a passivated HR handle wafer, as illustrated in Figure 3.3. This technique implies that passivation is performed at a wafer fabrication level, and thus that the passivation layer remains thermally stable throughout a complete SOI CMOS process. Again, the results reported in [10] regarding the thermodynamic instability of *amorphous* silicon suggest that this material is not adequate for this approach. On the other hand *polysilicon* grains are expected to be much more stable with temperature since they are made of crystallized silicon (with different crystal orientations). As the results presented in [11] further infer that polySi-passivation is a highly efficient method, this approach has been adopted in this work and is widely investigated in this chapter. It is also adapted

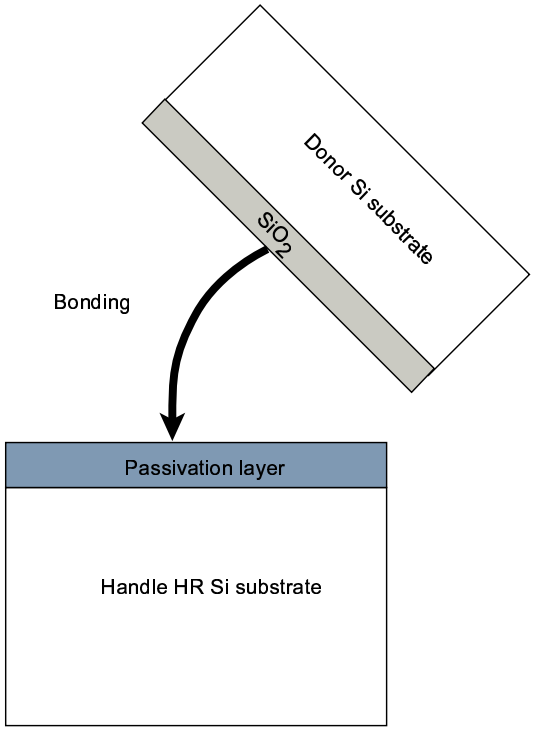


Figure 3.3: Illustration of the process step investigated in this work for the fabrication of passivated UNIBOND HR SOI silicon wafers: bonding between a passivated HR handle wafer and an oxidized donor wafer.

for the particular case of UNIBOND HR SOI wafer fabrication, as presented below.

3.3 Proposed method for substrate passivation in UNIBOND HR SOI wafers

Figure 3.4 shows the fabrication process of UNIBOND wafers, which was detailed in Chapter 1. The figure shows that during the fabrication of UNIBOND wafers, the HR Si handle substrate is directly bonded onto the oxide of the donor substrate, which forms the buried oxide of the fabricated SOI wafer. When thick buried oxides are desired the handle wafer can also be first oxidized and the bonding is then performed at an SiO_2/SiO_2 interface. In both cases, a non passivated SiO_2/Si silicon interface is formed between the BOX and the HR Si substrate. We propose here a simple method to passivate that interface, which consists in depositing a

layer of undoped polysilicon on the surface before the bonding step. In this case the bonding is formed at a $SiO_2/polySi$ interface and an additional chemico-mechanical polishing (CMP) step might need to be performed on the polySi surface in order to reduce the surface roughness to acceptable values before the bonding, as illustrated in the third column of Figure 3.4. As it is performed at a wafer processing level, this simple method does not require any complex or expensive CMOS processing. It furthermore uses a CMOS-friendly material (polySi).

To be successful in its "passivating" task, the deposited polySi layer needs to have the following characteristics:

- high passivation efficiency: the number of traps within the layer must be high enough to completely absorb free carriers from the Si surface, regardless of the bias conditions and of the CMOS process for which the wafer will be used,

- high thermodynamic stability: it is crucial that both mechanical and electrical properties of the layer remain unaltered by high thermal budgets.

A low surface roughness could also provide a significant advantage by suppressing the need for a CMP on the polySi layer before the bonding, thus reducing total time and fabrication cost. The surface roughness of the deposited polySi is therefore an important parameter to consider. Passivation efficiency, thermodynamic efficiency and surface roughness of the deposited polySi layer are therefore the key parameters investigated in the coming sections as a function of polySi deposition conditions.

3.4 Influence of polysilicon layer deposition parameters

3.4.1 Classical polysilicon deposition method: LPCVD

Polycrystalline silicon or polysilicon is a material consisting of multiple small silicon grains with different crystal orientations. The grains are separated by the so-called grain boundaries, which are rich in defects and surface states.

Owing to its excellent chemical, mechanical and electrical properties, polysilicon is a key material in current microelectronics. It is for instance used in gate electrodes of MOSFET devices, thin-film-transistors (TFT) for flat panel displays and is also largely employed in solar cell fabrication. The industrial use of polysilicon requiring high volume processing, polysilicon is usually obtained in low-pressure (LP) hot-walls reactors using a chemical vapor deposition (CVD) technique [18]. This particular deposition method is therefore considered here also.

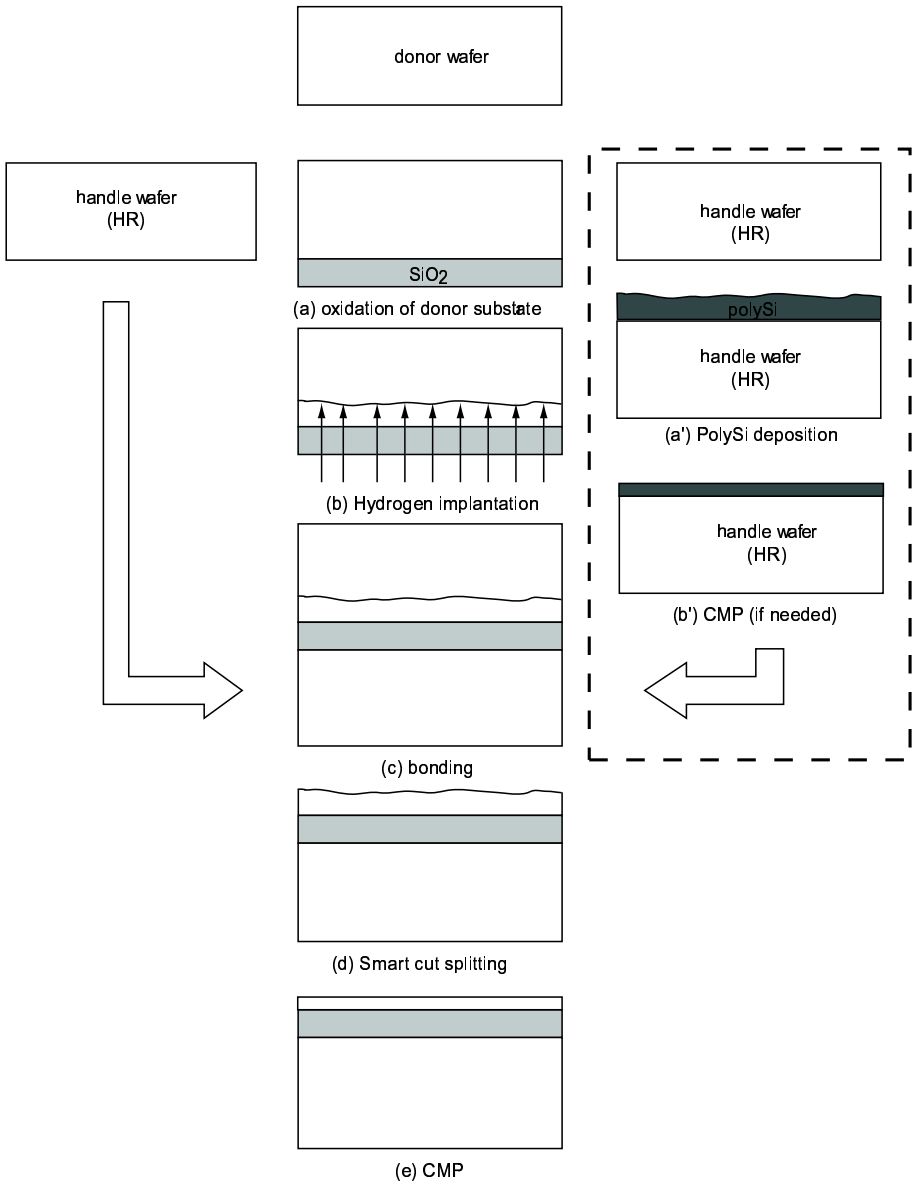


Figure 3.4: Left and middle columns: Basic steps for the fabrication of UNIBOND wafers using the Smart-Cut technique. Right column: modification proposed in this work to process HR SOI wafers with a polySi-passivated substrate surface.

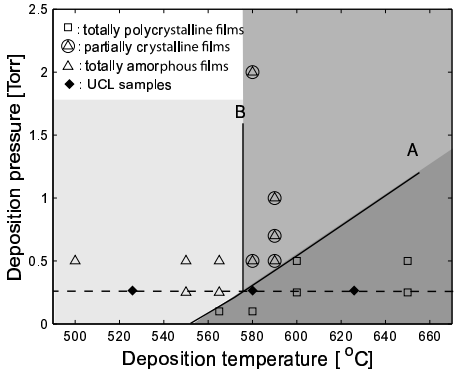


Figure 3.5: Pression-temperature phase diagram for LPCVD silicon films (from [17]).

The LPCVD technique is based on the thermal decomposition of silane (SiH_4), which releases silicon and molecular hydrogen according to the following reaction:

$$SiH_4(g) \rightarrow Si(s) + 2H_2(g) \tag{3.1}$$

The structural properties of the silicon layer resulting from this process mainly depends on two ambient parameters: the temperature and the pressure inside the furnace. As shown Figure 3.5 (figure reproduced from [17]), these two parameters can determine by themselves the amorphous ($\alpha - Si$), partially crystalline ($PC - Si$), or polycrystalline (polySi) state of the deposited layer. More precisely, the graph identifies three specific areas in the pressure-phase diagram, each corresponding to a certain morphology [17]:

- at low temperatures ($T \leq 565$°C) and high pressures ($P > 100$ mT), the deposited film is purely amorphous,

- at high temperatures and at limited pressures (below line A), the film is totally polycrystalline,

- in the intermediate range of temperatures and pressures (between lines A and B), the deposited film is only partially crystallized, with most of the amorphous silicon lying on top of the polycrystalline silicon.

Table 3.2: Process parameters for the passivated samples with passivation layers deposited at different temperatures. Sample BHR5 corresponds to the reference, unpassivated wafer.

Sample	T [°C]	time [min]	t [nm]	d.r. [nm/min]	oxide layer
BHR32	525	333	305	0.9	500 nm-PECVD
BHR6	580	120	335	2.8	1000 nm-APCVD
BHR10	625	38	325	8.6	1000 nm-APCVD
BHR5	//	//	//	//	300 nm th. + 1000 nm-APCVD

3.4.2 Impact of deposition temperature

The purpose of the investigation reported in this section is to quantify the impact of the silicon texture ($\alpha - Si$, $PC - Si$ or polySi) on the passivation efficiency when the substrate surface is passivated with LPCVD silicon. The passivation efficiency is here quantified using the concept of effective resistivity, which was developed in Section 2.3.2. In order to fabricate samples with the three desired structural types, the deposition parameters were initially chosen so as to define points that each fall into one of the three subsets of the $P - T$ LPCVD silicon diagram phase of Figure 3.5. As for technical reasons the internal pressure of the LPCVD reactor at UCL could not be raised to a higher value than ~0.25 mT during the deposition process only the deposition temperature was varied: values of 525 and 625°C were chosen for $\alpha - Si$ (wafer BHR32) and polySi (wafer BHR10), respectively. A sample (wafer BHR6) was also processed at a temperature of 580°C, in which case the graph does not allow a positive identification of the partially or totally crystallized state of the deposited silicon layer. The investigated $P - T$ points are reported in the figure. In all cases, the silane flow was maintained at 105 sccm.

The deposition time, layer thickness (measured by ellipsometry on test samples) and estimated deposition rate (d.r.) are reported in Table 3.2. For the three investigated values of deposition temperature, test samples were also processed without covering oxide in order to analyze the texture of the deposited silicon layer by X-Ray diffraction. This method indeed allows the determination of crystalline phases in the material [18]. Some results of the X-ray measurements are plotted in Figure 3.6. The measurements were respectively performed on the bare substrate (subfigure a), a layer deposited at 525°C (b) and one at 625°C (c).

It can be inferred from comparing Figures 3.6a and b that the peak observed for the 525°C-deposited Si layer can be associated with "noise" from the substrate. In the latter case, Figure 3.6b further shows that no other crystallographic orientation was recorded on that sample, which demonstrates that amorphous silicon

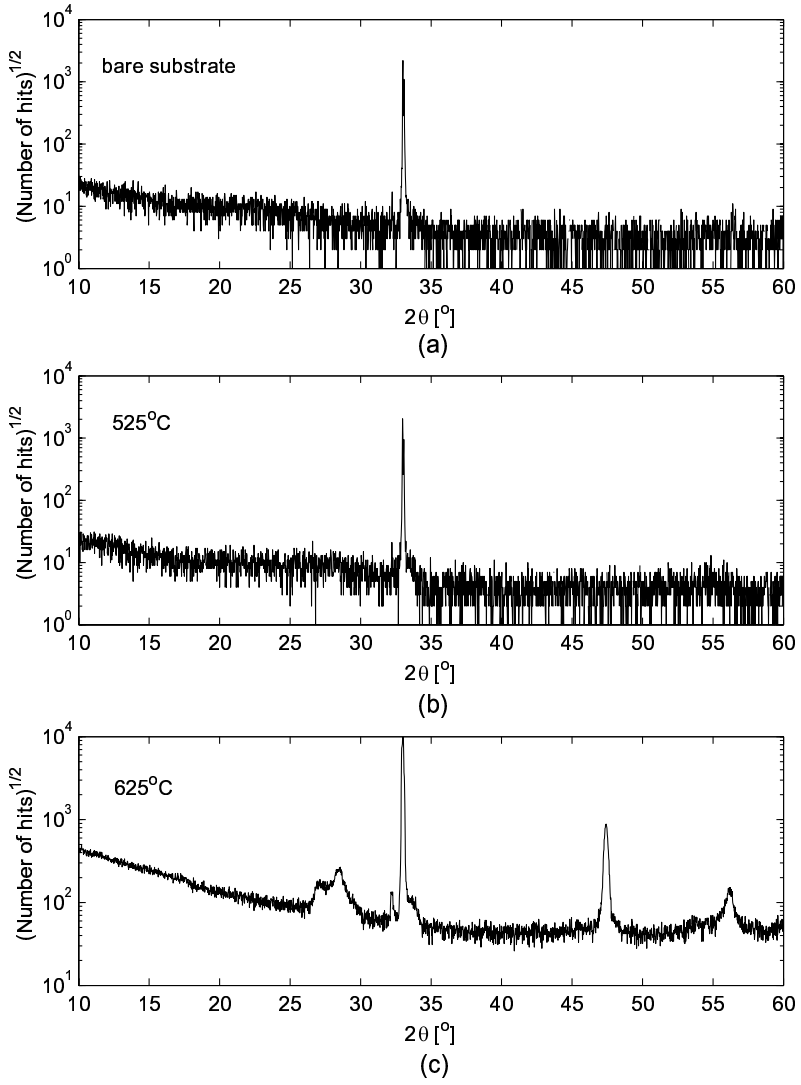


Figure 3.6: Results of X-ray diffraction measurements performed on different samples: (a) naked substrate, (b) 525°C, and (c) 625°C-deposited Si layer.

was obtained at 525°C. On the other hand, our 625°sample (Figure 3.6c) outlines clear evidences of multiple crystallographic orientations. Similar results were obtained on an additional sample with a Si layer deposited at 585°C (data not shown). This indicates that at least some polysilicon was obtained in these two last cases. Unfortunately, these data are not suitable to accurately determine the level of crys-

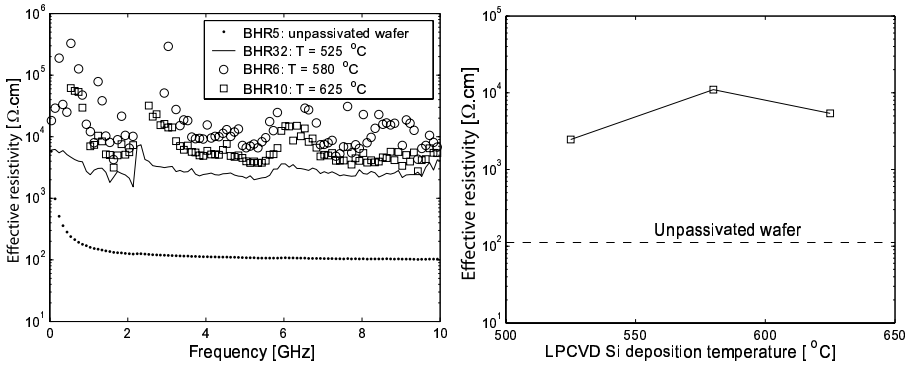


Figure 3.7: Effective resistivity values extracted on the passivated wafers as a function of (a) frequency and (b) deposition temperature of the passivation layer.

tallization inside the samples.

Table 3.2 reports that the three LPCVD Si-passivated HR samples were also oxidized. A 1 μm-thick atmospheric-pressure (AP) CVD oxide layer was deposited on wafers BHR6 and BHR10. In the case of wafer BHR34, a 500 nm-thick oxide was deposited by PECVD. The wafers then received a 1 μm-thick front-side aluminium metalization and 50 Ω CPW lines were patterned to extract the substrate effective resistivity on all samples according to the method depicted in Section 2.3.2. The extracted values of ρ_{eff} are reported as a function of frequency and deposition temperature in Figures 3.7a and b, respectively. The data presented in Figure 3.7b represent the mean ρ_{eff} values extracted in the 4-4.5 GHz range, where the $\rho_{eff}\ vs\ f$ curves exhibit reduced noise. In both figures the ρ_{eff} value extracted on the reference wafer was also included. This HR wafer received no passivation and a double oxidation (thermal + APCVD).

Both figures clearly outline the interest of passivation, since substrates covered with a LPCVD deposited layer exhibit ρ_{eff} values that are more than one order of magnitude higher than the reference, unpassivated wafer. The figures also seem to indicate that better results are obtained with the PC-Si (580°C) or polySi (625°C) layer, since the extracted ρ_{eff} values are more than 2.5 times higher in those cases than when the substrate is passivated with amorphous silicon. This observation is interpreted here by the fact that the *bulk* trap density (expressed in $/cm^3/eV$) is higher in a polycrystalline (or partially crystalline) silicon layer than in a layer of amorphous silicon, as inferred in [19]. This is because the origin of the traps

differs in both types of materials:

- in a disordered layer of amorphous silicon exponential tails of localized states are formed at the band edges, which extend into the forbidden bandgap. The trap densities exponentially decay from the band edges [20] and are therefore very low near midgap.

- in polycrystalline silicon, the traps are mostly formed at the grain boundaries, where they are associated with silicon dangling bonds (i.e., unsatisfied covalent bonds) [18]. This type of traps is known to introduce deep states in the silicon bandgap, and are therefore expected to result in much higher trap densities near midgap.

3.4.3 Impact of layer thickness and thermal anneal

In both amorphous and polycrystalline silicon the effective surface sate density (D_{iteff}, expressed in $/cm^2/eV$) is created by traps distributed across the silicon layer (*bulk* traps D_{itb}) and by traps present at the oxide/passivation layer interface (*interface* traps, D_{its}):

$$D_{iteff} = D_{its} + \int_0^t D_{itb} dx \tag{3.2}$$

where t is the passivation layer thickness. It can be reasonably assumed that interface trap densities, which are mostly associated with Si dangling bonds, are roughly similar for both deposited amorphous and polycrystalline silicon. In addition, as the results presented in the previous section seem to indicate that better passivation is obtained using polySi instead of $\alpha - Si$, *bulk* traps can be expected to play a dominant role in the substrate passivation mechanisms. In that case the thickness of the passivation layer is an important factor determining the final D_{iteff} value. Indeed, the above expression indicates that D_{iteff} resumes to $D_{its} + D_{itb}.t$ if we further assume that bulk traps are uniformly distributed across the layer.

To validate this expectation and quantify the impact of the layer thickness on its passivation efficiency, samples with varying passivation layer thicknesses were processed. In this case, two deposition temperatures were considered: 580 and 625°C. Process details are summarized in Table 3.3 for the different samples.

The extracted value of resistivity is plotted as a function of the passivation layer thickness for the two investigated deposition temperatures in Figure 3.8a. The results confirm the trend that the effective resistivity is an increasing function of the layer thickness for the two investigated Si-deposition temperatures. In

Table 3.3: Deposition parameters for passivated samples with a varying passivation layer thickness and for two deposition temperatures.

Sample	T [°C]	time [min]	t [nm]	d.r. [nm/min]	oxide layer
BHR14	580	7	10.5	1.5	3000 nm-PECVD
BHR15	580	37	93	2.5	3000 nm-PECVD
BHR16	580	70	190	2.7	3000 nm-PECVD
BHR6	580	120	335	2.8	1000 nm-APCVD
BHR17	625	3	19	6.3	3000nm-PECVD
BHR18	625	9	76	8.4	3000nm-PECVD
BHR19	625	20	172	8.6	3000nm-PECVD
BHR10	625	38	325	8.6	1000 nm-APCVD

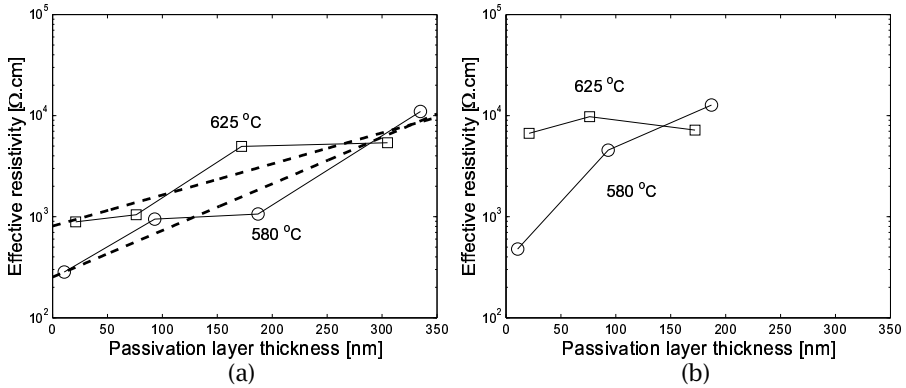


Figure 3.8: Effective resistivity values extracted on the passivated wafers as a function of passivation layer thickness (a) before and (b) after a 4h30 thermal anneal at 950°C in neutral ambient.

both cases, extrapolated data seem to indicate that a film thickness of 300~350 nm is sufficient to obtain a 10 kΩ.cm ρ_{eff} value and achieve full substrate passivation. For lower thickness values it is also seen from the figure that when substrate passivation is achieved with a 625°C-deposited polySi film, higher values of effective resistivity are obtained than when the silicon layer is deposited at 580°C. This is more than likely related to the lower density of traps in the latter material, which could be explained by a mixed texture of polycrystalline (higher D_{itb}) and amorphous (lower D_{itb}) silicon. From now on this layer is then treated as partially crystallized silicon ($PC-Si$).

The results presented in Figures 3.7 and 3.8 allow us to conclude that from a passivation efficiency perspective only, polycrystalline silicon layers should be favored over partially crystalline and amorphous silicon. However, as previously mentioned, another crucial characteristic of the passivation layer is its thermodynamic stability: to be reliable, both mechanical and electrical properties of the deposited layer must remain unaffected by long thermal budgets. Therefore, in order to investigate the impact of a thermal budget on the passivation efficiency of both $PC-Si$ and polySi layers, some of the wafers presented in Table 3.3 were cut in halves and one half was submitted to a 4h30-long thermal anneal at 950°C in a neutral nitrogen ambient. The ρ_{eff} value extracted on these samples is plotted as a function of the layer thickness in Figure 3.8b. It is seen that for both types of layer, a visible increase of the effective resistivity is obtained on the samples that endured the thermal anneal. This improvement is related to an increase of the effective surface state density, which is believed to result from the following mechanisms:

- first, as the $PC-Si$-passivated samples are submitted to an ambient temperature higher than 700°C, the amorphous silicon islands of the $PC-Si$ layer crystallizes in such a way as to form a completely crystallized polysilicon layer [21]. This is expected to increase the overall density of grain boundaries, and thus trap density. It is however not clear whether this mechanism favors the formation of *larger* or *new* polysilicon grains, which are expected to result in different bulk trap densities.

- second, high temperature anneals of polysilicon performed in a neutral ambient cause an effusion of its hydrogen content [18, 22]. This leads to a release of the hydrogen atoms occupying dangling Si bonds and which neutralize (or passivate) some of the traps. As a consequence, dangling bonds located both at grain boundaries and at the oxide/silicon interface are un-passivated during the anneal and the effective density of surface states is increased.

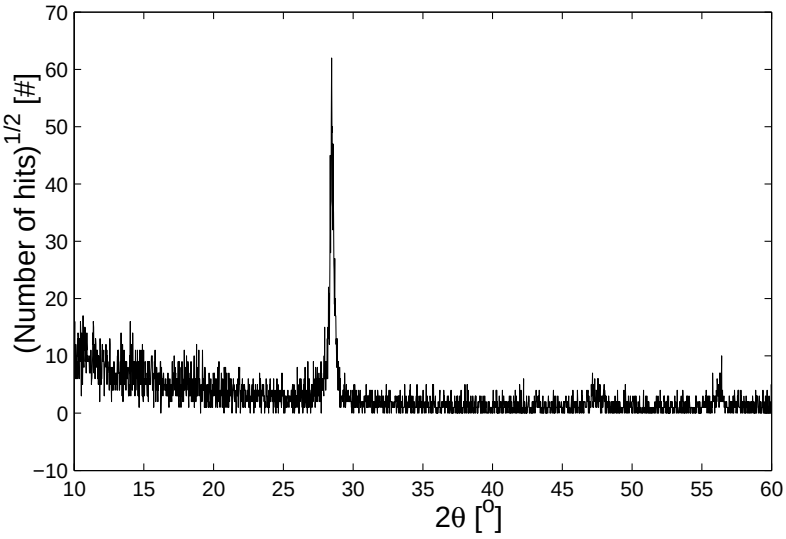


Figure 3.9: Results of X-ray diffraction measurements performed on a 400 nm-thick polysilicon layer obtained by (1) LPCVD at 525°C of amorphous silicon and (2) RTA at 900°C during 30 s.

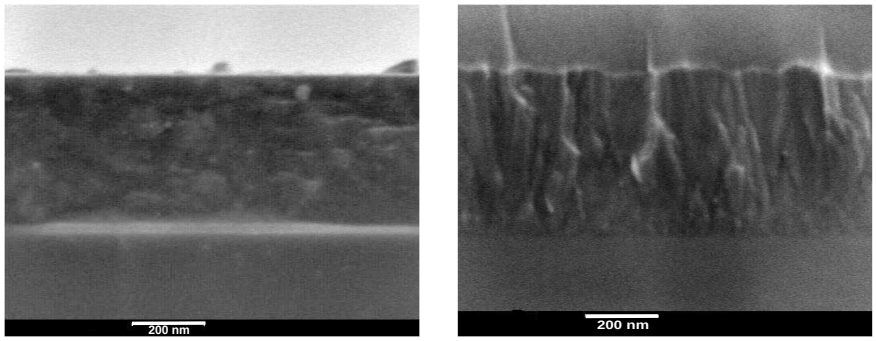
3.5 Enhancement of passivation layer properties

The results shown in Figures 3.8a and b suggest that substrate passivation with a polysilicon layer of thickness close to 300 nm should provide effective resistivity values in the 5-10 kΩ.cm-range, and also indicate that this range should even slightly increase under high thermal budgets. This makes polysilicon a very interesting candidate for substrate passivation.

However, it is also believed that the passivation efficiency could be even further improved by increasing the number of traps within the polySi layer. As those traps are mainly located at grain boundaries, one method to increase D_{itb} consists in developing a deposition process, preferably cheap, that results in the creation of smaller polysilicon grains, and thus a higher density of grain boundaries. In order to achieve this, the two-step following process was therefore investigated:

- deposition of LPCVD amorphous silicon at 525°C on the entire substrate surface,
- silicon crystallization by rapid thermal annealing (RTA) at high temperature (900°C or higher) during a short time (several tens of seconds).

X-ray diffraction measurements reported in Figure 3.9 actually confirm that polycrystalline silicon is obtained using this basic process.



(a) (b)

Figure 3.10: Scanning electron microscopy pictures of (a) RTA-crystallized and (b) as-deposited (625°C at 0.1 Torr) polysilicon layers.

Another interesting feature of this approach is that it is also expected to provide lower surface roughness than in the case of as-deposited polySi. Crystallization of amorphous silicon using thermal anneals is indeed known to retain the smooth surface of amorphous silicon [18, 23]. The surface characteristics of such a layer are discussed in the next section.

3.5.1 Morphology of RTA-crystallized polysilicon layer

The size of the grains in a RTA-crystallized polysilicon layer was investigated using scanning electron microscopy (SEM). The SEM picture is shown in Figure 3.10a where it is compared with a similar picture obtained on a polySi layer that was deposited at 625°C (Figure 3.10b). It can be seen that the texture of the RTA-crystallized film significantly differs from that of the polySi layer in which the shape of the grains exhibits a typical columnar structure [18]. The grains in the RTA-crystallized layer have a rounder shape and are much smaller. This is the result of the fast and high thermal stress produced by the RTA, which is believed to have favored the creation of a larger number of nucleation sites, and thus also a higher number of smaller grains.

The SEM pictures also suggest that because of the smaller grain size in RTA-crystallized polysilicon that layer presents a smoother surface than in the case of LPCVD polysilicon. This observation was further confirmed by atomic force microscopy (AFM) measurements, which are presented in Figure 3.11: the pictures obtained on the polySi (Figure 3.11c) layer clearly outlines a much rougher sur-

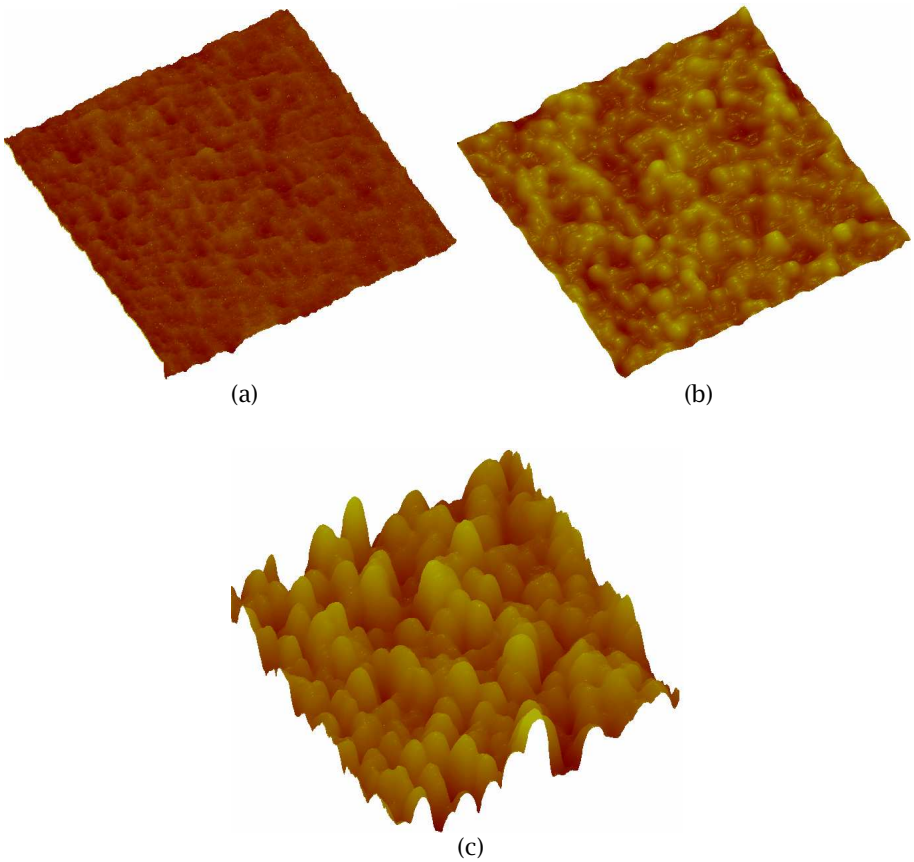


Figure 3.11: AFM pictures of (a) amorphous silicon, (b) RTA-crystallized polysilicon and (c) as-deposited (625°C) polysilicon.

face (and larger grain size) than for the RTA-crystallized sample (Figure 3.11b). As shown in Table 3.4, the rms roughness/maximum height values extracted from the AFM data were respectively 2.24/16.5 and 0.37/3.14 nm for the RTA-crystallized and the as-deposited polysilicon layers. Figure 3.11 and Table 3.4 also show that the morphological data obtained on the RTA-crystallized sample closely correspond to those measured on a smooth, purely amorphous sample (Figure 3.11a), and agree with results previously published in [24].

According to data presented in [25], such a smooth surface could enable a direct bonding between the RTA-crystallized polysilicon and an oxidized donor substrate. The results of preliminary bonding tests are presented in the next section.

Table 3.4: RMS surface roughness and maximum height values extracted from AFM measurements on amorphous silicon, RTA-crystallized polysilicium (RTAC-polySi) and as-deposited polysilicon (polySi). Measured surfaces were 2x2 μm^2 squares.

Sample	RMS roughness [nm]	Maximum height [nm]
$\alpha - Si$	0.364	5.4
RTAC-polySi	0.37	3.14
polySi	2.24	16.5

3.5.2 Bonding between RTA-crystallized polysilicon and oxide

To assess the bonding ability of RTA-crystallized polysilicon, preliminary studies were performed at the laboratory[2] between amorphous silicon deposited on handle substrates (wafers A and B in Table 3.5) and an oxide layer on donor substrates (wafers A' and B' in Table 3.5). As shown in Table 3.5 two different process options were considered: the amorphous silicon layer was RTA-crystallized either *before* (bonded wafer AA') or *after* (bonded wafer BB') the bonding.

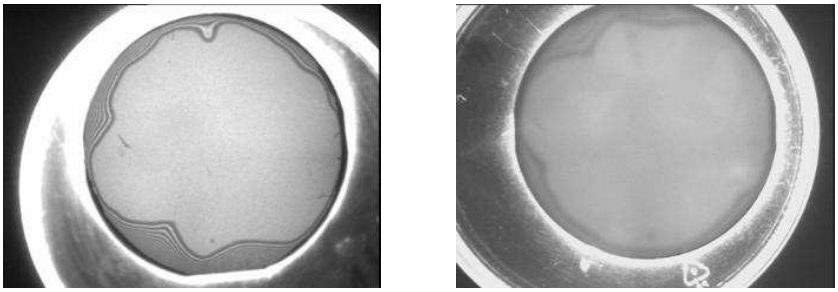
Table 3.5: Process details of the wafer bonding experiments.

Process step	Layer thickness [nm]	A	B	A'	B'
α_{Si} deposition (525°C, 0.1 T)	170	x	x		
Wet oxidation (850°C)	80			x	x
RTA (950°C, 15 sec)	//	x			
Surface activation	//	x	x	x	x
Bonding	//	x		x	
Bonding	//		x		x
RTA (950°C, 15 sec)	//		x	//	//
Thermal anneal (1000°C, 5 hours)	//	x	x	//	//
RTA (950°C, 15 sec)	//	x	x	//	//

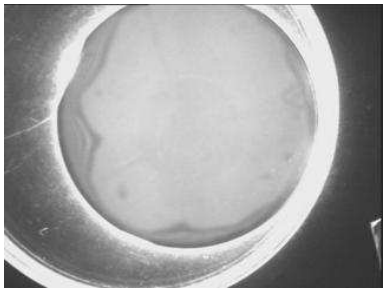
In both cases, the bonding operation was preceded by oxygen plasma-assisted surface activation. This process step increases the density of free covalent bonds at the bonding interface and therefore eases the bonding between the two surfaces [26].

In this early investigation the success of the bonding was assessed by infrared (IR) imagery. By looking "through" the wafer this method indeed provides a cheap and simple means to detect voids and bubbles that are formed at the bonded interface and which prevent successful bonding [27]. IR pictures were taken at

[2] Thanks are addressed to Rémy Charavel and Benoît Olbrechts from the Microwave Laboratory of UCL for processing and measuring the samples.



(a) (b)

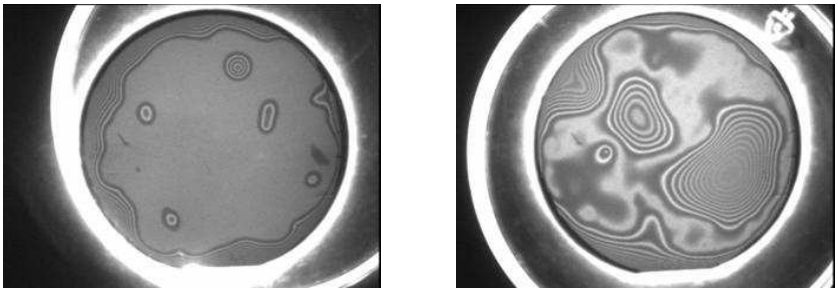


(c)

Figure 3.12: Infrared pictures of RTA-crystallized polySi passivated wafer bonded with oxidized donor wafer (sample AA'): (a) after the bonding, (b) after the 5 hour-long anneal in neutral ambient at 1000°C (c) after the second RTA.

different process stages for both the AA' and BB' samples. Those pictures are presented in Figures 3.12 and 3.13 for the AA' and BB' samples, respectively. In the case of wafer AA' Figure 3.12a seems to indicate that a successful bonding was achieved at the center of the sample. An increase of the bonded surface could be achieved by submitting the bonded wafer to a 5 hour-thermal anneal in nitrogen at 1000°C (Figure 3.12b). In this case the IR image shows a void-free bonding all across the wafer. An additional RTA was then performed on the sample to test the bonded surface. The IR picture (Figure 3.12c) demonstrates that the bonding was not affected by the RTA.

In the case of wafer BB' ($\alpha - Si$) some bubbles remained after the bonding (Figure 3.13a), which might have been caused by hydrogen atoms present in the amorphous silicon layer. As explained in [28] residual hydrogen bonds to silicon atoms at the surface of the amorphous layer and thus reduces the availability of silicon bonds for strong silicon-oxygen bonding at the interface. In this respect, it can also be expected that due to the RTA processed on wafer A, the hydrogen



(a) (b)

(c)

Figure 3.13: Infrared pictures of $\alpha - Si$-passivated wafer bonded with oxidized donor wafer (sample BA'): (a) after the bonding, (b) after the crystallizing RTA, (c) after the anneal.

content of that sample (especially at the layer surface) is reduced, resulting in a better bonding for wafer AA'.

Figure 3.13b and c further indicate that the post-bonding RTA applied on wafer BB' completely damaged the bonded interface and that the neutral anneal could not provide any improvement.

These preliminary bonding tests therefore provide encouraging results suggesting that, due to their excellent surface smoothness properties, RTA-crystallized polysilicon layers can be directly bonded onto a silicon dioxide surface without the need of CMP. These early findings should nevertheless be confirmed by further mechanical testing such as wedge-opening [29]. Bonding tests with larger wafers (8 or 12 inch) should also be performed.

3.5.3 Passivation efficiency vs thermal budget

The crystallization of amorphous silicon and its beneficial impact on the substrate effective resistivity is illustrated in Figure 3.14. In this set of experiment four

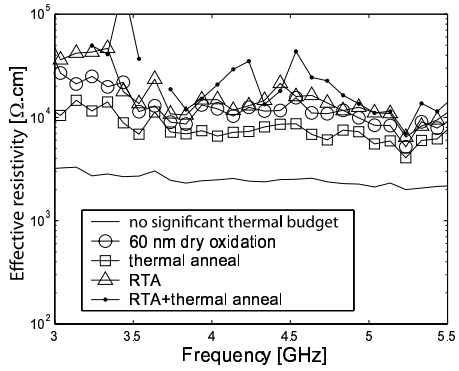


Figure 3.14: Effective resistivity values extracted on $\alpha - Si$ passivated wafers as a function of f and for varying anneal conditions.

Table 3.6: Process details of the samples passivated with LPCVD amorphous silicon crystallized by submitting the wafers to distinct thermal budgets.

Sample	Thermal budget	Oxidation type
BHR31	1h40 at 950°C in O_2 (oxidation)	60 nm-thick dry
BHR32TA	4h at 900°C in N_2 (slow ramp)	450 nm-thick PECVD at 300°C
BHR34	3min at 900°C in N_2 (fast ramp)	450 nm-thick PECVD at 300°C
BHR34TA	3min at 900°C in N_2 (fast ramp) + 4h at 900°C in N_2 (slow ramp)	450 nm-thick PECVD at 300°C

different HR Si samples were passivated with a 300 nm-thick 525°C LPCVD silicon layer and were then submitted to distinct thermal budgets: oxidation at 950°C during 1h40 (BHR31), 4 hour-long thermal anneal (TA) in nitrogen ambient at 900°C (BHR32TA), rapid thermal anneal (RTA) at 900°C during 3 minutes (BHR34) and 3 min-long RTA followed by a 4h00-long anneal at 900°C (BHR34TA). Oxidation details are provided in Table 3.6. All these thermal budgets were expected to crystallize the deposited silicon layer.

Figure 3.14 also includes the data obtained on the unannealed α-Si passivated wafer to allow easy comparison. The results presented in the figure clearly indicate that in all cases the crystallization of the deposited amorphous silicon results in an increase of the passivation efficiency, which is related to the higher trap density

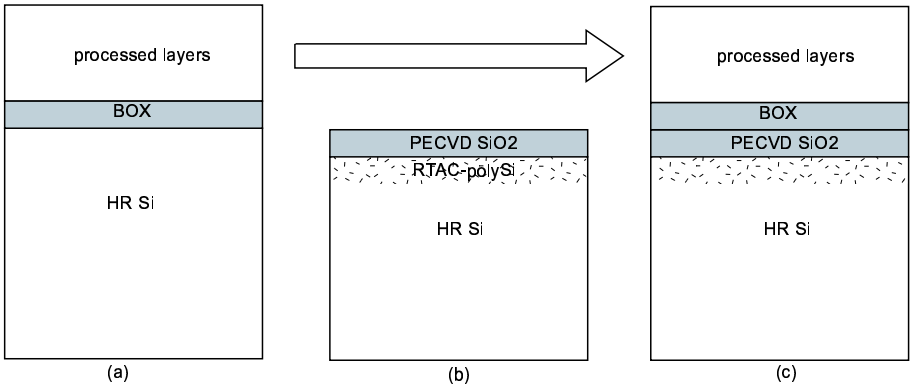


Figure 3.15: Illustration of the layer transfer process: (a) processing of a HR SOI wafer at ST Microelectronics, (b) preparation of the passivated HR Si substrate at UCL, (c) transfer of the SOI top layers onto the passivated substrate using a substrate transfer technique at TraciT Technologies.

in the so-formed polysilicon layers. The data also suggest that even slightly better results are obtained when the Si crystallization is performed using RTA, in which case the average ρ_{eff} value seems to go beyond 10 kΩ.cm. This is also higher than in the case of polysilicon layers deposited at 625°C (Figure 3.8a). A likely explanation for this observation is that, as already mentioned, grains of smaller size are formed during the RTA process. It can be noticed that in this case also, an additional thermal anneal performed in neutral ambient (wafer BHR34TA) seems to provide a beneficial impact on the effective resistivity.

3.5.4 Passivation efficiency of RTA-crystallized polysilicon on industrial SOI technology

The passivation efficiency of RTA-crystallized polysilicon was also investigated on an industrial multilevel SOI technology from ST. The analysis was performed by comparing an unpassivated HR (wafer J409) with a passivated HR wafer (wafer Tracit4). Both wafers originated from the same ST lot. As illustrated in Figure 3.15, the passivation of the second sample was obtained by transferring the processed layers (BOX+front end+back end) (Figure 3.15a) onto a passivated HR silicon wafer (Figure 3.15b) with the method presented in [30]. The wafer resulting from this operation (Figure 3.15c) was therefore a passivated HR SOI substrate with a ST process on the top layers. It must be mentioned that for the transfer process an

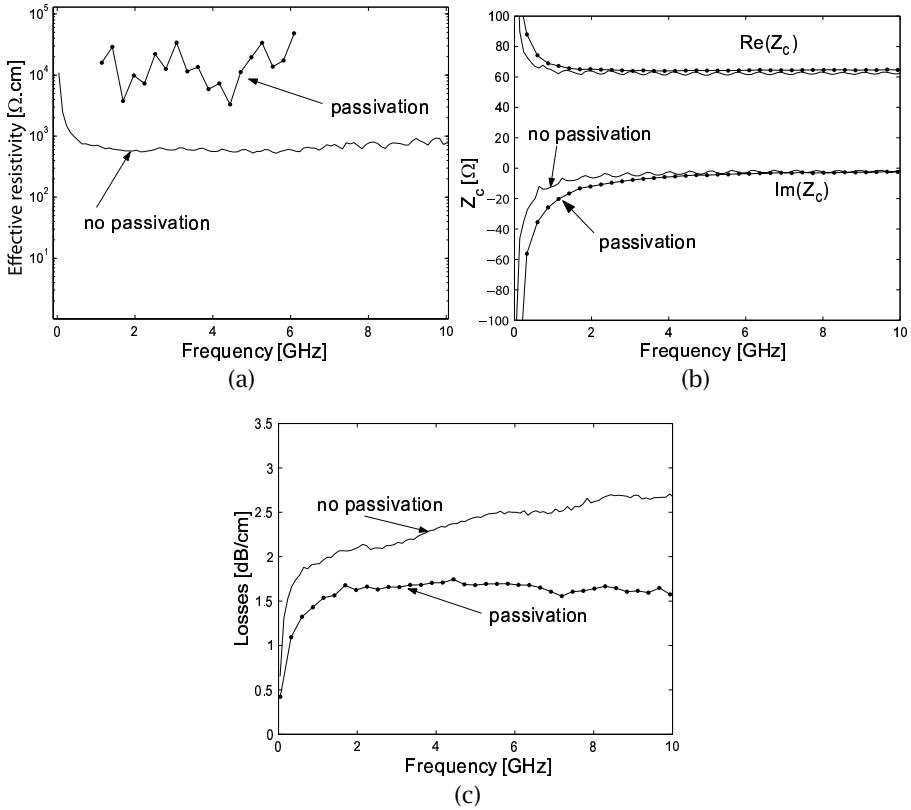


Figure 3.16: Comparison of CPW performance between ST technology processed on an unpassivated SOI substrate and transferred onto a passivated HR Si substrate: (a) effective resistivity, (b) line characteristic impedance and (c) total losses.

additional PECVD oxide needed to be deposited on the passivation layer before the process. The buried oxide of the passivated wafer therefore consisted in a stack formed by the deposited oxide and the BOX of the original wafer, making it thicker (975 nm) than in the case of the unpassivated wafer (450 nm).

3.5.4.1 Impact of passivation on passive devices

The passivation efficiency of the RTA-crystallized polySi layers was analyzed in the case of CPW lines and crosstalk structures. The lines were designed to have a 50 Ω characteristic impedance (W_c = 40 μm, W_g = 206 μm and S = 24 μm, corresponding to Set b in Table 2.2) and the crosstalk structures were similar to the one presented in Figure 2.48a.

The results from the line measurements are reported in Figure 3.16 for the

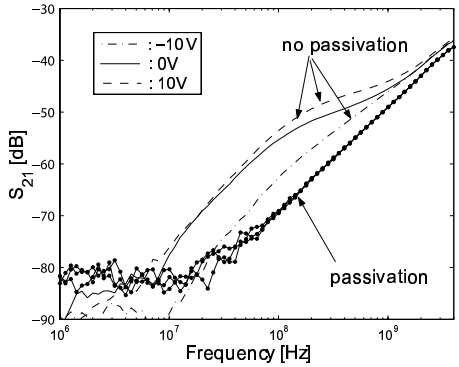


Figure 3.17: Comparison of crosstalk performance between wafers J409 (no passivation) and Tracit4 (passivation).

two wafers. Not surprisingly, a much higher effective resistivity is reported for the passivated wafer, lying around 10 kΩ.cm (Figure 3.16). This causes substrate losses to be virtually null for the passivated wafer. Besides, as the characteristic impedance of the line was not significantly altered by the thicker oxide in the passivated wafer (as shown in Figure 3.16b), the loss difference observed between the two wafers (Figure 3.16c) can be purely attributed to substrate losses in the unpassivated wafer. These losses amount to 30∼70 % of conductor losses in the 1-10 GHz range for this particular line.

The results obtained on the crosstalk structures are presented in Figure 3.17. The measurements are also shown for varying bias conditions. It is seen that:

- a significant crosstalk reduction is obtained on the passivated wafer, which behaves as lossless in the measured frequency range. This reduction is close to 13 dB at 100 MHz and 0 V.
- the passivated substrate, in contrary to the unpassivated substrate, exhibits no bias dependence.

These experimental results confirm the excellent passivation properties of RTA-crystallized polySi and also demonstrate that significant substrate loss reduction and substrate crosstalk can be obtained by passivating the substrate in current industrial HR SOI technologies.

3.5.4.2 Impact of passivation on active devices

The electrical behavior (DC currents, AC capacitances, self heating and RF performance) of active devices was also compared on both wafers in order to check if

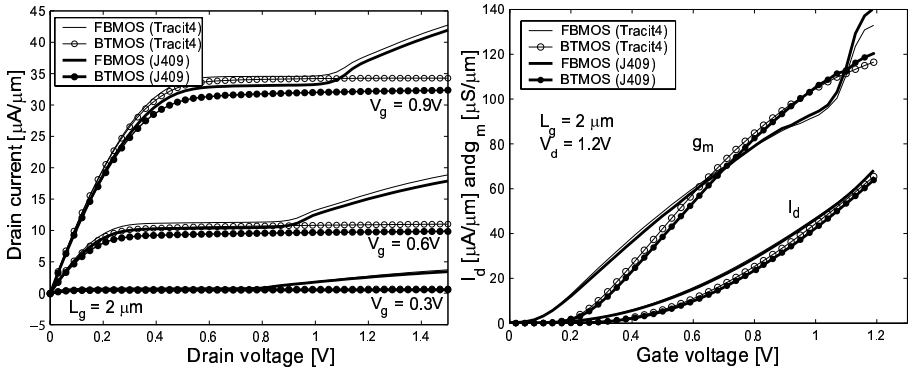


Figure 3.18: Normalized (a) $I_d - V_d$ and (b) $I_d - V_g$ curves measured on wafers J409 and Tracit4 for the 2 μm-long floating body and body-tied devices.

Table 3.7: Threshold voltages (in [V]) extracted on the measured devices.

	$L_g = 2\ \mu m$		$L_g = 0.13\ \mu m$	
	FBMOS	BTMOS	FBMOS	BTMOS
UCL4	0.385	0.278	0.316	0.381
J409	0.437	0.292	0.367	0.386

the polysilicon layer below the BOX has an impact on the device properties. The studied devices were 130 nm and 2 μm gate length (L_g) partially depleted (PD) SOI MOSFETs with 30 fingers. The width of the fingers was 2 μm (resp. 4 μm) for the short (resp. long) devices. Both floating body (FB) and body-tied (BT) MOSFETS were considered.

DC currents. The normalized $I_d - V_d$ curves recorded for the 2 μm-long transistors are presented in Figure 3.18a. It is seen that for both the BT and FB devices the curves outline similar DC behavior on the two wafers. In particular, the well-known kink (related to floating body effects) appears at a similar V_d value (which is V_g-dependent) for both the passivated and the unpassivated substrate and in both cases too the kink was totally suppressed using a body-tied architecture.

The figure also outlines slightly higher currents for the passivated wafer, which were probably associated to the smaller threshold voltages reported on that wafer (Table 3.7).

The I_d-V_g curves of the long devices were also measured in saturated and linear regimes. The drain current as well as the gate transconductance are plotted in Figure 3.18b along with the gate transconductance (g_m) in saturation. Excellent matching is here also observed between the two investigated wafers. In linear regime the g_m/I_d curves presented in Figure 3.19 outline the same body factor

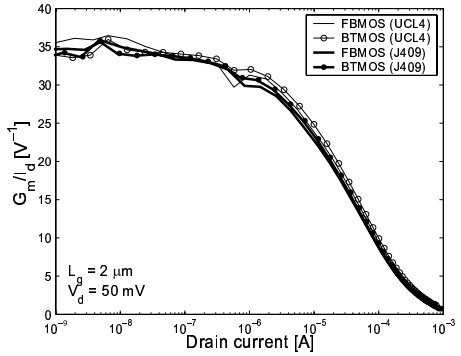
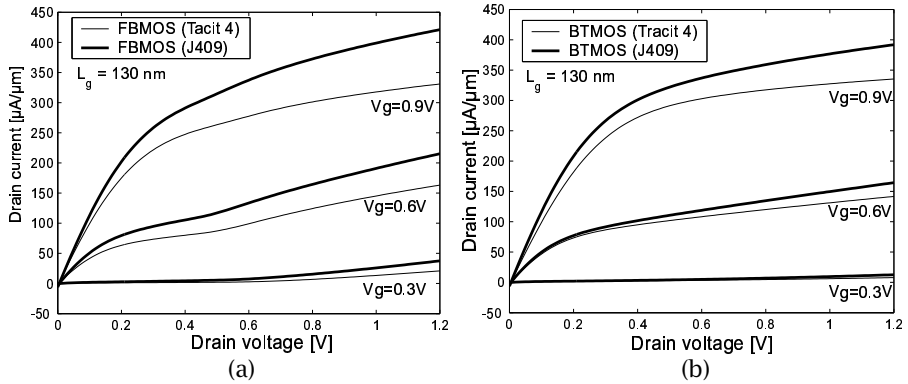


Figure 3.19: Gate transconductance over drain current ratio measured in linear regime on wafers Tracit4 and J409 for the 2 μm-long devices.

(which is inversely proportional to the g_m/I_d ratio in weak inversion) for both wafers, suggesting that in this range of values (close to 1 μm) the thickness of the BOX and the passivation layer do not impact on the DC behavior of long devices.

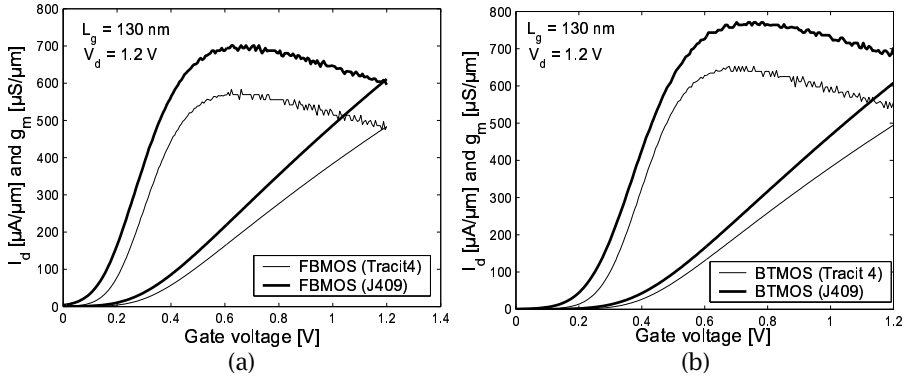
However, for the devices with the shortest channel length significant differences were found both in the $I_d - V_d$ (Figure 3.20) and in $I_d - V_g$ curves (Figure 3.21). Higher currents and higher maximum values of gate transconductance (g_{mmax}) were observed on the unpassivated wafers for both the BT and FB MOSFETs, despite slightly higher (or similar) threshold voltage values for that wafer (Table 3.7). The g_m/I_d curves reported in Figure 3.22a also indicate higher short channel effects in the case of the unpassivated wafer (lower value of $(g_m/I_d)_{max}$), which is also further supported by the higher DIBL values reported on that wafer: 230 (resp. 169) compared to 148 (resp. 128) mV/V for the FB MOSFET (resp. BT MOSFET). The DIBL was obtained by comparing the threshold voltages in linear and in saturation regimes. The value of V_t in saturation regime was extracted from the measurements by extrapolating the $\sqrt{(I_d)}\ vs\ V_g$ curve, as illustrated in Figure 3.22b.

AC capacitances. In order to explain these differences RF multiport measurements were performed on devices with 3 RF accesses and with identical dimensions on both wafers. In such devices the third access is connected to the body of the devices. As explained in the 4th chapter of this work, this characterization method provides a powerful means to see the transistor from "inside", i.e., from the body node.



(a) (b)

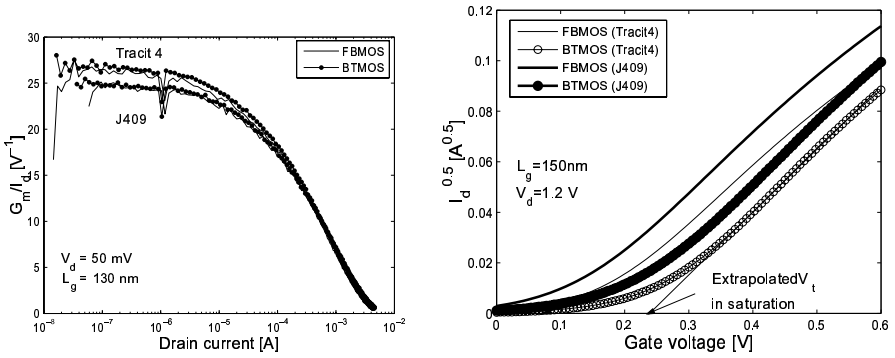
Figure 3.20: Normalized $I_d - V_d$ curves measured on wafers Tracit4 and J409 for the measured 130 nm-long (a) floating body and (b) body tied devices.



(a) (b)

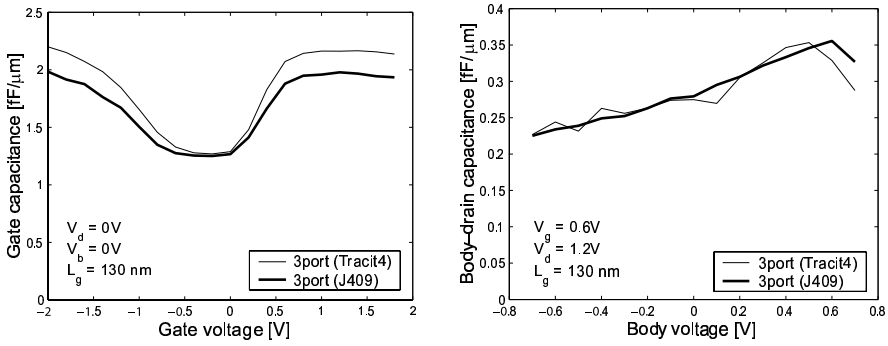
Figure 3.21: Normalized $I_d - V_g$ curves measured on wafers Tracit4 and J409 for the measured 130 nm-long (a) floating body and (b) body tied devices.

Figure 3.23a illustrates the variations of the input gate capacitance as a function of the gate voltage at $V_d = 0$ V. The devices from both wafers exhibit C-V curves that are typical to those of MIS capacitors, with capacitance values close to C_{ox} when the device is either accumulated (negative V_g in these nMOS devices) or inverted (positive V_g). The figure also shows that higher C_{ox} values are reported on the passivated wafer (Tracit4), suggesting that devices on this wafer presents either smaller oxide thickness or longer effective gate length. However, the current level similarities observed between the two wafers in the case of long devices overrule the first hypothesis, and actually comforts the second presumption since a given variation of effective gate length is expected to have a large impact on small devices and be negligible in the case of long devices.



(a) (b)

Figure 3.22: (a) Gate transconductance over drain current ratio measured in linear regime on wafers Tracit4 and J409 for the 130 nm μm-long devices; (b) square root of I_d *vs* V_g curves for V_t extrapolation in saturation regime.

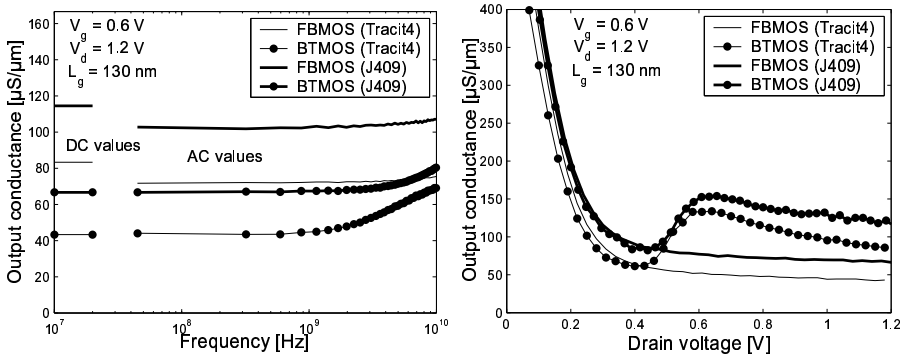


(a) (b)

Figure 3.23: Normalized (a) gate and (b) body-drain capacitances extracted from multiport measurements on 130 nm-long RF 3-port devices from wafers Tracit4 and J409.

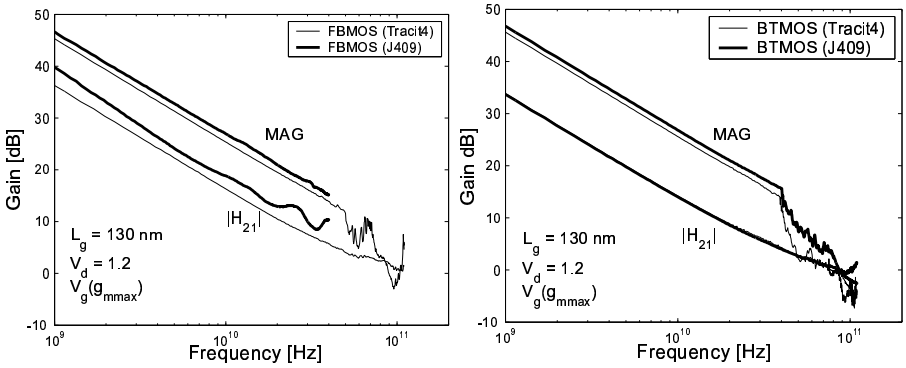
The measurements of the body-drain capacitance yielded approximately the same values on both wafers (Figure 3.23b), suggesting that the HALO doping levels were similar on both wafers. The variations of the effective gate length are suspected to originate from variations of the physical polysilicon gate length. Besides, a shorter gate length in the case of the unpassivated wafer can also explain the stronger short channel effects reported for that wafer.

Self heating. It is also worth mentioning that the thicker buried oxide in the case of the passivated wafer did not induce any current deterioration related to self heating for the investigated 130 nm-long devices. The buried oxide is indeed



(a) (b)

Figure 3.24: Normalized output conductance measured on wafers Tracit4 and J409 for the 130 nm-long floating body and body tied devices as a function of (a) frequency (b) drain voltage.



(a) (b)

Figure 3.25: Current and maximum stable gains measured on the 130 nm-long (a) FBMOS and (b) BTMOS devices from the unpassivated and passivated wafers.

known to form a strong barrier to heat dissipation due its poor thermal conductivity (100 times lower than that of silicon). As the device heats up due to Joule effect the carrier effective mobility is reduced due to higher thermal agitation, which translates into a reduction of both drain current and output conductance. Under AC operation, the reduction of the output conductance is yet annihilated at frequencies higher than the cut off frequency of heat dissipation. This means that an increase of the output conductance is usually observed in the 10^{6-8} Hz range when the device is self heated [31]. In our case, we observe a good correspondence between the DC and AC values of the output conductance for the BT MOSFETs on the two wafers (Figure 3.24a), which suggests that the self heating is

negligible in both cases. The discrepancies observed between DC and AC values for the FB MOSFETs are due to floating body effects, which increase the DC value of the output conductance in the sub-kink region (Figure 3.24b). As discussed in the next chapter, this increase is suppressed for frequencies higher than $\sim 10^5$ Hz.

RF performance. The RF properties of the devices were also briefly investigated on the two-port devices from both wafers. The current and maximum stable gains are plotted in Figures 3.25a and b for the 130 nm-long floating body and body tied devices, respectively. In general, slightly lower gains were recorded on the passivated wafer, with an exception for $|H_{21}|$ on the BT MOSFET. This is more than likely due to the lower g_{mmax} values recorded on that wafer and related to the longer effective channel length.

These curves demonstrate that substantially high RF performance can be achieved in substrate surface-passivated HR SOI wafers.

3.6 Conclusion

Relying on the experimental findings reported in the previous chapter, the main objective of this section was to propose a new technique to passivate the substrate surface of UNIBOND HR SOI wafers. At a wafer fabrication level, the most suitable method consists in depositing the passivation layer at the top of the HR handle wafer before the bonding. The passivation techniques proposed in the literature for conventional HR bulk wafers were then reviewed. Amongst all proposed solutions, passivation with deposited silicon appeared to be the most promising technique, due essentially to the CMOS compatibility of this material and the excellent results reported in earlier works ([11,16]). The passivation efficiency of deposited silicon was therefore quantified as a function of deposition temperature and layer thickness. Various deposition temperatures lead to distinct morphological structures: amorphous silicon and polysilicon were respectively deposited by LPCVD at 525 and 625°C. The morphological textures were confirmed by X-ray diffraction. An intermediary deposition temperature of 580 °C was also investigated, for which a mixture of amorphous and polycrystalline silicon was probably obtained. The impact of heavy thermal budgets on the passivation efficiency of the deposited layers was also studied.

The quantification of the passivation efficiency was performed by effective resistivity (ρ_{eff}) extraction, a method described in the previous chapter. The experimental data lead to the following conclusion:

· the best passivation efficiency (highest ρ_{eff} value, in the 5-10 k Ω.cm range) was

obtained using polycrystalline silicon, which is likely to be related to the higher density of traps in such a layer,

- the best passivation efficiency was obtained for a layer at least 300 nm-thick,
- on all types of layer (amorphous, mixed polycrystalline or fully crystallized polysilicon) an increase of the passivation efficiency was observed after long thermal anneals in neutral ambient, which was attributed to the recrystallization of silicon in the case of deposited amorphous (or mixed) layers and to the effusion of hydrogen atoms from the passivation layer.

On the basis of these results, a new type of passivation layer was investigated: polysilicon obtained by Low Pressure Chemical Vapor Deposition (LPCVD) of amorphous Si at 525°C followed by a rapid thermal anneal (RTA)-induced silicon crystallization (RTAC). The resulting polycrystalline texture was confirmed by both X-ray diffraction and SEM pictures. Compared to as-deposited polysilicon, this particular layer showed:

- excellent passivation properties (with ρ_{eff} values in the 10 kΩ.cm), which was demonstrated for the case of an industrial multilevel SOI technology from ST Microelectronics. The better passivation property of RTAC-polySi is related to the smaller grain size, as confirmed by SEM pictures.
- excellent surface roughness (rms σ of 0.37 nm).

Preliminary bonding tests also demonstrated that bonding of a RTAC-polySi surface onto a thermal oxide was successful without CMP. This bonding was shown to sustain high thermal budgets, such as RTA. The non requirement of CMP to achieve successful bonding reduces the cost of integration of such a layer within the fabrication process of UNIBOND SOI wafers.

As a conclusion, the experimental results presented in this chapter show that the electrical, morphological and thermodynamics properties of RTAC-polySi makes this particular material the best candidate for substrate passivation in UNIBOND HR SOI wafers at reduced cost. Future work should consist in performing additional testing focusing on the following aspects:

- electrical characteristics: a specific method should be set up to quantify the level of bulk and interface trap densities in the deposited layer, in order to provide a process control parameter,
- thermodynamic behaviour: further testing should be performed to understand and identfy the dominant mechanisms by which the effective resistivity is increased during thermal anneals on the RTAC-polySi layer,

- wafer bonding:
  - the mechanical strength of the bonding should be evaluated by wedge-opening measurements such as in [29],
  - the quality of the bonding should be assessed over a complete CMOS processing,
  - the feasibility of the bonding should also be investigated on wafers of larger diameters, since currently fabricated UNIBOND SOI wafers are 12 inch-wide,
  - the feasibility of the bonding should also be evaluated between an oxidized substrate covered with RTAC-polySi and a naked HR substrate, in which case the bonding would be performed between RTAC-polySi and thermal oxide surfaces,
- mechanical properties: the mechanical properties of RTAC-polySi such as residual stress and thermal expansion coefficient have not been investigated. It is expected that due to the random distribution of crystal orientations as well as the round shape of the grains in the RTA-crystallized polySi layer, this material presents low residual stress. It is also expected that, as a silicon-based material its thermal properties should be similar to those of the substrate and that thermal mismatching (which causes undesired wafer warping after high thermal processing) should therefore not occur. This CMOS-compatibility should nevertheless be confirmed by additional experiments.

And last, the impact on active devices of a surface-passivating polysilicon layer below the BOX was also investigated in the case of an industrial 130 nm SOI technology from ST. The passivated wafer had a BOX thickness around twice higher (975 nm) than the unpassivated wafer (450 nm) used for comparison. Very similar results were observed between the two wafers for long channel devices and slight differences were reported for short channel length (130 nm) due to effective gate length variations between the two wafers. It could be concluded from those experimental data that no significant degradation of the DC and RF characteristics were observed for such value of BOX thickness. Better results may actually be expected as the BOX thickness is scaled down since by capturing free carriers from the bulk the polysilicon layer forms a pseudo ground plane below the BOX. Thinner BOX and ground planes below the BOX are both known to contribute to the reduction of SCE in sub 0.1 μm devices [32]. Further work should also be performed to confirm this trend.

References

[1] [Online]. Available: http://www.spectrum.ieee.org

[2] [Online]. Available: http://www.sciencedirect.com

[3] C. Detcheverry, W. van Noort, and R. Havens, "New low-cost thermally stable process to reduce silicon substrate losses: A way to extreme frequencies for high volume Si technologies," *Digest of 2004 International Electron Device Meeting*, pp. 463–466, 2004.

[4] G. Posada, G. Carchon, P. Soussan, G. Poesen, and B. N. abd W. De Raedt, "High resistivity silicon surface passivation for the thin-film MCM-D technology," *6th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 46–49, San Diego, January 2006.

[5] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, C. P. Liao, S. C. Pai, and C. C. Chi, "The fabrication of very high resistivity silicon with low loss and cross talk," *IEEE Electron Dev. Lett.*, vol. 9, pp. 653–655, 2000.

[6] ——, "RF loss and crosstalk on extremely high resistivity (10k-1MΩ.cm) Si fabricated by ion implantion," *2000 IEEE International Microwave Symposium Digest*, pp. 221–224, 2000.

[7] R. Doerner, J. Gerdes, C. Rheinfelder, F. J. Schmuckle, W. Heinrich, K. Strohm, F. Schaffler, and J. Luy, "Modelling of passive elements for coplanar SiGe MMIC's," *IEEE MTT-S 1995 Int. Microwave Symp. Dig.*, vol. 3, pp. 1187–1190, 1995.

[8] Y. Wu, S. Yang, H. Gamble, B. Armstrong, V. F. Fusco, and J. Stewart, "The effect of SiO_2 interface layer on CPW lines and schotky barrier diodes," *Digest of Silicon Monolithic Integrated Circuits in RF Systems*, pp. 178–180, 1998.

[9] Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 1, pp. 10–12, 1999.

[10] B. Rong, J. N. Burghartz, L. K. Nanver, B. Rejaei, and M. van der Zwan, "Surface-passivated high resistivity silicon substrates for RFICs," *IEEE Electron Dev. Letters*, vol. 25, no. 4, pp. 176–178, 2004.

[11] H. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, and J. A. C. Stewart, "Low-loss CPW lines on surface stabilized high-resistivity silicon," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 10, pp. 395–397, 1999.

[12] H.-T. Lue, T.-Y. Tseng, and G.-W. Huang, "A method to characterize the dielectric and interfacial properties of metal-insulator-semiconductor structures by microwave measurements," *J. App. Ph.*, vol. 91, no. 8, pp. 5275–5282, 2002.

[13] A. Jansman, J. v. Beek, M. v. Delden, A. Kemmeren, A. d. Dekker, and F. Widdershoven, "Elimination of accumulation charge effects for high resistive silicon substrates," *Digest of 2003 European Solid-State Device Research*, pp. 3–6, 2003.

[14] E. Valletta, J. v. Beek, A. d. Dekket, N. Pulsford, H.F.F.Jos, L. d. Vreede, L. Nanver, and J. Burghartz, "Design and characterization of integrated passive elements on high ohmic silicon," *2003 IEEE International Microwave Symposium Digest*, pp. 1235–1238, 2003.

[15] S. Franssila, *Introduction to Microfabrication*. England: John Wiley and Sons, 2004.

[16] P. Baine, M. Jin, H. Gamble, B. Armstrong, D. Linton, and F. Mohammed, "Crosstalk suppression in SOI substrates," *Solid State Electronics*, vol. 49, no. 9, pp. 1461–1465, 2005.

[17] R. Bisaro, J. Magariñio, N. Proust, and K. Zellama, "Structure and crystal growth of atmospheric and low-pressure chemical-vapor-deposited silicon films," *Journal of Applied Physics*, vol. 59, pp. 1167–1178, 1986.

[18] T. Kamins, *Polycrystalline Silicon for Integrated Circuit Applications*. Norwell, MA: Kluwer Academic Publishers, 1988.

[19] M. Hack, J. G. Shaw, P. G. Lecomber, and M. Willums, "Numerical simulations of amorphous and polycrystalline silicon thin-film transistors," *Japanese Journal of Applied Physics*, vol. 29, no. 12, pp. 2360–2362, 1990.

[20] R. A. Street, *Technology and Applications of Amorphous Silicon*. Springer, 1999.

[21] E. P. Donovan, F.Spaepen, D. Turnbull, J. M. Poate, and D. C. Jacobson, "Calorimetric studies of crystallization and relaxation of amorphous si and ge prepared by ion implantation," *Journal of Applied Physics*, pp. 1795–1804, 1985.

[22] A. Szekeres, M. Gartner, F. Vasiliu, M. Marinov, and G. Beshkov, "Crystallization of α-Si:H films by rapid thermal annealing," *Journal of Non-Crystalline Solids*, pp. 954–957, 1998.

[23] G. Harbeke, L. Krausbauer, E. F. Steigmeier, A. Widner, H. Kappert, and G. Neubebauer, "Growth and physical properties of LPCVD polycrystalline silicon film," *J. Electrochem. Soc.*, vol. 131, no. 3, pp. 675–682, 1984.

[24] T. Lee, *The design of CMOS radio-frequency integrated circuits.* Cambridge, United Kingdom: Cambridge University Press, 1998.

[25] N. Miki and S. M. Spearing, "Effect of nanoscale surface roughness on the bonding energy of direct-bonded silicon wafers," *Journal of Applied Physics*, vol. 94, no. 10, pp. 6800–6806, 2003.

[26] Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology*. Wiley-Interscience, 1998.

[27] T. Piotrowski and W. Jung, "Characterization of silicon wafer bonding by observation in transmitted infrared radiation from an extended source," *Thin Solid Films*, vol. 364, pp. 274–279, 2000.

[28] J. Wei, S. M. L. Nai, C. K. S. Wong, Z. Sun, and L. C. Lee, "Low temperature glass-to-glass wafer bonding," *IEEE Trans. Advanced Packaging*, vol. 26, no. 3, pp. 289–294, 2003.

[29] Y. Bertholet, F. Iker, J.-P. Raskin, and T. Pardoen, "Steady-state measurement of wafer bonding cracking resistance," *Sensors and Actuators A*, vol. 110, pp. 157–163, 2004.

[30] C. Lagahe-Blanchard, B. Aspar, P. Paillet, V. Ferlet-Cavrois, N. Fel, C. Pavageau, J. du Port de Poncharra, and H. Moriceau, "New SOI devices transferred onto fused silica by direct wafer bonding," *207th ECS Meeting: 12th International Symposium on Silicon-on-Insulator Technology and Devices*, Quebec City, 2005.

[31] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, R. J. T. Bunyan, and M. J. Uren, "Self-heating effects in SOI MOSFET's and their measurements by small signal conductance techniques," *IEEE Trans. Electron Dev.*, vol. 43, no. 12, pp. 2240–2248, 1996.

[32] T. Ernst, C. Tinella, and S. Cristoloveanu, "Fringing fields in sub-0.1 μm FD SOI MOSFETs: Optimization of the device architecture," *Solid State Electronics*, vol. 46, no. 3, pp. 373–378, 2002.

CHAPTER 4

FLOATING BODY EFFECTS: A WIDEBAND CHARACTERIZATION OF THE BODY NODE IN PD SOI DEVICES BY MULTIPORT MEASUREMENTS

4.1 Introduction

As inferred in the introductory chapter of this work, the SOI technology is well suited for low power RF applications due, essentially, to a reduction of leakage current provided by the insulating buried oxide and a reduction of the junction capacitances. Substrate losses can also be dramatically reduced when high resistivity substrates are used.

From an analogue/RF application perspective, FD devices are known to provide superior characteristics than their PD counterparts in terms of analogue [1] (normalized gate transconductance, normalized drain current), RF [2] (cut off frequencies) as well as noise [3] properties. However, the fabrication of FD devices is more challenging than for PD devices, since FD are very sensitive to film thickness variations and inherently present higher source/drain resistances. On the other hand PD SOI processing techniques can be easily imported from planar bulk technologies, thus leading to significantly lower processing cost. Essentially for this reason all major foundries (IBM, AMD, Freescale,..) currently producing SOI chips for digital logic have adopted the PD architecture, which forms the mainstream of the SOI market.

At a transistor level a challenging issue related to the PD SOI architecture consists in the well-known *floating body effects* (FBE) [4]. Those effects are associated with the body region in the silicon film that is left unconnected or floating. The potential of the body is then mainly controlled by external mechanisms, such as capacitive coupling with the other electrodes and charge injection. As the body region forms a back gate in the intrinsic core of the devices, its potential largely influences the device behaviour. It is the time variations of the body potential which are at the origin of the FBE and which have caused many surprising behaviors in SOI transistors and digital circuits.

One purpose of this chapter is to present a small signal AC investigation of

FBE in PD MOSFETs for two sources of FBE: impact ionization and gate tunneling. It is shown here that AC characterization of the devices, and in particular of the body region, is of substantial interest for a better understanding of the physics involved in those mechanisms. The analysis is performed using a small signal modeling approach, for which the model includes a fourth node associated with the body. In the case of floating body (FB) devices this node is simply left floating in the model.

Under DC conditions, FBE are traditionally suppressed by fixing the body potential to a constant value, which is typically accomplished by providing lateral contacts to the body region. In that case, body-contacted (BC) devices are formed. These contacts are then either connected to the source or to the gate, forming respectively, body-tied (BT) or dynamic threshold (DT) MOSFETs. AC analysis of both BT and DT MOSFETs are then also be performed in this chapter, and the efficiency of their body contact is assessed. One outcome of this study is that the high value of the body contact resistance in current technologies plays a detrimental role on the quality of the body contact, and thus on the RF performance of the devices: above a certain frequency the body contacts loose their efficiency and the AC body potential becomes controlled by capacitive coupling with the other nodes. Accurate characterization of the body resistance and the body capacitances is therefore crucial for a correct prediction of the RF behaviour of body-contacted PD SOI MOSFETs. It is shown in the last section of this chapter that RF measurements performed on 3-port devices (for the gate, drain and body) with multiport VNA measurements can be very helpful for a deep characterization of those parameters.

Unless otherwise stated all measurement results presented in this chapter were obtained from devices processed at ST Microelectronics using a 0.130 μm PD SOI technology with a film thickness (t_{Si}) of 150 nm, a gate oxide thickness (t_{ox}) of 2.3 nm and 6 metal levels.

4.2 FBE under static regime

In Partially Depleted SOI technology, the thickness of the silicon film is larger than the width of the depletion region that extends below the channel. A quasi-neutral region (called the body) therefore exists within the silicon film, which is sandwiched between the depletion region and the top of the buried oxide. This region being inherently isolated from the "outside world", its potential is mainly determined by external influences such as capacitive coupling and charge injection. The main mechanisms of charge injection consist in impact ionization, gate tunneling,

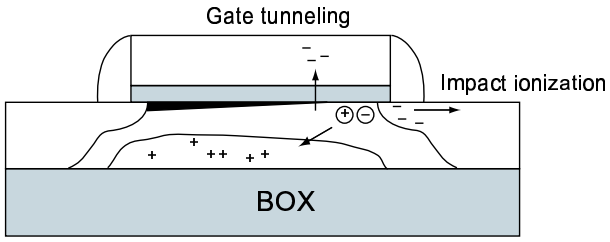


Figure 4.1: Main mechanisms of body charging in FB PD SOI MOSFETs: gate tunneling and impact ionization.

and leakage currents through the forward biased and reverse-biased source/body and drain/body junctions. Time variations of the body potential largely affect the device behaviour and are responsible for the well known *floating body effects*, which impact on circuit performance.

In digital applications, floating body effects are mostly associated with capacitive charging of the body and carrier recombination. They can cause undesired leakage (parasitic bipolar leakage in passgate circuits [5]), hysteresis and history dependence of gate delay [6, 7]. These issues can yet be solved or minimized by proper circuit design [5, 7].

In low frequency analog applications FBE are predominantly governed by mechanisms of charge injection into the body region. Until recently, the main physical phenomenon responsible for body charge injection was impact ionization at the drain side. In saturated regime, holes generated by impact ionization accumulate in the body, which leads to an increase of the body potential [4]. This is illustrated in Figure 4.1. The potential of the body (V_{bi}) is raised until the source/body junction becomes forward biased, which allows the additional hole flow to leave the body region or recombine with incoming electrons.

In recent technologies however, the aggressive downscaling of device dimensions has put a high pressure on the gate oxide also, which has now become thin enough as to allow significant amounts of current leakage through the gate. When the device is biased in strong inversion, this current is mostly associated with holes or electrons tunneling through the oxide: holes originate from the gate polysilicon valence band (HVB) and electrons issue from the conduction band (ECB) or the valence band (EVB) of the silicon film [8]. In the latter case unbalanced holes are left in the body [9] and, similarly to impact ionization, the resulting current tends to positively charge the body region (Figure 4.1), thus also leading to an increase

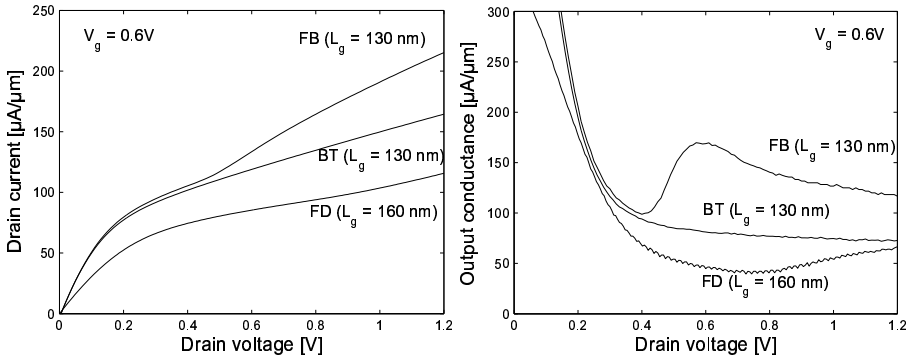


Figure 4.2: Typical $I_d - V_d$ (a) and $g_d - V_d$ (b) curves measured on floating body (FB), body-tied (BT) and fully depleted (FD) devices, illustrating the kink effect.

of V_{bi}.

A direct consequence of the body potential increase is a reduction of the threshold voltage of the front gate channel, which in turn induces an increase of the drain current. However, it is important to notice that both mechanisms of charge injection affect the device behaviour under distinct external bias conditions:

- Impact ionization produces a noticeable increase in the $I_d - V_d$ curves for values of V_d typically higher than the threshold of impact ionization in doped silicon. This threshold depends on the doping level, and therefore also on transistor generation. For the 0.130 μm SOI technology investigated here, it is approximately 0.5 V. The sudden current rise induced by impact ionization is called *kink* in the $I_d - V_d$ curves or *kink effect.* As shown in Figure 4.2a the kink effect is typical to FB PD SOI technology. It can be suppressed when the body region is connected to a fixed potential, as in the case of BT MOSFETs. It is also strongly reduced when a FD technology is used [10]. In this figure the FD devices were made at Leti. From an analogue designer point of view the kink in the $I_d - V_d$ curve induces a large parasitic increase of the device output conductance (Figure 4.2b), which can have negative impacts on the performance of analogue circuits [11, 12].

- On the other side, gate tunneling current becomes significant for gate bias values sufficiently large as to reduce the potential barrier for electrons across the gate stack ($\simeq$ 1.1 V in this 0.130 μm technology). The increase of drain current in this case affects the $I_d - V_g$ curves and produces a second "hump" in the $g_m - V_g$ curves, which is called *linear kink effect* (LKE) [13] or *gate-induced floating body effect* (GIFBE) [14]. It is shown in Figure 4.3 for 2 μm-long devices that, similarly

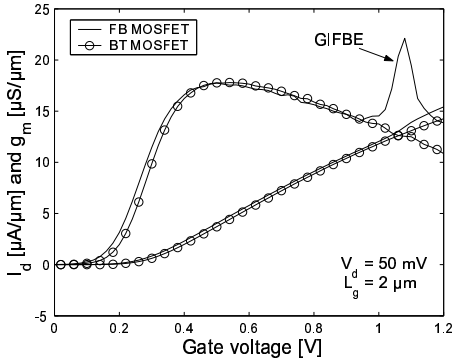


Figure 4.3: Typical $I_d - V_g$ and $g_m - V_g$ curves observed in linear regime on a FB and a BT devices illustrating the GIFBE.

to the kink effect, the GIFBE does not take place when the body is contacted.

As the floating body effects are associated with body voltage fluctuations both the kink effect and the GIFBE quantitatively depend on device history, which is illustrated in Figure 4.4 for 2 μm-long devices. Both the kink effect (Figures 4.4a and b) and the GIFBE (Figures 4.4c and d) are shown, as a function of the delay time used for the measurement in *forward bias* (Figures 4.4a and c) and in *reverse bias* (Figures 4.4b and d) modes. It is clear from the figures that for the two investigated floating body effects the position of the g_d and g_m peaks is a strong function of the measurement condition. In particular, in forward bias mode and for longer delay times the peaks are shifted to lower bias values, which is attributed to the lower body potential (and thus the lower value of V_d or V_g required to induce significant impact ionization or gate tunneling, respectively) in the case of slower measurements [14]. Indeed in that case the increase of V_{bi} generated by capacitive coupling is reduced by higher carrier recombination in the body region. When the device is reverse-biased it can be seen from Figures 4.4c and d that the intensity of the peaks is reduced regardless of the delay time used for the measurements. The explanation for this observation is that in this case the body is pre-charged under high-bias conditions. At lower bias, impact ionization or gate tunneling become negligible and the body voltage slowly recovers its equilibrium state through carrier recombination.

The correct prediction of the kink effect as well as GIFBE is crucial for the design of successful analogue circuits, which can only be achieved if accurate models exist. The elaboration of such models requires a quantitative understanding of the

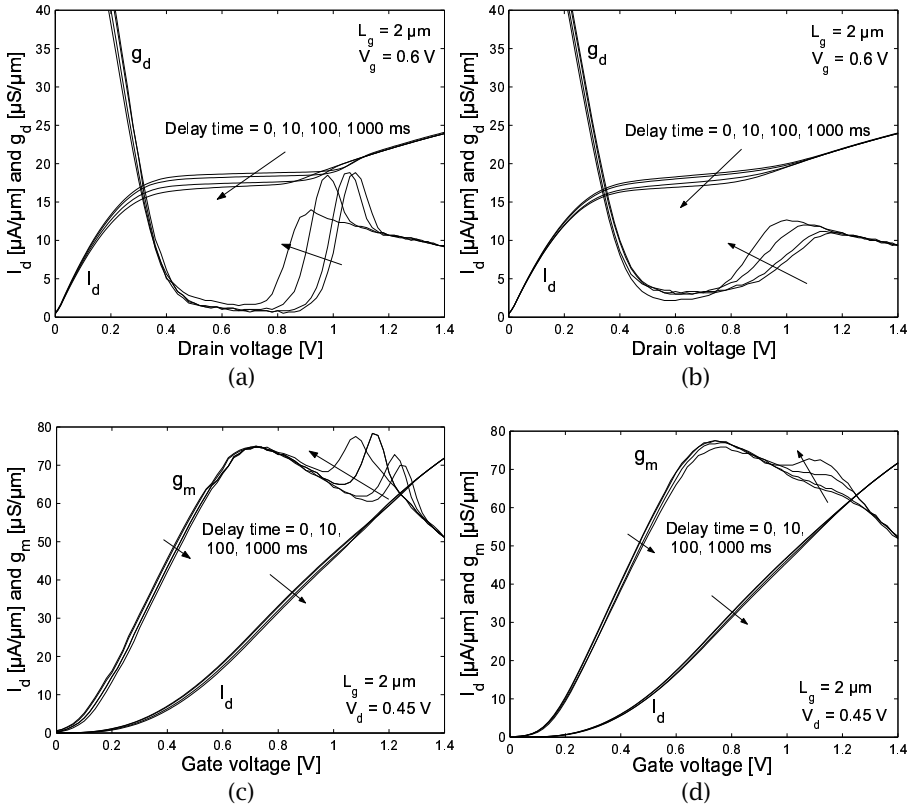


Figure 4.4: Illustration of the kink effect (resp. GIFBE) as a function of delay time in (a) (resp. (c)) forward bias and (b) (resp. (d)) reverse bias modes.

body charging mechanisms, such as body-source and body-drain junction leakage, hole-electron recombination inside the body, gate tunneling current and impact ionization current. The dynamics of the body charging should also be well appreciated, since the transient behavior of the body voltage quantitatively determines the amplitude of the kink and GIFBE peaks.

In that respect AC characterization can provide both qualitative and quantitative support. The results of AC measurements performed on FB, BT and DT MOSFETs are therefore presented in the following sections along with the time constant associated with both the kink effect and the GIFBE. These experimental data are then explained on the basis of a complete small signal model including the body node. It is shown that an accurate modeling of the AC behaviour of FBE requires as accurate characterization of the body node, which, as reported in the

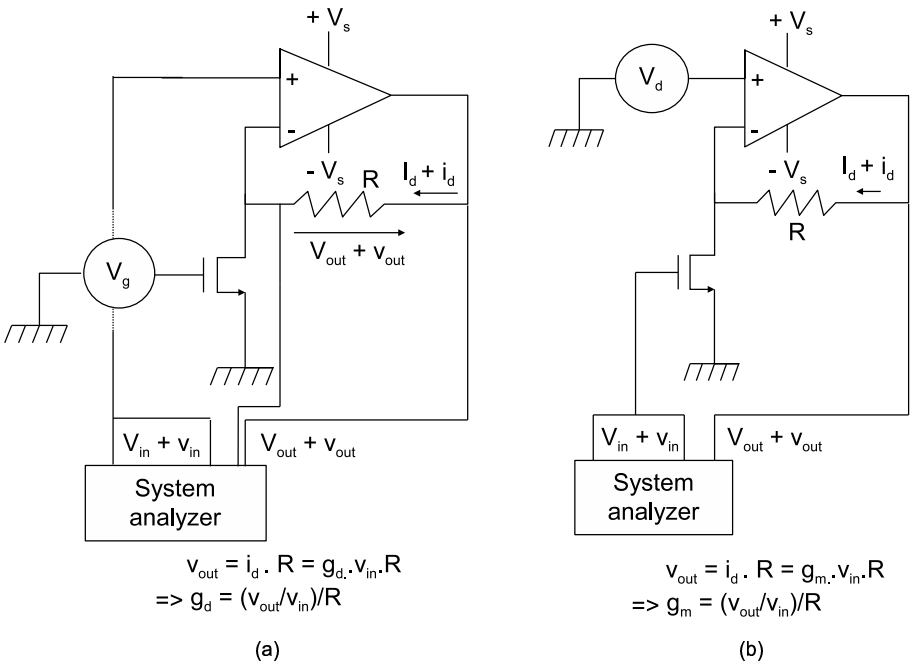


Figure 4.5: Experimental setup for the AC measurements of the kink effect (a) and the GIFBE (b).

last part of this chapter, can be performed by the measurements of three-port devices.

4.3 AC behavior of floating body effects

To gain more insight of the dynamics associated with both the kink effect and the GIFBE, these two floating body effects were measured as a function of frequency. As both mechanisms are characterized by very low cut-off frequencies (below 10 kHz) a specific experimental set up was required. The core of the equipment used was a System Analyzer from HP (HP8163), which can compute the transfer function (i.e., ν_{out}/ν_{in} as a function of frequency, where ν_{out} and ν_{in} are respectively the small signal output and input signals) of a given circuit. An operational am-

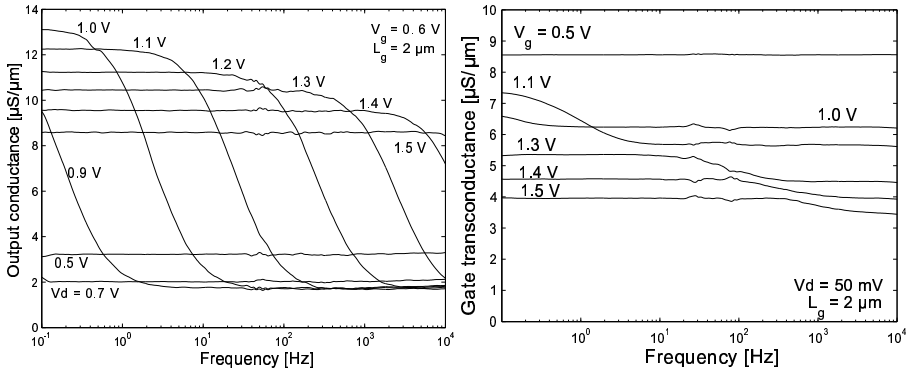


Figure 4.6: Dynamic behavior of the (a) kink effect and the (b) GIFBE in FB SOI MOSFETs as a function of frequency.

plifier (TL071CN from ST) was also used to measure the small signal g_d and g_m parameters without altering the applied bias on the drain side. The complete set up is given in Figures 4.5a and b for the AC measurements of the kink effect and the GIFBE, respectively.

The results of the AC measurements for a 2 μm-long PD SOI MOSFET are plotted as a function of frequency in Figures 4.6a and b, for, respectively, the kink effect and the GIFBE and for arbitrary bias points. The results presented in Figure 4.6a are very similar to the ones reported earlier for silicon-on-sapphire devices in [15] or FB SOI MOSFETs [16,17]. In this case the figure clearly outlines the analogy that exists between the kink effect and the GIFBE. In particular, the AC curves outline the following attributes for the two types of floating body effects:

- the increase of the small signal parameter (g_d or g_m) observed under DC conditions is characterized by a very low cut off frequency, ranging from below 1 Hz to a few kHz. More precisely, the frequency dependence of the curves is characterized by a pole (f_p)-zero (f_0) pair in that frequency range.

- in both cases both f_p and f_0 are bias dependent: they increase at higher bias values.

The results of the AC measurements are also plotted as a function of the DC bias and compared with the DC measurements in Figures 4.7a and b. In this case the DC measurements were performed in forward bias mode and using a long delay time (1 second). This figure again highlights the similarity between the dynamic behaviours of the kink effect and the GIFBE: in both cases the AC measurements performed at (very) low frequency closely agree with the DC data, thus outlining

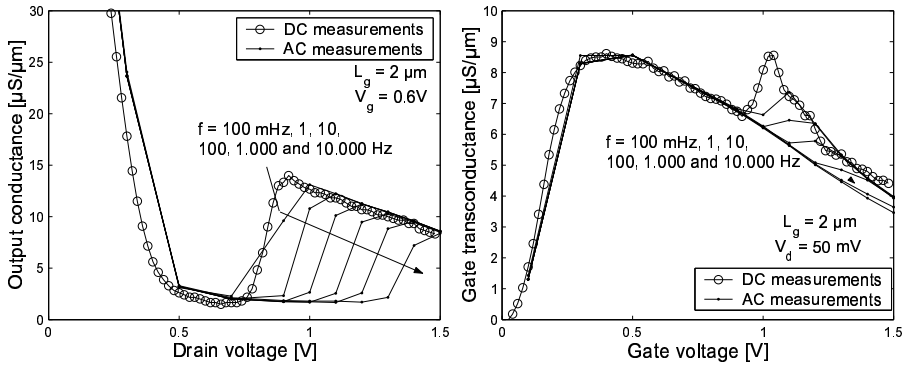


Figure 4.7: Dynamic behavior of the (a) kink effect and the (b) GIFBE in FB SOI MOSFETs as a function of applied bias.

strong FBEs. At higher frequencies the AC curves are more and more exempted from FBE and gradually tend toward a curve similar to the one that would be obtained if the device were free from floating body effects. For a clear interpretation of these results, a small signal approach is proposed in the next section.

4.4 Small signal modeling of the kink and GIFBE effects

4.4.1 Presentation of the small signal model

For MOSFET devices, the definitions of the output conductance (g_d) and of the gate transconductance (g_m) are respectively given by:

$$g_d = \left.\frac{\partial I_d}{\partial V_d}\right|_{V_g,V_b=cst} = \left.\frac{i_d}{v_d}\right|_{v_g,v_b=0} \tag{4.1}$$

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d,V_b=cst} = \left.\frac{i_d}{v_g}\right|_{v_d,v_b=0} \tag{4.2}$$

In these expressions and for the rest of this work, the following convention is used:

- entities used to designate the DC values of voltage and current at any terminal of the device start with a capital letter,
- entities represented by lower case characters refer to their small signal variations.

The small signal equivalent circuit proposed in this chapter to model the AC behaviour of common source PD MOSFET devices is displayed in Figure 4.8a. In

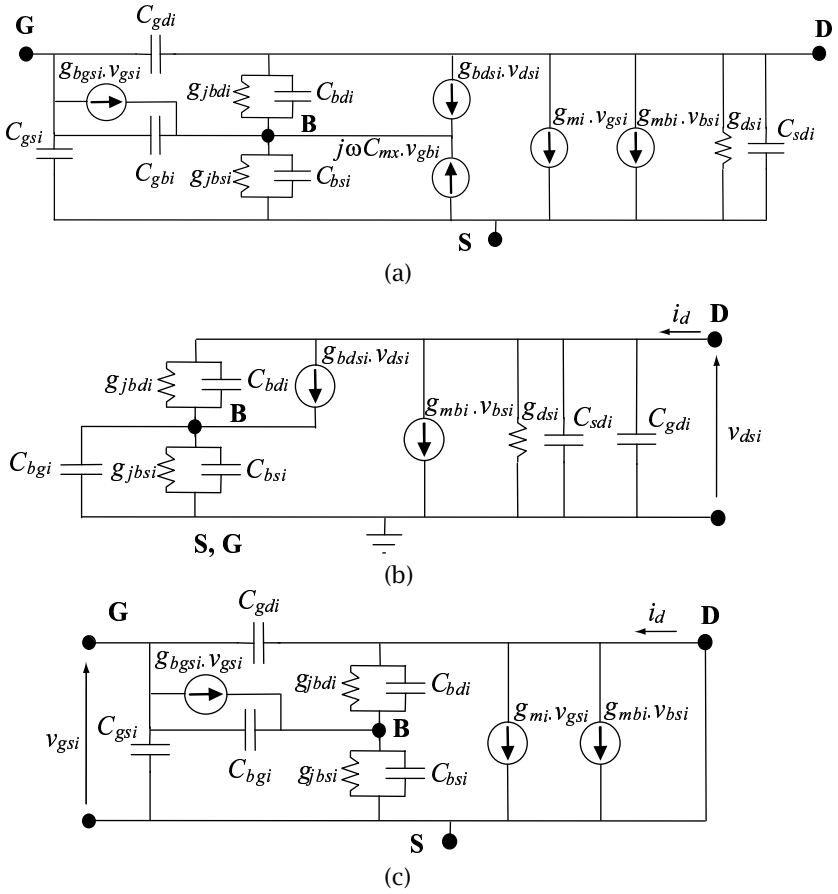


Figure 4.8: (a) Small signal model of the intrinsic part of PD SOI MOSFETs considered in this work including the body node and simplified model used for (b) g_d and (c) g_m calculations.

this analysis only the *intrinsic* elements of the device are represented and are all denoted with the subscript i. *Extrinsic* elements associated with external accesses are treated later in this chapter. The circuit is inspired from the model of the high frequency four-terminal device proposed by Y. Tsividis [18]. It considers all non-reciprocal C_{ij} capacitances:

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j}\bigg|_{V_{k\neq j}=cst} \tag{4.3}$$

with i and j being any of the four intrinsic nodes: **G**, **D**, **B**, **S**. As explained in [18], these capacitances reflect the variation of the charge at one node induced by a

small signal voltage applied to another node. They should not be associated with any physical capacitor-like structures inside the transistor. To remain consistent with the principle of charge conservation inside the device, the non-reciprocal capacitances should all be introduced in the model. Among the multiple ways to achieve this, one elegant method consists in introducing the modified transconductances [18]:

$$g_{m'} = g_{mi} + j\omega C_m \tag{4.4}$$

$$g_{mb'} = g_{mbi} + j\omega C_{mb} \tag{4.5}$$

as well as the following transcapacitances in the circuit:

$$C_m = C_{dgi} - C_{gdi} \tag{4.6}$$

$$C_{mb} = C_{dbi} - C_{bdi} \tag{4.7}$$

$$C_{mx} = C_{bgi} - C_{gbi} \tag{4.8}$$

The contributions of C_m and C_{mb} are yet usually neglected when performing RF small signal circuit modeling of PD MOSFETs [19,20] and are therefore not considered here.

For the investigation performed in this chapter the initial model of Tsividis is then completed in order to account for impact ionization, gate current and body leakage.

- The impact ionization current is modeled with a v_{dsi} (= $v_{di} - v_{si}$)-driven current source of transconductance g_{bdsi}, similarly to what is proposed in [15].

- Following the same simple approach the small signal gate current is represented by a v_{gsi} (= $v_{gi} - v_{si}$)-driven current source of transconductance g_{bgsi}. Analytical expressions for g_{bgsi} can be obtained by differentiating the $I_g(V_g)$ formulas provided in [9].

- In order to also account for the leakage of current through the body-source and body-drain junctions a body-source (g_{jbsi}) and a body-drain g_{jbdi} conductances were included in parallel with, respectively, C_{bsi} and C_{bdi}.

4.4.2 Derivation of analytical expressions for g_m and g_d

The analytical expressions of g_d and g_m can be easily computed using the small signal model presented in Figure 4.8a and by considering, respectively, the drain (Figure 4.8b) and gate (Figure 4.8c) node connected to the ground terminal. In

these two cases the equivalent circuits can be further simplified by removing the body-source transcapacitance (C_{mx}) and by replacing C_{gbi} with C_{bgi}. According to these models, the main contributors to g_d and g_m are their respective intrinsic components (g_{dsi} and g_{mi}) and an additional quantity related to the body potential fluctuations:

$$g_d = g_{dsi} + g_{mbi} Re\left[\frac{\nu_{bi}}{\nu_{di}}\right] \tag{4.9}$$

$$g_m = g_{mi} + g_{mbi} Re\left[\frac{\nu_{bi}}{\nu_{gi}}\right] \tag{4.10}$$

These expressions indicate that the frequency dependence of g_d (resp. g_m) outlined in Figure 4.6a (resp. b) can only be contained in the ν_{bi}/ν_{di} (resp. ν_{bi}/ν_{gi}) ratio. This frequency dependence is therefore related to the dynamic fluctuations of the voltage at the body node, which is connected to the "outside world" by a network of admittances ($y_{bdi} = g_{jbdi} + j.\omega C_{bdi}$, $y_{bsi} = g_{jbsi} + j.\omega C_{bsi}$ and $y_{bgi} = j.\omega C_{bgi}$) and two current sources ($g_{bgsi}\nu_{gsi}$ and $g_{bdsi}\nu_{dsi}$). Eqs. 4.9 and 4.10 can therefore be rewritten as:

$$g_d = g_{dsi} + g_{mbi} Re\left[\frac{g_{bdsi} + y_{bdi}}{y_{bsi} + y_{bgi} + y_{bdi}}\right] \cong g_{dsi} + g_{mbi} Re\left[\frac{g_{bdsi} + j\omega C_{bdi}}{g_{bbi} + j\omega C_{bbi}}\right] \tag{4.11}$$

$$g_m = g_{mi} + g_{mbi} Re\left[\frac{g_{bgsi} + y_{bgi}}{y_{bsi} + y_{bgi} + y_{bdi}}\right] = g_{mi} + g_{mbi} Re\left[\frac{g_{bgsi} + j\omega C_{bgi}}{g_{bbi} + j\omega C_{bbi}}\right] \tag{4.12}$$

where $g_{bbi} = g_{jbsi} + g_{jbdi}$ and $C_{bbi} = C_{bsi} + C_{bdi} + C_{bgi}$ respectively represent the total conductance and total capacitance between the body and the external nodes. In Eq. 4.11 it is assumed that $g_{jbdi} << g_{bdsi}$ since the body drain diode is strongly reverse biased in situations where the kink effect is observed (i.e., for saturated devices).

These expressions highlight the two main factors determining the AC body potential: small signal current injection into the body (through g_{bdsi} and g_{bgsi}) and coupling with the other nodes via an admittance network. They therefore provide a quantitative and qualitative description of the dynamic behaviours of the kink effect and the GIFBE presented in Figures 4.6 and 4.7, as detailed below.

- *Low frequency region (i.e., $f < f_p$)*: Under low frequencies, the capacitive terms can be neglected in Eqs. 4.11 and 4.12, which then simplify into:

$$g_{d,LF} \cong g_{dsi} + g_{mbi}\frac{g_{bdsi}}{g_{bbi}} \cong g_{dsi} + g_{mbi}\frac{g_{bdsi}}{g_{bsi}} \tag{4.13}$$

$$g_{m,LF} \cong g_{mi} + g_{mbi}\frac{g_{bgsi}}{g_{bbi}} \cong g_{mi} + g_{mbi}\frac{g_{bgsi}}{g_{bsi} + g_{bdi}} \tag{4.14}$$

Again, the body-drain junction conductance is neglected in Eq. 4.13 due to the reverse biasing of the body-drain diode. Under low V_d bias (which is assumed in Eq. 4.14), the values of g_{jbdi} and g_{jbsi} are expected to be of the same order of magnitude. g_{jbdi} should however rapidly decrease as the device is asymmetrically biased (positive V_d).

Expressions 4.13 and 4.14 indicate that the increase of output conductance (resp. gate transconductance) recorded at low frequencies is mainly dictated by the ratio between the impact ionization (resp. gate tunneling) transconductance and the conductance of the body-source junction. As the back gate transconductance is a reasonable fraction of the output conductance (or the back gate transconductance), the visible increases of g_d observed in the curves of Figure 4.6 imply that when impact ionization becomes significant g_{bdsi} is at least of the same order of magnitude as g_{jbsi}. For a similar reason, g_{bgsi} is at least of the same order of magnitude as g_{jbsi} when the GIFBE occurs.

· *High frequency region (i.e., $f > f_0$)*: In this case the capacitive terms in Eqs. 4.11 and 4.12 dominate and the high frequency limits of g_d and g_m become:

$$g_{d,HF} \approx g_{dsi} + g_{mbi}\frac{C_{bdi}}{C_{bbi}} \tag{4.15}$$

$$g_{m,HF} \approx g_{mi} + g_{mbi}\frac{C_{bgi}}{C_{bbi}} \approx g_{mi} \tag{4.16}$$

In both cases the AC potential of the body is therefore dictated by a capacitive divider, which provides a lower contribution to the back gate modulation than the real parts in Eqs. 4.13 and 4.14. This is because in both cases the capacitive coupling between the body node and the AC excitation node (the drain in the case of g_d and the gate in the case of g_m) is much smaller than the coupling with the ground node (at the source). Indeed,

- under strong impact ionization regime and positive body voltage we can reasonably assume that $C_{bdi} << C_{bsi}$ due to the forward biasing of the body-source junction [15];
- in linear regime at high gate bias we can consider that $C_{bgi} \cong 0$ since the front channel shields most of the electric field lines that run between the gate and the body region.

As a consequence at high frequencies the increases of output conductance or gate transconductance provided by the back gate modulation in Eqs. 4.15 and

4.16 are smaller than at low frequencies and this explains why a decrease of the AC curves are observed in both cases (Figures 4.6).

· *Pole-zero region*: According to Eqs. 4.11 and 4.12, the zero expressions for the kink effect and the GIFBE are respectively given by:

$$f_{0,kink} = \frac{1}{2\pi}\frac{\sqrt{g_{bdsi}g_{bbi}}}{\sqrt{C_{bdi}C_{bbi}}} \tag{4.17}$$

$$f_{0,GIFBE} = \frac{1}{2\pi}\frac{\sqrt{g_{bgsi}g_{bbi}}}{\sqrt{C_{bgi}C_{bbi}}} \tag{4.18}$$

while both are characterized by the same pole expression:

$$f_p = \frac{1}{2\pi}\frac{g_{bbi}}{C_{bbi}} \tag{4.19}$$

Since in both cases the transconductance associated with the floating body effects (g_{bdsi} or g_{bgsi}) is of the same order of magnitude than g_{jbsi} (and thus g_{bbi}) and the coupling capacitance (C_{bdi} or C_{bgi}) is much smaller than C_{bbi}, the comparison between the pole zero expressions indicates that $f_p < f_0$. In other words, we have:

$$\frac{f_p}{f_{0,kink}} = \sqrt{\frac{g_{bbi}C_{bdi}}{g_{bdsi}C_{bbi}}} < 1 \tag{4.20}$$

$$\frac{f_p}{f_{0,GIFBE}} = \sqrt{\frac{g_{bbi}C_{bgi}}{g_{bgsi}C_{bbi}}} < 1 \tag{4.21}$$

for floating body devices, which is consistent with the results presented in Figures 4.6.

The very low frequency of the pole observed in the figures can also be explained with Eq. 4.19: when the body-source junction is forward biased due to either impact ionization or gate tunneling current, we have $g_{jbsi} >> g_{jbdi}$ and the body conductance simply reduces to g_{jbsi}. This parameter has typical values in the $10^{-11} \sim 10^{-7}\ S/\mu m$ range for V_bi values in the 0.2-0.5 V range [10], which explains why very low cut off frequencies are reported in Figures 4.6 for both the dynamic behaviours of the kink effect and the GIFBE. Besides, as g_{jbsi} exponentially increases with V_{bi} this also explains why the pole frequency is an increasing function of the drain (resp. gate) voltage.

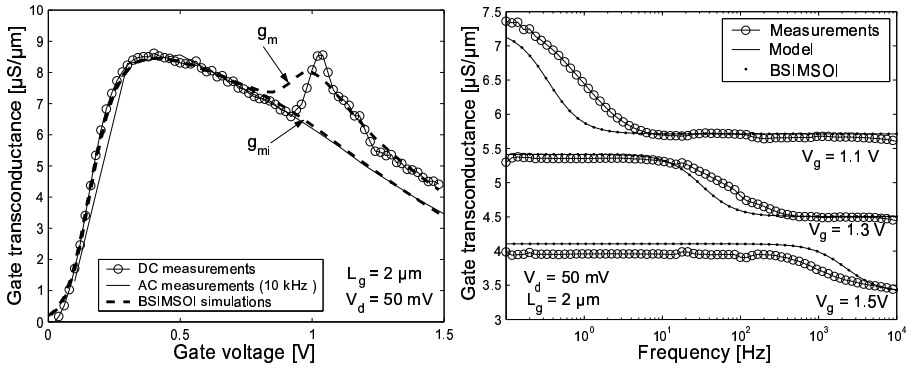


Figure 4.9: GIFBE simulations using Eldo and BSIMSOI: (a) comparison between measured and simulated DC intrinsic and extrinsic transconductance values as a function of V_g and (b) comparison between measured, simulated and modeled AC values.

4.4.3 Comparison with BSIMSOI

The validity of the proposed small signal approach was further assessed in the GIFBE case and using AC Eldo simulations with BSIMSOI [21], which is a SPICE compact model for SOI circuit design already being used in production by major semiconductor companies such as IBM and AMD. This analytical and scalable model considering the GIFBE, the mobility and gate tunneling parameters of the model were tuned to obtain a close fit between the measured and the simulated DC curves of the studied device as shown in Figure 4.9a. This figure also reports the total (g_m) and intrinsic (g_{mi}) values of the gate transconductance calculated by BSIMSOI: a very good correspondence is observed between the high frequency values of g_m (AC curve obtained at 10 kHz) and the intrinsic g_{mi}, which confirms the validity of Eq. 4.16.

In Figure 4.9b the simulated data are plotted as a function of frequency. The AC measurements are also reported in the figure for reference. The elements of the small signal circuit were obtained in this case from the values of the intrinsic node parameters provided by the DC BSIMSOI simulations. An excellent correspondence is observed here between the measured and simulated data, confirming that the small signal model given in Figure 4.8 correctly predicts the AC behavior of the gate transconductance in PD FB SOI devices. More importantly, this also validates the interpretation of the GIFBE dynamic behaviour provided in the previous section. It is anticipated that our description of the dynamic behaviour of the kink effect is also correct, on the basis of previous similar work [15].

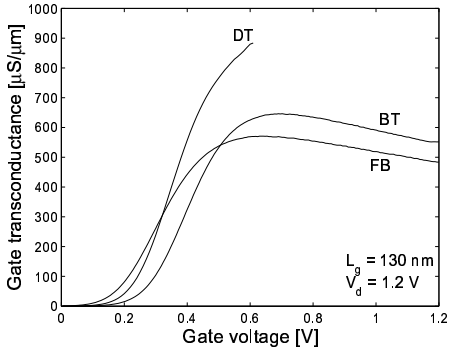


Figure 4.10: Extrinsic transconductance measured on a FB, BT and DT MOSFETs from a 0.130 nm technology, outlining the substantial increase of g_m when the body is connected to the gate (DT MOSFET).

4.5 Body-contacted devices

As inferred in a previous section, floating body effects are traditionally avoided in PD SOI technology by connecting the body to an external node. In both body-tied devices and dynamic threshold MOSFETs the DC body potential is controlled by an external access, which prevents V_{bi} increases related to either impact ionization or gate current. As illustrated in Figures 4.2 and 4.3 for body-tied devices this also suppresses the kink effect and the GIFBE. As a result, the DC values of g_d in body-contacted MOSFETs and under high V_d bias are lower than for their floating body counterparts. In linear regime, the gate transconductance of body-contacted MOSFETs is also lower under high gate voltage (where GIFBE is typically observed). In the case of DT MOSFETs, higher values of g_m are however expected compared to FB or BT MOSFETs since both the front and back gate contribute to the device transconductance (i.e., $g_m = g_{mi} + g_{mbi}$). This is shown in Figure 4.10 on 0.130 μm devices.

The AC behaviour of g_d and g_m for body-contacted devices are investigated in the following sections.

4.5.1 Output conductance of body-contacted PD SOI MOSFETs

In this paragraph, 0.18 μm-long devices were measured with a low frequency (10 kHz-4 GHz) Vector Network Analyzer from Rhode & Schwartz (ZVR) under varying biasing conditions. For each measurement the Y parameters were de-embedded from the raw parameters using a classical open subtraction method [22].

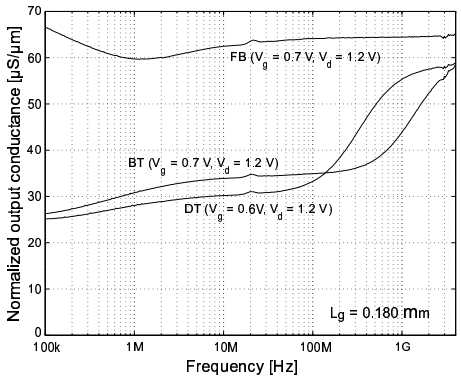


Figure 4.11: Output conductance measured on body-contacted (BT and DT MOSFETS) and FB devices from a 0.18 μm technology.

The extrinsic output conductance was then computed from the Y parameters according to [19]:

$$g_d = Re(Y_{22}) \tag{4.22}$$

The output conductances of the measured BT and DT devices are presented in Figure 4.11 as a function of frequency. The measurements recorded on a FB device from the same technology are also included for comparison.

At low frequencies, Figure 4.11 highlights the significant improvement obtained on g_d by connecting the body to the source or the gate, since both the DT and BT structures exhibit a value of g_d more than two times lower than for the FB device. However, the measurements also show that this positive effect is lost at higher frequencies, since both DT and BT devices suffer from a 150 % g_d degradation between the low frequency and high frequency ($\sim$ 4 GHz) levels.

This clearly defined increase of output conductance observed in the case of body-contacted devices can simply be explained by considering a similar equivalent circuit as the one proposed in Figure 4.8a in which an additional resistance (R_{be}) is connected to the body node. It is obvious that this resistance is placed in parallel with C_{bdi} and g_{bgsi} in the case of DT MOSFETs and with y_{bsi} in the case of body-tied devices. The resulting small signal equivalent circuit used for g_d calculation is presented in Figure 4.12. It can be seen that R_{be} shorts all body-to-ground impedances at low frequencies. It is also worth noticing that the circuit is identical for both DT and BT devices since the output conductance is defined by grounding all terminals except the drain. This already explains why similar AC g_d behaviours are observed for the DT and and the BT MOSFETs in Figure 4.11.

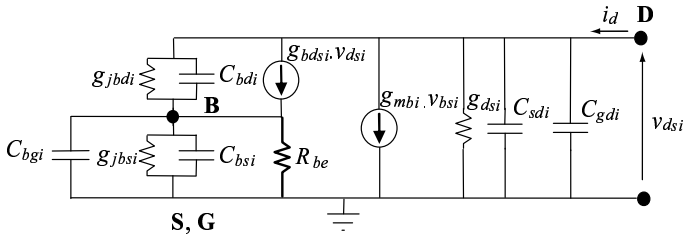


Figure 4.12: Equivalent circuit of a body-contacted PD SOI MOSFET seen from the drain terminal and used for g_d calculation. This circuit can be used both for DT (body node connected to the gate) and BT (body node connected to the source) MOSFETs.

In both cases the g_d expressions developed above (Eqs. 4.11, 4.13 and 4.15) can be rewritten as:

$$g_d = g_{dsi} + g_{mbi} Re\left[\frac{g_{bdsi} + j\omega C_{bdi}}{R_{be}^{-1} + j\omega C_{bbi}}\right] \tag{4.23}$$

$$g_{d,LF} \approx g_{dsi} + g_{mbi}\frac{g_{bdsi}}{R_{be}^{-1}} \approx g_{dsi} \tag{4.24}$$

$$g_{d,HF} \approx g_{dsi} + g_{mbi}\frac{C_{bdi}}{C_{bbi}} \approx g_{dsi} + g_{mbi}\frac{C_{bdi}}{C_{bsi}} \tag{4.25}$$

It is seen in these expressions that at low frequencies the device output conductance is roughly equal to the intrinsic conductance of the channel since the body resistance is several orders of magnitude lower than g_{bdsi}. In this case the body region becomes a cold node, which prevents the impact ionization current to have any effect on the body potential. At higher frequencies however, the non zero value of the body resistance induces a zero-pole pair in the g_d curves. This pair is similar to what occurs in FB devices, except that in this case the zero is observed at a lower frequency than the pole. This is attributed to the much higher value of the body-to-ground conductance in the case of body-contacted devices (R_{be}^{-1}) than in the case of FB MOSFETs ($g_{jbsi} + g_{jbdi}$). Indeed, for DT and BT devices the zero and the pole expressions are:

$$f_0 \approx \frac{1}{2\pi}\frac{\sqrt{g_{bdsi}R_{be}^{-1}}}{\sqrt{C_{bdi}C_{bbi}}} \tag{4.26}$$

$$f_p \approx \frac{1}{2\pi}\frac{R_b^{-1}}{C_{bbi}} \tag{4.27}$$

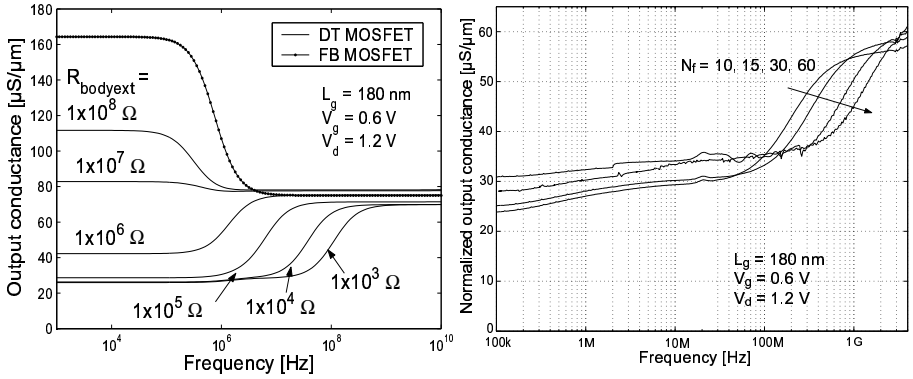


Figure 4.13: Effect of R_{be} on the AC behaviour of g_d in the case of a DT MOSFETs: (a) Eldo simulations performed by varying the resistance of the external body connection ($R_{bodyext}$), (b) Experimental results on devices with a varying number of gate fingers and a constant width of 60 μm.

and Eq. 4.20 becomes :

$$\frac{f_p}{f_{0,kink}} \approx \sqrt{\frac{R_{be}^{-1} C_{bdi}}{g_{bdsi} C_{bbi}}} > 1 \tag{4.28}$$

due to the high value of R_b^{-1}.

At higher frequencies ($f > f_p$), Eq. 4.25 indicates that the body potential is determined by the same capacitive divider as in the case of floating body devices (Eq. 4.15). The high frequency g_d values of DT and BT devices then become similar to those found for the FB MOSFETs, despite their different DC body bias, as observed in Figure 4.11. This is also shown by Eldo simulations presented in Figure 4.13a, which outline the gradual transition of the g_d curves when the body resistance is reduced:

- at very high R_{be} values, the simulated DT device behaves closely like a FB MOSFET with $g_{d,LF} > g_{d,HF}$ and $f_p < f_0$,
- as R_b decreases the device starts behaving like the measured DT or BT MOSFET with $g_{d,LF} < g_{d,HF}$ and $f_0 < f_p$.

For these simulations an external body resistance was added to connect the body node to the gate. It is also seen in the figure that as the body resistance is further reduced the zero-pole pair is rejected to higher frequencies, which is beneficial for the use of body-connected devices in RF applications. This is illustrated in Figure 4.13b in which a reduction of R_{be} was obtained by increasing the number

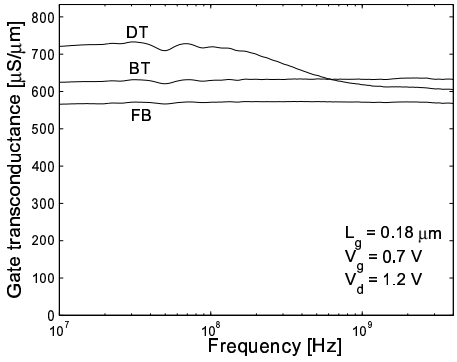


Figure 4.14: Measured g_m as a function of frequency on a FB, DT and BT devices.

of parallel gate fingers of the RF device while keeping a fixed total device width of 60 μm.

4.5.2 Gate transconductance of body-contacted PD SOI MOSFETs

Following the same approach as in the previous paragraph, the extrinsic gate transconductance of the investigated body-contacted devices was computed from the Y parameters:

$$g_m = Re(Y_{21}) \tag{4.29}$$

The measured data are plotted in Figure 4.14 for a FB, a BT and a DT MOSFET. It is seen that only the DT MOSFET device exhibits a strong reduction of g_m above a certain frequency limit.

Once more, these observations can be interpreted by considering a small signal circuit of the devices that includes the body resistor: R_{be} is either connected to the gate (Figure 4.15a) or the ground (Figure 4.15b), for respectively, DT and BT MOSFETs. According to those models the gate transconductances of a DT MOSFFET and a BT MOSFET in saturated regime are respectively given by:

$$g_{m,DT} = g_{mi} + g_{mbi} Re\left[\frac{g_{bgsi} + R_{be}^{-1} + j\omega C_{gbi}}{R_{be}^{-1} + j\omega C_{bbi}}\right] \tag{4.30}$$

$$g_{m,BC} = g_{mi} + g_{mbi} Re\left[\frac{g_{bgsi} + j\omega C_{gbi}}{R_{be}^{-1} + j\omega C_{bbi}}\right] \tag{4.31}$$

in which, again, it is assumed that R_{be}^{-1} is several orders of magnitude than g_{jbsi}, g_{jbdi} and g_{bgsi}. These expressions show that at low frequencies we have $g_{m,LF} \approx$

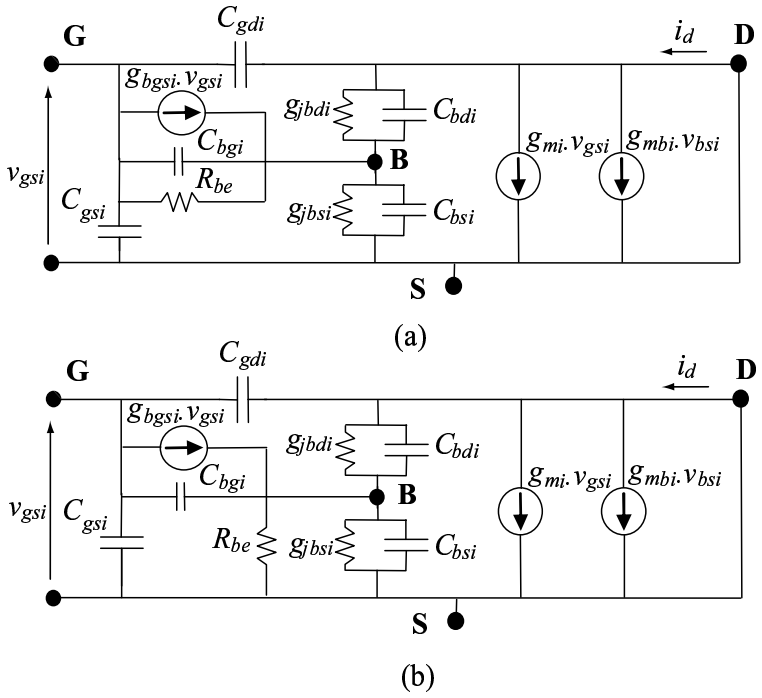


Figure 4.15: Equivalent circuit of the (a) DT and (b) BT MOSFETs used for g_m calculation.

$g_{mi} + g_{mbi}$ for the DT device and $g_{m,LF} \approx g_{mi}$ for the BT device. In both cases the high frequency expression is determined by the same body capacitance network as for FB or BT :

$$g_{m,HF} \approx g_{mi} + g_{mbi}\frac{C_{gbi}}{C_{bbi}} \approx g_{mi} + g_{mbi}\frac{C_{gbi}}{C_{bbi}} \tag{4.32}$$

These observations imply that as C_{gbi} is much smaller than C_{bbi}, the high frequency value of g_m becomes close to g_{mi} for all DT, BT and FB devices. In the case of DT MOSFETs, a noticeable reduction of g_m is then observed at higher frequencies as illustrated in Figure 4.14 [23]. This can also be interpreted as a loss of control from the back gate on the front channel. In the case of BT devices, the LF and HF limits are roughly equal, which translates into a relatively flat frequency behaviour.

Table 4.1: Low and high frequency expressions for g_m and g_d considering floating body or body resistance effects in FB, BT and DT MOSFETs.

	FB	**BT**	**DT**
$g_{m,LF}$	$g_{mi} + g_{mbi}\frac{g_{bgsi}}{g_{jbsi}+g_{jbdi}}$	g_{mi}	$g_{mi} + g_{mbi}$
$g_{m,HF}$	$g_{mi} + g_{mbi}\frac{C_{gbi}}{C_{bbi}}$		
$g_{d,LF}$	$g_{dsi} + g_{mbi}\frac{g_{bdsi}}{g_{jbsi}}$	g_{dsi}	g_{dsi}
$g_{d,HF}$	$g_{dsi} + g_{mbi}\frac{C_{bdi}}{C_{bbi}} \approx g_{dsi} + g_{mbi}\frac{C_{bdi}}{C_{bsi}}$		

4.5.3 Summary

The expressions developed above indicate that both LF and HF values of the two most important IC analogue device figures of merit (g_m and g_d) are a strong function of body-related parameters, such as the back gate transconductance and the body capacitances. An accurate modeling of those parameters is then crucial to correctly predict the AC behavior of advanced PD SOI MOSFETs. As valid models can only be obtained by confronting them with real life measurements, this means that experimental characterizations of the body region are vital for the assessment of PD SOI MOSFETs models such as BSIMSOI. The next part of this chapter describes how a deep characterization of the body node can be performed by using multiport RF measurements.

4.6 Body characterization by multiport S-parameter measurements

4.6.1 Geometry of the investigated structures

This section demonstrates the possibility of characterizing the body node of PD SOI MOSFETs under dynamic conditions by multiport S-parameter measurements. This characterization method requires a multiport Vector Network Analyzer (VNA), a piece of equipment that has now been commercially available by all major VNA providers. Classically, a multiport VNA has four RF ports and enables to measure the S-parameters between each pair of ports. According to the number of ports used, the measured S-parameters can therefore be presented under 2x2 (as in classical 2-port S parameter measurements), 3x3 or 4x4 scattering matrices.

In the context of PD SOI device characterization the advantages provided by multiport measurements can be exploited by connecting (at least) one of the RF ports to the body of the device. This of course implies properly designing the device layout: providing a body contact and a connection to an additional RF probing

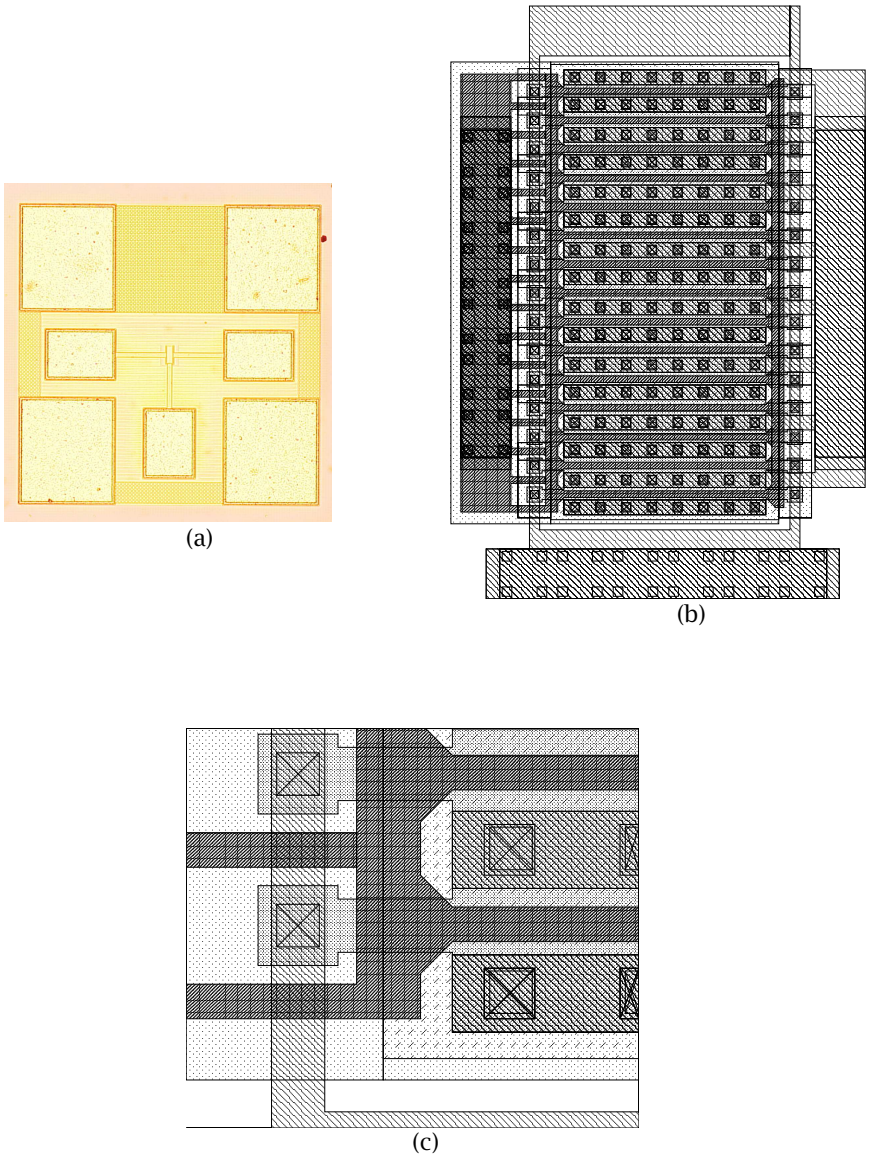


Figure 4.16: (a) Top view of a 3-port PD SOI MOSFET embedded in its RF pads, (b) core view of the device (15 fingers of 4 μm each) and its external connections, (c) zoom on body contacts at left edge of the polysilicon fingers.

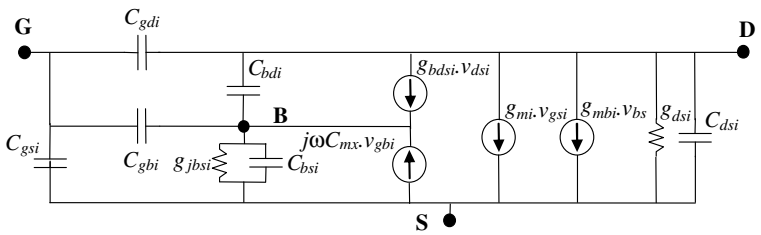


Figure 4.17: Intrinsic part of a 3-port PD SOI MOSFET in saturation.

pad. In H-like gate architecture, body contacts are traditionally provided at both ends of the polysilicon fingers. When these two body contacts are connected together a 3-port RF device is formed and the body can be measured independently from the gate and drain accesses (Figure 4.16a). If, on the contrary, the body contacts are each connected to a different probing pad, a 4-port RF device is formed and both accesses of the body region can be independently measured. The results of 3-port characterization on 0.13 μm-long devices are presented in the next sections .

For this purpose, a complete small signal model for the measured 3-port devices including extrinsic elements is first presented. This model is then used to characterize the intrinsic and extrinsic part of the devices and to illustrate the possibility of modeling the AC behaviour of the measured 3-port under any given bias condition. The bias point selected in this work is that of a saturated 0.13 μm DT MOSFET at its nominal drain voltage, i.e. $V_g = V_b = 0.6$ V and $V_d = 1.2$ V.

4.6.2 Small signal circuit description

Intrinsic elements. According to the circuit presented in Figure 4.8, the intrinsic part of a body-contacted PD SOI MOSFET measured in *saturation* can be described with the simplified model of Figure 4.17. In this last circuit it is assumed that V_d is high enough to create impact ionization at the drain side and V_g is too small to produce significant gate tunneling current. The gate tunneling transconductance (g_{bgsi}) is then removed from the circuit. In addition, the body-drain junction conductance (g_{jbdi}) is assumed to be negligible due to the reverse-biasing of the body-drain junction and is therefore not considered either.

In such conditions, the Y matrix of the given three-port network (YY_i) is simply:

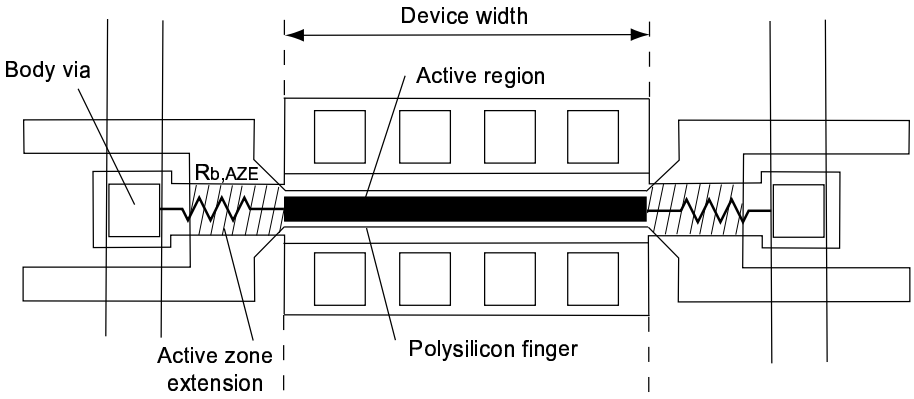


Figure 4.18: One finger-schematic view of a BC PD SOI MOSFET, defining the physical locations of the device intrinsic region as well as the active zone extensions at both edges of the polysilicon finger.

$$YY_i = \begin{bmatrix} j\omega(C_{gsi}+C_{gdi}+C_{gbi}) & -j\omega C_{gdi} & -j\omega C_{gbi} \\ g_{mi}-j\omega C_{gdi} & g_{dsi}+j\omega(C_{sdi}+C_{bdi}+C_{gdi}) & g_{mbi}-j\omega C_{bdi} \\ -j\omega(2C_{gbi}-C_{bgi}) & -g_{bdsi}-j\omega C_{bdi} & g_{jbsi}+j\omega(C_{bsi}+C_{bdi}+2C_{gbi}-C_{bgi}) \end{bmatrix} \tag{4.33}$$

Extrinsic elements. For a quantitative RF characterization of the intrinsic part of the devices, it is crucial to consider the parasitic elements in the small signal equivalent circuit. The *parasitic* elements are defined here as being all electrically active parts of the device structure that affect the signals before they reach the active region of the device, while the *active region* consists in all the portions of channel-doped silicon located below the polysilicon fingers and limited by the specified (or drawn) device width. This is illustrated in Figure 4.18. For the investigated BC PD MOSFETs, the following assumptions are made:

- All parasitics are due to *resistive* effects and *capacitive* coupling. In other words, inductances associated with access lines are considered to be negligible in the investigated frequency range.
- The resistive effects inside metallic lines are negligible compared to the ones produced inside the silicon region (for the source, drain and body accesses) or the polysilicon fingers (for the gate access).
- All capacitors (intrinsic and extrinsic) in the structure are assumed to be either *directly proportional* to the drawn gate width (W_f) or *independent* on W_f.

Based on these assumptions and the geometry of the investigate structures, the identified parasitics (Figure 4.19) can be classified as follows:

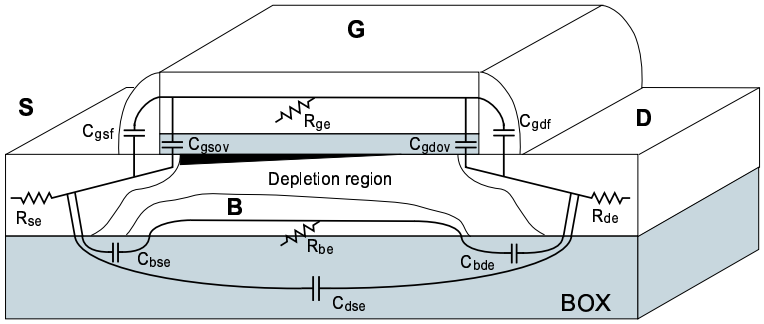


Figure 4.19: Parasitic fringing capacitors around and below the channel in BC PD SOI MOSFETs. The parasitic resistances are also illustrated.

- *extrinsic capacitors.* These capacitors directly scale with the device width and are associated with fringing fields both *above* ($C_{gse} = C_{gsf} + C_{gsov}$, $C_{gde} = C_{gdf} + C_{gdov}$) and *below* ($C_{dse}$, C_{bde} and C_{bse}) the channel, as illustrated in Figure 4.19. These parasitics shunt the intrinsic capacitors in the equivalent circuit and are therefore not dissociated here from the intrinsic capacitors.

- *extrinsic resistors.* As shown in Figure 4.19 the source (R_{se}) and drain (R_{de}) extrinsic resistors are associated with the diffusion regions. The gate (R_{ge}) and body (R_{be}) resistors are associated, respectively, with the polysilicon fingers and the silicon region located *below* the active region.

- *AZE capacitors.* These capacitors are associated with the lateral extensions of the active zone (AZE) below the polysilicon fingers (Figure 4.18) which are required to access the body region. They are bias dependent and W_f independent. In general, they contribute to an additional body-source ($C_{bs,AZE}$), body-drain ($C_{bd,AZE}$), body-gate ($C_{bg,AZE}$), gate-source ($C_{gs,AZE}$) and/or gate-drain ($C_{bg,AZE}$) coupling, which is shown in the following paragraphs.

- *access capacitors.* These capacitors represent the coupling between *metallic lines* at both edges of the polysilicon fingers. They are assumed to be independent on the device width and are denoted using the subscript a. (Ex.: C_{bda}).

- *extrinsic-extrinsic capacitors.* Similarly as in [20, 24], these capacitors (C_{xyee}) represent the capacitive coupling between *metallic lines above* the silicon region and the polysilicon fingers. Depending on the structure, some extrinsic-extrinsic coupling also occurs at the external sides of the two external fingers. In all cases, the C_{xyee} capacitors directly scale with W_f and shunt the access capacitances.

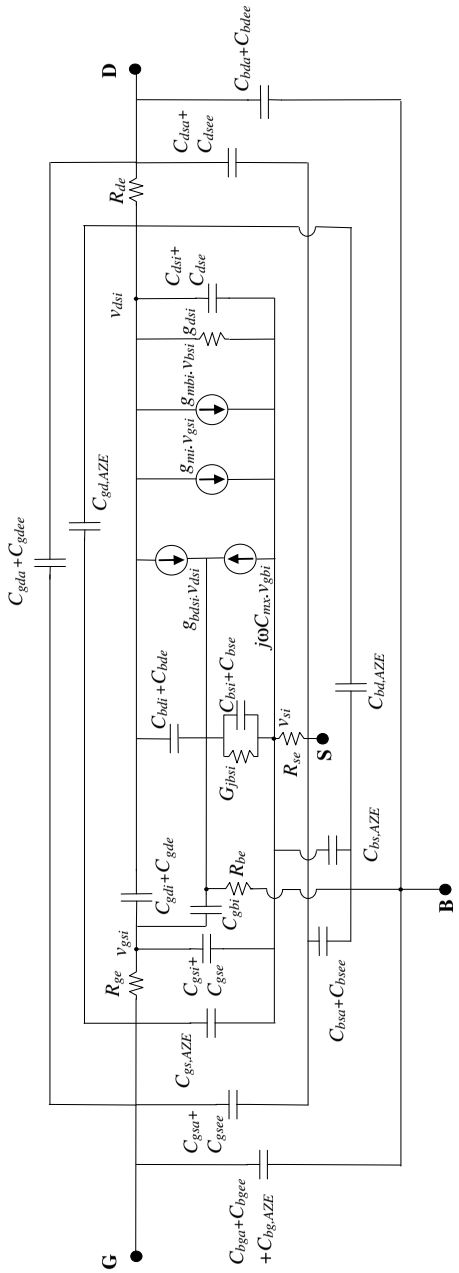


Figure 4.20: Equivalent circuit of the 3-port RF device presented in Figure 4.16 in saturation and including extrinsic elements associated with the external connections.

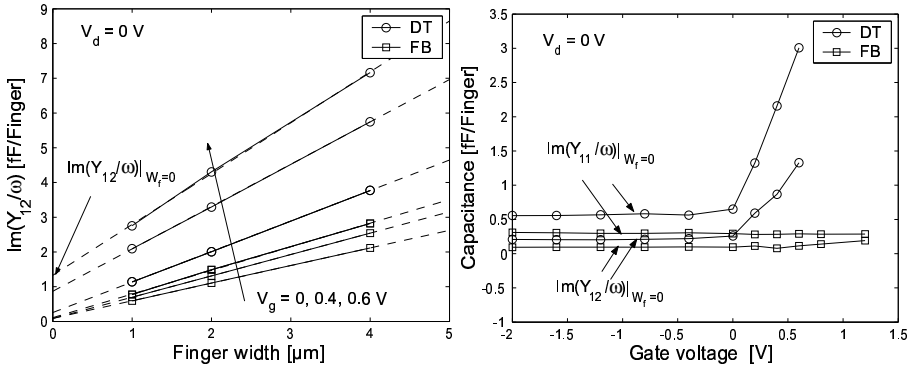


Figure 4.21: (a) Measured input capacitance ($Im(Y_{11})/\omega$) as a function of the finger width for DT MOSFETs and FB MOSFETs on the investigated technology. (b) Extrapolated values of $Im(Y_{11})/\omega$ and $Im(Y_{12})/\omega$ at $W_f = 0$ as a function of V_g for the DT and FB MOSFETS.

The complete equivalent circuit considered in this work and including all intrinsic and extrinsic elements is presented in Figure 4.20. It can be seen that this circuit is quite complex due to the high number of elements present in the model. However, the idea developed in the coming sections is not to extract all those elements from the measured S-parameters. It is simply to focus on the body-related parameters only, and to illustrate the easiness with which those parameters can be extracted using 3-port S-parameter measurements.

4.6.3 Importance of the AZEs in body-contacted devices

In body-contacted PD SOI MOSFETs, AZEs play an important role on the electrical behaviour of the devices. Being located directly beneath the gate stack and electrically connected to the channel, these regions behave as parasitic transistors at both ends of the polysilicon fingers and therefore actively contribute to the device operation. This has already been experimentally observed in [25].

The impact of the AZEs is mostly noticeable on the behaviour of the device capacitances. This is illustrated in Figures 4.21a and b. Linear regressions of the $Im(Y_{12})/\omega$ parameters obtained on DT and FB devices with distinct finger widths and several V_g values are presented in Figure 4.21a. This type of regression is classically used to extract the device parasitic gate-to-drain access capacitances (C_{gda}) at $W_f = 0$, as explained in [19, 20]: the devices are traditionally biased in deep depletion (in which case the equivalent circuit largely simplifies) and are assumed to show no dependence on the applied bias. The measurements performed on

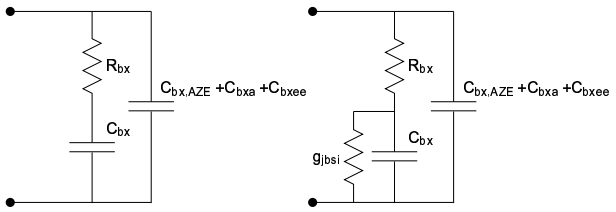


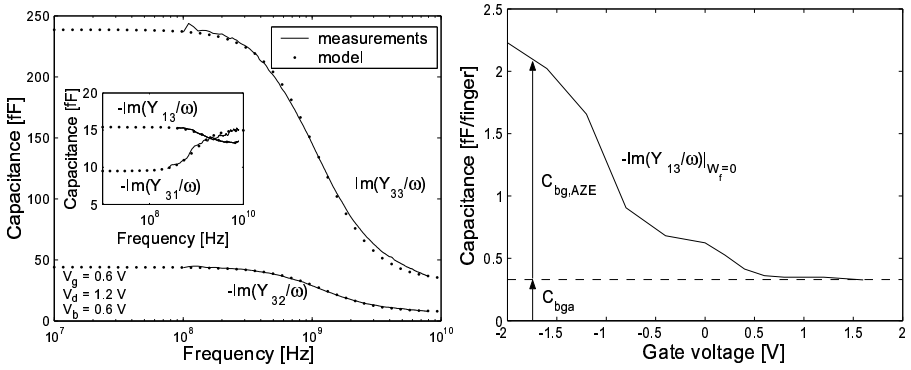
Figure 4.22: Small signal equivalent circuit used to model (a) the measured $Im(Y_{13})$, $Im(Y_{32})$, $Im(Y_{33})$ and (b) the measured $Re(Y_{33})$ parameters. These simplified circuits were obtained from the one presented in Figure 4.20.

the FB devices confirm this expectation, as demonstrated in Figure 4.21b, which also outlines no V_g dependence for the extrapolated value of the *input* capacitance ($Im(Y_{11})/\omega$) on the FB devices. On the contrary, the two figures outline a large V_g dependence for the extrapolated values of both $Im(Y_{11}/\omega)$ and $Im(Y_{12}/\omega)$ and for V_g values higher than V_t. This bias dependence can be directly attributed to the AZEs in the DT (or, more generally in body-connected PD SOI) devices: for values lower than V_t the silicon surface below the AZEs is depleted and this intrinsic part of the AZEs does not contribute to any increase of the gate-to-source or gate-to-drain capacitance. For values higher than V_t an inversion layer is formed at the silicon surface everywhere below the gate stack. In this case, the silicon surface below the AZE becomes electrically connected via the channel with both (under linear regime) the source and drain diffusion regions and a substantial increase of the gate-to-drain (in $Im(Y_{12}/\omega)|_{W_f=0}$) and gate-to-source (in $Im(Y_{11}/\omega)|_{W_f=0}$) coupling is observed.

The bias-dependent characteristics of those parasitics should be clearly kept in mind when characterizing any type of BC (BT, DT or three-port BC MOSFETs) devices. Ignoring this effect can lead, for instance, to severe underestimations of the device input capacitance when biased in saturation and thus, to strong discrepancies between measured and simulated circuit or device performance.

4.6.4 Extraction of the body capacitances

Using small signal simulations of the circuit presented in Figure 4.20, it is possible to show that a good approximation for the $-Im(Y_{13})$, $-Im(Y_{32})$, $-Im(Y_{31})$ and $Im(Y_{33})$ parameters can be obtained by considering the admittance of the circuit presented in Figure 4.22a, in which the intrinsic capacitance is put in series with the body resistance, both being shunted by the extrinsic capacitances. In the first two cases ($-Im(Y_{13})$ and $-Im(Y_{32})$), the subscript x for the elements of the figure



(a) (b)

Figure 4.23: (a) Imaginary parts of $-Y_{13}$, $-Y_{31}$, $-Y_{32}$ and $-Y_{33}$ as a function of frequency, which are shown to closely match the simple RC network presented in Figure 4.22a, (b) $-Im(Y_{13})|_{W_f=0}$ as a function of V_g.

can be replaced by g and d respectively. This also holds for the third parameter ($-Im(Y_{31})$), with the exception in this case that the intrinsic capacitance (C_{bx}) is given by $2C_{gbi} - C_{bgi}$ (Eq. 4.33). For the last parameter ($Im(Y_{33})$), the capacitances must be replaced by the sum of all capacitances seen from the body to the external nodes (i.e., $C_{bx,AZE} = C_{bg,AZE} + C_{bs,AZE} + C_{bd,AZE}$) while keeping for the "intrinsic" part: $C_{bx} = C_{bdi} + C_{bsi} + 2C_{gbi} - C_{bgi}$ (Eq. 4.33).

As illustrated in Figure 4.23a this simple 2-port model adequately fits the measured values. It is therefore considered in the following lines as the base tool for the extraction of the body capacitances. Indeed, the low frequency input capacitance value for the 2-port network given in Figure 4.22a is equal to the sum of all capacitances in the circuit:

$$C_{LF} = \boldsymbol{C_{bx}} + C_{bx,AZE} + C_{bxa} + \boldsymbol{C_{bxee}} \tag{4.34}$$

while the high frequency value is simply the sum of all parasitic capacitances:

$$C_{HF} = C_{bxa} + C_{bx,AZE} + \boldsymbol{C_{bxee}} \tag{4.35}$$

In these expressions bold parameters highlight the width-dependent capacitances. These terms can be removed by extrapolating the expressions at $W_f = 0$:

$$C_{LF}|_{W_f=0} = C_{HF}|_{W_f=0} = C_{bxa} + C_{bx,AZE} \tag{4.36}$$

It results from the above equations that the values of C_{bxee} and C_{bx} can easily be

extracted from the measured data according to:

$$C_{bxee} = C_{HF} - C_{LF}|_{W_f=0} \tag{4.37}$$

$$C_{bx} = C_{LF} - C_{LF}|_{Wf=0} - C_{bxee} \tag{4.38}$$

$$\tag{4.39}$$

while only the sum of C_{bxa} and $C_{bx,AZE}$ can be obtained from 4.36. From a small signal modeling perspective, this can be a problem since both C_{bxa} and $C_{bx,AZE}$ are separated elements in the circuit of Figure 4.20. There is however one particular case where C_{bxa} can be dissociated from $C_{bx,AZE}$, which is when the devices are measured in strong inversion. In this case, the inversion layer formed in the AZEs completely screens the body from the field lines that emanate from the gate polysilicon and we therefore have $C_{bg,AZE} = 0$. The low frequency value of $-Im(Y_{13}/\omega)|_{W_f=0}$ is then simply C_{bga}. The gate bias dependence of this parameter is illustrated in Figure 4.23b. In the cases of the body-source and body-drain capacitances, the small signal circuit can be approximated by placing the $C_{bsa,AZE}$ and $C_{bda,AZE}$ terms in parallel with, respectively, C_{bsa} and C_{bda}. This approximation can be performed when R_s and R_d are small compared to the other resistive terms (R_{ge} and R_{be}) in the circuit. In this case, only the sums of C_{bxa} and $C_{bx,AZE}$ (for $x = s$ and $x = d$) are required for a complete small signal description of the device AC behaviour.

The extracted values of the body capacitances are summarized in Table 4.2. Extrinsic extrinsic elements were found to be negligible on the studied devices.

Table 4.2: Extracted body capacitances on the measured 3-port devices in saturation ($V_g = V_b = 0.6$ V, $V_d = 1.2$ V).

C_{bd} [fF/μm]	C_{bs} [fF/μm]	C_{bgi} [fF/μm]	C_{gbi} [fF/μm]
0.32	1.62	0.08	0.02
$C_{bda}+C_{bd,AZE}$ [fF/finger]	$C_{bsa}+C_{bs,AZE}$ [fF/finger]	C_{bga} [fF/finger]	$C_{bg,AZE}$ [fF/finger]
0.24	0.55	0.35	0.10
C_{bdee} [fF/μm]	C_{bsee} [fF/μm]	C_{bgee} [fF/μm]	
≈0	≈0	≈0	

4.6.5 Extraction of the body resistance

The value of the body resistance can easily be extracted by considering the two-port network of Figure 4.22a. When this circuit is used to model the $Im(Y_{33})$

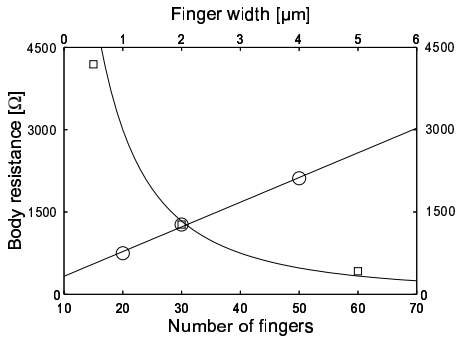


Figure 4.24: Extracted value of R_{be} as a function of device width (W_f) and number of fingers (N_f).

parameters, the R_{bx} resistor is indeed directly associated with the body access resistance R_{be}:

$$R_{bx} \approx 1/3 R_{be} \tag{4.40}$$

In this expression, the $1/3$ factor accounts for the distributed nature of the RC network associated with the body region. This factor is also traditionally considered to model the gate resistance in RF devices [26].

Figure 4.24 shows the value of R_{be} obtained for devices with a varying finger width (W_f) and for devices with a varying number of fingers N_f (keeping a constant $N_f.W_f$ product). It is seen that R_{be} (1) displays a linear dependence with respect to W_f and (2) closely decreases as $(1/N_f)^2$. This behaviour is very similar to that of the gate resistance, which further supports the validity of the extraction method.

The extrapolated value of R_{be} obtained for $W_f = 0$ ($\simeq 150\,\Omega$) also provides a good estimation of the parasitic resistance associated with the body interconnects in the AZE ($R_{b,AZE}$). The figure shows that its contribution is not negligible with regards to the overall value of R_{be}. Indeed normalized values of R_{be} and $R_{b,AZE}$ were found to be respectively close to 63 k$\Omega/\mu m.finger$ and 7.75 $k\Omega/finger/contact$.

4.6.6 Extraction of the body source junction conductance

The extraction of the body-source junction conductance (g_{jbsi}) can be directly achieved by considering the real part of Y_{33}. Indeed, the 2-port network seen from the body node can be improved by including g_{jbsi} (Figure 4.22b). The admittance of this circuit is characterized by a pole-zero pair and the low and high frequency values of $Re(Y_{33})$ are respectively given by:

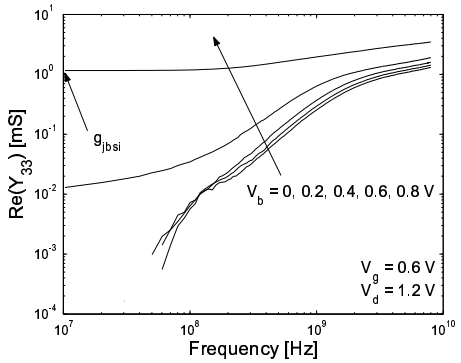


Figure 4.25: $Re(Y_{33})$ measured as a function of the frequency for different body bias values.

$$Re(Y_{33})|_{LF} = \frac{1}{R_{be} + \frac{1}{g_{jbsi}}} \tag{4.41}$$

$$Re(Y_{33})|_{HF} = \frac{1}{R_{be}} \tag{4.42}$$

Thus, for low body bias values we have $R_{be} << 1/g_{jbsi}$ and $Re(Y_{33}) \simeq g_{jbsi}$.

The experimental data obtained on the investigated device are plotted in Figure 4.25. In this figure, $Re(Y_{33})$ was plotted as a function of frequency for several body bias values. The zero-pole created by the body resistance is clearly outlined. It is also observed that the LF value of this parameter is an increasing function of V_b since the junction becomes forward biased at higher body voltages. The figure also indicates that the extraction of g_{jbsi} for values below 1 μS seems to be jeopardized by the accuracy of the measurement set-up. For V_b=0.6 V, the body junction conductance tends to a value on the order of 10 μS. Note in this case that due to the forward biasing of the body junctions and the distribution of these junctions along the device width, the body potential is expected to vary along the device width. In this case the extracted value of g_{jbsi} is only an indication of the "average" conductance seen from the body to the source via the junctions and may not be extrapolated for other device widths.

The reader might also have noticed that according to the above expressions the high frequency value of $Re(Y_{33})$ should, in theory, directly yield the value of R_{be}. However, it can be seen in Figure 4.25 that this parameter does not tend to a clearly distinct plateau level, which might be related to second order effects that were not considered in the model or related to the accuracy limitation of the

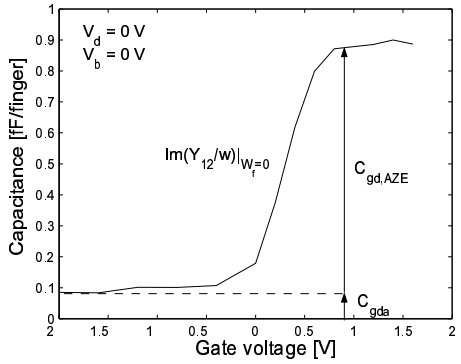


Figure 4.26: Imaginary part of Y_{12}/ω extrapolated at $W_f = 0$ as a function of the gate bias.

open-deembedding procedure. Attempting to extract R_{be} using this method might therefore lead to inaccurate results.

4.6.7 Comparison between modeled and measured data

The extraction of the gate-source, gate-drain and drain-source capacitances of the circuit could theoretically be accomplished according to the methods described in [20]. This exhaustive work details how it is possible to dissociate the intrinsic from the extrinsic, extrinsic-extrinsic and access capacitances. In our work a simpler approach was used: the extrinsic extrinsic capacitances were neglected as they were found negligible in the body connections. The sum of the access and AZE capacitances could then directly be extracted using a linear extrapolation at $W_f = 0$. As in the case of the body-gate capacitance, the $C_{gs,AZE}$ and $C_{gd,AZE}$ terms could be dissociated from, respectively, C_{gsa} and C_{gda} by applying a specific bias on the gate. For instance, the V_g dependence of $Im(Y_{12}/\omega)|_{W_f=0}$ is illustrated in Figure 4.26. According to the circuit of Figure 4.20, this term provides all width-independent gate-drain capacitances. Figure 4.26 indicates that it presents a low value when the device is biased in deep depletion: in this case the 'intrinsic' contribution from the AZEs is assumed to be negligible and we have $Im(Y_{12}/\omega)|_{W_f=0} \approx C_{gda}$. A similar approach was used to determine C_{gsa}.

The intrinsic capacitances are then classically obtained from the $Im(Y_{ij})$ parameters (with $i, j = 1, 2$) [19] and the rest of the parasitics extraction is achieved by determining the values of the source, drain and gate resistances using the strong inversion method proposed in [27]. The intrinsic front and back gate transconduc-

tances can then be evaluated from the following expressions, which are only valid at low frequencies and account for the presence of the source and drain resistances:

$$Re(Y_{21}) = \frac{g_{mi}}{1 + g_{mi}R_{se} + g_{di}(R_{se} + R_{de})} \tag{4.43}$$

$$Re(Y_{23}) = \frac{g_{mbi}}{1 + g_{mbi}R_{se} + g_{di}(R_{se} + R_{de})} \tag{4.44}$$

And finally, the output conductance is classically obtained by considering the low frequency value of $Re(Y_{22})$:

$$Re(Y_{22}) = g_{di} + \frac{1}{R_{se}} + \frac{1}{R_{de}} \tag{4.45}$$

To conclude this section, the entire equivalent circuit that can be extracted from the measured 3-port device using multiport measurements is presented in Figure 4.27. This model is slightly simplified from the one presented in 4.20 but it is worth noting that merely all parameters could be independently extracted. (The parameters that could not be dissociated are grouped into common brackets.) In this model the g_{jbsi} and g_{jbdi} terms were neglected. The g_{bdsi} term associated with the kink effect is also not considered, as the characteristics frequencies associated with the kink effect are lower than than the available frequency range of the multiport VNA.

As shown in Figures 4.28 and 4.29, the model still adequately fits with the measured real and imaginary parts of the 3-port Y-parameters. It can also be observed that the model closely agrees with data obtained on a DT MOS device, in which case the body node in the small signal equivalent circuit is connected to the gate terminal.

4.7 Conclusion

In this chapter we investigated from an analogue perspective two important floating body effects (FBE) that are known to play critical issues in partially depleted (PD) SOI-based digital logic. These FBE are related to impact ionization and gate leakage currents, which respectively induce an increase of output conductance (g_d) in saturated devices and an increase of gate transconductance (g_m) in linear regime. Unlike previous works reported in the literature, a small signal approach was adopted here to study the AC behaviour of these two types of FBEs on a 0.13 μm technology from ST Microelectronics. A small signal equivalent circuit of the PD device including the floating body node was then used in order to

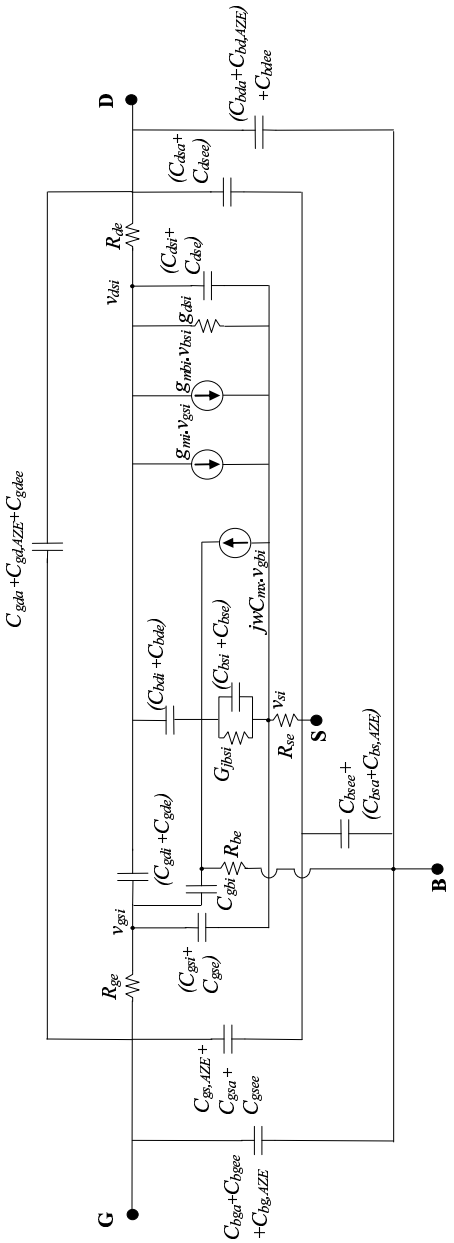


Figure 4.27: Equivalent circuit of the 3-port RF device extracted in this chapter on the basis of 3-port RF measurements.

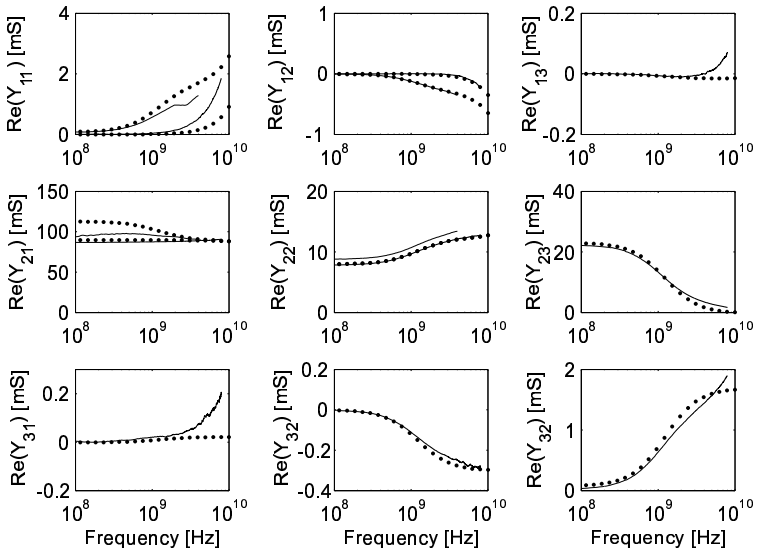


Figure 4.28: Real parts of the Y_{ij} parameters as measured on a 3-port and a DT RF devices and as modeled using the equivalent circuit of Figure 4.27 in which the g_{bdsi} and g_{jbsi} terms are neglected.

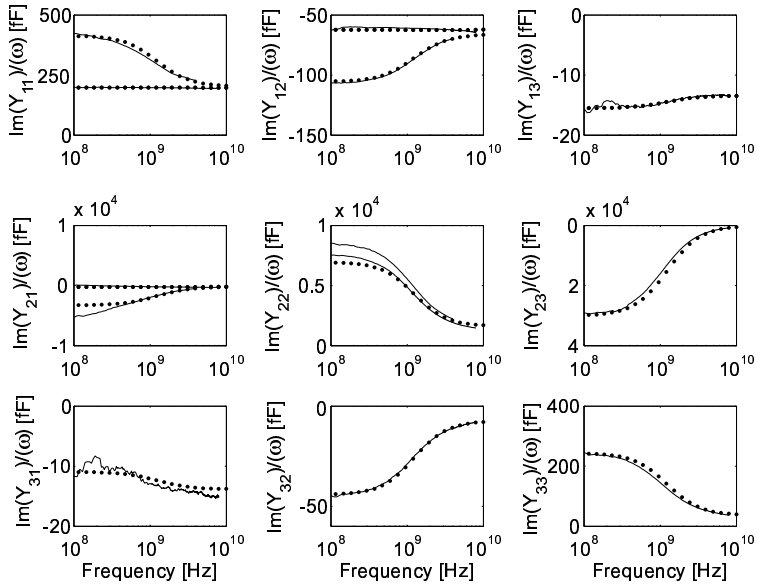


Figure 4.29: Imaginary parts of the Y_{ij} parameters as measured on a 3-port and DT devices and as modeled using the equivalent circuit of Figure 4.27 in which the g_{bdsi} and g_{jbsi} terms are neglected.

model the experimental data and derive analytical expressions of the measured g_d and g_m. These expressions were shown to accurately describe the frequency behaviour of the output conductance and that of the gate transconductance. They also highlighted the very high similarities that exist between both phenomena.

As FBE are traditionally prevented by providing lateral contacts to the body region, body-contacted devices were also measured and modeled using the same small signal approach. Two classical device architectures were considered: with the body either connected to the source (body-tied or BT devices) or to the gate (dynamic threshold or DT devices). The frequency analysis clearly indicated that the benefits gained under DC conditions by the body contacts (yet, to the cost of die area consumption) were lost at high frequencies: the output conductance of BT devices increase and the gate transconductance of DT devices decrease for frequencies typically higher than a few hundreds of MHz. A large difference therefore exists between the DC and RF values for these two factors of merit, which can lead to serious circuit performance issues if ignored at a circuit design stage.

However, using a two-port small signal model these observations could be very simply explained by the quite large value of the body resistance and the body contacts (R_{be}). This high resistance leads to the undesired situation that the AC body potential is fixed by capacitive coupling with the other nodes at frequencies higher than $1/(2\pi R_{be}C_{bb})$, in which C_{bb} represents the total body capacitance. These findings therefore clearly suggest that an accurate modeling of the AC behaviour of BC devices requires an as accurate knowledge of the body resistance as well as the body capacitances.

The last section of this chapter was therefore devoted to illustrate the use of a novel method for the characterization of the body node in BC devices, consisting in multiport VNA measurements on devices with 3 RF-probing pads (two conventional pads connected to the gate and the drain and one additional pad connected to the body contacts). The multiport measurements (and the resulting 3x3 Y matrices) could be fully exploited to extract all intrinsic capacitances, the body resistance and almost all of the extrinsic capacitances. It was shown in particular that the parasitic capacitances associated with the lateral extensions of the active zone below the gate polysilicon (required for the body contacts) are strongly bias dependent and may clearly not be neglected for an accurate modeling of the device behaviour. Other intrinsic parameters, such as the back gate transconductance and the body junction conductances could also be extracted from the measurements (to the limit of the equipement accuracy). After injecting the extracted values of both intrinsic and extrinsic parameters into a complete 3-port small signal model, the wideband frequency behaviour of the measured device could be quite accurately predicted.

A precise modeling of a DT MOSFET of identical geometry and originating from the same technology could also be achieved by simply connecting the body to the gate node in the model, thus supporting the accuracy of the model and the extraction procedure.

The small signal modeling approach presented here provides a complementary approach to large signal models (such as the ones presented in [28,29]), which consider devices as pure black boxes and for which the behaviour is described using merely blind, though accurate, mathematics. The strong accuracy of large signal models for the time, amplitude and frequency dependence of the device behaviour makes that kind of models particularly well suited for circuit design applications. On the other hand, the wideband multiport small signal modelling approach developed here deeply penetrates into the device physics. It not only sorts out the contribution of the parasitics from that of the intrinsics but also allows to differentiate and describe the different mechanisms that occur inside the devices and which alter its electrical behaviour, such as the body coupling with the other nodes. By doing so, this approach can therefore be of great support for the parameterization of SOI compact models (such as BSIMSOI). Compact models indeed require the precise determination of numerous parameters, many of them being directly associated with the body and traditionally obtained by fitting methods. Also, one advantage of using multiport VNA measurements is that both real (such as conductances and transconductance) as well as imaginary (such as intrinsic and extrinsic capacitive terms) parameters can be all extracted using only a few measurements (at different biases) while keeping the same equipment set-up. This extraction method is therefore cost- and time-effective.

References

[1] V. Kilchytska, A. Neve, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. D. Meyer, C. Raynaud, M. Dehan, J.-P. Raskin, and D. Flandre, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 577–588, 2003.

[2] O. Rozeau, J. Jomaah, C. Boussey, C. Raynaud, J. L. Pelloie, and F. Balestra, "Comparison between fully- and partially-depleted SOI MOSFET's for low-power radio-frequency applications," *Proc. of IEEE International SOI Conference*, pp. 22–23, 1999.

[3] Y.-C. Tseng, W. Huang, M. Mendicino, D. J. Monk, P. J. Welch, and J. C. S. Woo, "Comprehensive study on low-frequency noise characteristics in surface channel SOI MOSFETs and device design optimization for RF ICs," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1428–1437, 2001.

[4] J.-P. Colinge, *Silicon-On-Insulator technology: Material to VLSI.* USA: Springer, 2004.

[5] G. Shahidi, A. Ajmera, F. Assaderaghi, R. J. Bolam, H. Hovel, E. Leobandung, W. Rausch, D. Sadana, D. Schepis, L. Wagner, L. Wissel, K. Wu, and B. Davari, "Device and circuit design issues in soi technology," *Proc. IEEE Custom Integrated Circuits*, pp. 339–346, 1999.

[6] T. Poiroux, O. Faynot, C. Tabone, H. Tigelaar, H. Mogul, N. Bresson, and S. Cristoloveanu, "Emerging floating-body effects in advanced partially-depleted SOI devices," *IEEE International SOI Conference*, pp. 99–100, 2002.

[7] K. K. Das and R. B. Brown, "Novel circuit styles of minimization of floating body effects in scaled PD-SOI," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 29–34, 2003.

[8] Y. Shi, T. Ma, S. Prasad, and S. Dhanda, "Polarity dependent gate tunneling currents in dual-gate CMOSFETs," *IEEE Trans. Electron Dev.*, vol. 45, no. 11, pp. 2355–2360, 1998.

[9] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," *IEEE Trans. Electron Dev.*, vol. 48, no. 7, pp. 1366–1373, 2001.

[10] M. Chan, P. Su, H. Wan, C.-H. Lin, S. K.-H.Fung, A. M. N. C. Hu, and P. K. Ko, "Modeling the floating body effects of fully depleted, partially depleted and body grounded SOI MOSFETs," *Solid State Electronics*, vol. 48, pp. 969–978, 2004.

[11] C. F. Edwards, W. Redman-White, B. M. Tenbroeck, M. S. L. Lee, and M. J. Uren, "The effect of body contact series resistance in SOI CMOS amplifier stage," *IEEE Trans Electron Devices*, vol. 44, no. 12, pp. 2290–2294, 1997.

[12] Y.-C. Tseng, W. M. Huang, D. J. Monk, P. Welch, J. M. Ford, and J. C. S. Woo, "AC floating body effects and the resultant analog circuit issues in submicron floating body and body-groundend SOI MOSFET's," *IEEE Trans Electron Devices*, vol. 46, pp. 1685–1692, 1999.

[13] A. Mercha, J. M. Rafí, E. Simoen, E. Augendre, and C. Claeys, "Linear kink effect induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETs," *IEEE Trans. Electron Dev.*, vol. 50, no. 7, pp. 1675–1682, 2003.

[14] J. Pretet, T. Matsumoto, S. Cristoloveanu, R. Gwoziecki, C. Raynaud, A. Roveda, and H. Brut, "New mechanism of body charging in partially depleted SOI MOSFETs with ultra-thin gate oxides," *Proc. of ESSDERC*, pp. 515–518, Florence (Italy), 2002.

[15] R. Howes and W. Redman-White, "A small-signal model for the frequency-dependent drain admittance in floating-substrate MOSFETs," *IEEE J. of Solid State Circuits*, vol. 27, pp. 1186–1192, 1992.

[16] S. Fung, M. K. Wong, M. Chan, C. Nguyen, and P. Ko, "Frequency dispersion in partially depleted SOI MOSFET output resistance," *Proc. of IEEE Int. SOI Conf.*, pp. 146–147, 1996.

[17] D. Sinitsky, R. Tu, C. Liang, M. Chan, J. Bokor, and C. Hu, "AC output conductance of SOI MOSFETs and impact on analog applications," *IEEE Electron Device Letters*, vol. 2, pp. 36–38, 1997.

[18] Y. P. Tsividis, *Operation and modeling of the MOS transistor*. Mc Graw Hill, 1987.

[19] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker, and J.-P. Colinge, "Accurate SOI MOSFET characterizaton at microwave frequencies for device performance optimization and analog modeling," *IEEE Trans. on Electron Devices*, vol. 45, no. 5, pp. 1017–1025, 1998.

[20] M. Dehan, "Characterization and modeling of SOI RF integrated components," Ph.D. dissertation, UCL, Louvain-la-Neuve, Belgium, 2003.

[21] [Online]. Available: www-device.eecs.berkeley.edu/~bsimsoi

[22] P. J. van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A new straightforward calibration and correction procedure for 'on wafer' high frequency *S*-parameter measurements (45 MHz-18 GHz)," *IEEE Bipolar Circuits Technol. Meeting*, pp. 70–73, 1987.

[23] M. Dehan, D. Vanhoenacker, and J.-P. Raskin, “Partially depleted SOI dynamic threshold MOSFET for low-voltage and microwave applications,” *203rd Meeting of the Electrochemical Society*, April 2003.

[24] M. Goffioul, D. Vanhoenacker, and J.-P. Raskin, “Direct extraction techniques of microwave small-signal model and technological parameters for subquarter micron SOI MOSFETs,” *5th Symposium Diagnostics and Yield: SOI material, device and characterization*, p. p. 8, July 2000.

[25] B.-J. Lee, K. Kim, C.-G. Yu, J.-H. Lee, and J.-T. Park, “Effects of gate structures on the RF performance in PD SOI MOSFETs,” *IEEE Microwave and Wireless Components Lett.*, vol. 15, no. 4, pp. 223–225, 2005.

[26] B. Razavi, R.-H. Yan, and K.-F. Lee, “Impact of distributed gate resistance on the performance of MOS devices,” *IEEE Trans. Circuits and Systems*, vol. 41, no. 11, pp. 750–754, 1994.

[27] A. Bracale, V. Ferlet-Cavrois, N. F. D. Pasquet, J. L. Gautier, J. L. Pelloie, and J. du Port de Poncharra, “A new approach for SOI devices small-signal parameters extraction,” *Analog Integrated Circuits and Signal Processing*, vol. 25, no. 2, pp. 157–169, 2000.

[28] A. Siligaris, G. Dambrine, D. Schreurs, and F. Danneville, “A new empirical nonlinear model for sub-250nm channel MOSFET,” *IEEE Microwave and Wireless Comp. Lett.*, vol. 13, no. 10, pp. 449–451, 2003.

[29] ——, “130-nm paritally depleted SOI MOSFET nonlinear model including the kink effect for linearity properties investigation,” *IEEE Trans. Electron Dev.*, vol. 52, no. 12, pp. 2809–2812, 2005.

CHAPTER 5
RF CHARACTERIZATION OF TRIPLE GATE DEVICES

5.1 Introduction

As CMOS technologies continue to scale down increasingly challenging issues are faced to maintain high performance (HP) logic circuits. According to the predictions made by the 2005 ITRS Roadmap [1], the primary challenges in the forthcoming six years will consist in the implementation of devices with enhanced mobility, high gate dielectric and metal gate electrodes. A number of these improvements will be achieved on planar bulk CMOS devices but the bulk CMOS technology should reach the limit of scaling by 2013, which corresponds to the production year of 13 nm-physical gate length for HP logic ($L_{g,HP}$). Beyond 2013 more advanced technologies will need to be considered, such as ultra-thin body (UTB) fully depleted SOI MOSFETs or multiple-gate MOSFETs (MUGFETs) with quasiballistic enhanced transport [1]. These two technologies should already come on the production stages by 2008 ($L_{g,HP}$ = 22 nm) and 2011 ($L_{g,HP}$ = 16 nm), respectively. However, the ultimate MOSFET is projected to be the multiple-gate device since the scaling of MUGFETs is superior to that of UTB FD MOSFETs. This improved scaling is essentially due to a better control of short channel effects in MUGFETs. Leading IC manufacturers such as AMD [2], Intel [3], IBM [4] and Freescale [5] have all been devoting much effort in the past years to the fabrication and integration of such devices.

The successful fabrication of multiple gate devices is currently a hot topic. A variety of device geometries have been explored [6] such as double (Figure 5.1b) or triple gate MOSFETs (quantum wire [7] (Figure 5.1c), FinFET [8] Figure 5.1d), Δ-channel SOI MOSFET [9]), quadruple-gate devices (gate all-around (GAA, Figure 5.1e) device [10], DELTA transistor [11], vertical pillar MOSFET [12], Pi-gate SOI (Figure 5.1f) MOSFET [13] and Omega-gate SOI MOSFET [14] (Figure 5.1g)) and, more recently, the inverted T structure or ITMOSFET [5] (Figure 5.1h). Comparative studies performed on multiple gate devices generally show that for a given silicon volume devices with a higher gate area present a better control of short channel effects [6,15,16], and thus, better DC performance. Unfortunately, the fabrication of multiple gate devices is in most cases hardly compatible with classical planar CMOS processing due to their 3-D gate configuration. Nevertheless, some devices

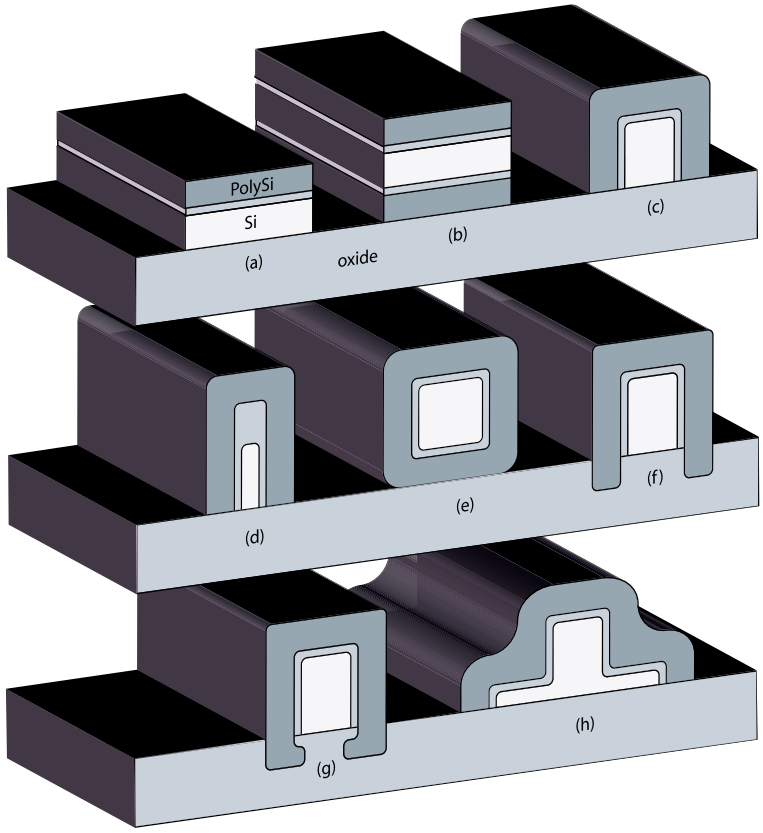


Figure 5.1: Schematic description of the (a) single gate, (b) double gate, (c) triple gate, (d) FinFET, (e) gate-all-around, (f) Pi-gate, (g) Omega-gate devices and (h) inverted T MOSFETs.

present a better compatibility than others with standard CMOS technologies, such as FinFETs and triple gate structures. Real FinFET structures were already presented for the first time in 1989 [11] under the name of *DEpleted Lean-channel TrAnsistors* (DELTA). Some advantages offered by FinFETs devices are the natural self alignment of the two gates, their compatibility with strained Si and their higher area efficiency (especially if spacer lithography is used [17, 18]). This kind of devices currently appears as the most promising Si-based transistors to meet the ITRS Roadmap requirements for device performance in future generations.

So far, much of the effort devoted to the realization of FinFETs and triple gate structures has focused on their technological aspects [4, 17, 19–22], on design considerations [6, 16, 23–26] and their perspectives for digital applications [2, 19, 27]. Very little work has thus been performed to assess their analogue figures of merit

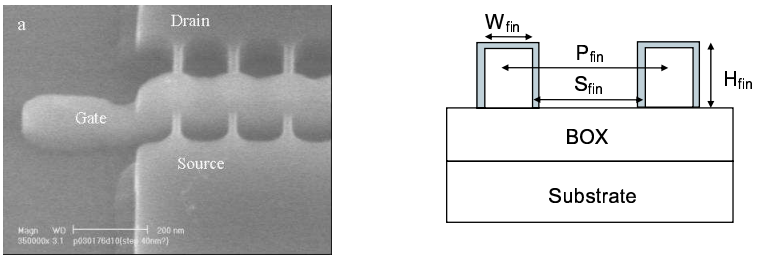


Figure 5.2: (a) Picture of the fins after the deposition of the polysilicon. (b) Cross section of the fins and definition of the geometrical parameters.

[28]. The aim of this chapter is to partially fill this lack by providing an investigation of the RF properties of such devices. The DC behavior of the measured devices is first presented. The results of the RF characterization are described next, on the basis of a small signal analysis.

5.2 Investigated triple gate devices

The n-type devices investigated here were fabricated at IMEC, Leuven, Belgium, on standard resistivity UNIBOND SOI wafers with a buried oxide thickness of 145 nm. Devices originating from two different lots (A and B) were measured. The fin patterning was performed using either e-beam lithography and dry etching (lot A) or 193 nm-lithography and hard mask trimming (lot B, comprising two wafers: D19 and D20). In the latter case a hydrogen anneal and a sidewall oxidation were used for surface smoothening and corner rounding. The fin height/spacing ratio (H_{fin}/S_{fin}) were 75 nm/100 nm and 60 nm/328 nm for the devices of lots A and B, respectively. The fin pitch (P_{fin}) is given by $S_{fin} + W_{fin}$ (Figure 5.2b).

In the case of lot A, the threshold voltage was adjusted using a channel implant and a 2.0 nm-thick $SiON$ + 100 nm PolySi gate stack. For lot B, no implantation was made and a high K ($SiON + HfO$) + metal ($TiCN$) + 100 nm PolySi gate stack was made for V_t tuning. A picture of the fins after the polySi deposition is presented in Figure 5.2a. In the case of Wafer D20 from lot B a 40 nm-thick selective epitaxial growth (SEG) was performed on the source/drain extensions. No SEG was made on the other wafers. After the HDD implantations and RTA, NiSi was used as silicide and only one metal level was deposited.

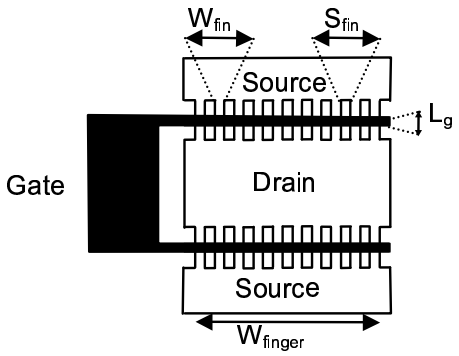


Figure 5.3: Geometry of the studied RF FinFETs: illustrative example with 2 fingers of 10 fins each.

As in this fabrication process a horizontal gate is naturally formed on the top of the fin the fabricated devices are treated here as *triple gate* devices [16], in opposition to *FinFETs* which present no top conduction [8]. According to Figure 5.2b, the total channel width in a single fin device is simply given by: W_{tot}=2xH_{fin} + W_{fin}. This parameter is of course to be multiplied by the number of fins in multiple (parallel) fin devices such as in Figure 5.2a.

A schematic top view of the RF structure is also provided in Figure 5.3 for a clear understanding of the RF architecture. It is seen that the classical multifinger RF structure has been preserved, and that in this case each polysilicon finger is composed of a certain number of fins. The total width of the device is thus given by:

$$W_{tot} = (2H_{fin} + W_{fin})N_{fin}N_{finger} \tag{5.1}$$

in which N_{fin} and N_{finger} respectively denote the number of fins per finger and the number of fingers. As the devices from lot A had only 2 fingers (compared to 50 for the devices from lot B) they were not optimized for maximum RF performance and most of the results presented in the following sections were obtained on devices from lot B. The nominal dimensions for devices of lot A and lot B are summarized

Table 5.1: Nominal dimensions of the RF devices from lots A and B.

	L_g [nm]	H_{fin} [nm]	W_{fin} [nm]	S_{fin}	N_{fin} [/finger]	N_f	W_f [μm]
lot A	50	75	55	100	88	2	15
lot B	60	60	32	328	6	50	2

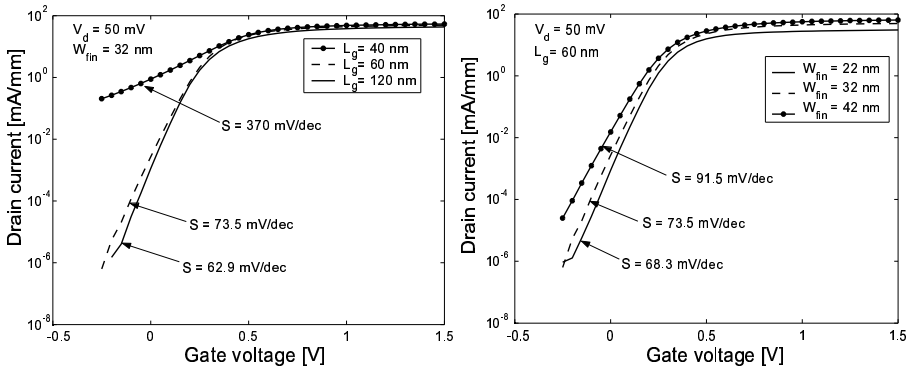


Figure 5.4: Normalized drain current and subthreshold swing (a) vs gate length and (b) vs fin width.

in Table 5.1. When not explicitly stated in the text, the geometrical dimensions of the referred devices correspond to their nominal values.

On both lots, single gate devices were also processed in the exact same way as the triple gate structures, with the exception that the active region was not additionally patterned to form fins. The device width in this case roughly corresponds to the width of the active region (W_f), also reported in the table.

5.3 DC characteristics of the triple gate structures

The DC and RF analyses were performed on the RF devices from lot B - Wafer D20, unless otherwise stated, with 50 gate fingers of 6 fins each and for a nominal gate length of 60 nm and a nominal fin width of 32 nm. The subthreshold slope in linear regime (or linear swing, S) measured on the devices is reported in Figures 5.4a and b, for devices with different gate length (40, 60 and 120 nm) and fin width (22, 32 and 42 nm), respectively. The current data in both figures were normalized by considering the total device gate width (Eq. 5.1).

As shown in Figure 5.4a, the 60-nm technology investigated here outlines a good control over SCE, with a subthreshold slope close to 73.5 mV/dec. This value is even close to the ideal figure for L_g = 120 nm (S= 62.9 mV/dec). Such performance largely competes with data reported in other published works for FinFETs and triple gate devices with similar dimensions (Table 5.2). The swing is seen to be largely degraded for a gate length of 40 nm, due to a small L_g/W_{fin} ratio and excessive short channel effects [16, 26].

As expected from both experimental [21] and numerical [16, 26] works, the

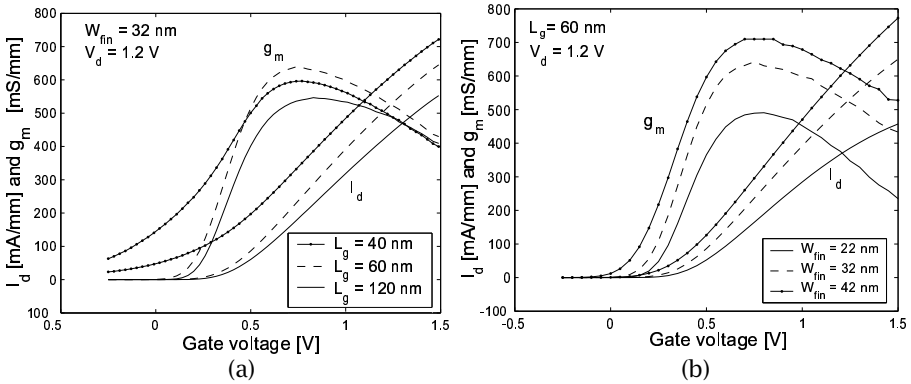


Figure 5.5: Normalized transconductance (a) vs gate length and (b) vs fin width.

devices also exhibit reduced SCE as the fin width is reduced. This is shown in Figure 5.4b, which reports lower S values for narrower fins, and may be explained by a higher control from the gate on the channel [16, 26].

The normalized drain currents and extrinsic transconductance (g_m) values obtained at V_d=1.2 V are reported in Figures 5.5a and b for the various L_g and W_{fin} values, respectively. For our nMOS devices, the <110> Si crystal orientation on the lateral channels provides a lower mobility for electrons than for holes [31]. This partly explains why device performances are inferior to those reported in previous works for devices with similar dimensions. They are also comparable to those of devices with longer gates, which might be related to lower mobility values or

Table 5.2: DC performance of the investigated triple gate structures and comparison with previous works (*: taken at $V_g = V_d = 1.3$ V, **: physical thickness, ***: on the side walls of the fins).

	[4]	[4]	[26]	[29]	[17]	[30]	[21]	[21]	[21]	[21]	This work
L_g [nm]	30	30	30	50	60	60	105	145	145	145	60
t_{ox}^{**} [nm]	1.6	1.6	/	1.8	2.5	1.5	2.2	2.2	2.2	2.2	2
H_{fin} [nm]	65	65	50	50	50	36	82	82	82	82	60
W_{fin} [nm]	10	20	10	30	40	55	13	13	23	63	32
Si orientation***	/	<100>	/	/	<110>	/	<111>	<111>	<111>	<111>	<110>
SEG	Yes	No	No	No	No	Yes	No	No	No	No	Yes
S_{lin} [mV/dec]	75	75	77	/	70	68	73	64	65	80	73.5
$I_{on}\|_{V_{go}=1V}$ [$\mu A/\mu m$]	1460	675	800	470	400	1140*	600	/	/	/	520
V_d [V]	1.5	1.5	1	1	1	1.3	1	1	1	1	1.2
g_{mmax} [$\mu S/\mu m$]	1330	/	/	/	/	/	700	600	600	590	650

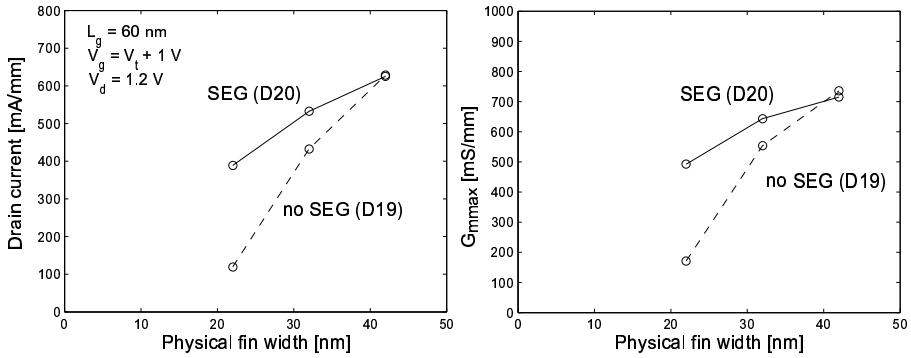


Figure 5.6: (a) Normalized drain current and (b) maximum value of normalized transconductance as a function of fin width for the wafers with (D20) and without (D19) SEG.

higher parasitic source/drain resistance. It is also seen here that the increase of g_m expected by a reduction of L_g is lost at L_g=40 nm due to pronounced SCEs. This additionally leads to a noticeable reduction of the threshold voltage.

A decrease of the fin width, which is necessary to reduce short channel effects, is seen here to have a strongly detrimental impact on both the normalized drain current and maximum value of gate transconductance (g_{mmax}). This is illustrated in Figures 5.6a and b, which respectively report the normalized currents (for V_d=1 V and $V_g - V_t$=1 V) and the maximum g_m (at V_d=1.2 V) values as a function of W_{fin} for the two investigated wafers. As inferred by previous works this observation may partly be explained by the increase of the parasitics source/drain resistance as the fins are made thinner [4,18,32]. This is further supported here by the obvious lower device performance on the wafer that received no SEG (wafer D19).

From the perspective of device DC performance, Figures 5.4b, 5.6a and 5.6b clearly highlight the fact that, unless the device fabrication process is further improved, the fin geometry must be chosen by considering the trade off that exists between a good control over short channel effects (for which thin fins are needed) and high drain current values (for which lower parasitic S/D resistances, and thus thicker fins, are required). Thinner fins could be favored in low power applications (with reduced off state current) while devices with wider fins might be more appropriate for high performance digital circuits. As we see in later sections the fin width also has a strong impact on the device RF properties.

5.4 RF properties of the investigated triple gate MOSFETs

The aim of the RF characterization performed in the following paragraphs is triple.

- First, it is to assess the RF performances of the available triple gate devices in terms of gain and cut off frequencies and compare them with those of planar devices with similar gate length.
- Second, it is to extract the intrinsic and extrinsic elements of an equivalent small signal model for the nominal device geometry. As illustrated later in this chapter, this approach is a powerful means to identify the technological issues arising during the fabrication process.
- And last, it is to provide different technological paths to optimize the device RF performance. Performance predictions for optimized devices can then be easily performed on the basis of the small signal model previously obtained.

5.4.1 Factors of merit investigated in this work

5.4.1.1 Current and power gains

One important factor of merit that is used to characterize the RF properties of transistors consists in the current gain ($|H_{21}|$), which is given by:

$$|H_{21}| = \frac{|Y_{21}|}{|Y_{11}|} \tag{5.2}$$

The current gain is often used since it is traditionally considered to reflect the RF properties of the intrinsic core of the devices (i.e., without being affected by the access parasitics) [33]. However, by definition the computation of the current gain imposes a short load condition at the output port and this factor is therefore not representative, by itself, of the power gain that can be expected from a given device.

For this reason the MAG is more often used, which is defined as the *maximum power gain* that can be extracted from a given transistor. According to two-port theory, it is obtained under conjugate matched conditions at both input and output. The MAG can be written in terms of the device S-parameters as follows:

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(k - \sqrt{k^2 - 1}\right) \tag{5.3}$$

where k is Rollet's stability factor:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{5.4}$$

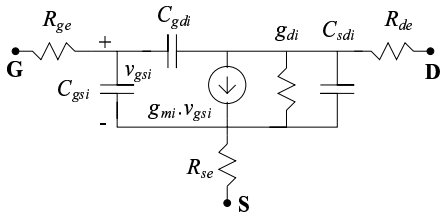


Figure 5.7: Classical equivalent circuit of a MOSFET in which the non quasi-static effects are not considered.

with $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

The MAG also accounts for the stability of the device through the factor k. When k>1 (and $|S12|.|S21| > 1 - |S_{ii}|^2$ with $i = 1, 2$), the device is unconditionally stable, which means that it will not oscillate regardless of the input and output load impedances. When k<1, the device may become unstable under some input/output load conditions and the MAG becomes undefined. In such conditions the *maximum stable gain* (MSG) is traditionally used. It is computed from:

$$MSG = \frac{S_{21}}{S_{12}} \tag{5.5}$$

The MSG represents the gain that would be achieved if the conditionally stable device were first terminated with resistors to the point where it becomes unconditionally stable (i.e., k=1), and then conjugately matched at both the input and the output.

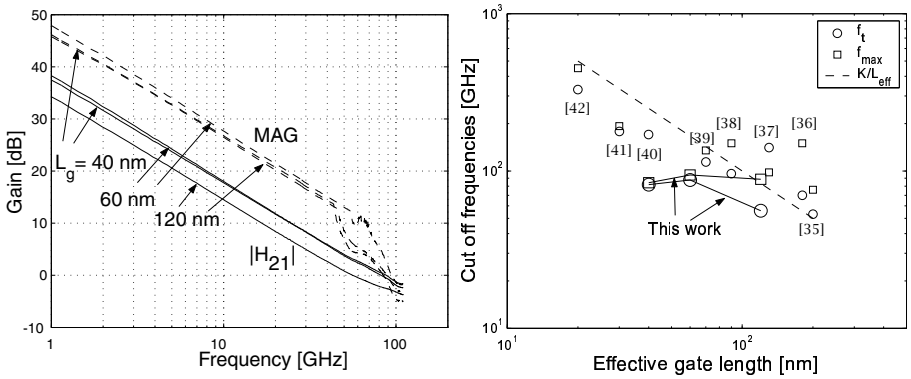
5.4.1.2 Cut-off frequencies

Two additional figures of merit are considered in this work: the cut-off frequency of the current gain (f_t) and the cut-off frequency of the maximum power gain, also referred to as the *maximum oscillation frequency* (f_{max}). For the classical small signal equivalent circuit presented in Figure 5.7, Ref. [34] provides the following expressions:

$$f_t \simeq \frac{f_c}{1 + \frac{C_{gdi}}{C_{gsi}}\left(1 + (R_{se} + R_{de})(g_{mi} + g_{di})\right) + (R_{si} + R_{di})g_{di}} \tag{5.6}$$

$$f_{max} \simeq \frac{f_c}{\left(1 + \frac{C_{gdi}}{C_{gsi}}\right)\sqrt{4g_{di}\left(R_{ge} + R_{se}\right) + 2\frac{C_{gdi}}{C_{gsi}}\left(\frac{C_{gdi}}{C_{gsi}} + g_{mi}R_{se})\right)}} \tag{5.7}$$

where f_c is given by $\frac{g_{mi}}{2\pi C_{gsi}}$.



(a) (b)

Figure 5.8: (a) Measured gain curves as a function of frequency and gate length on the devices from lot B and (b) comparison of the corresponding f_t and f_{max} values with published data measured on bulk and SOI technologies. NB: for our devices the *physical* polysilicon gate length is reported.

In these expressions, both C_{gsi} and C_{gdi} include the overlap capacitances and fringing fields between the polysilicon gate and the S/D extensions. The expressions indicate that both f_t and f_{max} are negatively affected by the device parasitics, namely R_{se}, R_{de}, R_{ge} as well as the extrinsic capacitances.

The impact of those parasitics on the RF properties of the investigated multiple gate structures is detailed in the coming sections. However, it must be kept in mind that these expressions provide only approximate values of f_t and f_{max}, which for instance do not include the effect of C_{ds}. Besides, they appear to loose their accuracy for low values of the C_{gs}/C_{gd} ratio. They are introduced here for illustrative purposes only. For a better accuracy of the work presented in the following sections, f_t and f_{max} predictions for optimized devices are based on small signal circuit simulations and are then extracted from the modeled $|H_{21}|$ and MAG vs frequency curves, respectively.

5.4.2 RF performance vs gate length

The investigated devices were measured up to 110 GHz with an Agilent VNA mounted on a Cascade prober and 100 μm-pitch Picoprobes. A two step deembedding method (open and short subtraction) was applied to remove the access parasitics from the measured S-parameters. The current gains, MSG and MAG of the devices are reported for the three available gate lengths (W_{fin}=32 nm) in Figure 5.8a. The corresponding measured cut off frequencies (f_t and f_{max}) are plotted in Figure 5.8b as a function of L_g. In this figure, the data are compared

with those obtained on other currently available or recently developed Si-based technologies. It is to be noted that since these are the first RF measurements of TG structures, the comparison is performed here with either bulk, fully-depleted or partially-depleted SOI technologies.

The figure shows that, even if f_{max} values close to 100 GHz could be reached, they remain lower than what was reported in earlier works for planar devices. The same comments also apply for the f_t data. As inferred by Eqs. 5.6, this might be related to the presence of stronger parasitics in the TG structures, which is what is analyzed in the following paragraphs. The first investigated parasitics are related to the gate. The gate resistance is known to be a factor severely limiting the maximum oscillation frequency of RF planar devices.

5.5 Issues related to the gate processing in TG MOSFETs

From the perspective of device RF performance, patterning low-resistance gate fingers at a desired length in TG or FinFET structures presents two major issues:

- An efficient silicidation of the gate polysilicon is a troublesome task, considering the highly nonuniform thickness (topography) of the polysilicon sheet.

- A particular care must be taken to prevent polysilicon residues along the fins, which can largely contribute to increase the level of parasitic capacitance at the gate.

5.5.1 Gate silicidation

As explained in [43], two main approaches are currently under development to provide a reliable gate process scheme that is compatible with CMOS mass production, keeping in mind that the primary concerns in this area are to obtain a controllable threshold voltage value and to ensure reduced gate leakage.

The first method consists in forming the gate using mid-gap metals (for V_t tuning) and high-K (to reduce gate leakage) dielectric, which is a difficult approach due to the high gate topography of TG structures. The deposited metal layer is on the order of several nm-thick [44] and the gate stack is therefore completed with an additional polysilicon (or amorphous Si as in [44]) layer. In this context, one advantage gained by using a metallic layer is the absence of depletion effects in the polysilicon. From an RF performance perspective, the deposited metal is too thin to provide any reduction of the gate resistance and the polysilicon layer must therefore be silicided. The gate silicidation is traditionally performed at the

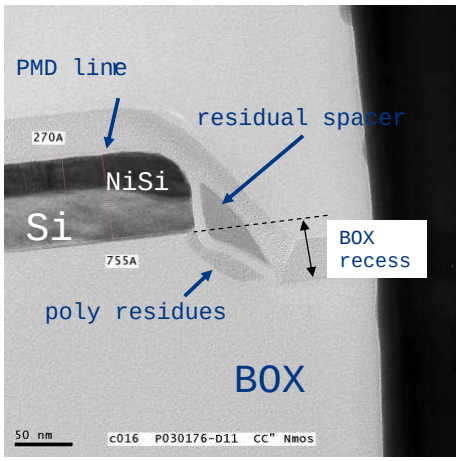


Figure 5.9: SEM picture taken across the fin in a TG device from lot A, illustrating the presence of residual spacers and residual polysilicon along the fins in the BOX recess.

same time as that of the S/D extensions. A second approach, which seems to be more promising to simultaneously tune the threshold voltage to the desired value and achieve low gate resistance, is called full gate silicidation (FUSI). In this process, the patterned gate polysilicon is converted into $NiSi$ [45] or $CoSi$ [22] by a silicidation step that completely consumes the gate poly-Si. Since both the S/D extensions in the fins and the polysilicon gate do not have the same thickness, the gate silicidation is differentiated from that of the S/D extensions [43]. In this case, the V_t tuning can be obtained by segregating the appropriate impurity at the silicide gate oxide interface [46], and the full silicidation of the gate is expected to provide low values of gate sheet resistivity. However, even for planar devices there are still two serious challenges to $NiSi$ integration: incomplete gate silicidation, which is a length dependent phenomenon, and variations in the gate silicide phase [47].

In Figures 5.10a and b we present the results of $|H_{21}|$, MSG and MAG measurements obtained on the 50 nm-long SG and TG devices (respectively) from lot A. For the TG devices a poor gate silicidation was performed. Post-process investigation and SEM pictures actually identified residual spacers on the polysilicon as the reason for this: the presence of the spacers locally prevented the silicidation of the polysilicon. A SEM picture illustrating the presence of spacer residue on the sides of the fins is given in Figure 5.9. The picture shows the right side of a (wide) fin and is taken in the S/D extensions.

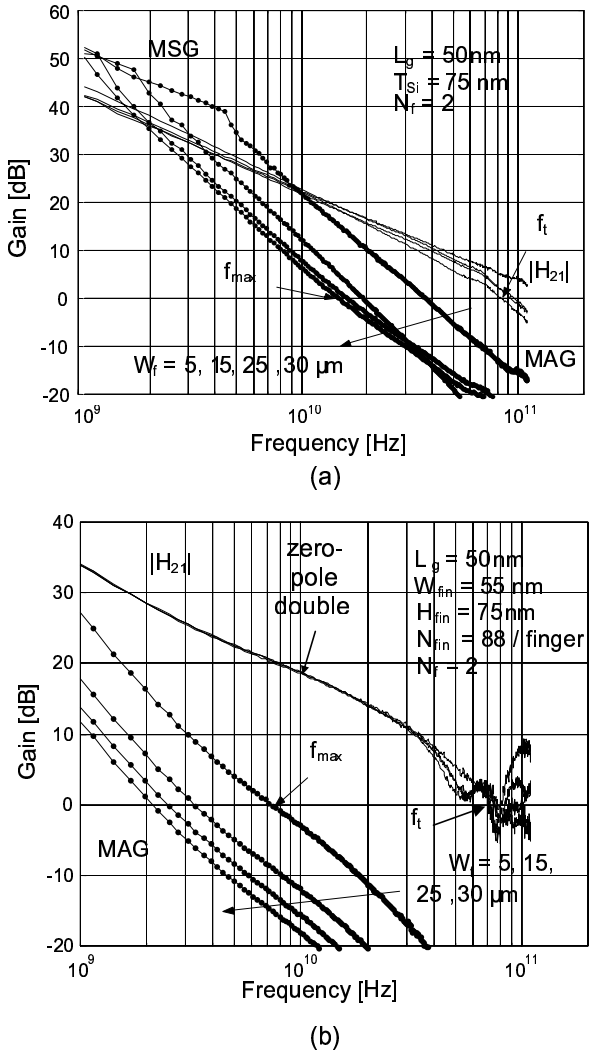


Figure 5.10: H_{21}, MSG and MAG measured on (a) single and (b) triple gate devices with unoptimized geometry and incomplete gate silicidation.

For the TG devices the figure clearly outlines very poor values of f_{max} (lower than 8 GHz) due to the non-optimized device geometry (the RF structures were made of only two, unfolded, 5 to 30 μm-wide fingers) but also to the high value of the polysilicon finger sheet resistivity.

The figure also highlights an unusual behaviour for the H_{21} and MSG curves of the TG devices: the curves exhibit a zero-pole pair that is not observed in the

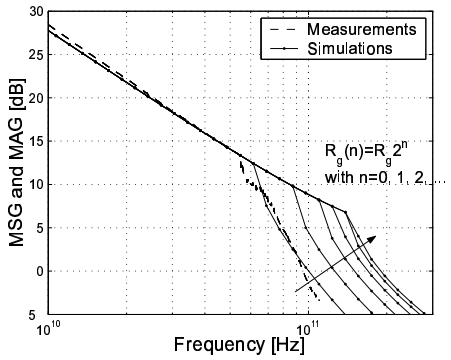


Figure 5.11: Illustration of the f_{max} increase obtained by a reduction of R_g for a device from lot B (W_{fin}=42 nm).

case of the SG devices. An explanation for such behaviour is given in the next paragraph.

The sheet resistivity of the deposited polysilicon in the TG structures ($R_{\square}$) was obtained by first extracting the gate resistance (R_{ge}) from the RF measurements using the strong inversion method proposed in [48] and then by normalizing R_g according to:

$$R_{\square} = \frac{3R_{ge}N_f L_g}{W_{poly}} \tag{5.8}$$

In this expression, N_f represents the total number of fingers and W_{poly} considers the total "folded" width of a single finger: $W_{poly} = \Delta W + (2H_{fin} + W_{fin})N_{fin} + S_{fin}(N_{fin} - 1)$ where ΔW is the distance between the metal contact at the gate access and the active region. The factor 3 in Eq. 5.8 accounts for the distributed nature of the extracted R_g value [49]. In the case of lot A the extracted $R_{\square}$ value was 48 $\Omega/\square$ for devices with W_f=15 μm, N_f=2, N_f=88 fins/finger, W_{fin}=55 nm, S_{fin}=100 nm and H_{fin}=75 nm. This value was also extracted from single-gate (SG) devices processed on the same wafer but for which no e-beam fin patterning was performed. In this case the length of the polySi fingers was simply given by $W_{poly} = \Delta W + W_f$ with W_f being the width of the active region. The comparison yielded a value of $R_{\square}$ more than three times higher for the TG structures than for the SG devices ($R_{\square}$=15 $\Omega/\square$), which could be uniformly silicided.

In the case of lot B, the silicidation process was improved by removing the spacers using an etch-back step and the values of sheet resistivity for the TG and SG structures of identical geometry (W_f=2 μm, N_f=50, N_{fin}=50 fins/finger, W_{fin}=32 nm, S_{fin}=328 nm and H_{fin}=60 nm) were found to be 37 and 42 $\Omega/\square$, respectively.

Table 5.3: Values of the small signal parameter extracted from the measured devices and used in the simulations.

	W_{fin} [nm]	$g_{mieff,HF}$ [mS]	g_{di} [mS]	R_{ge} [Ω]	R_{se} [Ω]	R_{de} [Ω]
EXP1	22	21.3	3	4	18.3	21.3
EXP2	32	27.3	4.5	8	8.5	10.25
EXP3	42	29	6	10	5.5	6.5
	C_{gs} [fF]	C_{gd} [fF]	C_{ds} [fF]	f_t [GHz] (meas/ sim)	f_{max} [GHz] (meas/ sim)	
EXP1	32	13.2	15.5	69/69	91/87	
EXP2	32	14	14.5	91/98	93/101	
EXP3	31	15	14.5	100/95	95/100	

Though a slight reduction of $R_{\square}$ was obtained in this case for the TG devices these values are still 4≃5 times higher than what can be expected by successful gate silicidation in planar devices with similar gate length [50]. This observation implies that silicidation is a challenging issue in TG or FinFET devices and that for optimized RF device performance it must be adapted to the high fin topography.

To evaluate the impact of the sheet resistivity on the f_{max} performance of the investigated FinFETs, small signal simulations were performed using the simple circuit presented in Figure 5.7. The elements of that circuit were extracted using conventional extraction techniques [48, 51] and their values are reported in Table 5.3 (EXP1). In this case the capcitance values represent the sum of their corresponding intrinsic *and* extrinsic contributions. Figure 5.11 displays the MSG/MAG curves for a device with L_g=60 nm and W_{fin} =42 nm (N_f=50, W_f=2μm). The figure reports both the measured and simulated data for the extracted R_g value (n=0 in the graph) and a close match is observed between the two curves. The other simulated curves illustrate the enhancement of the MSG/MAG curves (and of f_{max}) obtained when reducing the gate resistance by multiples (n) of 2. It is seen that for the investigated device a 4 times reduction of $R_{\square}$ could increase f_{max} up to 150 GHz. Larger reductions of $R_{\square}$ could even increase f_{max} up to higher values. However this effect is seen to saturate due to the importance of the other parasitics (R_s, R_{de} and fringing capacitances) in the TG devices.

5.5.2 Polysilicon residues

Another particular source of trouble in the gate processing of multi-gate devices is the complete etching of the polysilicon when defining the gate length. During the gate definition, the removal of the fin oxide creates an undercut in the BOX

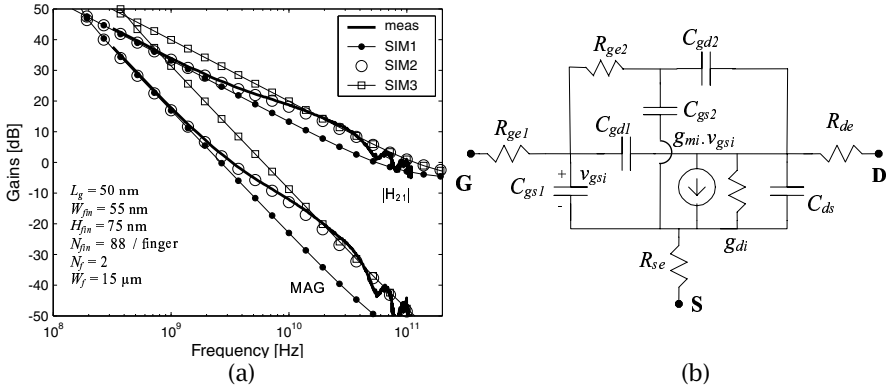


Figure 5.12: (a) Comparison between simulated and measured gain curves for devices from lot A: SIM1 data were obtained with the classical small signal equivalent circuit of Figure 5.7 and SIM2 data were obtained with that of Figure b. (b) Classical equivalent circuit in which the non quasi-static effects are neglected and which includes an additional parasitic RC network associated with polysilicon residues along the fins.

(also called BOX recess) at the fin/BOX corner. As a consequence, the polysilicon that is deposited to form the gate may not be totally removed from the undercuts if a classical poly etch method is used during the resist trimming operation, in which case polysilicon residues may be left along the fins. These residues can be removed by an additional etching step called polysilicon etch back [52].

When unwanted residues are still present they form polysilicon lines that are electrically connected to the gate and contribute to a large increase of the parasitic gate-source as well as gate-drain capacitances. These parasitics do not affect the device DC behavior and can therefore only be highlighted by an AC or RF characterization of the devices. The direct impact of those extra-parasitic is a reduction of the C_{gs}/C_{gd} ratio and of f_{max} (Eq. 5.6).

In the case of lot A, no polySi etch back was used and polysilicon residues were clearly left along the fins. This is also illustrated in the SEM picture of Figure 5.9. It is assumed that these un-silicided polysilicon residues present a much higher resistivity than the rest of the gate. As was shown in Figure 5.10b, these extra parasitics are suspected to induce an apparent zero-pole pair in the gain curves of the TG structures, which was not observed for the corresponding SG devices (Figure 5.10a). Figure 5.12a (SIM1) indicates that such behaviour can clearly not be modeled using the classical small signal circuit presented in Figure 5.7. For an accurate description of the $|H_{21}|$ as well as the MSG/MAG vs frequency curves (SIM2) an additional RC network therefore needs to be included in the model, which

is displayed in Figure 5.12b. In this case the values of R_{ge1}, R_{ge2}, C_{gs1}, C_{gs2}, C_{gd1} and C_{gd2} were tuned to obtain a close match between the modeled and measured data. This could however only be achieved for values such that:

$$R_{ge} \simeq R_{ge1} \tag{5.9}$$

$$C_{gs} = C_{gs1} + C_{gs2} \tag{5.10}$$

$$C_{gd} = C_{gd1} + C_{gd2} \tag{5.11}$$

in which R_{ge}, C_{gs} and C_{gd} are, respectively, the values of the gate resistance, gate-source and gate-drain capacitances extracted from the measurements when the classical model of Figure 5.7 is used (SIM1).

For the investigated device of lot A, a C_{gs}/C_{gd} ratio of 1.27 is found. This is a poor value as further detailed in Section 5.6.3. If no polysilicon residues had been left in the structures, the parasitic RC network could have been removed from the circuit of Figure 5.12a and a C_{gs1}/C_{gd1} ratio of 1.8~2 would have been obtained. This value is close to what is reported for devices of lot B and for which a polysilicon etch back step was processed (Section 5.6.3). Figure 5.12a (SIM3) illustrates the effect on the gain curves of suppressing the parasitic network. The comparison with the SIM2 curve indicates that the reduction of the capacitance in this case has no effect on f_t because the pole-zero frequencies associated with R_{g2} are lower than f_t. A 100 % increase of f_{max} is however observed, due to the strong increase of the C_{gs}/C_{gd} ratio (and the high value of the gate resistance in this case).

5.5.3 Metal gate processing

The processing of metal gate/high K devices that preserve their integrity at high frequency is also a troublesome task, as illustrated in this section. The deembedded S-parameters of a device from lot B - wafer D20, for which the gate stack consisted in $SiON$+MOCVD $TiCN$+HfO_2+polySi, are shown in Figure 5.13. In this case the low frequency parts of th e curves were obtained using a low frequency (10 kHz-4 GHz) VNA from R&S and a HF VNA (50 MHz-110 GHz) from Agilent. The figure outlines the presence of severe kinks in both the S_{21} and S_{22} curves. As shown in Figures 5.14a and b, these kinks are associated with a low frequency drop of the device transconductance and a low frequency increase of the device output conductance, respectively. These observations can be interpreted as a partial loss of control from the gate on the channel for frequencies higher than a certain cut-off frequency (f_c). For the 40 nm-long device, these variations occur

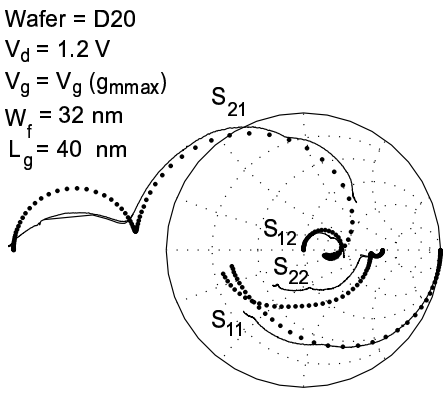


Figure 5.13: Typical S-parameters measured on the devices from lot B (high K/metal gate stack), outlining the presence of a severe kink in the S_{21} and S_{22} data.

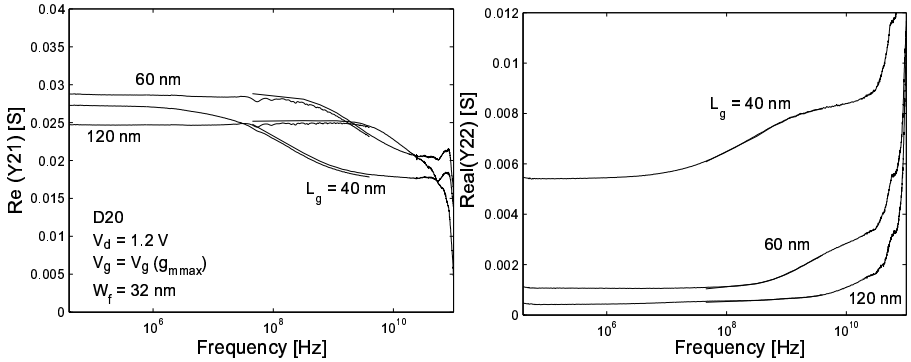


Figure 5.14: Real parts of the (a) Y_{21} and (b) Y_{22} parameters as a function of frequency and gate length for devices from lot B.

in the 10^7-10^9 Hz range. It is however seen in both figures that this range and its associated f_c are an increasing function of the device gate length, while it displays no dependence with respect to W_{fin} (Figure 5.15).

As also shown in Figure 5.13, the kink in the S_{21} and S_{22} curves can be reproduced using the equivalent circuit of Figure 5.16, in which an additional RC network has been added at the gate access. In this circuit, C_{gs2} can be neglected at low frequencies and the *effective* intrinsic transconductance ($g_{mieff,LF}$) is simply g_{mi}. For frequencies above f_c, C_{gs2} shunts R_{ge2} and the amplitude of the signal

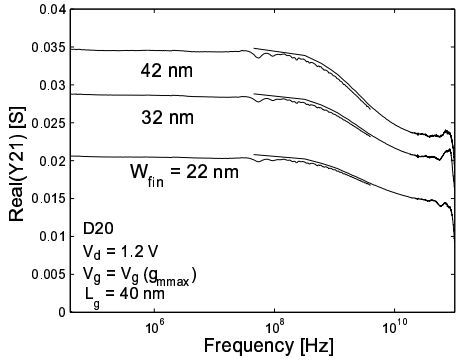


Figure 5.15: Real parts of the Y_{21} parameters as a function of frequency and fin width for devices from lot B.

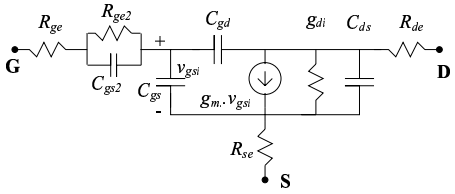


Figure 5.16: Equivalent circuit used to model the kink in the S_{21} and S_{22} curves of the devices from lot B.

across C_{gs} is the result of a capacitive divider. We therefore have:

$$g_{mieff,LF} = g_{mi} \tag{5.12}$$

$$g_{mieff,HF} = g_{mi} \frac{C_{gs2}}{C_{gs2} + C_{gs} + C_{gd}} \tag{5.13}$$

The extracted values of $g_{mieff,LF}$ and $g_{mieff,HF}$ are reported in Table 5.4 as a function of W_{fin}. The extrinsic transconductance values (i.e., including the effects of the S/D resistances) are also included in the table (g_m).

The physical origins of these kinks are not yet clearly understood. They were observed on the SG and TG devices of both wafers from lot B (though much lower f_c values were recorded for wafer D19) and were not observed on lot A. This suggests that they could be inherent with the processing of the high K/metal gate stack. To our knowledge, the RF properties of high K metal/metal gate MOSFETs have not been studied elsewhere. Further investigation should be performed to understand the causes of this phenomenon.

Table 5.4: Transconductance values extracted from the measured devices as a function of W_{fin}.

W_{fin} [nm]	g_m [mS]	$g_{mieff,LF}$ [mS]	$g_{mieff,HF}$ [mS]	$g_{mieff,LF}/g_{mieff,HF}$	$g_{mieff,LF}$ [$\mu S/\mu m$]	$g_{mieff,HF}$ [$\mu S/\mu m$]
22	20	37	21.3	1.73	868.5	500.0
32	28.7	40	27.3	1.46	877.2	598.7
42	34.5	45.5	29	1.57	936.2	596.7

5.5.4 Gate resistance reduction

Besides a complete or improved silicidation of the polysilicon, two other obvious methods for reducing the gate resistance in the investigated devices are briefly mentioned here:

- *Optimized device design*: First, a further reduction of R_{ge} by a factor of 4 could have easily be obtained by providing a metallic connection to both sides of the polysilicon fingers. For the classical RF multifinger geometry this however requires a multilevel processing. In our case the device fabrication was stopped at Metal 1 to reduce the time and cost of fabrication. The impact of a R_{ge} reduction on f_{max} was illustrated in Figure 5.12a for a device from lot B with W_f=42 nm.

- *Optimized fin pitch design*: Second, another approach to reduce R_{ge} is to decrease the spacing between adjacent fins. Indeed in this region the polysilicon simply acts as a medium for charge transportation and does not actively contribute to the device transconductance. In this respect, e-beam lithography (such as in lot A) can provide much lower spacing than optical lithography, but this expensive approach is not adequate for mass production. An alternative and more promising technique consists in using spacer lithography [17], which is also called *sidewall transfer process* [18]. This technique makes use of spacers at the sidewalls of a sacrificial layer to provide a hard mask. This mask is then used to pattern the fins [17] (Figure 5.17a'-c'). With this approach no fin trimming is required and one every two fin spacings (S_{fin1}) may be made equal to the lithographic spacing (S_L) minus twice the fin width. The other fin spacing (S_{fin2}) is then defined by the lithographic width of the sacrificial fin. When using conventional lithographic fin definition (Figure 5.17a and b), a fin trimming technique must be employed to reduce the fin width to nanoscale dimensions. This contributes to an increase of S_{fin} by twice the thickness of the trimmed layer (Δ_S). Note that the spacer technique also provides a doubling of the number of fins for a given lithographic fin pitch (P_{fin}), thereby doubling the current density for a given layout area.

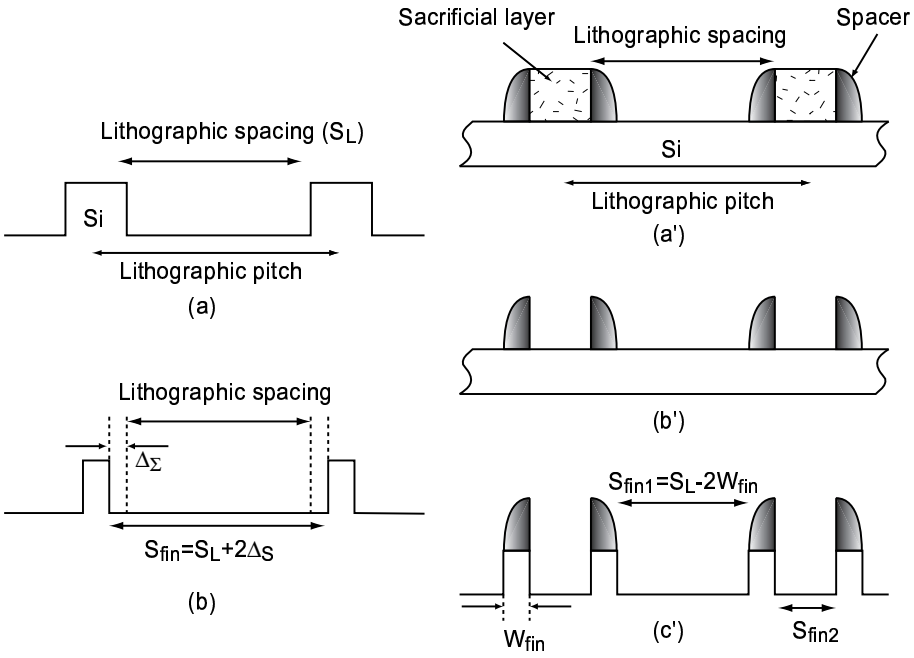


Figure 5.17: Description of fin spacing definition during (a)-(b) an optical lithographic process and (a')-(c') a spacer layer transfer process.

If a spacer layer transfer technique had been used in the case of lot B, the fin spacing could have been easily reduced by a factor of 2 (~150 nm). Though this is still far from the theoretical optimum value (10~15 nm) reported in [53], such a reduction of S_{fin} (while keeping the same number of fins) would have led to a non negligible R_{ge} decrease of roughly 30 %.

5.6 *Parasitic source/drain resistances* - Effect of fin width on RF performance

The important source/drain resistances encountered in FinFET and thin-fin TG devices is an important factor limiting their DC or digital performance since they contribute to a non negligible reduction of the drain current and of the gate transconductance [4, 17]. As was illustrated in Figure 5.6 this parasitic effect is increased for thinner fins due, partly, to the increase of the S/D resistances as the fin cross-section is reduced [32]. Reducing the resistances of the S/D regions is therefore crucial to ensure high performance of TG and FinFET devices. This is currently

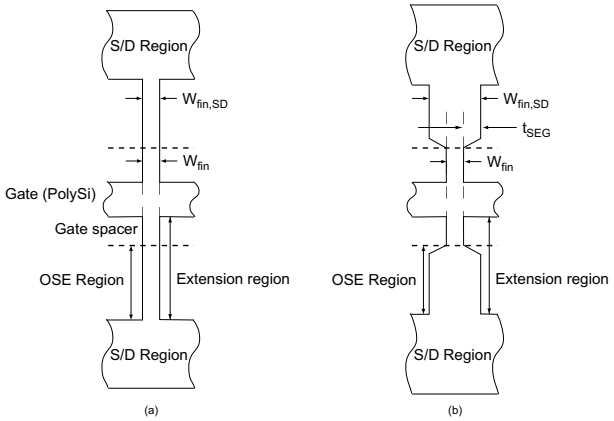


Figure 5.18: Schematic top view of the S/D geometry of the investigated TG devices (a) without and (b) with SEG-raised source and drains. The silicide film is not represented but is assumed to cover the OSE and S/D regions.

achieved using two different techniques.

5.6.1 Reduction of S/D resistances using silicon epitaxy

In this approach, the cross section of the fins is increased by performing a selective epitaxial growth (SEG) on the S/D extensions. This technique has been investigated by many research groups [4, 17, 18] and was used on the investigated devices.

The parasitics R_{se} and R_{de} resistances were extracted from the RF measurements on devices from lot B using the strong inversion method proposed in [48]. These series resistance include the contribution of the following regions (Figure 5.18a): the extensions below the spacers, the extensions between the spacers and the S/D regions (referred here as the *outside-spacer extension* regions or OSE regions), and the S/D silicide region.

Figure 5.19a shows the S/D resistances obtained as a function of the fin width for the devices with (wafer D20) and without (wafer D19) the 40 nm-thick SEG. Please note that the reported fin widths are those measured after the fin patterning and therefore correspond to the physical values in the channel region only. If a uniform SEG can be performed on the whole fin periphery the fin width in the OSE regions is expected to be close to $W_{fin,SD} = W_{fin} + 2t_{SEG}$ where t_{SEG} is the thickness of the epitaxial layer.

The figure clearly highlights the tremendous benefit gained from using a SEG process in the investigated TG devices, especially for thinner fins. The figure also

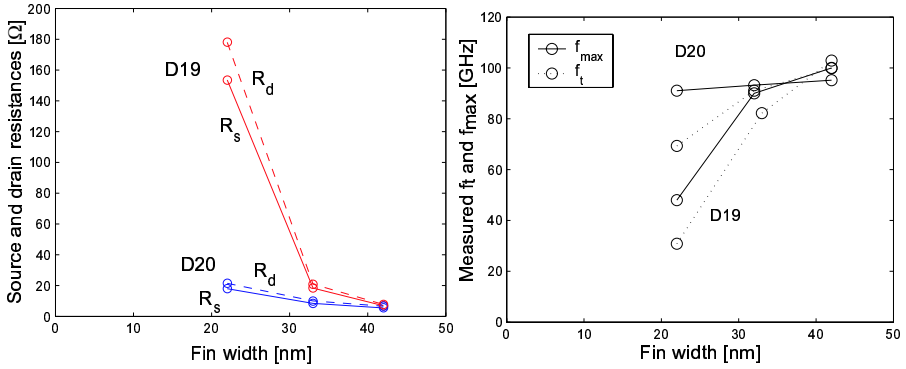


Figure 5.19: Fin width dependence of (a) source and drain resistance and (b) f_t and f_{max} values for the TG devices from lot B.

outlines the strong increase of the S/D resistances as W_{fin} is reduced. This is also true for the devices that received the SEG, for which a 16 % reduction of $W_{fin,SD}$ leads to an increase of R_{se} and R_{de} by a factor close to 3.5! As explained in [32], this large increase may be partially explained by the complex dependence of the total S/D resistance on the fin geometry and process parameters such as the area-dependent Si-NiSi contact resistance.

Another reason for this unexpected resistance rise in the SEG-processed devices could be non uniform or uncomplete deposition of the SEG layer on the periphery of the fins, due to the presence of residual spacers along the fins. These spacers, formed during the gate spacer definition, were shown in [18] to significantly impair the efficiency of the SEG. As reported earlier, the SEM picture presented in Figure 5.9 actually indicates that such spacers were present in the devices from lot A.

The impact of W_{fin} on f_t and f_{max} is illustrated in Figure 5.19b for the devices with and without SEG. In both case the value of f_t is seen to be significantly affected by a fin width reduction. According to Eq. 5.6, this can be partly attributed to an increase of the S/D resistances, which explains why the devices without raised source and drains suffer much more from a W_{fin} reduction. However, another factor can empirically explain the reduction of f_t and f_{max} caused by shrinking the fins: as reported in Table 5.4 a decrease of $g_{mieff,LF}$ is also observed while the input gate capacitance remains roughly unchanged despite a small reduction of W_{tot} (Table 5.3). For frequencies above f_c, Table 5.4 also suggests that the $g_m/(2\pi C_{gin})$ ratio is further reduced for thinner fins because a higher $g_{mieff,LF}/g_{mieff,HF}$ ratio is reported on those devices, indicating a more pronounced loss of gate control at high frequencies.

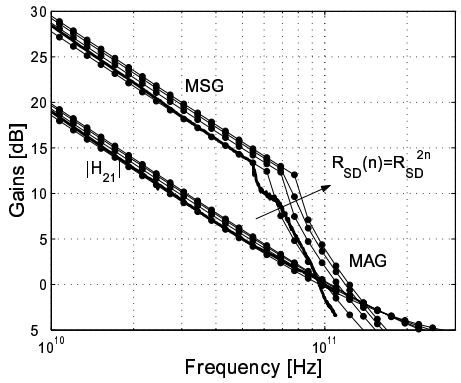


Figure 5.20: Simulated impact of R_{se} and R_{de} on the gain curves of a device from lot B (L_g=60 nm, W_{fin}=42 nm, N_{fin}=50 /finger).

Several reasons can explain the reduced normalized $g_{mieff,LF}$ value reported in Table 5.4 for thinner fins, such as a reduction of the mobility and/or a reduction of the effective gate-source and gate drain voltage due to higher S/D resistances. The main contributor to this observation in the measured devices is still undefined.

5.6.2 Reduction of S/D resistances using low Schottky barrier junctions

An alternative approach to solve the problem of parasitics S/D resistance in multiple gate devices consists in using metallic, or low Schottky barrier (LSB) source and drain extensions. This technique is still under development but has already been successfully implemented on FinFET devices [54, 55]. Another advantage of LSB junctions is the reduction of overlap capacitances due to the limited diffusion of dopants below the gate oxide. In our case it is difficult to accurately predict the reduction of the source and drain resistances that could be expected from using (LSB) junctions, since it merely depends on the contact resistance between the Si and the silicided Si, which is itself critically conditioned by the silicidation process parameters. Figure 5.20 illustrates the theoretical improvements of f_t and f_{max} obtained for the same device as of Figure 5.11 by reducing the parasistic S/D resistances with arbitrary factors (multiples of 2). In this case the value of g_{mi} was kept constant and the impact is seen to be more more pronounced on f_{max} than on f_t.

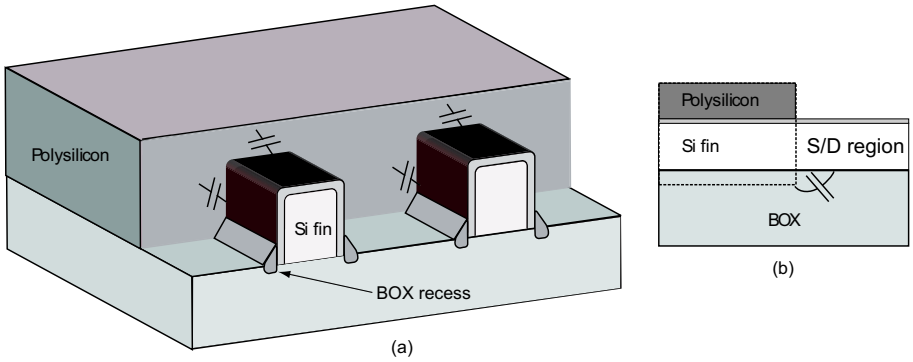


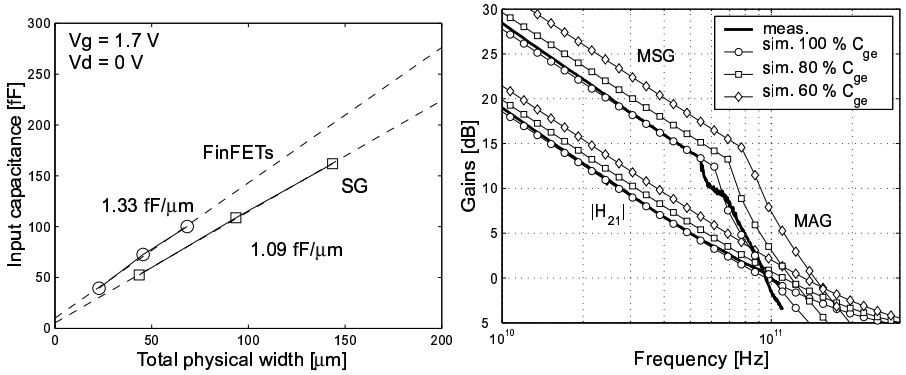
Figure 5.21: Illustration of the parasitic gate fringing capacitances in TG devices at the fin edges: (a) above and (b) inside the BOX.

5.6.3 Parasitic capacitances in TG devices

It is well known that the high frequency performances of RF devices are negatively affected by parasitic capacitances, which are mainly attributed to gate overlaps (C_{gso} and C_{gdo}), gate fringing fields (C_{gsf} and C_{gdf}) and interconnects outside the active area (C_{gsa} and C_{gda}). We neglect here the contributions of C_{gsa} and C_{gda} and as in the previous chapter, we use the following notations for the *extrinsic* capacitances: $C_{gse} = C_{gso} + C_{gsf}$ and $C_{gde} = C_{gdo} + C_{gdf}$. Extrinsic capacitances associated with fringing fields at the edges of the fins are illustrated in Figure 5.21a. Additional fringing taking place in the BOX recess at the fin edges is illustrated in Figure 5.21b.

The input capacitance (C_{gin}) of the investigated TG devices was extracted from the low frequency part of $Im(Y_{11})/(\omega)$ after de-embedding. It is plotted in Figure 5.22a for devices from lot B and is compared to that of single gate devices from the same wafer and with identical gate length. The selected bias was a point in strong inversion (V_g=1.7 V and V_d=0 V) because the single gate devices could not be measured in deep depletion mode due to pronounced short channel effects.

The data are plotted as a function of the device gate width (W_{tot}) and the figure shows that a first order extrapolation of the measured data yields normalized C_{gin} values of 1.33 $fF/\mu m$ for the TG structures and only 1.09 fF per μm of active gate width for the SG device. This indicates a 20 % higher value in the case of the TG MOSFETs. Assuming that the normalized oxide capacitance is equal in both SG and FinFET devices, this increase is solely due to additional fringing effects in FinFETs. Using additional gate-drain capacitance data in strong inversion, the extrinsic gate



(a) (b)

Figure 5.22: (a) Extracted input capacitance of TG and SG devices on wafer D20 from lot B as a function of the total device width, and (b) simulated impact of a reduction of $C_{ge} = C_{gse} + C_{gde}$ on the gain curves of a device from lot B (L_g=60 nm, W_{fin}=42 nm, N_{fin}=50 /finger).

capacitance was actually found to be 50 % higher for the TG MOSFETs.

Such an increase of capacitance in TG devices is obviously related to the three dimensional nature of the fins. 3D Silvaco simulations performed in [15] on both SG and triple gate devices have actually pointed out that this increase was essentially due to additional fringing at the vertical edges of the fins, i.e. above and below (inside the BOX) the fins. These simulations therefore indicated that one way of reducing this parasitic effect could be to increase the H_{fin}/W_{fin} ratio, thus designing taller and thinner fins. Another source of parasitics might also be the polysilicon regions located between the fins that induce extra fringing from the gate to the S/D extensions and also to the BOX. Dissociating the relative contributions of each source requires an extensive investigation using 3D field solvers, which was not performed in this work.

For the simulated device of Figures 5.11 and 5.20, the $C_{gs}/C_{gd} = (C_{gsi} + C_{gse})/(C_{gdi} + C_{gde})$ ratio obtained in saturation was found to be close to 2.1. It is expected that this value could be further improved by fin design optimization. Figure 5.22b illustrates the important f_t and f_{max} improvements that could be expected from reducing the parasitic capacitances by 20 and 40 % and increasing the C_{gs}/C_{gd} ratio to, respectively, 2.3 and 2.7.

5.7 Conclusion

FinFETs and triple gate MOSFETs are known to be promising devices for future IC generations since they appear to provide the best alternatives over bulk CMOS technologies to meet the performance targets set by the ITRS Roadmap in future IC generations. These devices therefore currently constitute a "hot" topic in todays microelectronic industry and have been the subject of numerous investigations. However, almost all of the work reported in the literature has focused on the digital factors of merit of such devices, such as the current density, the I_{on}/I_{off} ratio, the subthreshold slope, the DIBL, ... while only a few have attempted to assess their analogue performance. This chapter has provided for the first time an investigation on the RF properties of sub-100 nm triple gate devices.

The main RF factors of merit considered here were the transition frequencies of the current gain ($|H_{21}|$) and of the maximum available gain (MAG), respectively f_t and f_{max}. The parasitics that affect these factors of merit have therefore been extracted from the RF measurements using a small signal modeling approach. This approach has shown that building the gate stack is a critical issue in FinFETs or triple gate devices, for several reasons.

- First, special care must be used not to leave polysilicon residues in the BOX recess along the fins. These residues do not affect the device DC behaviour but, being directly connected to the gate, they do increase the parasitic gate capacitances and significantly reduce the RF performance of the devices.

- Second, achieving a uniform gate silicidation also presents a major issue in FinFETs or TG structures which are characterized by a major current flow below the vertical gates. To be effective, the gate silicidation must be adapted to the high topography of the fins. Residual spacers along the polysilicon fingers must also be removed to prevent partial silicidation. As the gate resistance strongly affects the value of f_{max} in RF devices, this is a critical point. The gate resistance can also be reduced by decreasing the distance between adjacent fins, which could be achieved using a spacer lithography instead of a classical optical lithography.

- Third, the processing of gate stack consisting in high K+metal+polySi (which is a widely investigated combination for leakage current reduction and V_t tuning) has also proved itself to be a troublesome task, since devices with such gate stack exhibited a loss of gate control above a certain frequency. As this effect was observed on both single gate (SG) and TG devices from the same wafer and was not on devices with SiON+polySi gate stack, it is believed to have been caused by an unknown process irregularity or to be inherent with the gate stack

processing. No literature data could be found over the RF properties of devices with high K/metal gates.

Another particular source of trouble in the design of FinFETs and TG devices is the high S/D resistance, which severely limits the I_{on} in this type of devices. A reduction of the source and drain resistances is classically achieved by performing a selective growth epitaxy (SEG) on the fins by a fin silicidation. In our case, the RF measurements performed on devices with and without SEG clearly outlined the tremendous f_t and f_{max} benefit gained in S/D-raised devices. Besides, the extraction of the S/D resistances on devices with fin widths varying from 22 nm to 42 nm also indicated that a significant R_{se} and R_{de} increase was obtained for thinner fins, leading to a direct degradation of f_t and f_{max}. Thinner fin devices also present an increased control of short channel effects. In that respect, the f_t and f_{max} performance of RF FinFETs and RF TG structures therefore puts a constraint on the minimum allowable fin width. It is however believed that this constraint could be relaxed using metallic S/D regions and low Schottky barrier junctions, which is currently investigated by several research groups.

Finally, the parasitic capacitances associated with gate overlap and gate fringing have also been investigated and compared to those of SG devices of similar gate length and processed on the same wafer. The comparison indicated a 50 % increase of parasitic capacitance for the investigated TG devices. This increase of capacitances can be explained by the 3D configuration of the fins, leading to higher fringing at the top and the bottom of the fins. Another source of additional fringing is the non active polysilicon region located between the fins. It is believed that a 10~20 reduction of these parasitics could be obtained by increasing the fin height and reducing the fin pitch. This might however also lead to an increased complexity of the gate silicidation due to the higher fin topography.

Despite all these difficulties in fabricating highly performant RF FinFET or TG devices, it is worth mentioning that f_t and f_{max} values as high as 100 GHz were recorded for these "unoptimized" devices, providing encouraging results. Additional simulation results displayed in Figure 5.23 illustrate the f_{max} improvements that could be gained by, successively (and additionally), reducing R_{ge} by a factor of 8 (a factor of 4 can easily be obtained by connecting the gate fingers at both sides, an additional factor of 2 could be obtained by improving the gate silicidation or using fully silicide gates), reducing R_{se} and R_{de} by a factor of 2 (anticipating the use of metallic sources and drains) and by considering a 20 % reduction of the fringing capacitances (which could be partially achieved by reducing the fin spacing and/or increasing the fin height). It is seen that for this "golden" transistor a theoretical f_{max} value close to 260 GHz could be achieved. Knowing that for RFIC

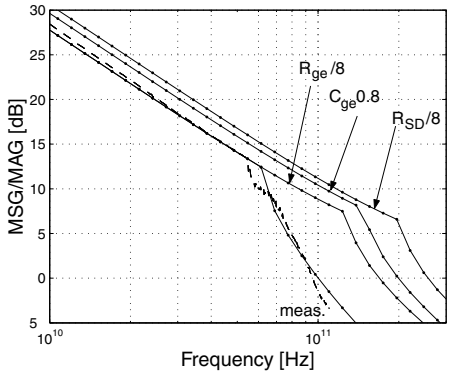


Figure 5.23: Anticipated increase of f_{max} by optimizing the investigated TG structure of lot B.

circuits such as distributed amplifiers the DC gain - bandwith product represents 70~80 % of f_{max} [56], these early measurements tend to show that FinFETs and TG structures are promising devices for future low power RF applications.

References

[1] "Process integration, devices, and structures." [Online]. Available: http://www.itrs.net/Common/2005ITRS/PIDS2005.pdf

[2] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Belland, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," *IEDM Tech. Dig.*, pp. 251–254, 2002.

[3] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," *VLSI Symp.*, 2006.

[4] J. Kedzierski, M. Ieong, E. J. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, "Extension and source/drain design for high performance FinFET devices," *IEEE Trans. Electron Dev.*, vol. 50, no. 4, pp. 942–957, 2003.

[5] L. Mathew, M. Sadd, S. Kalpat, M. Zavala, T. Stephens, R. Mora, S. Bagchi, C. Parker, J. Vasek, D. Sing, R. Shimer, L. Prabhu, G. Workman, G. Ablen, Z. Shi, J. Saenz, B. Min, D. Burnett, B.-Y. Nguyen, J. Mogab, M. Chowdhury, W. Zhang, and J. Fossum, "Inverted T channel FET (ITFET) - fabrication and characteristics of vertical-horizontal, thin body, multi-gate, multi-orientation devices, ITFET SRAM bit-cell operation. a novel technology for 45 nm and beyond CMOS," *IEDM Tech. Dig.*, pp. 713–716, 2005.

[6] J. T. Park and J. P. Colinge, "Multiple gate SOI MOFETs: device design guidelines," *IEEE Trans. Electron Device.*, vol. 49, no. 12, pp. 2222–2229, 2002.

[7] J. P. Colinge, X. Baie, V. Bayot, , and E. Grivei, "A silicon-on-insulator quantum wire," *Solid-State Electron.*, vol. 39, no. 1, pp. 49–51, 1996.

[8] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, and C. Hu, "Sub 50 nm FinFET: PMOS," *IEDM Tech. Dig.*, pp. 67–70, 1999.

[9] Z. Jiao and C. A. T. Salama, "A fully depleted δ-channel SOI nMOSFET„" *Proc. Electrochem. Soc.*, pp. 403–408, 2001.

[10] J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device," *IEDM Tech. Dig.*, pp. 595–598, 1990.

[11] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET," *IEDM Tech.Dig.*, pp. 833–836, 1989.

[12] C. P. Auth and J. D. Plummer, "A simple model for threshold voltage of surrounding-gate MOSFET's," *IEEE Trans. Electron Devices*, pp. 2381–2383, Nov. 1998.

[13] J. T. Park, J. P. Colinge, and C. H. Diaz, "Pi-gate SOI MOSFET," *IEEE Electron Device Lett.*, vol. 22, pp. 405–406, Aug. 2001.

[14] J. P. Colinge, "Novel gate concepts for MOS devices," *Proc. of 34th European Solid-State Device Research Conf.*, pp. 45–49, 2004.

[15] T. M. Chung, A. Kranti, and J.-P. Raskin, "2-D and 3-D wideband simulations of multi-gate SOI MOSFETs," *6th European Conference on ULtimate Integration of Silicon - ULIS 05*, pp. 83,86, 2005.

[16] J. P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electron.*, vol. 48, pp. 897–905, 2004.

[17] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale CMOS spacer FinFET for the terabit era," *IEEE Electron Dev. Lett.*, vol. 23, pp. 25–27, 2002.

[18] A. Kaneko, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, S. Inaba, T. Izumida, T. Kanemura, N. Aoki, K. Ishumaru, H. Ishiuchi, K. Suguro, K. Eguchi, and Y. Tsunashima, "Sidewall tranfer process and selective gate sidewall spacer formation technology and for sub-15 nm FinFET with elevated source/drain extension," *Dig. of IEDM*, pp. 844–847, 2005.

[19] J. Kedzierski, D. M. Fried, E. J. Nowak, T. Kanarsky, J. Rankin, H. Hanafi, W. Natzle, D. Boyd, Y. Zhang, R. Roy, J. Newbury, C. Yu, Q. Yang, P. Saunders, C. Willets, A. Johnson, S. Cole, H. Young, N. Carpenter, D. Rakowski, B. A. Rainey, P. Cottrell, M. Ieong, and P. Wong, "High performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," *IEDM Tech. Dig.*, pp. 437–440, 2001.

[20] D. Woo, B. Y. Choi, W. Y. Choi, M. W. Lee, J. D. Lee, and B.-G. Park, "30 nm self-aligned FinFET with large source/drain fan-out structure," *Electronics Letters*, vol. 39, no. 15, pp. 1154–1155, 2003.

[21] Y. Liu, K. Ishii, T. Tsutsumi, L. Masahara, and E. Suzuki, "Ideal rectangular cross-section si-fin channel double-gate MOSFETs fabricated using orientation-dependent wet etching," *IEEE Electron Dev. Lett.*, vol. 24, no. 7, pp. 484–487, 2003.

[22] W.-S. Liao, C.-N. Wu, S.-S. Chen, C.-R. Hsu, and W.-T. Shiau, "A novel high aspect ratio FinFET with cobalt fully silicided gate structure," *Symp. VLSI Tech.*, pp. 114–115, 2005.

[23] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, and E.-C. Kan, "Finfet design considerations based on 3-d simulation and analytical modeling," *IEEE Trans. Electron Devices.*, vol. 49, no. 8, pp. 1411–1419, 2002.

[24] M. Kondo, R. Katsumata, A. Hideaki, T. Hamamoto, S. Ito, N. Aoki, and T. Wada, "A FinFET design based on three-dimensional process and device simulations," *International Conference on Simulation of Semiconductor Processes and Devices*, pp. 179–182, 2003.

[25] X. Wu, P. Chan, and M. Chan, "Impacts of nonrectangular fin cross section on the electrical characteristics of FinFET," *IEEE Trans. Electron Dev.*, vol. 52, no. 1, pp. 63–68, 2003.

[26] J.-W. Yang and J. Fossum, "On the feasibility of nanoscale triple-gate CMOS transistors," *IEEE Trans. Electron Dev.*, vol. 52, no. 6, pp. 1159–1165, 2005.

[27] D.-S. Woo, J.-H. Lee, W. Y. Choi, B.-Y. Choi, Y.-J. Choi, J. D. Lee, and B.-G. Park, "Electrical characteristics of FinFET with vertically nonuniform source/drain profile," *IEEE Trans. Nanotech.*, vol. 1, no. 4, pp. 233–237, 2002.

[28] V. Kilchytska, N. Collaert, R. Rooyackers, D. Lederer, J.-P. Raskin, and D. Flandre, "Perspective of FinFETs for analog applications," *Proc. of 33th European Solid-State Device Research Conf.*, pp. 65–68, 2003.

[29] N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, W.-C. Lee, T. J. King, J. Bokor, and C. Hu, "Sub-60-nm quasi-planar FinFETs fabricated using a simplified process," *IEEE Electron Dev. Lett.*, vol. 22, pp. 487–489, 2001.

[30] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Dev. Lett.*, vol. 24, pp. 263–265, 2003.

[31] M. Yang, "High performance CMOS fabricated on hybrid substrate with different crystal orientations," *IEDM Tech. Dig.*, pp. 453–456, 2003.

[32] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. D. Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs," *IEEE Trans. Electron Dev.*, vol. 52, no. 6, pp. 1132–1140, 2005.

[33] M. Dehan, "Characterization and modeling of SOI RF integrated components," Ph.D. dissertation, UCL, Louvain-la-Neuve, Belgium, 2003.

[34] R. Valentin, A. Siligaris, G. Pailloncy, E. Dubois, G. Dambrine, and F. Danneville, "Influence of gate offset spacer width on SOI MOSFETs HF properties," *6th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 77–80, 2006.

[35] C. Chen, S. J. Spector, R. M. Blumgold, R. A. Neidhard, W. T. Beard, D.-R. Yost, J. Knecht, C. K. Chen, M. Fritze, C. L. Cerny, J. A. Cook, P. W. Wyatt, and C. L. Keast, "High-performance fully-depleted SOI RF CMOS," *IEEE Electron Device Lett.*, vol. 23, no. 1, pp. 52–54, 2002.

[36] L. F. Tiemeijer, H. Boots, R. Havens, A. Scholten, P. de Vreede, P. Woerlee, A. Heringa, and D. B. M. Klaassen, "A record high 150 GHz f_{max} realized at 0.18 µm gate length in an industrial RF-CMOS technology," *IEDM Technical Dig.*, pp. 10.4.1–10.4.4, 2001.

[37] N. Zamdmer, A. Ray, J.-O. Plouchart, L. Wagner, N. Fong, K. A. Jenkins, W. Jin, P. Smeys, I. Yang, G. Shahidi, and F. Assaderghi, "A 0.13-μm SOI CMOS technology for low-power digital and RF applications," *Symp. on VLSI Technology*, pp. 85–86, 2001.

[38] M. Vanmackelberg, S. Boret, D. Gloria, O. Rozeau, R. Gwoziecki, C. Raynaud, S. Lepilliet, and G. Dambrine, "90 nm SOI-CMOS of 150 GHz f_{max} and 0.8 db nf_{min} at 6 ghz for SOC," *Proc. of IEEE International SOI Conf.*, pp. 153–154, 2002.

[39] T. Matsumoto, S. Maeda, K. Ota, Y. Hirano, K. Eikyu, H. Sayama, T. Iwamatsu, K. Yamamoto, T. Katoh, Y. Yamaguchi, T. Ipposhi, H. Oda, S. Maegawa, Y. Inoue, and M. Inuishi, "70 nm SOI-CMOS of 135 GHz fmax with dual offset-implanted source-drain extension structure for RF/analog and logic applications," *IEDM Technical Dig.*, pp. 10.3.1–10.3.4, 2001.

[40] H. Momose, E. Morifuji, T. Yoshitomi, T. Ohguro, M. Saito, and H. Iwai, "Cut-off frequency and propagation delay time of 1.5-nm gate oxide CMOS," *IEEE Trans. Electron Dev.*, vol. 48, no. 6, pp. 1165–1174, 2001.

[41] S. Narasimha, A. Ajmera, H. Park, D. Schepis, N. Zamdmer, K. Jenkins, J.-O. Plouchart, W.-H. Lee, J. Mezzapelle, J. Bruley, B. Doris, J. W. Sleight, S. Fung, S. Ku, A. Mocuta, I. Yang, P. Gilbert, K. Muller, P. Agnello, and J. Welser, "High performance sub-40 nm CMOS devices on SOI for the 70 nm technology node," *IEDM Technical Dig.*, pp. 29.2.1–29.2.4, 2001.

[42] S. Lee, L. Wagner, B. Jagannathan, S. Csutak, J. Pekarik, N. Zamdmer, M. B. R. Ramachandran, and G. Freeman, "Record RF performance of sub-46 nm l_{gate} NFETs in microprocessor SOI CMOS technologies," *IEDM Tech. Dig.*, pp. 241–244, 2005.

[43] N. Collaert, S. Brus, A. D. Keersgieter, A. Dixit, I. Ferain, M. Goodwin, A. Kottantharayil, B. Rooyackers, P. Verheyen, Y. Yim, P. Zimmerman, S. Beckx, B. Degroote, M. Demand, M. Kim, E. Kunnen, S. Locorotondo, G. Mannaert, F. Neuilly,

D. Shamiryan, C. Baerts, M. Ercken, D. Laidlcr, F. Leys, R. Loo, J. Lisoni, J. Snow, R. Vos, W. Boullart, I. Pollentier, S. D. Gendt, K. D. Meyer, M. Jurczak, and S. Biescmans, "Integration challenges for multi-gate devices," *Int. Conf. on Integrated Circuit Design and Tech.*, pp. 187–194, 2005.

[44] N. Collaert, M. Demand, I. Ferain, J. Lisoni, R. Singanamalla, P. Zimmerman, Y. S. Yim, T. Schram, G. M. M. Goodwin, J. Hooker, F. Neuilly, M. Kim, K. D. Meyer, S. D. Gendt, W. Boullart, M. Jurezak, and S. Biesemans, "Tall triple-gate devices with tin/hfo_2 gate stack," *Symp. on VLSI Tech.*, pp. 108–109, 2005.

[45] B. Tavel, T. Skotnicki, G. Pares, N. Carriere, M. Rivoire, F. Leverd, C. Julien, J. Torres, and R. Pantel, "Totally silicided (CoSi2) polysilicon:a novel approach to very low resistive gate without metal CMP or etching," *IEDM Tech. Dig.*, pp. 825–828, 2001.

[46] J. Kedzierski, D. Boyd, P. Ronsheim, S. Zafar, J. Newbury, C. C. Jr., M. Ieong, and W. Haensch, "Threshold voltage control in NiSi-gated MOSFETs through silicidation induced impurity segregation (SIIS)„" *IEDM Tech. Dig.*, pp. 315–319, 2003.

[47] J. Kedzierski, D. Boyd, Y. Zhang, M. Steen, F. F. Jamin, J. Benedict, M. Ieon, and W. Haensch, "Issues in $nisi$-gated FDSOI device integration," *IEDM Tech. Dig.*, pp. 18.4.1–18.4.4, 2005.

[48] A. Bracale, V. Ferlet-Cavrois, N. F. D. Pasquet, J. L. Gautier, J. L. Pelloie, and J. du Port de Poncharra, "A new approach for SOI devices small-signal parameters extraction," *Analog Integrated Circuits and Signal Processing*, vol. 25, no. 2, pp. 157–169, 2000.

[49] B. Razavi, R.-H. Yan, and K.-F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits and Systems*, vol. 41, no. 11, pp. 750–754, 1994.

[50] M. Jurczak, M. de Potter, R. Rooyackers, W. Jeamsaksiri, A. Redolfi, L. Grau, A. Lauwers, R. Lindsay, I. Peytier, E. Augendre, and G. Badenes, "Elevated co-silicide for sub-100nm high performance and RF CMOS," *Proc. of 32th European Solid-State Device Research Conf.*, pp. 311–314, 2002.

[51] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker, and J.-P. Colinge, "Accurate SOI MOSFET characterizaton at microwave frequencies for device performance optimization and analog modeling," *IEEE Trans. on Electron Devices*, vol. 45, no. 5, pp. 1017–1025, 1998.

[52] S. Bieseman, "Perspective on emerging devices and impact on scaling technologies," *Proceeding of the 4th COE Workshop*, Hi-

roshima, 2005. [Online]. Available: $http://www.rcns.hiroshima-u.ac.jp/21coe/pdf/4th\_WS/plenary-p14.pdf$

[53] W. Wu and M. Chan, "Gate resistance modeling of multi-fin MOS devices," *IEEE Electron Dev. Lett.*, vol. 27, pp. 68–70, 2006.

[54] C. Chen, S. J. Spector, R. M. Blumgold, R. A. Neidhard, W. T. Beard, D.-R. Yost, J. Knecht, C. K. Chen, M. Fritze, C. L. Cerny, J. A. Cook, P. W. Wyatt, and C. L. Keast, "High-performance P-channel Schottky-barrier SOI FinFET featuring self-aligned PtSi Source/Drain and electrical junctions," *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 102–104, 2003.

[55] B.-Y. Tsui and C. P. Lin, "Process and characteristics of modified Schottky barrier (msb) p-channel FinFETs," *IEEE Trans. Electron Device*, vol. 52, no. 11, pp. 2455–2462, 2005.

[56] J. Beyer, S. N. Prasad, R. C. Becker, J. E. Nordman, and G. K. Hohenwarter, "MESFET distributed amplifier design guidelines," *IEEE Trans. Microwave Theory Tech.*, vol. 32, no. 3, pp. 268–275, 1984.

CHAPTER 6
CONCLUSION

This work contributes to the assessment of the performance of the SOI technology for current and future analogue/RF applications. The investigation was performed in the context of both *passive* and *active* device integration. In Chapters 2 and 3, the investigation performed on *passive* devices mainly focused on the evaluation of the *substrate performance*, which largely determines that of passive devices such as transmission lines and inductors. This investigation confirmed that a substantial enhancement of the device electrical characteristics can be obtained by using high resistivity (HR) substrates instead of standard resistivity (ρ_{Si}=20 $\Omega.cm$) substrates. However, the major part of the work showed that the *effective* resistivity (ρ_{eff}) of HR SOI wafers can be strongly affected by parasitic conduction at the substrate surface, and that, in general, the value of ρ_{eff} is at least one order of magnitude lower than the nominal wafer resistivity ($\simeq$ 10 kΩ.cm). This generates additional losses in the substrate and, strictly speaking, the wafers can no longer be considered as lossless despite what could have been hoped by using such a type of substrate. In particular noticeable increases in CPW line losses and crosstalk level were observed on the non-passivated HR SOI wafers. Line losses can be reduced by stacking higher numbers of metal levels, but crosstalk issues are expected to even worsen in future generations of SOI wafers for which a reduction of the BOX thickness is envisaged in order to reduce self heating and short channel effects [1]. BOX thickness reduction in combination with parasitic substrate conduction (PSC) in HR SOI wafers might also lead to an increase of undesired S/D coupling in short length devices. Such coupling is known to increase the device output conductance [2], thereby altering their performance for analogue/RF applications.

From a substrate engineer point of view, the high performance of HR SOI wafers can therefore still be further improved. This point was thoroughly investigated in Chapter 3, in which a cost effective, CMOS compatible and efficient optimization pathway was demonstrated. The proposed method is based on a passivation of the substrate surface with RTA-crystallized silicon, which completely prevents PSC. Compared to literature data, this technique was proved to be the only one that simultaneously combines a high passivation efficiency, a high thermodynamic stability and a high compatibility with the UNIBOND SOI wafer fabrication process. An outcome of this investigation is that substrate-passivated HR SOI wafers fully recover their nominal value of substrate resistivity (i.e. $\simeq$ 10 kΩ.cm) and can there-

fore be considered as lossless. This makes substrate-passivated HR SOI wafers highly competitive with regards to more exotic (and more expensive) dielectric substrates, such as fused silica, which are often used for RF applications. Preliminary testings also tend to indicate that for substrate-passivated HR SOI wafers active SOI devices do not suffer from the presence of the underlying polySi layer. Further work in this direction should however be performed to test the full compatibility of polySi substrate-passivted HR SOI wafers with complete CMOS process schemes.

At an *active* device level, the work presented in this thesis intensively used a small signal approach to provide wideband device characterization. The investigation was performed on both partially depleted (PD) SOI MOSFETs and fully depleted (FD) triple gate (TG) SOI MOSFETs in Chapters 4 and 5, respectively.

The work presented in Chapter 4 showed that the dynamic behaviour of the gate-induced floating body effect in PD SOI devices, which is caused by gate tunneling current in sub 250 nm CMOS technologies, presents large similarities with that of the well-known kink effect. As a consequence both mechanisms can be treated the same way from a small signal point of view and a unified small signal model that includes the body node was proposed to account for both effects. An accurate determination of the body-related parameters therefore proved to be crucial for a correct frequency modeling of those mechanisms. In this respect wideband multiport VNA measurements, as performed in this work for the first time on 3-port body-contacted RF PD SOI MOSFETs, were shown to provide a cost and time effective tool to completely describe the body parameters, including both intrinsic and (some being bias-dependent) extrinsic parameters. This allowed for instance an accurate extraction of the body resistance, including both the contribtions from the active zone and that of the active zone extensions. In the case of dynamic threshold (DT)MOSFETs, the small signal modeled and the measurements also demonstrated that the DC gain in transconductance obtained by connecting the body to the gate is actually lost at frequencies higher than 1-2 GHz due to the high value of the body resistance and a loss of control of the AC body potential. This also leads to a similar increase in device output conductance but does not affect the device cut-off frequencies, namely f_t and f_{max} (data not shown here). More efficient body contacts (i.e., of lower resistitivity) would help increase the frequency range throughout which the higher performance of the DTMOSFETs is preserved. This might make them strong candidates for RF applications in the largely exploited 2.5 GHz range.

In Chapter 5, the RF performance of *multiple gate* SOI MOSFETs, which form the future of the 2005 ITRS Roadmap, was investigated for the first time. The AC

analysis showed that fabricating high quality RF triple gate devices is more complex than in the case of planar devices, which is essentially due to the 3D nature of the MUGFETs. The analysis pointed out the silicidation of the polysilicon gate fingers as well as that of the source and drain extensions as the major technological issues directly affecting their RF characteristics. Compared to planar devices, additional parasitic fringing was also found to reduce the device cut off frequencies. However, it is to be noted that despite those issues the investigated 50 nm-long devices outlined cut-off frequencies on the order of 100 GHz. It is expected that by proper process (such as the use of FUSI gates and several metal layers) and device geometry (such as a reduction of the fin spacing) optimization cut-off frequencies higher than 200 GHz could be obtained making such devices promising contenders for mixed signal RF applications.

To conclude, the work performed in this thesis also showed that (1) *AC* and (2) *wideband* measurements along with small signal modeling are essential to achieve accurate device characterization and assist device processing:

1. In the context of technology and device development, *AC* measurements provide complementary information compared to DC data. Numerous examples can be found in this sense, especially in Chapter 5 of this work. For instance, the additional parasitic capacitances formed by polysilicon residues along the fins in the studied TG structures do not affect the DC device characteristics and therefore could not have been identified by DC measurements only. In a similar way, the noticeable reduction of the gate transconductance occurring in the several hundreds of MHz range for devices with a metal gate/high-k gate stack clearly pointed out some technological issue(s) at the gate, probably related to the complex gate stack of those devices. This issue could not have been pointed out by purely DC measurements either. In Chapter 3, multiport RF measurements applied to body-contacted PD SOI devices have also provided data that could not have been obtained using DC measurements. In fact, these 3-port measurements enabled for the first time a complete small signal modeling of body-contacted SOI MOSFETs including the parasitic effects of the non perfect body resistance.

2. Still in the context of technology and device development, *wideband* measurements can in certain cases prove themselves as a substantial source of information. As outlined in the different chapters of this work, effects impacting on the electrical behaviour of active and passive SOI devices are characterized by very distinct time constants and associated cut-off frequencies, such as 1 Hz-10 kHz (floating body effects in floating body partially depleted SOI MOSFETs), ~10 MHz

(self heating effects in SOI MOSFETs, not reported in this work), 100 MHz-1 GHz (loss of body voltage control in body-contacted SOI MOSFETs), ~1 GHz (dielectric relaxation in HR SOI substrates suffering from parasitic surface conduction), ≥100 GHz (f_t and f_{max} values of current Si-based RF technologies)... It is clear that this list is not exhaustive and it is expected that new phenomena, with their own characteristic frequencies, will affect the behaviour of new devices in next IC generations.

Thus, in all cases, a small signal characterization based on wideband measurements helps identifying and understanding the origin of the mechanisms occurring in the studied devices. This also suggests that, by providing technological feedbacks to process engineers, using AC measurements and AC characterization in parallel with DC measurement at early stages of transistor development can largely facilitate the fabrication and integration of new devices. In our case, this win-win approach was successfully applied from the very start of FinFET device development at IMEC and in the frame of an IMEC-UCL collaboration.

References

[1] "Front end processes." [Online]. Available: http://www.itrs.net/Common/2005ITRS/FEP2005.pdf

[2] V. Kilchytska, D. Levacq, D. Lederer, J.-P. Raskin, and D. Flandre, "Floating effective back gate effects on the small-signal output conductance of SOI MOSFETs," *Electron Device Letters*, vol. 24, pp. 414–416, 2003.