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High-resistivity with PN interface passivation in 22 nm FD-SOI technology for low-loss passives at RF and millimeter-wave frequencies

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ABSTRACT

In this paper, GlobalFoundries' 22 nm fully depleted (FD) silicon-on-insulator (SOI) process is run on standard and high-resistivity wafers with a specially designed PN junctions interface passivation solution to counteract parasitic surface conduction (PSC) effects. Substrate quality is evaluated at RF and mm-wave frequencies through the on-wafer measurements of a set of passives: coplanar waveguides (CPW) lines, two inductors and a crosstalk structure. The effective resistivity (ρ_{eff}), losses and harmonics generated by the substrate are monitored based on CPW lines measurements, fabricated in either bottom or top metal layers. Several PN patterns are examined and they demonstrate effective passivation of the PSC, enabling ρ_{eff} values in the kΩ.cm range (up to ~6 GHz) and > 100 Ω.cm up to ~60 GHz. Patterns with intrinsic region separating the P- and N- doping regions show better performance, which can further be improved applying a reverse PN bias to widen the depletion regions. 50 Ω CPW line designed with PN interface passivation achieves 0.22 dB/mm lower propagation losses at 50 GHz than 50 Ω thin-film microstrip line in this technology. Impact of substrate quality on two spiral inductors is analyzed by comparing substrates with standard resistivity, high-resistivity with PSC and high-resistivity with PN junction solution. The high-resistivity substrate with PN junction solution shows an up to 62% and 15% increase in quality factor with respect to the standard substrates for the 5–20 GHz and 30–60 GHz inductors, respectively. Finally, measurements of a crosstalk structure show a strong isolation improvement in crosstalk through the substrate with the PN interface passivation solution.

1. Introduction

Nowadays, advanced CMOS nodes are competitive for radio-frequency (RF) and millimeter-wave (mm-wave) applications. In particular, fully depleted silicon-on-insulator (FD-SOI) devices feature transistor cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) metrics in the range of 300 to 400 GHz [1]. Recent CMOS technologies targeting mm-wave applications typically offer rich back-end-of-line options with several thick metal layers, enabling high-Q RF/mm-wave passives and interconnects.

In general, the silicon substrate is part of the electromagnetic environment of such passives and devices, with a potentially strong impact on their high-frequency behavior. The substrate can be responsible for significant amounts of losses, coupling and non-linear signal distortion [2] if the silicon resistivity is low.

High-resistivity (HR) silicon substrate (with nominal resistivity ρ_{nom} > 1 kΩ.cm) improves these effects compared with standard resistivity silicon (ρ_{nom} = 10 to 20 Ω.cm), though the benefits are hindered by the *parasitic surface conduction* (PSC) effect. A PSC layer is induced by fixed positive charges at the Si/SiO_2 interface that attract significant amounts of free electrons, forming a thin and highly conductive layer [3,4]. The PSC effect deteriorates (decreases) the *effective resistivity* (ρ_{eff}) sensed by coplanar circuitry overlying the Si-substrate stack.

Several interface passivation solutions have then been developed to counter the PSC layer, the most widespread of which is the *trap-rich* solution. In trap-rich substrates, a thin layer of polysilicon is created between the SiO_2 and Si, that is rich in defects that trap free carriers and yields the highly resistive interface [4]. Despite its strong industrial

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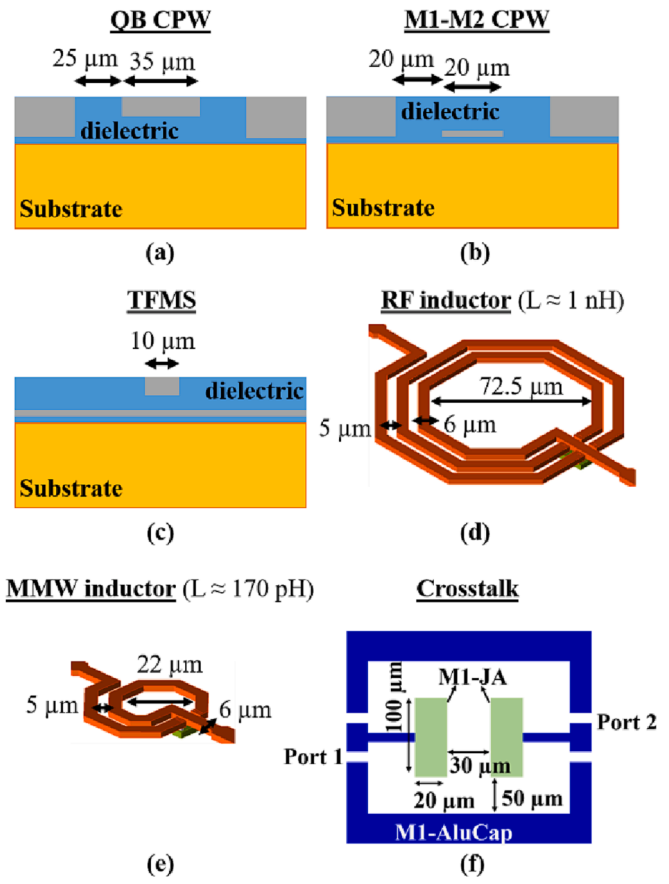
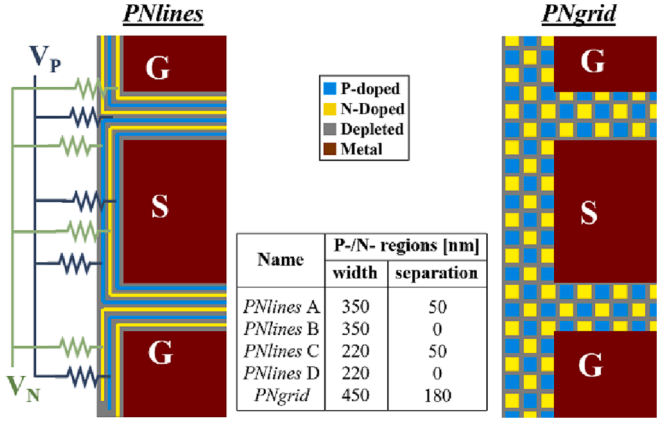


Fig. 1. Sketches along with main dimensions of all passive structures fabricated and characterized in this paper: (a), QB CPW, (b) M1-M2 CPW, (c) TFMS, (d) RF inductor, (e) MMW inductor, (f) Crosstalk structure.



Name	P-/N- regions [nm]	
	width	separation
PNlines A	350	50
PNlines B	350	0
PNlines C	220	50
PNlines D	220	0
PNgrid	450	180

Fig. 2. Sketch and dimensions of designed PN passivation patterns: *PNlines* (left) and *PNgrid* (right).

success in in PD-SOI nodes [2], its transposition to FD-SOI technologies is not straightforward and there are no trap-rich options available for the moment, thus motivating the development of alternative interface passivation schemes.

The *PN interface passivation* technique is then particularly of interest for FD-SOI. By implanting alternating regions of P- and N-type dopants close to the lower Si/SiO2 interface, the PSC layer is interrupted locally by induced depletion junctions. The series combination of low resistivity (N- and P-doped) and high resistivity (depletion junction) regions result in a strong increase in overall substrate RF impedance (ρ_{eff}). This

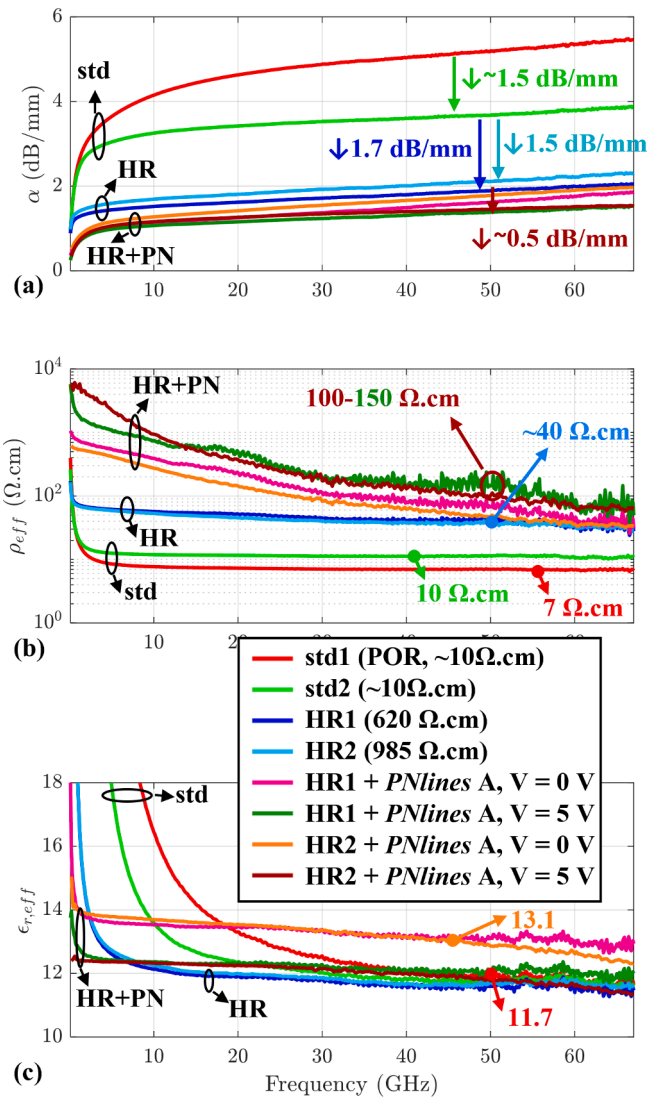


Fig. 3. Propagation losses (a), and substrate parameters: effective resistivity (b) and permittivity (c), from M1-M2 CPW line measurements.

passivation solution was first described in [5,6], though in those works the lithography resolution was limited by the university laboratory equipment to 1 µm. Still, the ρ_{eff} of measured CPW lines was shown to be increased from a few tens of Ω.cm on a HR substrate (with PSC) to around 1 kΩ.cm. Then, the same interface passivation scheme was tested in a short-loop process with better lithography (smaller features) resulting in improved RF performance [7,8]. In [9,10], the *PN interface passivation* solution is applied within the industrial GlobalFoundries' 22FDX® line run on standard and HR SOI wafers provided by Soitec.

In this paper, we analyze in detail the effect of different PN passivation patterns designed and fabricated in the same run as in [9–11] on several passive structures. This paper is structured as following: Section 2 describes the fabricated passives and PN patterns. Then, the substrate RF performance and the *PN interface passivation* solution are evaluated on the behavior of several passives across Sections 3 to 5. Section 3 presents results of coplanar waveguide (CPW) lines, in terms of substrate losses (described by the effective resistivity, ρ_{eff}) and non-linearity. Section 4 presents quality factors of spiral inductors. Finally, Section 5 analyzes crosstalk through the substrate between adjacent pads.

2. Fabricated structures

Several passives and PN passivation patterns are designed. Each

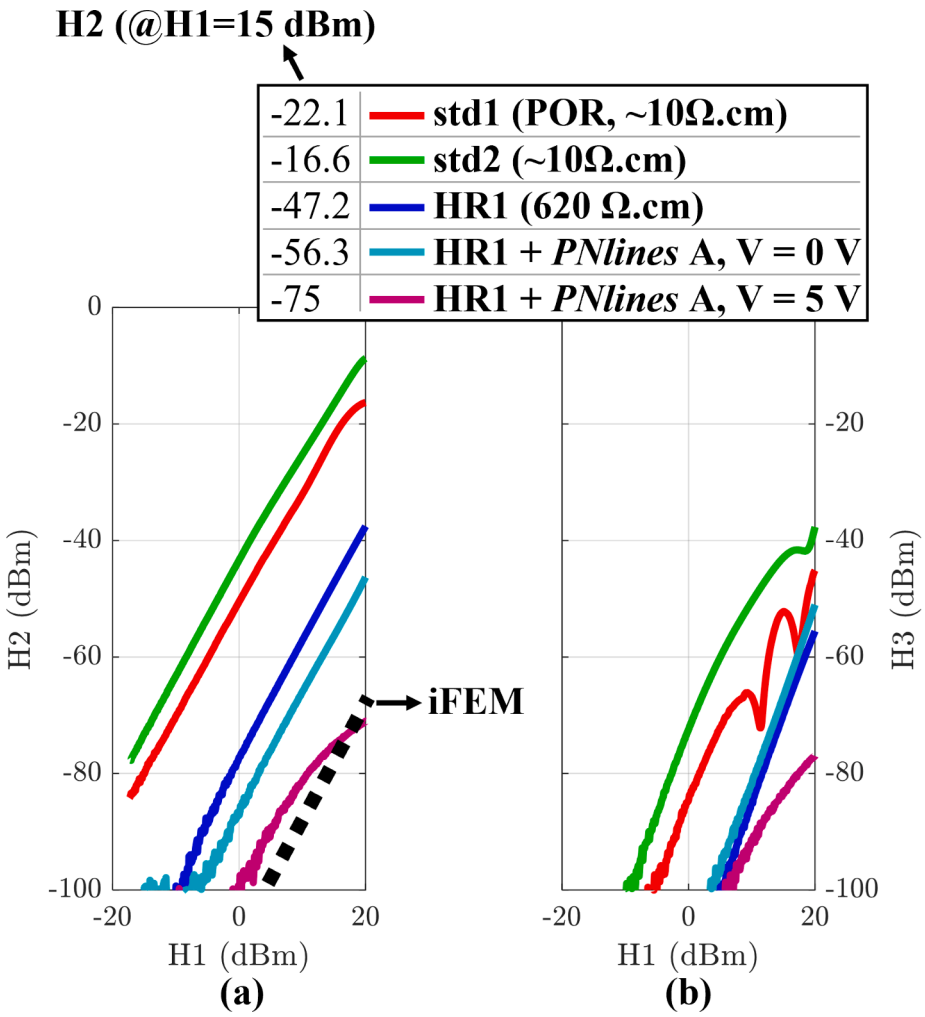


Fig. 4. Substrate non-linearity benchmark. Measured second (a) and third harmonic (b) levels versus power at fundamental of the output signal propagating in a 2 mm-long M1-M2 CPW line on different substrates. The H2 levels at H1 = 15 dBm are reported in the legend. Estimated harmonic distortion for the same CPW lines on a iFEM™ substrate, in thick, black, dashed lines.

passive is replicated several times to include different PN passivation patterns, and are fabricated in the industrial GlobalFoundries' 22FDX® line run on 4 wafers of different resistivities: two wafers around 10 Ω.cm (std1 and std2) – the process of record (POR) corresponding to std1 – 620 Ω.cm (HR1) and 985 Ω.cm (HR2). All the wafers include a BOX and are thus subject to PSC, even though it is only a strong problem for high-resistivity substrates for which the highly-resistive-bulk-associated improvements are hindered.

2.1. Passive structures

The first set of CPW lines is designed in the last Cu layer "QB" (3 μm thick and approximately 10 μm away from the Si substrate) and has a signal line width w of 35 μm, and a signal to ground spacing s of 25 μm (Fig. 1(a)). The second set of CPW lines is formed in stacked M1 and M2 (combined thickness of 0.17 μm, and approximately 130 nm from the Si substrate) using w = 20 μm and s = 20 μm (Fig. 1(b)). Additionally, a set of thin film microstrip lines (TFMS) is designed with the signal line width of 10 μm implemented in QB, ground plane in the 5 thin bottommost metal layers stacked for a combined thickness of ~400 nm at a distance of approximately 9 μm below the signal line (Fig. 1(c)). The CPW and TFMS lines dimensions are selected to have a 50 Ω characteristic impedance (Z_c) for a meaningful performance comparison. Lines of multiple lengths (760 μm and 2000 μm) are fabricated, along with dedicated Open and Thru structures, to enable a wideband multi-Through-Reflect-Line (mTRL) calibration and extraction of the line's equivalent RLGC parameters [12].

Two inductors are also designed, targeting different operating frequencies: 5–20 GHz (called RF inductor) and 30–60 GHz (called MMW inductor). These inductors are designed on the QB layer. A sketch of the inductors and their geometrical dimensions are presented in Fig. 1(d) and (e). The dummy fills are minimized to avoid degrading the inductor quality factors.

A crosstalk structure is designed as two pads, stacking the bottommost 8 metal layers (M1 to JA), facing each other with a width of 20 μm, length of 100 μm and spacing of 30 μm as reported in Fig. 1(f).

2.2. PN interface passivation patterns

Two types of PN passivation patterns are designed and presented in this paper: (i) *PNlines* and (ii) *PNgrid*. They are both represented in Fig. 2, and serve to increase the impedance between two terminals through the substrate (for instance the S and G lines of the CPW by impeding the E-field path between these with multiple highly-resistive depletion regions). The *PNlines* pattern includes a DC biasing option through on-chip high-valued resistor elements. This allows for the reverse DC biasing of the PN junctions, to widen the depletion regions and further increase the substrate impedance. Out of the *PNlines* type solution, four different patterns are obtained: (i) different P-/N-doped region widths, (ii) presence of an intrinsic region between the P-/N-doped regions or not. Small

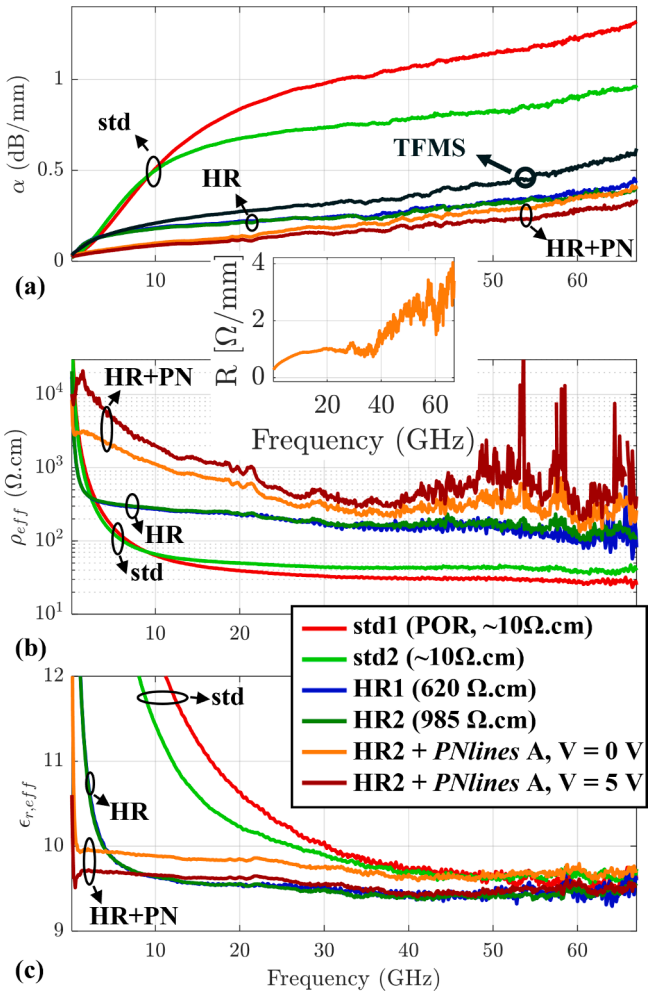


Fig. 5. Substrate parameters: effective resistivity (a) and permittivity (b), from M1-M2 CPW line measurements on 985 Ω.cm high-resistivity substrate with different PN pattern designs. The measurements in this figure are noisier than in Fig. 3, because only 760 μm-long CPW lines and thru lines are available for the different PN patterns to save test chip area.

dimensions are used to define the patterns in compliance with the process design rules (Fig. 2).

3. RF performance results – Transmission lines

The transmission line measurements are first corrected by a Line-Reflect-Reflect-Match (LRRM) calibration performed on an impedance standard substrate (ISS). Then, pads are de-embedded and the line's equivalent RLGC parameters are extracted based on the multi-line Thru-Reflect-Line (mTRL) method explained in [12].

3.1. CPW in M1-M2

Fig. 3 shows the total transmission losses (α), the substrate effective resistivity (ρ_{eff}) and the substrate effective permittivity (ε_{eff}) extracted from the M1-M2 CPW lines on different substrates. As expected, the effective resistivity and permittivity of the standard resistivity substrates reach $\rho_{eff} = 7$ and 10 Ω.cm, for std1 and std2, respectively, and $\varepsilon_{r,eff} \approx 11.7$ (the underneath stack includes a thin layer of oxide and a 152 μm-thick substrate), beyond the slow-wave mode cut off frequency f_{sw} (>40 and 30 GHz for std1 and std2, respectively). The 985 Ω.cm (HR2) and 620 Ω.cm (HR1) high-resistivity substrates without any interface passivation suffer from PSC effects, featuring an effective resistivity of 36 and 42 Ω.cm (at 50 GHz), representing an improvement of 1.5 and 1.7 dB/mm in α, respectively, with respect to the standard resistivity substrate (std2). It is interesting to note how a small absolute variation in ρ_{eff} (from 7 to 10 Ω.cm) among the std1 and std2 substrates leads to strong additional losses in the M1-M2 CPW lines: +1.5 dB/mm in α at all frequencies above f_{sw} (>40 GHz) from std2 to std1; whereas the difference of ρ_{eff} (from 36 to 42 Ω.cm) in HR1 and HR2 leads only to ~0.2 dB/mm of difference in transmission losses. The reason is that the rather large relative variation of ρ_{eff} among the std1 and std2 substrates significantly reduces the substrate losses that are much larger for a ρ_{eff} ~ 10 Ω.cm effective substrate than a ~ 40 Ω.cm effective substrate.

Fig. 3 also shows that the *PNline* pattern (A) effectively solves the PSC issue and retrieves high values of effective resistivity (~300–1000 Ω.cm at 10 GHz). The series combination of highly doped and depleted regions at the silicon-oxide interface slightly changes the electric field configuration inside the substrate by increasing by a small extent its concentration at the interface. Therefore, the effective permittivity sensed by the CPW lines increases a little (13.1). Furthermore, the effectiveness of the PN patterns decreases with frequency due to the frequency-decreasing capacitive impedance in the depletion regions [5], which globally decreases the total impedance in the cross-section between the S and G terminals of the CPW line (see Fig. 2). This frequency-dependent mitigation of the enhancement brought by the PN passivation is translated into a decreasing effective resistivity with frequency. Nevertheless, applying a reverse-bias to the P-doped and N-doped regions enlarges the depletion regions, which (i) overall improves the effective resistivity (to 100 and 150 Ω.cm at 50 GHz for HR2 and HR1, respectively) and propagation losses (0.7 and 0.6 dB/mm losses improvement compared to HR2 and HR1, respectively, without interface passivation), (ii) as well as its roll-off with frequency and (iii) reduces the effective permittivity to ~12.

Large-signal measurements of the 2 mm-long M1-M2 CPW lines are also carried on. The power of a 900 MHz single-tone input signal is swept and the spectral content of the output is measured. The substrate non-linearity, distorting the signal propagating along the CPW line, is benchmarked in Fig. 4, where the output harmonic components H2 (1.8 GHz) and H3 (2.7 GHz) are plotted relative to the H1 fundamental power.

The HR substrate achieves a 25–30 dB reduction in substrate-induced second harmonic level compared with the std substrates. H2 is further reduced by 9 and 28 dB when the interface is passivated with the *PNlines* A pattern, with 0 V and 5 V reverse-bias, respectively. The same CPWs on an iFEM™ are expected to have a H2 of −77 dBm (at H1 = 15 dBm) for an f_0 of 900 MHz, according to the large-signal substrate model developed and described in [4]. So, at f_0 of 900 MHz, the linearity results (H2 = -75 dBm at H1 = 15 dBm for the reverse-biased *PNlines* A on HR1) are competitive to those estimated for the same CPW line on trap-rich iFEM™ substrates.

Several PN patterns with different dimensions (cfr. Fig. 2) are designed and fabricated. Fig. 5 shows the impact of those dimensions on the effective resistivity and relative permittivity for M1-M2 CPW lines from the 985 Ω.cm HR substrate. For both pattern widths, the presence of an intrinsic region between the P-/N-doping regions improves the effectiveness of the PN passivation solution by widening the depletion regions. In this run (with fixed implant energy and dose parameters), a width of 350 nm yields the best results. It is also worth noting that applying a reverse bias to the PN junctions improves the substrate losses resulting in almost the same ρ_{eff} for all *PNlines* patterns.

More interestingly is the fact that the *PNgrid* passivation method features the highest effective resistivity among zero- or unbiased PN patterns. Indeed at high frequencies (above 10 GHz), the *PNgrid* pattern features an effective resistivity (~440 Ω.cm at 15 GHz) really close to the reverse-biased *PNline* patterns (~440–570 Ω.cm at 15 GHz). Although the reverse-biased *PNlines* patterns perform better (mainly < 10 GHz), the *PNgrid* pattern offers the great advantage of not requiring a co-design between the PN interface passivation solution and the overlying layout, therefore significantly saving design time. In terms of area

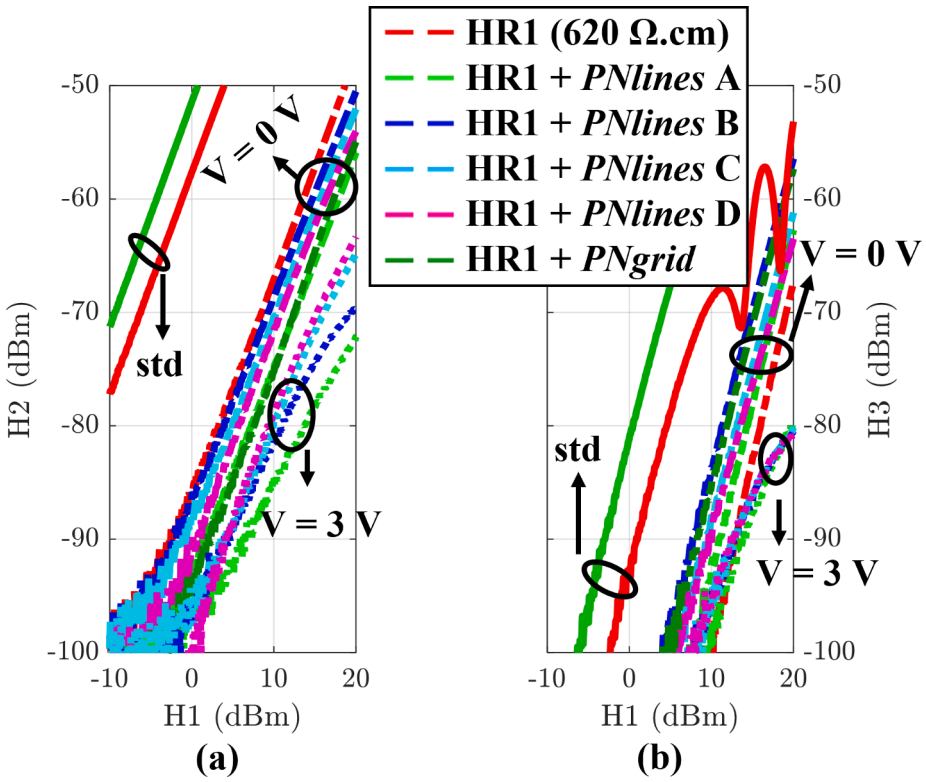


Fig. 6. Substrate non-linearity benchmark. Measured second (a) and third harmonic (b) levels versus power at fundamental of the output signal propagating in a 760 μm-long M1-M2 CPW line on different substrates. std1 and std2 measurements are added in solid lines for reference.

Table 1
Substrate non-linearity benchmark of the different PN patterns. Reported H2 values at H1 = 15 dBm.

Substrate options	H2 at H1 = 15 dBm (dBm)	
	Reverse bias = 0 V	*Reverse bias = 3 V*
HR1 (620 Ω.cm)	−57.1	/
HR1 + *PNlines* A	−65.4	−78.2
HR1 + *PNlines* B	−59.3	−74.3
HR1 + *PNlines* C	−61.1	−71.7
HR1 + *PNlines* D	−62.4	−70.4
HR1 + *PNgrid*	−64.5	/

consumption, both patterns are designed below the passives, such that they do not increase the overall footprint. It should be noted that the curves are somehow noisier in Fig. 5, compared to Fig. 3, because only 760 μm-long lines (as well as thru lines) are available on the mask to study the impact of PN patterning (as opposed to 2 mm-long lines for the lines with *PNlines* A pattern and the ones without PN junctions).

The substrate non-linearity performance of the different PN patterns is benchmarked in Fig. 6. The measurements of the 760 μm-long M1-M2 CPW lines are used (instead of the 2 mm-long lines), because not all PN patterns are available for the longest line. The length difference is the reason for the differences in absolute levels of H2 and H3 powers reported in Fig. 4 and Fig. 6 for identical substrates.

Similar observations made for the substrate losses (ρ_{eff}) above hold in terms of non-linear performance. (i) All PN patterns improve the harmonic levels compared to the case where the interface is not passivated. (ii) Increasing the depletion region (mostly by reverse biasing) greatly enhances the effectiveness of the PN passivation solution (and reduces the harmonic levels). (iii) The *PNgrid* pattern offers great performance (7 dB reduction compared to the HR case without passivation), nevertheless, (iv) the best performance is achieved with the reverse-biased *PNlines* A pattern (14 dB of further improvement). A summary of the different PN patterns large-signal performances is reported in Table 1 showing the H2 level at H1 = 15 dBm.

3.2. CPW and TFMS in QB

The total propagation losses and effective substrate parameters extracted from the CPW lines in QB are shown in Fig. 7. Due to the ~10 μm-thick dielectric stack between the CPW line and substrate, the effective permittivity and resistivity are averaged out and yield a lower $\varepsilon_{r,eff}$ and larger ρ_{eff} compared to the values extracted from the M1-M2 CPW lines. The same trends are observed with respect to the effective resistivity among the various substrates. From a ρ_{eff} value of 30 and 42 Ω.cm at 50 GHz for the std1 and std2 substrates, respectively, the ρ_{eff} is increased to ~150 Ω.cm with HR substrates. The *PNlines* A pattern enhances the performance with an ρ_{eff} increase from ~350 Ω.cm (0 V bias) up to ~1 kΩ.cm (5 V reverse biasing).

The bump in $\rho_{eff}(f)$ around 25–40 GHz (mostly visible for the low-loss substrates) is non physical and is caused by a misrepartition of total losses α among metallic resistive (R) and substrate-related losses (G) [12]. Indeed at those frequencies, the R(f) term has a non physical bump as can be seen in the inset of Fig. 7(b). This bump in measurements is attributed to some probe coupling to the chip environment and which is only partially corrected by the mTRL de-embedding. Such bump and probe coupling is also present in the measurement of the MMW inductor as explained in a subsequent section.

The propagation losses of a TFMS line designed for 50 Ω characteristic impedance is also shown in Fig. 7(a). TFMS lines are usually preferred in CMOS technology using standard resistivity substrate thanks to the shielding ground plane that prevents any substrate losses. Neglecting losses in the BEOL dielectric layer, it is assumed here that the only losses present in TFMS lines are thus metallic losses. Nevertheless when a quasi-lossless substrate is available a CPW topology seems more interesting as it offers the possibility of synthesizing a given characteristic impedance with wider conductors, and hence reduced metallic

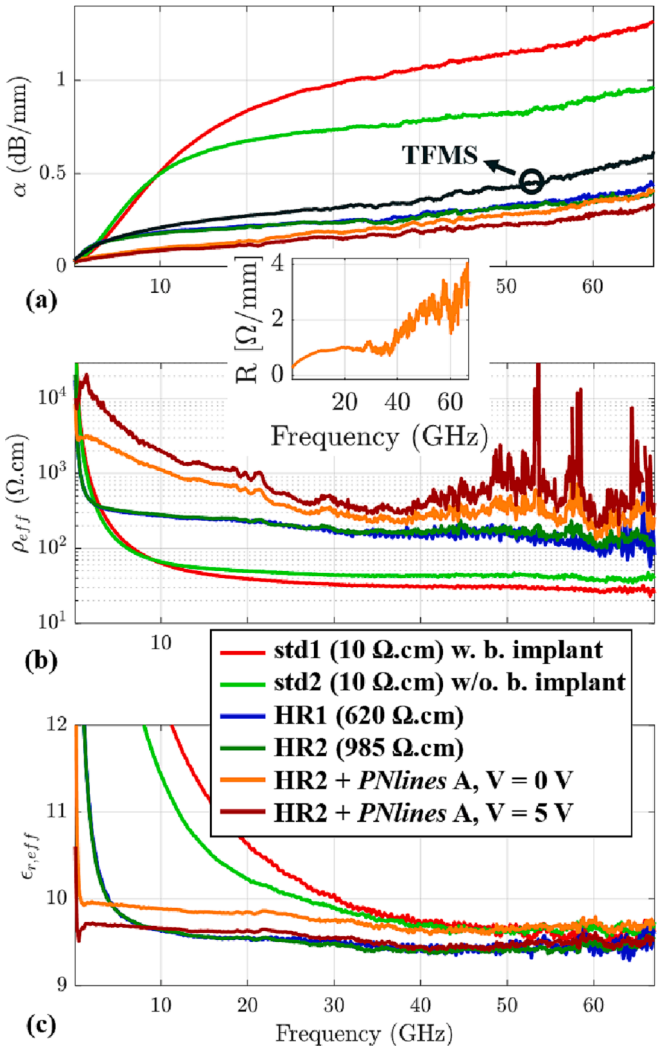


Fig. 7. Propagation losses (a), and substrate parameters: effective resistivity (b) and permittivity (c), from QB CPW and TFMS lines measurements. Inset: extracted lineic series losses R(f) (from the RLGC model) from CPW lines measurements.

losses. The resulting 50 Ω Z_c TFMS line in this work has a signal width of ~10 μm, yielding α = 0.42 dB/mm at 50 GHz. As expected, the designed 50 Ω CPW line fabricated on a standard resistivity substrate suffers from significant substrate losses and α = 1.14 and 0.83 dB/mm at 50 GHz for std1 and std2, respectively, which is much larger than the TFMS line losses. However, when a low-loss substrate is available (i.e. high-resistivity substrate with or even without PN junctions), the designed CPW line becomes a better choice of transmission line featuring α = 0.22 dB/mm at 50 GHz in the best case, thanks to reduced metallic losses and small or negligible substrate losses.

The above results demonstrate the effectiveness of the PN interface passivation solution to counter the PSC effect, demonstrating low substrate losses and harmonic distortion through the measurement of CPW lines designed with different metal layers. These encouraging results are confirmed in the following sections with other types of passive devices.

4. RF performance results – Inductors

The inductors are measured from 100 MHz to 67 GHz. A 2-step calibration is performed (LRRM calibration on an ISS, followed by an on-wafer mTRL calibration using the TFMS set of lines [13]) to move the reference plane to the device under test (DUT) vicinity with high accuracy at mm-wave frequencies [14]. Then, the S-parameters are transformed in Y-parameters and the inductance (L) and quality factor (Q) of the inductors are computed as

$$L = \mathrm{Im}\left(\frac{1}{Y_{11}}\right)\cdot\frac{1}{\omega} \quad \text{and} \quad Q = \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})}. \tag{1}$$

4.1. RF inductor

Fig. 8 shows the 1 nH inductance and quality factor of the RF inductor on several substrates. There is a small difference in the RF inductor quality factor between the std substrates: the std1 features a peak Q of 15.6 while the peak Q of std2 is 16, in agreement with the larger substrate losses for std1 already observed in the previous section. A great improvement in the RF inductor quality factor is achieved with a HR substrate thanks to a much greater bulk resistivity. Indeed, the peak Q value is around 1.4 times higher (from 16 to 23) and shifted to higher frequencies. Further improvement (from 23 to 25) is achieved thanks to the 5 V reverse-biased PN junctions, which significantly increase the substrate resistivity at the interface (and overall the substrate losses at high frequencies as seen in the previous section).

The impact of substrate losses to the peak Q between std1 and std2 (15.6 to 16) or between the HR substrate with and without PN passivation (23 to 25) is much lower than the observed substantial increase in effective resistivity and reduction in CPW losses (α) from the previous section (in particular for the M1-M2 CPW lines). For instance, the effective resistivity of CPW lines in QB on HR substrate gets an up to x4 increase with PN junctions (see Fig. 7). The corresponding gain in propagation losses is also considerable (-0.1 dB/mm at 20 GHz), but is not as large as the one achieved for the CPW lines in M1-M2 (-0.5 dB/mm at 20 GHz). As explained above and similarly to the CPW lines in QB, the signal line in QB is separated from the substrate by a ~10 μm-thick dielectric stack. As a consequence, the inductor's overall shunt losses through the substrate (related to the effective resistivity) are already rather low, because there is a lower concentration of electric field inside the substrate (compared to the CPW lines in M1-M2).

4.2. MMW inductor

Fig. 9 reports the measurement of the 170 pH inductance and its quality factor on different substrates. In Fig. 9(b), the measured inductor quality factor shows little variation among different substrates. The inductors on both standard resistivity substrates feature a similar quality factor with a peak value around 21.1. The inductor on HR2 without interface passivation exhibits a quality factor very close to std1 and std2 ones, with a potential improvement that is clouded by the measurement noise at such high frequencies. The inductors with PN patterns feature a small, but noticeable, improvement in quality factor and, more importantly, applying a reverse-bias to the PN junctions results in a small, but consistent and distinct, improvement in quality factor. Overall, the improvement is small, estimated to be no >15% (the main curves from Fig. 9(b) are reported again in Fig. 9(c) to ease the reading).

In Fig. 9 (b) the curves from the inductor measurement on HR2 with *PNlines* D pattern are affected by a bump in measurements from 45 to 63 GHz. The data points have then been removed from the figure to avoid any misinterpretation. The origin in the bump is the same as the one in the 25–40 GHz measurements of the QB CPW lines from the previous section, i.e. an uncorrected probe coupling to the nearby chip environment. The environment (and thereby the coupling) varies between DUTs and the on-wafer calibration structures, therefore a remaining error is sometimes present in the corrected measurements.

The above measured trends are confirmed by EM simulations performed with Keysight Momentum as shown by the circle data points in Fig. 9(c). Detailed explanations on how EM simulations are performed, de-embedded and how the EM stack of the HR substrate with PSC is calibrated to this study can be found in [11]. The improvement reported

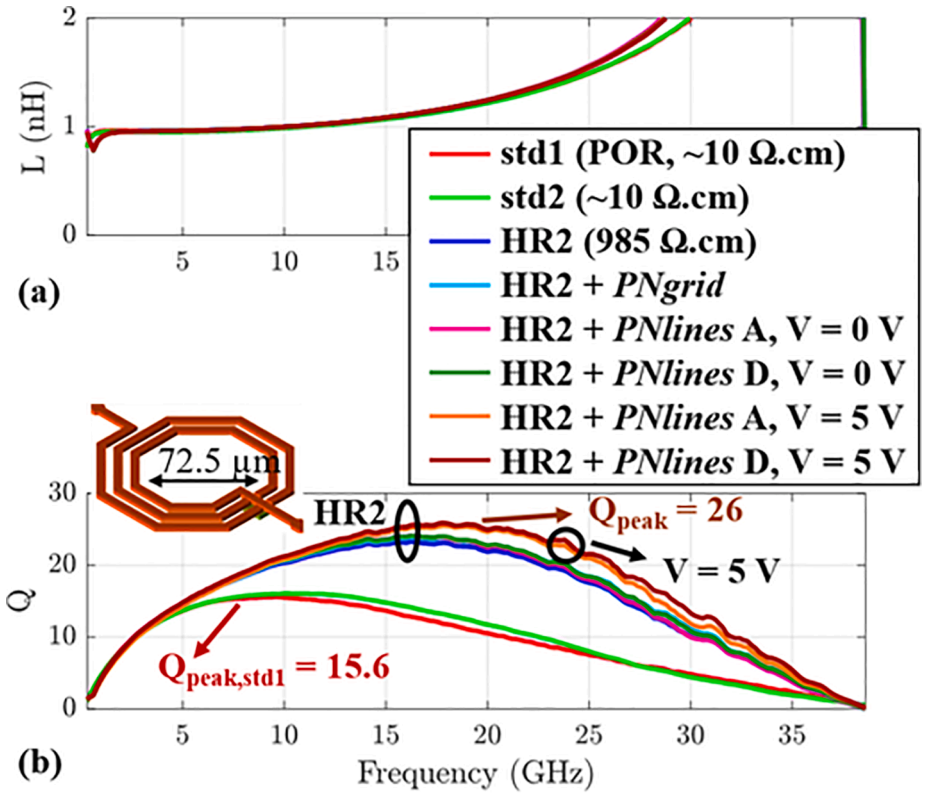


Fig. 8. (a) Inductance (L) and (b) quality factor (Q) of 5–20 GHz inductors on different substrates, with or without interface passivation.

here for this MMW inductor is smaller than the RF inductor or previously reported studies [15,16] mainly because of the smaller geometry of the MMW inductor, scaling down with higher operating frequency. Indeed, the smaller geometry of the MMW inductor, which is also far from the substrate (~10 µm), leads to a reduced concentration of electric field (E-field) and eddy currents inside the substrate, thus attenuating the impact of substrate resistivity on the inductor quality factor. A second effect of higher operating frequency is an increase in metallic losses due to skin and proximity effects, which further reduce the relative impact of substrate losses on the overall inductor losses.

In the case of the MMW inductor, full-wave 3D EM simulations (performed at 30 GHz with Ansys HFSS, driven modal solution type, with bridge-type lumped ports, up to 46,000 tetrahedra) show that 24% of the E-field is concentrated inside the substrate, as shown in Fig. 10 [11]. A different layout design of this MMW inductor (targeting mm-wave frequencies, such as 28 or 39 GHz) could have been proposed by stacking several metal layers to reduce metallic losses. By stacking the metal layers, the distance between the coil and substrate is reduced, making the inductor more sensitive to the substrate resistivity (due to an increased E-field concentration inside the substrate). Such inductor design (shown in Fig. 10) is investigated via simulations in [11] for which a ~35% improvement in quality factor is expected moving from a std to a HR substrate with interface passivation.

The reduction in substrate losses achieved with a surface-passivated high resistivity substrate is again demonstrated in this section through the quality factor improvement of two inductors designed at RF (5–20 GHz) and mm-wave (30–60 GHz) frequencies. Although the improvement is rather small for the MMW inductor, a re-design of the inductor, taking benefit of the full back-end of line available in the technology, should again strongly benefit from a low-loss substrate such as proposed by the PN interface passivation solution.

5. RF performance results – Crosstalk structure

A crosstalk structure (sketch in Fig. 1(f)) is also designed and fabricated on several substrates. It consists of 2 metal pads in bottom metal layers facing each other. It is used to evaluate the amount of crosstalk through the substrate between two adjacent structures (transistors, circuits or systems [17]). The crosstalk structures are measured from 10 kHz to 100 GHz. The measurements are de-embedded with an open-pad measurement. The magnitude of S_{21} is plotted in Fig. 11 for different substrates.

The crosstalk structures can be modeled by the equivalent circuit shown in the inset of Fig. 11 [17]. For all substrates, the high frequency behavior of $|S_{21}|$ is dominated by the capacitive coupling between the two pads (through C_3). Since, all substrates have the same permittivity, all $|S_{21}|$ curves converge at high frequencies. Then, as frequency decreases, the $|S_{21}|$ slope starts flattening, $|S_{21}|$ tending to a plateau. This upper cutoff frequency ($f_{c,2}$), connecting the plateau to the high frequency 20 dB/dec slope in $|S_{21}|$ (indicated with arrows in Fig. 11) is related to the substrate resistivity profile. It depends on the C_3 and R_3 terms from the small-signal equivalent circuit:

$$f_{c,2} = \frac{1}{2\pi R_3 C_3}. \quad (2)$$

For a non-uniform substrate resistivity profile, such as is the case in HR substrates suffering from PSC, the R_3 term averages out the resistive behavior of the coupling between the two pads, in a similar way as the effective resistivity for substrate losses in CPW lines. In other terms, since C_3 is constant for all substrates (of same permittivity), $f_{c,2}$ (through R_3) is directly correlated to the substrate RF losses: the higher $f_{c,2}$, the lower R_3 (the lower the effective resistivity), the larger the RF losses. Indeed, the values of ρ_{eff} extracted from CPW lines measurements in Section 3.1 correlate well with the cutoff frequencies in the crosstalk measurements.

The highest cutoff frequencies around 10–20 GHz for the std

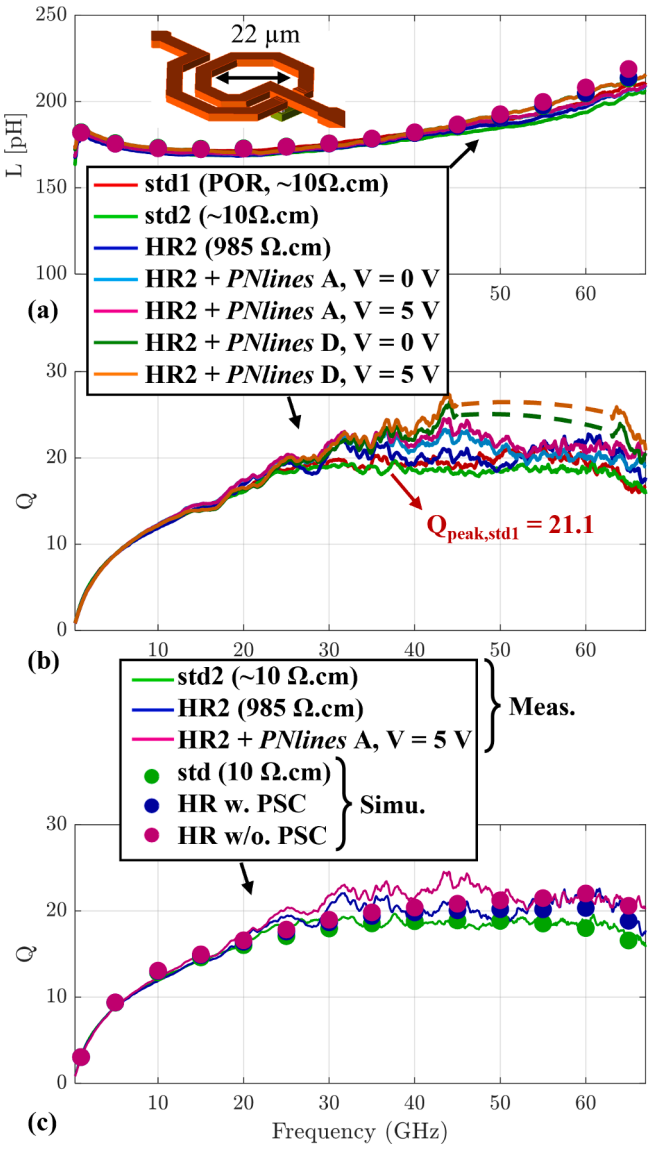


Fig. 9. (a) Inductance (L) and (b and c) quality factor (Q) of MMW inductors on different substrates, with or without interface passivation. Measurements in solid lines, EM simulations in circles.

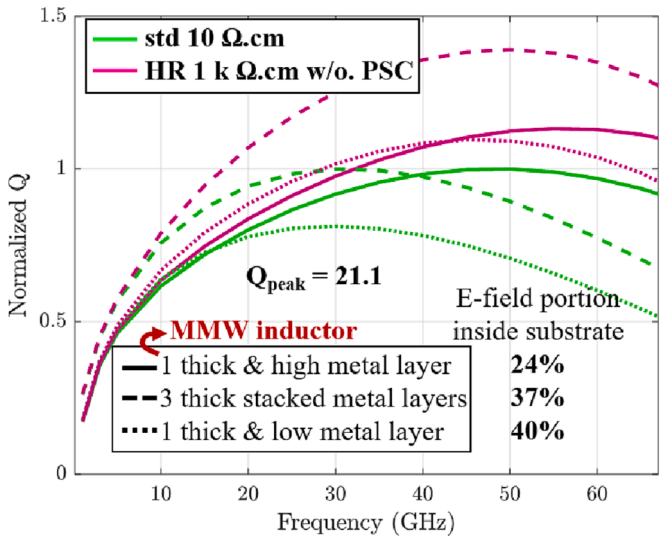


Fig. 10. EM simulations of inductors' Q normalized to the peak Q of the MMW inductor on std substrate (Qpeak = 21.1). 3 inductors are simulated: (i) MMW inductor (solid lines, ~10 µm away from the substrate, ~3 µm-thick metal), (ii) inductor on 3 thick Cu layers (dashed lines, ~2 µm away from substrate, ~7 µm-thick metal), (iii) inductor on 1 metal layer closer to the substrate (dotted lines, ~2 µm away from substrate, ~3 µm-thick metal), on top of two substrates: std (green), HR without PSC (purple).

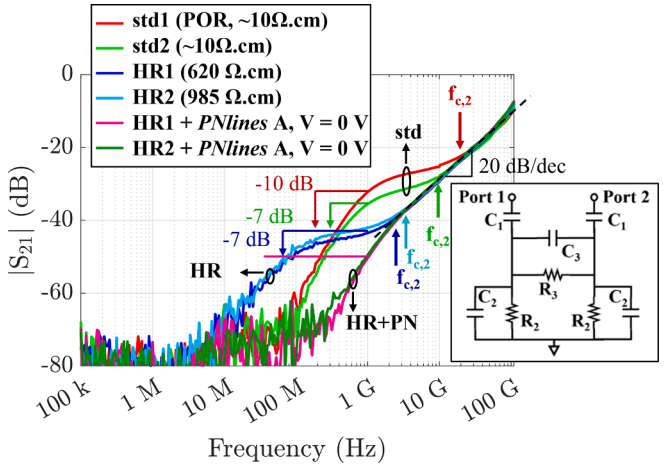


Fig. 11. Crosstalk measurements on different substrates. Higher cutoff frequency ($f_{c,2}$) are shown with arrows for each substrate. Crosstalk reduction with different substrates at 1 GHz are also indicated. Inset: small-signal equivalent circuit of the crosstalk structure.

resistivity substrates (std2 and std1) is mainly caused by the low bulk substrate resistivity. The HR substrates without PN implants feature lower cutoff frequencies (~3 GHz), but in these cases, R_3 is dominated by the thin conductive sheet at the interface due to the PSC effect. The higher cutoff frequency of the HR2 than the HR1 (without interface passivation) correlate well with the lower extracted ρ_{eff} from M1-M2 CPW lines, i.e. 50 and 68 Ω.cm at 50 GHz for HR2 and HR1, respectively. These observations show that the HR2 substrate feature a higher level of PSC than HR1. Whereas, the measured crosstalk structures on HR substrates with the designed PN pattern do not exhibit a plateau (above the measurement noise floor), demonstrating that the PSC effect has been effectively countered.

The $|S_{21}|$ behavior below the plateau strongly depends on the overall geometry of the crosstalk structure, mainly on the crosstalk pads distance to ground. The low frequency deviation from a 20 dB/dec slope (for the interface-passivated HR substrates) or plateau (for all other substrates) in the $|S_{21}|$ curve does not only depend on the substrate resistivity profile, but mainly on how the pads couple to the ground (hence on the structure layout). For that reason, the low frequency behaviors of the curves are considered out of scope of this paper and are not discussed. At 1 GHz (a frequency arbitrarily chosen to be high enough for the crosstalk to solely depend on the substrate resistivity profile), moving from a std resistivity (std2) to a HR substrate (with PSC) brings a 7 dB improvement in crosstalk, while a further 7 dB can be achieved when PN implants are used to negate the PSC effect. With a larger crosstalk pad spacing to ground (distance of 50 µm in Fig. 1(f)), the $|S_{21}|$ plateau would extend over a larger frequency range below $f_{c,2}$ and the crosstalk reductions from one substrate to another would be much larger at lower frequencies.

6. Conclusion

This paper studies the co-integration of an FD-SOI technology on a high-resistivity substrate, which unavoidably suffers from the parasitic surface conduction effect. Since the trap-rich interface passivation

cannot be easily applied to FD-SOI technology, other means to deal with the PSC effect are investigated. This paper studies the *PN interface passivation* solution applied to an advanced industrial flow, the 22FDX® node from GlobalFoundries.

Several PN patterns of different dimensions are fabricated to enhance the RF performance of HR substrate and are compared with HR suffering from PSC (without PN pattern) and standard resistivity substrates. Their performance is assessed via the measurements of several passives, i.e. CPW lines, inductors and a crosstalk structure. It is shown that, first, a high-resistivity substrate already significantly improves the substrate performance on all passives, and, second, all figures of merit are further greatly improved with the PN junctions passivation on high-resistivity substrates.

Indeed, from M1-M2 and QB CPW line measurements, the effective resistivity is increased at least by factor of 15 and 20, respectively, up to 50 GHz, when moving from a standard resistivity substrate (std2) to a HR with PN passivation. Great reduction in non-linearity generated by the substrate is also accomplished, i.e. a reduction up to 58 dB in the second harmonic level (for the same fundamental output power) is again achieved by moving from a std substrate (std2) to HR with reverse-biased *PNlines* A interface passivation. It yields competitive results to those estimated for the same CPW line on trap-rich iFEM™ substrates.

The inductors can also strongly benefit from a HR substrate. By changing the substrate from a std resistivity (std2) to a PN-passivated HR substrate, the RF inductor quality factor increases by up to 62%.

Lastly, great isolation of crosstalk through the substrate is achieved with the PN patterns on HR substrate, demonstrating successful suppression of the PSC effect with the PN junctions patterns.

Overall, the *PN interface passivation* solution offers high quality RF substrate at RF and mm-wave frequencies for low-loss passives compatible with an industrial FD-SOI technology.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

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