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Schottky-Barrier FET Ultra-Low-Power Diode

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***Abstract*—In this paper, for the first time, we apply the ultra-low-power (ULP) diode concept with Schottky Barrier (SB) transistors and analyze the performance in comparison to standard CMOS, using calibrated TCAD mixed-mode simulations. The negative impedance characteristics obtained in reverse mode with SB devices are shown to offer superior current performance compared to CMOS, especially as a function of temperature.**

***Index Terms*—ULP, Ultra-Low-Power, Schottky Barrier, SRAM, Diode**

I. Introduction

The demand for ultra-low-power (ULP) circuit drives worldwide interest, notably for Internet of Things (IoT) applications. In one such direction, CMOS technology downscaling has led to a reduction of V_{DD} (supply voltage) minimizing the operating power dissipation. The V_T (threshold voltage) of the MOSFETs is reduced as well to maintain adequate overdrive ($V_{DD} - V_T$) for high speed. The drawback of this aggressive downscaling results in an exponential increase of subthreshold leakage. The reduction of the static power dissipation has become a major concern for the IC industry. In this context, the ULP design concept proposed by Levacq et al. [1] offers CMOS composite diodes with ultra-low-leakage behavior, i.e. a p-type MOSFET is connected in series with the n-type one such that when the composite structure is switched off, the n-MOSFET (resp. p) gate-to-source voltage becomes negative (resp. positive), thereby reducing the off-leakage current and hence static power consumption (Figure 1). The concept has been successfully applied towards implementation in rectifiers for energy harvesting [2], charge-pumps for power voltage management, latches in dynamic logic circuits [3] or high-speed adders [4], low-V_{DD} SRAMs... from 1μm to 28nm CMOS nodes, with record power consumption of energy efficiency [5], [6]. The modeling, process dependence and temperature behavior or the structure have been discussed in details towards design optimization.

In this paper, we analyze the usage of Schottky Barrier (SB) transistors for ULP diode implementations, using simulations with the state-of-the-art Synopsis TCAD framework [7]. We will indeed show that ULP diodes can exploit the SB device well-known benefits at low voltage when compared to CMOS, while the higher off current of SB transistors linked to their ambipolar characteristic can be suppressed by the ULP concept.

The paper is organized as follows: Section II gives detailed information of the simulation setup. In section III the simulation results of CMOS vs. SB-FET ULP diodes are compared and discussed as a function of voltage and temperature ranges. Section IV concludes the paper.

II. Simulation Setup

The TCAD simulations have been calibrated on experimental SB devices with the settings of [8], [9] obtained from the simulated structures by process simulations and parameters shown in Table I.

Within the TCAD simulation environment the following models were activated: Fermi distribution, incomplete ionization, incomplete ionization on mobility, doping dependency on mobility, high field saturation on mobility, mobility degradation at interfaces, bandgap narrowing on effective intrinsic density in terms of old Slotboom model, lattice temperature, nonlocal tunneling at metal-semiconductor interfaces. Schottky Barrier Lowering effects (SBL) are not considered within this simulation. It is to be expected from past simulations that the currents will be slightly higher, for both on- and off-currents.

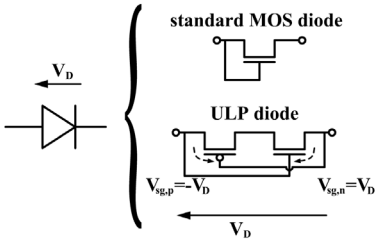

Fig. 1. Standard n-MOS diode and ULP CMOS diode architectures with forward I-V definitions.

However, the reason to skip SBL effects in this work is twofold. Firstly, single device simulations have shown that in the range of biases used for the ULP diodes, the impact of SBL was very low. Secondly, one cannot extract the correct current components of each device within mixed-mode simulations, which need to be performed for the ULP circuitry as proposed by [1]. Detailed information for the single device extraction of the SBL current can be found in [10].

Here, we want to show that in principle the performance of SB-FET ULP diode can be beneficial.

Figures 2 and 3 present the simulated structures for the classical n-MOS/p-MOS and n-SB-FET/p-SB-FET, respectively. These calibration settings were applied to the device simulations with the physical models for individual device I-V curves and next mixed-mode simulations for ULP circuits.

TABLE I
GEOMETRY AND MATERIAL PARAMETERS IN THE TCAD SIMULATION [7] FOR 300K. PARAMETERS FROM REFERENCES [7], [11], [12], [13].

	SB-FET	MOS		
L_{ch}	200	200	[nm]	effect. channel length
T_{ch}	$\approx$ 20	$\approx$ 20	[nm]	channel thickness
W_{ch}	1 (n-SB-FET), 10 (p-SB-FET)	1 (n-MOS), 2 (p-MOS)	[μm]	channel width
T_{ox}	1.8	2.5	[nm]	oxide thickness
N_B	10^{15}	10^{18}	$[1/cm^3]$	substrate doping
$N_{S,D}$	-	10^{20} (peak)	$[1/cm^3]$	Source/drain doping
N_{RG}	10^{18} (peak)	-	$[1/cm^3]$	Retrograde doping
ϵ_{ch}	11.7	11.7	[$-$]	channel permittivity
ϵ_{ox}	7	7	[$-$]	oxide permittivity
$\phi_{Bn,p}$	0.27 (ErSi), 0.22 (PtSi)	-	[eV]	SBH electrons
A_n^{**}	112	-	$[A/cm^2K^2]$	elec. Richardson constant
A_p^{**}	32	-	$[A/cm^2K^2]$	hole Richardson constant
m_n^*	0.19	-	[$-$]	electron effective tunneling mass
m_p^*	0.49	-	[$-$]	hole effective tunneling mass

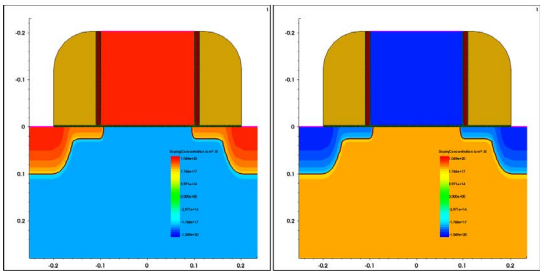

Fig. 2. n-MOS/p-MOS TCAD device structures.

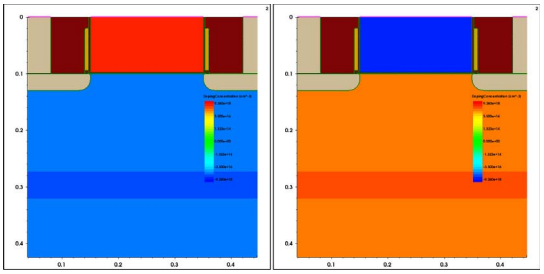

Fig. 3. n-SB-FET/p-SB-FET TCAD device structures.

III. RESULTS

Figures 4 and 5 show the drain current (I_d) vs gate voltage (V_g) characteristics, for different drain-to-source voltage (V_{ds}), of the n-MOS & p-MOS and n-SB-FET & p-SB-FET simulations, respectively, at the room temperature (RT) of 300K, focusing on subthreshold operation of highest relevance for the ULP diodes.

The typical behaviors of both classical MOS and SB-FET devices are observed for the different bias conditions. In OFF-regime, the higher the V_{ds}, the higher the leakage current in both devices, but for the SB-FETs the ambipolar current is significantly higher. In ON-regime, the p-SB-FET has low drive current but as discussed later in the ULP diode, this regime is not of importance for memory cell implementations. In subthreshold, the switching of the SB-FET performs better compared to the standard MOS if one takes the definition for V_T where I_d = 0.1μA. Here the difference between both is approximately 50 to 100mV. The target here is a similar on-current in MOS and SB-FETs at low supply voltage $V_{DD} \approx 0.4$V, which led to the scaling of W for the p-SB-FET. These choice lead to increased I_{off} in SB, which motivates the introduction of the ULP concept. Furthermore, for both simulations the intersection of n- and p- characteristics is around V_g of 0V related to the W choices of adequate device width.

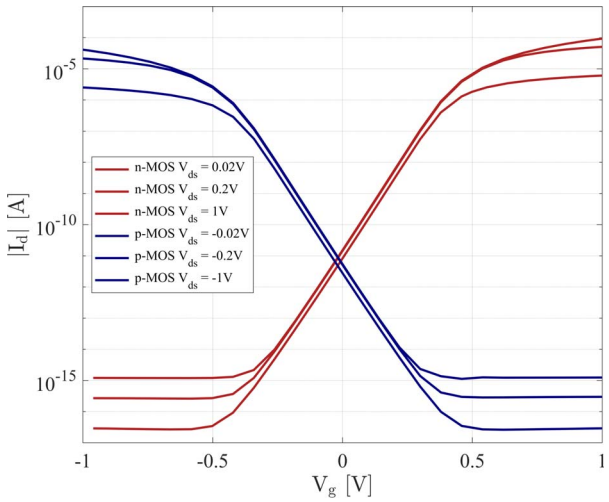

Fig. 4. $I_d - V_g$ curves of CMOS with n-MOS L=200nm, W=1μm & p-MOS with L=200nm, W=2μm, for different V_{ds}.

In Figure 6 the quick ON-switching of SB-FET ULP diode can be seen in the range from 0 to 300mV if one considers the whole T range in forward mode (Figures 7 and 8), but not beyond V_T due to current limitation in SB-FET related to the tunneling mechanism. In reverse, the SB ULP diode demonstrates a bell-shaped characteristic similar to what has been demonstrated in CMOS [1]–[6] previously. These curves also mimic the I-V behavior of resonant-tunneling diodes. The negative resistance behavior can be used to minimize the off-leakage current of diodes but also generate a latch effect for memory applications. In such case, the figures of merit are the peak and valley currents in reverse mode, as well as their ratios, their dependence on temperature and their corresponding biases. Please also note that the simulated CMOS bell-shaped curve is very similar in current and voltage amplitudes and relative values to what was measured in practice [5], [6].

In Figures 7 and 8 the different peak and valley currents of

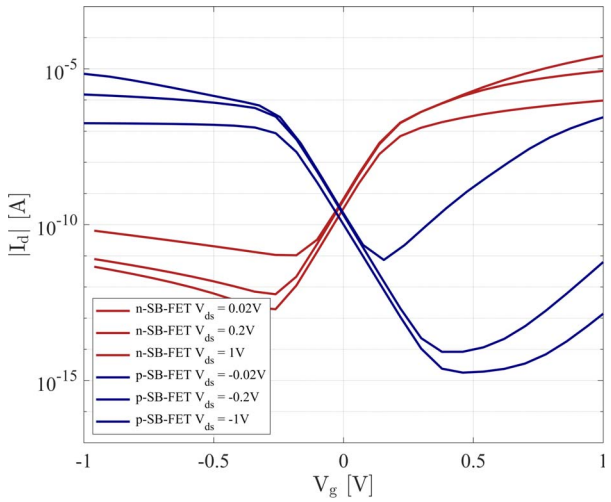

Fig. 5. $I_d - V_g$ curves of SB-FET with n-SB-FET L=200nm, W=1μm & p-SB-FET with L=200nm, W=10μm, for different V_{ds}.

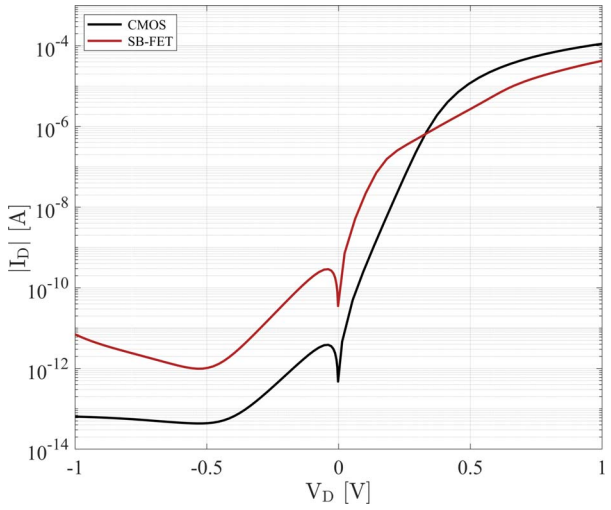

Fig. 6. $I_D - V_D$ of CMOS ULP vs. SB-FET ULP at RT.

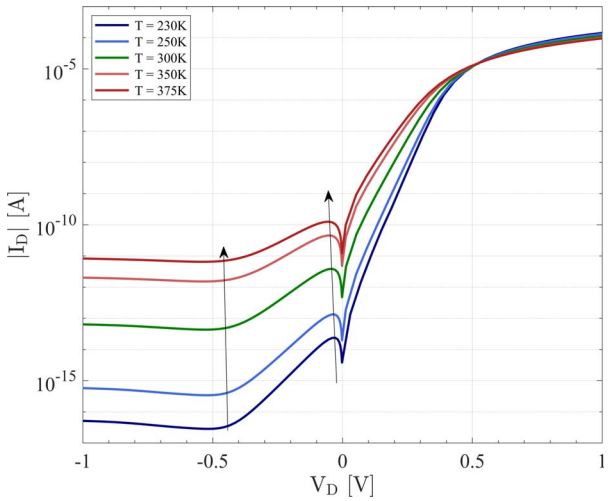

Fig. 7. $I_D - V_D$ curves of CMOS ULP diode vs. temperature.

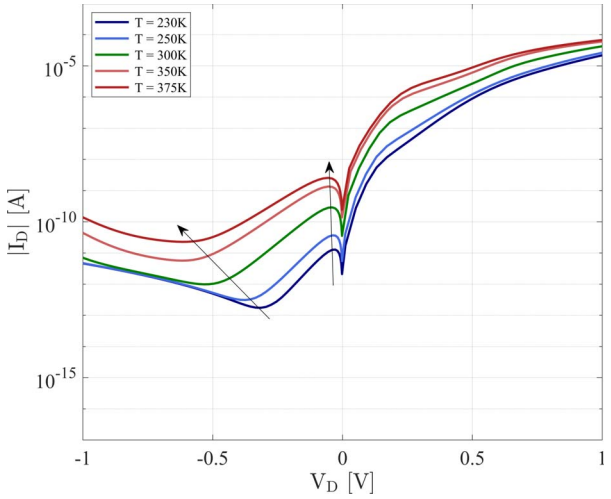

Fig. 8. $I_D - V_D$ curves of SB-FET ULP diode vs. temperature.

each ULP diode are shown for a temperature range of 230K to 375K. For the classical CMOS ULP diode the amount of peak degradation at lower temperature is much higher than in the counterpart with SB contacts. This is related to the strong sub-V_T I_d reduction in standard MOSFETs and is a limitation of the CMOS ULP diode at low temperatures. One can furthermore observe the valley movement for the SB-FET ULP diode towards higher biases the higher the temperature becomes. In all cases, the SB-FET outperforms the CMOS in the whole temperature range, i.e. considering the worse ON and peak currents at low T and worse OFF / valley currents at high T.

This observation can be seen in the Figures 9, 10 and 11, where the maximum (peak), minimum (valley) and peak-to-valley-ratio of the I_D current over temperature is extracted and analyzed. In Figure 9 the SB-FET ULP peak current is between two and three orders of magnitude higher compared to the CMOS ULP diode. It is also remarkable to note that the peak current of the SB diode at low T keeps over that of the CMOS at room T. This ensures that the SB diode can be used at low T in practical applications demonstrated for the CMOS above RT. Smaller widths could even be used in SB-FETs reducing footprint and leakage at high T.

On the other hand, the SB-FETs ULP valley current is between four and one orders of magnitude higher compared to the CMOS ULP diode as one can observe in Figure 10. This is obvious, because for the SB-FET ULP diode the ambipolar current has to be taken into account, which does not degrade with lower temperatures as for the CMOS ULP diode.

The peak-to-valley-ratio for the I_D current demonstrates a more robust behavior of the SB-FET ULP diode over temperature. Especially, for the higher temperatures the degradation of the SB-FET ULP diode is 3x (reference is RT) as for CMOS ULP diode it is 8x when an adaptive V_D circuit scheme is used to follow the valley shift. The lesser dependence of the ratio to T could be used to more easily and hence better optimize the design (i.e. choice of dimensions, W). In CMOS, low I_D peaks are critical at low T but low peak-to-valley ratio is critical at high T. In SB, a low T design would keep robust in the whole T range provided that adaptive supply voltage is used. This finally allows for the ULP peak current a reduction of the SB-

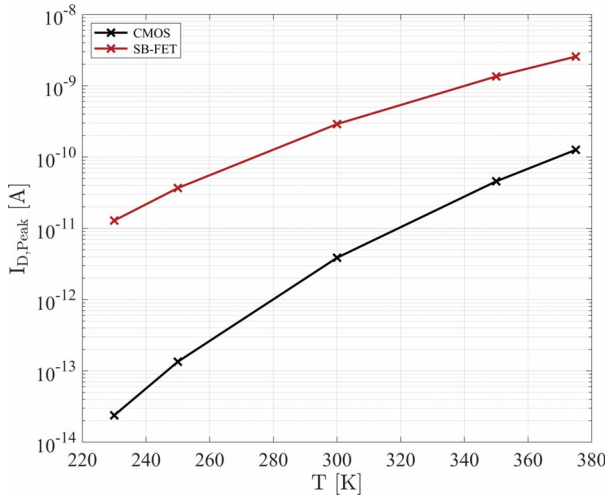

Fig. 9. Peak I_D of CMOS vs. SB-FET ULP diode in reverse mode over temperature. Corresponding V_D ranges in CMOS from -33mV to -51mV and SB-FET from -27mV to -52mV.

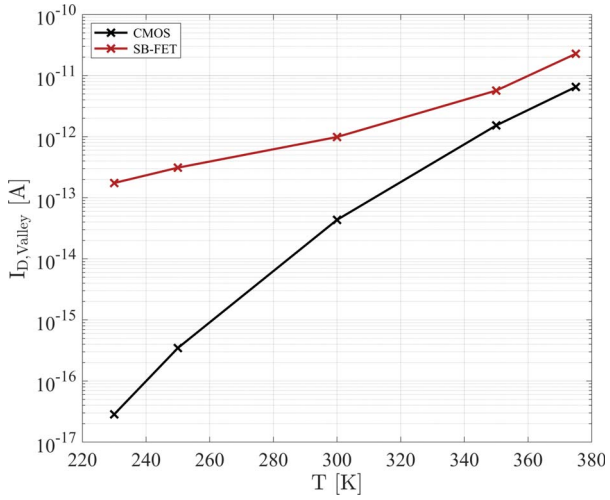

Fig. 10. Valley I_D of CMOS vs. SB-FET ULP diode in reverse mode over temperature. Corresponding V_D ranges in CMOS from -500mV to -558mV and SB-FET from -318mV to -606mV.

FETs (both n- and p-) widths (W) by 5, bringing the minimum W of the p-FET equal to CMOS and that of the n-FET to min W and hence, the SB-FET I_{off} close to that of CMOS.

IV. Conclusion

For the first, the ULP diode concept was applied to SB MOS transistors to mitigate their ambipolar leakage current. Using calibrated TCAD mixed-mode simulations, the SB-FET ULP diode is shown to offer superior performance in comparions to standard CMOS with regards to the bell-shaped I-V characteristics in reverse mode, of interest to design ULP latch circuits and SRAMs notably. This has been related to the better performance of the SB-FETs in weak inversion, and as a function of temperature. Compared to the CMOS counterpart, the SB-FET ULP diode can provide a peak current less degraded at low temperature, a valley current less degraded at high temperature and all together a more robust (i.e. constant) peak-to-valley ratio from 230K to 375K. The results finally

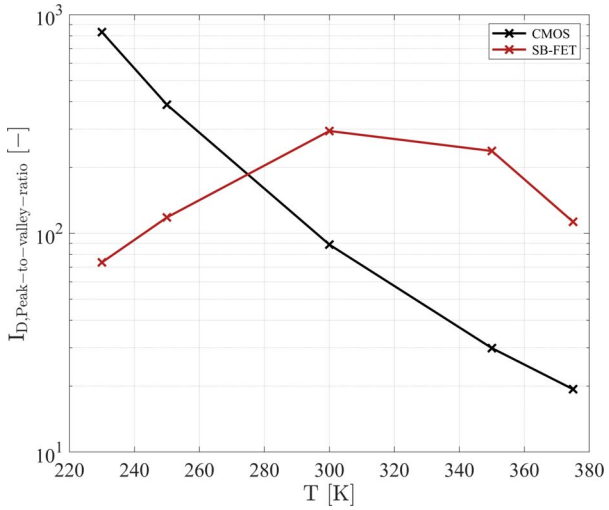

Fig. 11. Peak-to-valley ratio $I_{D,Peak-to-valley-ratio}$ of CMOS vs. SB-FET ULP diodes over temperature.

offer a possibility to design the SB-FET ULP diode with I-V curves compatible with the operation of memory cells, using about 2x less area than in standard CMOS.

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