SOI technologies for RF and millimeter-wave integrated circuits

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Performances of RF and millimeter-wave integrated circuits are directly linked to the analog and high frequency characteristics of the transistors, the quality of the back-end of line process as well as the electromagnetic properties of the substrate.
Silicon-on-Insulator (SOI) technology has taken the radio-frequency (RF) world by storm in the past decade. By offering high performance at low cost it has steadily displaced Gallium-Arsenide and Silicon-on-Sapphire technologies to become the mainstream technology for RF switch banks in mobile applications. In 2008, RF-SOI accounted for less than 10% of switching modules in handsets, and today (2022) virtually 100% of all modern-day smartphones include RF switches implemented in partially depleted (PD) SOI on engineered and optimized trap-rich (TR) silicon-based substrates [1]. The success of PD-SOI (130 nm) in today's RF market is not only due to significant technological improvements at the transistor level, but necessary optimizations have also been made at the substrate and back-end of line levels to enable performance RF applications.

With the circuit complexity of RF front-end modules (FEMs) in smart devices ever increasing as the next generations of telecommunication standards emerge (4G-LTE, 5G), more and more RF content is required in each device. This strong growth in the RF industry, expected to be led by 5G and Internet-of-Things (IoT) types of products, must be supported by a technology with a high-volume manufacturing capability. This requirement leads to a strong interest in silicon-based technology for RF applications, as it is a mature technology fully enabled on 300-mm-diameter wafers for high throughput.
Today, SOI is a strong candidate for a variety of RF circuit blocks, beyond RF switches where it has already made a name for itself over the past decade. Indeed, advanced PD-SOI nodes (sub-100 nm) as well as the most advanced fully depleted (FD) SOI nodes (28 and 22 nm) are demonstrating their potential for all kinds of RF and millimeter wave front-end circuit modules.

This talk aims to present the overall RF and mm-wave performance of SOI technologies, at the device, circuit and substrate levels, for telecommunications and FEM applications. First, the high-frequency characteristics at the transistor level are presented. In particular, FD-SOI's high speed (for performance mm-wave 5G applications) and low power consumption (for RF IoT) are presented [2], along with the useful functional effects of the applied back-gate bias [3]. Then, an overview of the state-of-the-art in terms of RF integrated circuits (ICs) is made, and the increased complexity and technological trends of FEMs are discussed. A review is presented to reveal the position of SOI for key RF and mm-wave circuits (switches, LNAs and PAs). Finally, the semiconductor substrate's impact is described at RF frequencies. Substantial losses arise in silicon substrates at RF frequencies due to the conductive nature of silicon, and simply reducing the nominal doping of the handle wafer is insufficient, as a parasitic conduction channel is induced by (even low-level) parasitic charged defects present at all silicon/insulator interfaces [4]. This effect -and ways to counter it- are described in depth as it is responsible for large amounts of RF losses, parasitic coupling and high levels of non-linear signal distortion [5, 6]. The latest results for the next generation silicon substrate solutions, including improved trap-rich SOI, implanted buried PN junctions underneath thin BOX [7], and silicon substrate backside porosification in post-CMOS [8], will be presented.

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