Back-Gate Network Extraction Free from Dynamic Self-Heating in FD SOI

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ABSTRACT

Back-gate and substrate networks modeling of FD SOI MOSFETs is crucial for RF and mm-wave applications due to their impact on RF performance. However, usual substrate models rely on the source to drain coupling through the back-gate, which appears in the same frequency range as the dynamic self-heating effect in such devices. This paper provides equations enabling dynamic self-heating removal from measurements to obtain isothermal Y-parameters, based on the knowledge of the frequency-dependent complex thermal impedance. This work shows that a large error on the back-gate related small-signal equivalent circuit, as well as on the output conductance, can be made if they are extracted without removal of dynamic self-heating.

INTRODUCTION

The continuous CMOS technology downscaling enabled increased integration and improved DC, analog and RF performances, becoming competitive to other technologies and broadening its range of applications. Wideband modeling of the transistor is essential for technologies targeting diverse applications and requires a proper substrate model. The drain to source coupling through the body (also called substrate effect) induces a transition in the Y-parameters over frequency. This substrate effect is commonly used to extract the substrate parameters from 2-port measurements [1-3]. Another consequence of gate length reduction is the larger current and power densities as well as an increased self-heating effect (SHE) [4]. Dynamic self-heating is known to induce a transition in the Y-parameters over frequency. In fully-depleted silicon-on-insulator (FD SOI) MOSFETs, the substrate effect (coupling through the back-gate instead of the body: Si substrate under the buried oxide [5]) transition occurs in a similar frequency range as the dynamic SHE [6]. Therefore, the back-gate and substrate nodes can no longer be accurately extracted from 2-port measurements if self-heating effect is not accounted for. [7] proposes a methodology for a separate analysis of those hardly distinguishable effects using measurements at the zero temperature coefficient (ZTC) bias point.

This paper goes further and shows how the isothermal Y-parameters, i.e. not affected by dynamic self-heating, can be computed from the measured Y-parameters. Then, a bias-dependent small-signal equivalent model is extracted from the 2-port isothermal Y-parameters, including the back-gate network. Finally, the extracted small-signal parameters are compared to the ones extracted from the measured Y-parameters, which include dynamic SHE.

DYNAMIC SELF-HEATING REMOVAL

When a small-signal is applied to the transistor, the lattice temperature follows it as long as it is "slowly" (w.r.t. its thermal time constant) varying in time, whereas it ceases to follow the AC signal at higher frequencies. This is the so-called dynamic self-heating effect that induces a "step" in the Y_{dd} (Y_{22}) and Y_{dg} (Y_{21}) parameters. Equations describing its effect on the Y-parameters of a general two-port device have already been presented in [8]. From those equations, one can derive the following system of linear equations:

$$\boldsymbol{A}.\bar{Y}_{iso} = \bar{b} \quad (1)$$

$$\boldsymbol{A} = \begin{pmatrix} 1+Z_{th}\frac{\partial I_g}{\partial T_A}V_g & 0 & Z_{th}\frac{\partial I_g}{\partial T_A}V_d & 0 \\ 0 & 1+Z_{th}\frac{\partial I_g}{\partial T_A}V_g & 0 & Z_{th}\frac{\partial I_g}{\partial T_A}V_d \\ Z_{th}\frac{\partial I_d}{\partial T_A}V_g & 0 & 1+Z_{th}\frac{\partial I_d}{\partial T_A}V_d & 0 \\ 0 & Z_{th}\frac{\partial I_d}{\partial T_A}V_g & 0 & 1+Z_{th}\frac{\partial I_d}{\partial T_A}V_d \end{pmatrix}$$

$$\bar{Y}_{iso} = (Y_{11,iso} \quad Y_{12,iso} \quad Y_{21,iso} \quad Y_{22,iso})^T$$

$$\bar{b} = \left(Y_{11} - Z_{th}\frac{\partial I_g}{\partial T_A}I_g \quad Y_{12} - Z_{th}\frac{\partial I_g}{\partial T_A}I_d \quad Y_{21} - Z_{th}\frac{\partial I_d}{\partial T_A}I_g \quad Y_{22} - Z_{th}\frac{\partial I_d}{\partial T_A}I_d\right)^T$$

It describes how the isothermal Y-parameters ($Y_{ij,iso}$) can be computed from the measured Y-parameters (Y_{ij}) and the thermal impedance Z_{th}. Since the gate current (I_g) and its derivative with ambient temperature (T_A) are very small, the effect of dynamic self-heating is limited to the Y_{22} and Y_{21} parameters. Once the frequency-dependent Z_{th} is known, (1) can be used to remove the dynamic self-heating effect from the measurements and thereby extract an electrical model of the transistor at different biases.

Determining an accurate estimation of $Z_{th}(f)$ is not straightforward, especially for FD SOI MOSFETs for which the drain to source coupling through the back-gate induces a transition in Y_{22} and Y_{21} (substrate effect) in a similar frequency range such that it is hardly distinguishable from the dynamic self-heating effect. [7] deals with this ambiguity and provides a method to accurately extract $Z_{th}(f)$ at different biases, which is observed to be bias-independent (to a first order), in agreement with [9]. The Z_{th} extraction procedure is out of scope of this paper. It is however applied here to extract $Z_{th}(f)$, which is then used to correct for dynamic self-heating with (1). Finally, the small-signal equivalent circuit present in Fig. 1 is extracted at different biases from curve fitting of the $Y_{ij,iso}$ from ~30 MHz to 10 GHz.

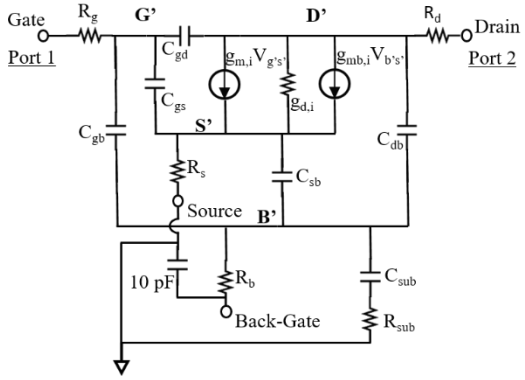

FIGURE 1. Small-signal equivalent circuit (SSEC) of an FD SOI including the back-gate and substrate nodes.

RESULTS

An FD SOI super-low threshold voltage nMOSFET from 22FDX® made of a gate length of 20 nm, finger width of 0.5 µm, 20 fingers and a multiplicity of 6 for a total width of 60 µm, is measured on-wafer from 100 kHz to 10 GHz. It is in a common source configuration with a decoupling capacitance of 10 pF connecting the back-gate to the source. Its S-parameters are measured using a VNA PNA N5291A from Keysight. The RF MOSFETs are probed using a Ground-Signal-

Ground (GSG) configuration. A Short-Open-Load-Thru (SOLT) calibration is performed and dedicated open and short structures are measured to de-embed the transistor data down to the first metal layer.

Fig. 2 shows the $C_{dd}(f)$ ($Im(Y_{22})/\omega$)) and $g_d(f)$ ($Re(Y_{22})$) for different V_g when dynamic self-heating is present (solid lines) and when it is removed (dashed lines). The larger the gate bias, the stronger the self-heating effect and the larger the mistake made while modeling the back-gate and substrate nodes (by ~30 MHz to 10 GHz Y-parameters fitting) if SHE is not removed. Indeed, stronger SHE induces a larger step in the $C_{dd}(f)$ and $g_d(f)$ curves, whereas the transition related to substrate effect is roughly bias-independent in the shown range as suggested by the overlapping $C_{dd}(f)$ dashed curves from 50 MHz to 3 GHz. The error made in the small-signal circuit modeling is glaring in Fig. 3.

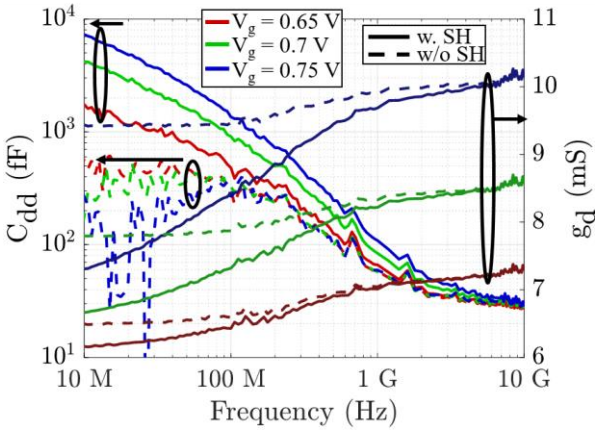

FIGURE 2, Output capacitance (C_{dd}) and conductance (g_d) versus frequency for different gate biases, V_d = 0.8 V and V_{bg} = 0 V. Measurements from which dynamic SHE is removed in dashed lines and including it in solid lines. The resonances in $C_{dd}(f)$ below 100 MHz for V_g = 0.75 V (dashed line) are due to a slightly imperfect removal of SHE resulting from a noisy subtraction of two large values.

Fig. 3 shows some parameters of the small-signal equivalent circuit at different front-gate biases for V_{bg} = 0 V and V_d = 0.8 V (saturation), either extracted from the $Y_{ij,iso}$ (SHE removed, dashed lines) or from Y_{ij} (SHE not removed, solid lines). The substrate related resistance and capacitance (R_{sub} and C_{sub}) as well as the extrinsic resistances (R_s, R_d, R_g, R_b) are assumed to be V_g-independent. The substrate effect affects all the Y-parameters, although only the frequency variations in Y_{22} and Y_{21} are sufficiently large to be distinguished from measurement noise and used in practice for model fitting. Due to the limited amount of fitting curves and large amount of fitting parameters, it is difficult to have an accurate quantitative extraction of these parameters solely based on 2-port measurements. Nevertheless, the trends extracted correlate well with TCAD Sentaurus simulations of similar devices in a 4-port configuration (not shown due to lack of space). For instance, the extracted $C_{gb}(V_g)$ in Fig. 3 is much larger than expected, but its decreasing trend with larger V_g agrees with a lower front-gate to back-gate coupling shielded by the formation of an inversion channel.

The very large apparent increase (up to 720%) in $g_{mb,i}(V_g)$ (whereas the peak $g_{m,i}$ is around 110 mS) and in $C_{sb}(V_g)$ in solid lines are a good example of the erroneous modeling when SHE is not removed. The curves start deviating at V_g = 0.62 V, which corresponds to the ZTC bias point, at which dynamic SHE vanishes (because $\partial I_d/\partial T_A = 0$) [7]. For V_g < 0.62 V, the dynamic SHE induces an opposite step in the Y-parameters that cannot be modeled with positive values of the back-gate and substrate network parameters and are thus not shown.

Although ignoring SHE does not significantly affect the $g_{m,i}(V_g)$ extraction, the $g_{d,i}(V_g)$ extraction is much more sensitive to SHE and ignoring it can lead to a strong misestimation (as large as 20%). Even though the main RF FoMs of MOSFETs (f_t and f_{max}) are not affected by dynamic SHE, the transistor model can be incorrectly extracted and physical mechanisms related to some small-signal parameters can be misevaluated, such as mobility degradation due to transverse electric field affecting the $g_{d,i}(V_g)$ behavior [10].

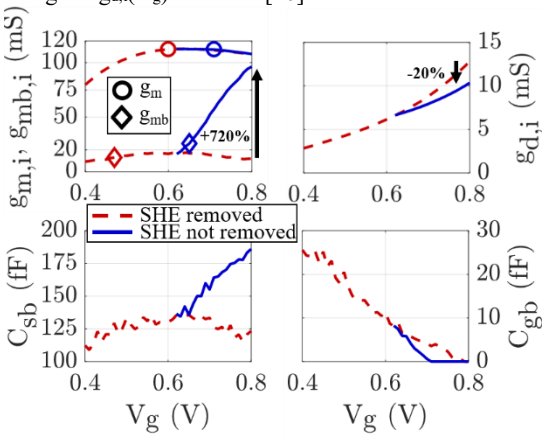

FIGURE 3. $g_{m,i}$ and $g_{mb,i}$ (top left), $g_{d,i}$ (top right), C_{sb} (bottom left) and C_{gb} (bottom right) parameters of the SSEC from Fig. 1 versus V_g. Extractions based on either $Y_{ij,iso}$ (SHE removed, in dashed lines) or Y_{ij} (SHE not removed, in solid lines) fitting from ~30 MHz to 10 GHz. V_d = 0.8 V and V_{bg} = 0 V.

CONCLUSION

In 20 nm FD SOI devices, dynamic self-heating induces a transition in the Y-parameters in a similar frequency range as the drain to source coupling through the back-gate, thereby strongly affecting the extraction of the back-gate and substrate node parameters. This paper introduces equations describing the procedure to extract dynamic self-heating-free parameters from measured Y-parameters that only require the knowledge of the frequency-dependent complex thermal impedance. Removing the dynamic SHE from measurements enables the direct bias-dependent extraction of the back-gate and substrate related parameters, without the need of a compact model. Even though the main RF FoMs such as f_t and f_{max} are not affected by dynamic SHE, ignoring it can lead to unphysical extraction of (i) the back-gate and substrate parameters and (ii) the output conductance upon which many device metrics depend.

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