Back-Gate Lumped Resistance Effect on AC Characteristics of FD-SOI MOSFET

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***Abstract*— In this work, the impact of a large lumped resistor connected to the back-gate (B-G) of an fully depleted silicon-on-insulator (FD-SOI) transistor is studied. A related transition in the frequency responses of output conductance and capacitance is evidenced experimentally by *S*-parameters measurements in a large frequency range up to 40 GHz. However, present compact model does not correctly reproduce the B-G/substrate network behavior. This calls for a model accounting for both n-well and substrate networks. A small-signal equivalent circuit including distributed elements is thus proposed and compared with experimental results.**

***Index Terms*— Back-gate (B-G) modeling, fully depleted silicon-on-insulator (FD-SOI) MOSFET, RF extraction, substrate coupling, ultrawideband modeling.**

I. Introduction

THE continuous downscaling of CMOS technology has both increased integration and improved device performances. Ultrathin body and buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) technology offers outstanding electrostatic control, very low mismatch, high performance in terms of low-power, high-speed, as well as attractive analog, and RF figure of merit (FoM) [1]–[5]. Wideband device modeling is essential for technologies targeting RF and millimeter-wave (mm-wave) range applications and requires an accurate substrate network description. Indeed, it has been shown that the drain to source coupling through the back-gate (B-G) node [or Si substrate under the buried oxide (BOX)] induces a transition in the Y-parameters over frequency [6], [7]. Various substrate models have been proposed in the literature. In bulk technology, many letters have reported scalable models of the substrate network [8]–[10]. Distributed substrate models have also been proposed [11], [12]. Four-port measurements are beneficial because they offer a straightforward and complete/extensive extraction of small-signal elements for the transistor's model [12], [13].

With regard to integrated circuit (IC) design, shunt parasitics between the active transistor region and the lateral RF ground were shown to be nonnegligible contributors to FET performance for mm-wave switch applications and complement the well-known FoM $R_{\text{on}} \cdot C_{\text{off}}$ product [14]. Indeed, shunt conductance to the substrate ground cannot be compensated with matching circuits and therefore, will be a source of additional losses [14]. In mm-wave switches, the gate and B-G are biased through large resistances (these nodes can be considered RF floating). Furthermore, in RF and mm-wave circuits using the B-G bias as a tuning knob, it is easier and more compact to put a large resistor to decouple RF and dc signals than large decoupling capacitors from a layout perspective [15]. These additional shunt losses observed in mm-wave switch measurements [14], as well as the frequent RF and dc decoupling strategy used in high-frequency circuits motivate the study of the complex n-well/substrate network with a large resistance connected to the B-G.

In this letter, the impact of a large lumped resistance connected to the B-G on the output conductance and capacitance frequency responses is studied using wideband measurements. We observe that this lumped resistor changes the frequency response of both output conductance and capacitance, showing the importance of having a good B-G/substrate model. A new model capturing the complexity observed in the measurements with distributed elements is then proposed. Finally, the results of the extracted small-signal equivalent circuit (SSEC) are compared with measurements.

II. Structures and Measurements

A. Devices Description

An FD-SOI super-low threshold voltage (SLVT) nMOSFET from 22FDX[1] [2] featuring a gate length of 20 nm, finger width of 0.5 μm, 16 horizontal fingers, two vertical fingers, and a multiplicity of 4 for a total width of 64 μm is studied. Two different B-G configurations are analyzed, one with a large resistance connected to the B-G and another with no resistance, thus serving as a reference. Both devices are in a common source configuration. The first device (device A)

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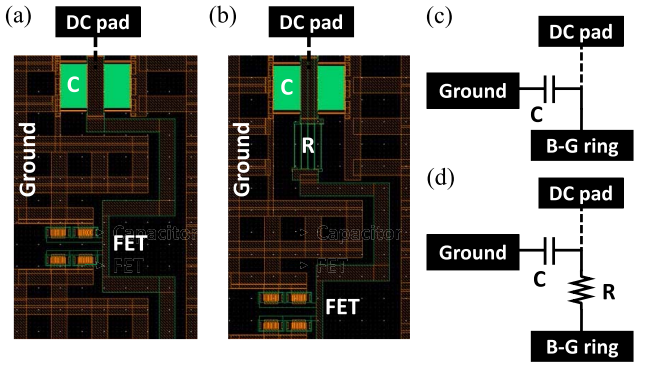

Fig. 1. Layout view of an FD-SOI nMOSFET with B-G connection consisting of (a) decoupling capacitance of 10 pF connecting the B-G to the ground and (b) large lumped resistor of ∼1 MΩ in addition to the decoupling capacitance. (c) and (d) Correspond, respectively, to the B-G connection schematics of (a) and (b).

features an access to the B-G with a decoupling capacitance of 10 pF connecting the B-G to the ground as shown in Fig. 1(a) whereas the second device (device B) adds, in addition to the decoupling capacitance, a large lumped resistor (∼1 MΩ) between the B-G dc pad and the B-G ring of the transistor as shown in Fig. 1(b). Schematics of their respective B-G connection are illustrated in Fig. 1(c) and (d).

B. Measurements

S-parameters are measured on-wafer from 10 kHz to 40 GHz using a vector network analyzer from Keysight. The B-G voltage (V_{bg}) is set to 0 V. The RF MOSFETs are probed using a ground-signal-ground (GSG) configuration. A short-open-load-thru (SOLT) calibration is performed and dedicated open and short structures are measured to deembed the transistor measurements down to the first metal layer.

Y-parameters are obtained from *S*-parameters measurements when the transistor is biased in saturation ($V_d = 0.8$ V) and at $V_g = 0.62$ V. This V_g point is chosen because it corresponds to the zero-temperature coefficient (ZTC) point of the studied devices. Indeed, as seen previously in [16], at ZTC bias point, the dynamic self-heating (SH) does not affect (to the first order) the ac curves and the observed transitions are thus related to the substrate effect.

Fig. 2 shows the variation of the output conductance $g_d(f)$ (solid lines) for both devices A and B biased at $V_{g,ZTC} = 0.62$ V, $V_d = 0.8$ V, and $V_{bg} = 0$ V. Looking at the measured output conductance of device A, a transition between 100 MHz and 10 GHz is clearly observed in the output conductance frequency response. Since the transistor is biased at ZTC point, and thus SH-related transition [16] is not expected to be observed, this transition is attributed to the substrate/B-G network effect. Moreover, one can observe a similar trend in the same frequency range (100 MHz and 10 GHz) for device B. However, in addition to this transition, another transition starting at lower frequency (around 300 kHz) also appears in g_d frequency response of device B. The only difference between devices A and B being the large lumped resistor (∼1 MΩ) connected to the B-G, this transition between 300 kHz and

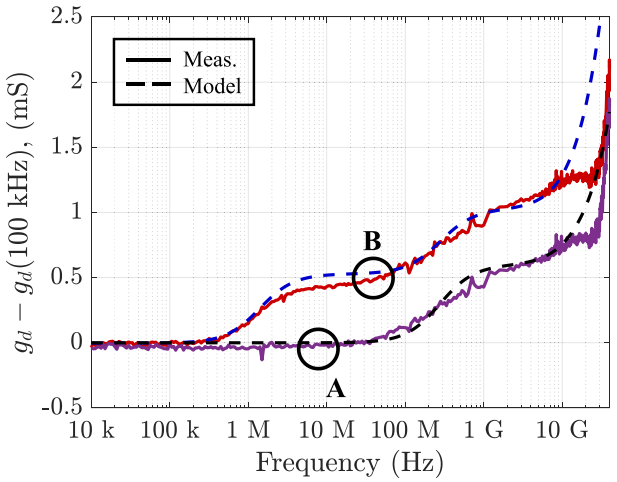

Fig. 2. Variation of the output conductance $g_d(f)$ (Re(Y_{dd})) w.r.t. its value at 10 kHz of a 20-nm FD-SOI nMOSFET (A) without a lumped resistor connected to the B-G terminal and (B) with a large lumped resistor (∼1 MΩ) connected to the B-G terminal. Measurements of both devices biased at $V_g = 0.62$ V, $V_d = 0.8$ V, and $V_{bg} = 0$ V in solid lines and model in dashed lines.

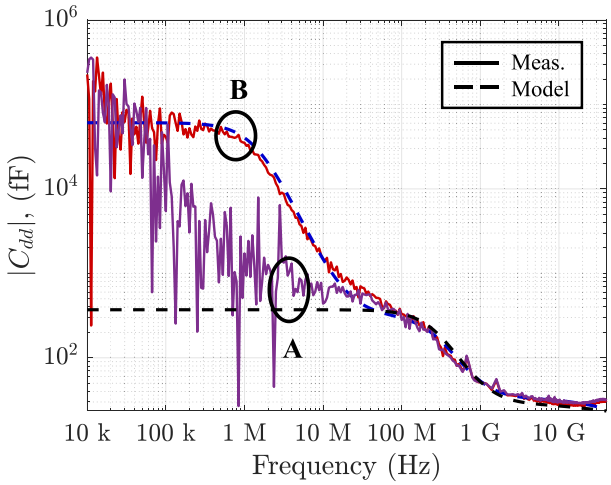

Fig. 3. Variation of the output capacitance $C_{dd}(f)$ (Im(Y_{dd})/ω) of a 20-nm FD-SOI nMOSFET (A) without a lumped resistor connected to the B-G terminal and (B) with a large lumped resistor (∼1 MΩ) connected to the B-G terminal. Measurements of both devices biased at $V_g = 0.62$ V, $V_d = 0.8$ V, and $V_{bg} = 0$ V in solid lines and model in dashed lines.

5 MHz is suggested to be related to the B-G connection. Similar trends are observed in the output capacitance C_{dd} computed as Im(Y_{dd})/ω in Fig. 3.

The additional step in both g_d and C_{dd} frequency response for device A can lead to an appreciable overestimation of SH effect when the RF extraction technique is applied (benchmark technique for such short device lengths). Hence, the relevance to correctly model the electrical substrate and B-G related transitions, for a proper SH parameters extraction [16].

III. Model and Extraction

A. Model Description

A schematic cross section of an FD-SOI SLVT nMOSFET is depicted in Fig. 4. The B-G access consists of a heavily doped n-type layer just under the BOX, or so-called

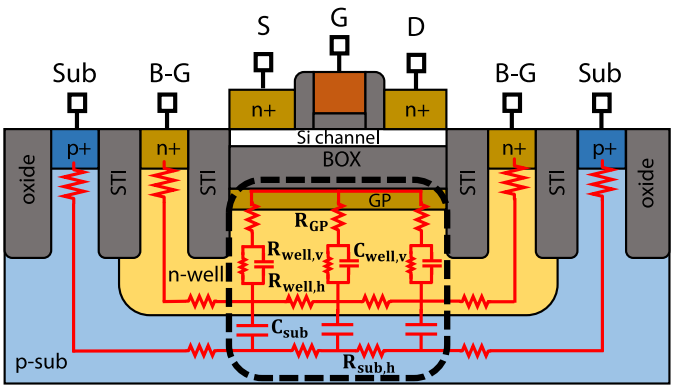

Fig. 4. Schematic cross section of an FD-SOI nMOSFET (not to scale) with distributed B-G/substrate impedance network.

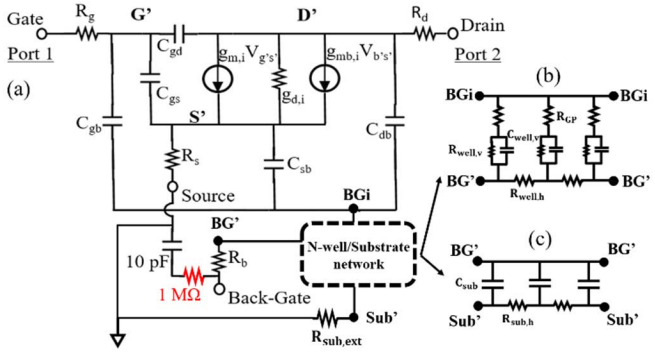

Fig. 5. (a) SSEC of an FD-SOI MOSFET including n-well/substrate network corresponding to the device B. N-well/substrate impedance network is represented in Fig. 4. On the right side, the independent distributed admittances (b) of the GP/n-well network and (c) of the substrate network are shown.

ground plane (GP), and an n-well contacted by a contact ring surrounding the transistor. Since the n-well/GP and substrate are distributed in nature, a distributed impedance network is proposed in Fig. 4 (dashed line) to correctly represent them.

The SSEC including the n-well/substrate network of Fig. 4 is presented in Fig. 5. In this case, a large lumped resistor (∼1 MΩ) is connected to the B-G node, thus corresponding to device B [Fig. 1(b)].

Analytical expressions of the n-well/substrate network are found by assuming two independent distributed admittances, one from the GP/n-well network and another from the substrate network. The admittance describing distributed elements can be derived from the telegraph equations [12].

B. Extraction

The parameters extraction is done in two steps using the experimental data obtained on both types of devices: device A (no additional resistor on its B-G) and device B (with a large resistor on its B-G) over a wide frequency range. First, series resistances (R_g, R_d, and R_s) are extracted in cold-FET regime ($V_d = 0$ V) using Bracale's method [17]. Other parameters including n-well/substrate network are then extracted by fitting simultaneously the SSEC proposed in Fig. 5 (without 1 MΩ resistor for device A) to the Y-parameters of both devices when transistors are biased in saturation ($V_d = 0.8$ V) and at ZTC bias point ($V_g = 0.62$ V). Device A and device B models are thus directly obtained from the best fit of the Y-parameters. All SSEC parameters of both devices are the same due to the extraction procedure, except for the large ∼1 MΩ resistance connected to the B-G of device B.

The model obtained for device B (Fig. 5) shows a good agreement with measurements as observed in Figs. 2 and 3 (dashed line). One can note that the transition at low frequency (∼300 kHz), observed in the output conductance frequency response of device B, disappears in device A model as expected. The other transition (between 100 MHz and 10 GHz), however, is present (as expected) being related to the n-well/substrate network impact on the g_d and C_{dd} frequency responses. The difference observed between the model and measurements of device A is probably related to the hypothesis of considering two independent distributed admittances for n-well and substrate. Using a coupled asymmetric transmission lines model is suggested as a way to further improve n-well/substrate network.

IV. Conclusion

In this work, the impact of the n-well/substrate network on the output conductance and capacitance frequency responses is studied through measurements and modeling of the devices with different configurations of B-G connection. A detailed analysis of experimental results highlighted that adding a large lumped resistor between the B-G dc pad and the B-G ring of the FET creates an additional transition between 300 kHz and 5 MHz in the g_d and C_{dd} frequency responses, to the transition observed between 100 MHz and 10 GHz, which attributed to n-well/substrate effect. This quest for an accurate compact model which considers not only intrinsic elements but also secondary effects related to "extrinsic elements" is essential for RF applications. Indeed, as it has already been demonstrated, neglecting such transitions in the electrical model of an FET can lead to significant misestimation of SH parameters for instance. A SSEC accounting for the distributed nature of the n-well/substrate has been thus proposed. Model parameters have been extracted at ZTC bias condition where Y-parameters are free from dynamic SH. The proposed model has shown good agreement with measurements.

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