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Back-gate bias effect on the linearity of pocket doped FDSOI MOSFET

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ABSTRACT

In this article, we investigate the feasibility of enhancing the linearity Figures of Merit (FoMs) by introducing pocket implant in the source/drain regions of the FDSOI MOSFET with ground plane (GP) under the influence of back-gate bias (V_B) effect. The current investigations are carried out using a well calibrated industry standard simulation tool Silvaco ATLAS. The proposed device architecture shows reduction in peak electric field, improvement in effective mobility (μ_{eff}), subthreshold slope (SS), threshold voltage (V_{TH}) & off-state current (I_{OFF}) by rearranging the accumulated charges that can mitigate impact ionization. The improvement in these parameters leads to enhanced the fundamental transconductance term (g_m) and in turn boosts the linearity, which can make it essential for RF/wireless IC designs. An investigation is performed to figure out the non-linear behaviour of proposed FDSOI MOSFET with pockets design by simulating the DC characteristics. The vital FoMs such as higher order transconductance coefficients, intermodulation distortion (IM) and input intercept point (IIP) are explicitly analysed along with the impact of V_B.

1. Introduction

The growing demand for technological advancements towards 5G communication systems in high frequency bands with stable operation and low coupling loss can be achieved by FDSOI MOSFET technology [1]. The SOI technology offers unique substrate and channel isolation with the help of an insulating material, preferably SiO_2 which can greatly diminishes the crosstalk phenomenon that is commonly observed in RF/wireless applications [2]. This feature of SOI technology makes it most appropriate for RF/wireless applications such as power amplifiers, low noise amplifiers and RF switches [3–6]. The power amplifier ICs utilize the back-gate bias feature of FDSOI-MOSFET for tuning the device performance which may lead to irregularities in the system [3]. Therefore it is indispensable to investigate the non-linearities of FDSOI MOSFET for reliable operation with back-gate bias feature.

Most of RF switches in present day are preferably fabricated using body contacted PDSOI technology and proved that body-bias feature is essential to achieve desirable linear operation even under large RF signal. However, the scalability of PDSOI is inferior due to its larger channel thickness and suffers from kink effect caused by impact ionization [5,7]. Some of the MOSFET technologies like cylindrical surrounding gate (CSG) MOSFET [8], gate material engineered cylindrical gate (GME CGT) MOSFET [9], underlap double gate (UDG) MOSFET [10] have been proposed to offer better linearity with complex architectures. However, the real world applications need more scalable, less complex and high packaging density designs that can be offered by FDSOI technology which tends to be free from kink effect. It can offer simpler designs and highly customizable substrates depending on the type of application [11,12].

Although, the FDSOI MOSFET offers high scalability and reduced short channel effects (SCEs) as compared to bulk CMOS technology [13,14], they suffer from self heating effects (SHEs) [15] which can degrade the device performance. One way to overcome these effects is to introduce p-implant (pockets) in source/drain (S/D) region of the device to rearrange the accumulated holes in the channel. This rearrangement of accumulated holes can reduce the peak electric fields and reduces the chance of impact ionization. Thereby, pockets in S/D regions can help in reduction of SHEs [16,17]. In addition to the pockets in S/D regions, FDSOI MOSFET technology offers superior threshold voltage modulation with the use of ground plane (GP) and back-gate bias effect [18–20]. With these characteristics combined, the device performance can be modulated between high performance (HP) and low standby power technology (LSTP) applications [21] depending on the consumer requirement without compromising on linear performance of the device.

Non-linear performance of a device often leads to system failure, which makes linearity an essential requirement for any system. Linearity in RF/wireless applications can be maintained with highly complex

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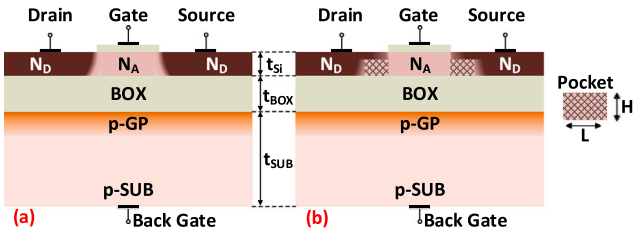

Fig. 1. Cross-section view of n-type (a) conventional FDSOI MOSFET without pockets, and (b) FDSOI MOSFET with pockets.

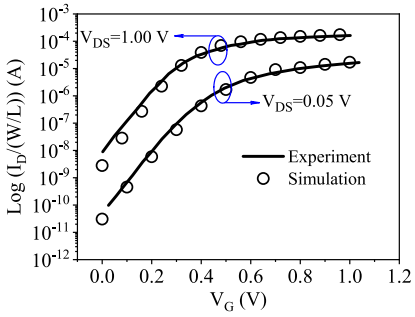

Fig. 2. Calibration with measured data of 28 nm FDSOI n-type MOSFET consists of high-k dielectric as gate stack on top of SiON interfacial layer with gate oxide thickness of 1.2 nm, silicon body thickness of 7 nm without any intentional channel doping, BOX thickness of 25 nm and the ground-plane is under the BOX at T = 300 K, the drain current is normalized for TCAD by taking W = 1 μm (typical value for 2D simulations) [29,30].

circuits. Efforts made at device level towards high linearity is much appropriate and can help in reducing area, power & complexity of the design [8–10,22–27]. The linearity study at device level involves investigation of linearity FoMs namely: higher order transconductance coefficients, intermodulation distortion (IM), and input intercept point (IIP). They play a major role in the investigation towards more linear operation of the device. A quantitative study on linearity FoMs is highly appropriate.

The objective of the work presented here involves:

- Introduction of pockets (optimized at 3 nm × 4 nm) in S/D region of FDSOI MOSFET with GP using calibrated simulation tool Silvaco ATLAS [28] with measured data [29,30].
- The benefit of adding pockets in S/D regions of FDSOI MOSFET with GP in a comparative investigation.
- The advantage of back gate bias (V_B) on the DC characteristics for the optimized FDSOI MOSFET with pockets implant is evaluated.
- Extraction of linearity FoMs from the DC characteristics [23,31] of the proposed device for linearity investigation.

The complete work is organized as follows: Section 2 gives the geometrical nomenclature of the proposed FDSOI MOSFET GP with pockets architectures in comparison with conventional one. Section 3 presents the simulation methodology. Section 4 gives a comprehensive understanding on the benefits of adding pockets in S/D regions. Section 5 explains the linearity FoMs from the DC characteristics for the proposed device. Section 6 presents the concluding remarks on the work.

2. Proposed structure configuration

Fig. 1(b) gives a schematic representation of the proposed structure FDSOI with pockets, along with the conventional FDSOI structure in Fig. 1(a). The location of pockets is clearly mentioned in Fig. 1 with the dimensions as length (L) and height (H) in nanometres (nm). It is expressed as L×H (nm× nm) pockets size for better understanding of pockets optimization. Both the devices have p-GP, since they are n-type MOSFETs that can help to suppress the depletion region under BOX which can improve the channel mobility [18,20,32]. The nomenclature of both the devices are almost the same except for the additional p-implant (same as channel doping) in the S/D regions of FDSOI. The geometrical nomenclature for both the devices is presented in Table 1.

3. Simulation methodology and fabrication procedure

The simulations are carried out in a technology computer aided design (TCAD) tool Silvaco ATLAS [28]. To carry out the simulations with utmost accuracy, the TCAD tool is calibrated to the measured data in [29]. The physical models used for calibration in Fig. 2 are similar to the current investigations. The physical models used are, concentration dependent Shockley–Read–Hall (SRH) which specifies the SRH recombinations at concentration dependent lifetimes. For accurately measuring high current densities, Auger recombination is reckoned. To observe the velocity saturation and heavy doping effects, field and concentration dependent mobility models are incorporated. Since, the S/D regions are heavily doped it is suggested to reckon band gap narrowing effects. The Selberherr's model is selected to capture the impact ionization phenomenon in the device. For obtaining the solutions, the simulations are carried out in an iterative fashion which uses numerical methods to obtain the results to the particular bias conditions [28].

The fabrication process flow for the proposed device can be achieved by following the process steps as shown in Fig. 3. The procedure involves two stages i.e., first stage is to obtain the FDSOI wafer [33]. It involves (i) two initial silicon wafers A & B, in which B wafer is having a P+ ground plane, typically the ground-plane is a well type implantation under the BOX. (ii) Oxidation is done for wafer A which can be later used as buried oxide. (iii) H+ implantation is done for donor wafer A to weaken the bonds. (iv) Wafer bonding is done for wafer A & B. (v) Smart Cut procedure reported by LETI [34] is done to separate the donor wafer and planarization is done by annealing and chemical mechanical polishing (CMP) finishes the first stage to obtain SOI wafer. The second stage of the fabrication process involves obtaining the proposed device structure i.e., (vi) Acceptor (N_A) doping through ion-implantation and ultra-thin SiO_2 formation for gate-oxide. (vii) Patterning of gate electrode for self-aligning the source and drain regions. (viii) Formation of the double spacers, outer spacer 2 in orange and inner spacer 1 in blue. Spacers 1 & 2 are of different materials. And source/drain donor (N_D^+) ion-implantation. (ix) Selective removal of the spacer 2 and shallow N_D^+ implantation. This step requires greater attention by the process engineer as the implantation must be done with low implantation energy and low dose rates in order to leave N_A doping at the bottom of the thin film. (x) Metallization and contacts formation finishes the second stage to fully obtain the proposed device structure [16,18].

4. Effect of pockets on device performance

In this section, we investigate the benefits of adding pockets/implant to FDSOI MOSFET in S/D regions. Although SOI devices are better suited for RF applications, they suffer from impact ionization which reduces the device performance by degrading the electron mobility caused by high electric fields in S/D regions. The pockets help in disseminating the accumulated charges at the S/D regions, thereby reducing the peak electric field and impact ionization [16,17,35].

To elaborate the above mentioned advantages of adding pockets the investigations are carried out essentially by extracting the DC transfer characteristics, transconductance (g_m), second- and third-order transconductance coefficients (g_{m2} & g_{m3}) for FDSOI-GP with and without pockets implant at high drain potential (V_D = 1 V) as depicted in Fig. 4(a), Fig. 4(b), Fig. 4(c) and Fig. 4(d) against gate overdrive voltage (V_{GS} - V_{TH}), respectively. The memoryless or static non-linear

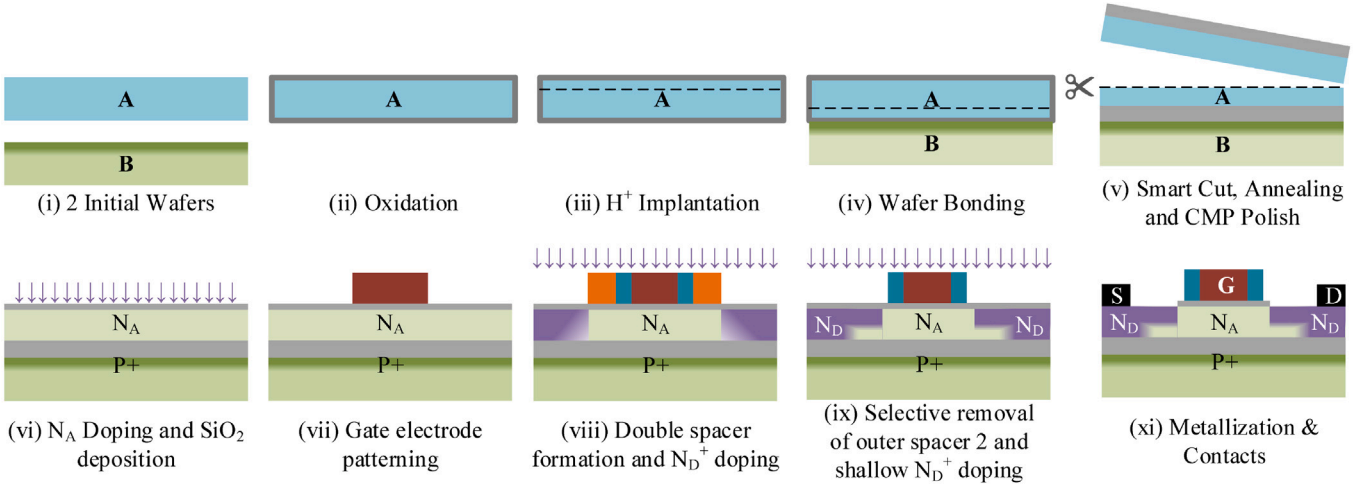

Fig. 3. Fabrication process flow for the proposed device structure.

Table 1
Geometrical nomenclature for both the devices.

Technology parameter	Symbol	FDSOI without pocket	FDSOI with pocket
Channel length	L_G	22 nm	22 nm
Silicon thickness	t_{Si}	6 nm	6 nm
Buried-oxide (BOX) thickness	t_{BOX}	25 nm	25 nm
Gate-oxide thickness	t_{OX}	1 nm	1 nm
Substrate thickness	t_{SUB}	50 nm	50 nm
Gate metal workfunction	ϕ_M	4.71 eV	4.71 eV
S/D doping	N_D^+	10^{20} cm^{-3} Gaussian profile (σ = 0.5 μm)	10^{20} cm^{-3} Gaussian profile (σ = 0.5 μm)
Channel doping	N_A	10^{14} cm^{-3} Gaussian profile (σ = 0.5 μm)	10^{14} cm^{-3} Gaussian profile (σ = 0.5 μm)
Substrate doping	p_{SUB}	10^{15} cm^{-3} uniform profile	10^{15} cm^{-3} uniform profile
p-GP doping	p_{GP}	10^{18} cm^{-3} Gaussian profile (σ = 0.5 μm)	10^{18} cm^{-3} Gaussian profile (σ = 0.5 μm)
Pocket length	L	–	3 nm
Pocket height	H	–	4 nm

characteristics of output I_D with respect to gate–source voltage (V_{GS}) can be modelled using Taylor series expansion [31], and given by:

$$I_D \approx g_{m1}V_{GS}(t) + g_{m2}{V_{GS}}^2(t) + g_{m3}{V_{GS}}^3(t) + \cdots + g_{mn}{V_{GS}}^n(t) \quad (1)$$

where, g_{m1}, g_{m2}, g_{m3}, …, g_{mn} are the transconductance coefficients responsible for producing static non-linearity due to its dependency on I_D with the input signal $V_{GS}(t)$. Static or memoryless non-linearity occurs when input has direct dependency on output.

From Fig. 4(a) & (b) we can observe that the FDSOI with pockets implant has lower I_{OFF} with slight compromise in I_{ON} and peak-g_m, while predominantly improving the subthreshold slope (SS) and I_{OFF} in comparison with the FDSOI without pockets implant. The higher order derivatives of g_m give us a preliminary device behaviour towards non-linearity, lower values of g_{m2} and g_{m3} predict improved linearity. From Fig. 4(c) & (d) we can observe the FDSOI with pockets implant has slightly lower g_{m2} and g_{m3} in major part of the gate overdrive sweep in comparison to FDSOI without pockets implant. This suggest an enrichment in the non-linear performance of the device along with improvement in static, analog/RF device performance parameters.

For a clear understanding of providing the pockets a comparison between the important device parameters: SS, V_{TH}, I_{OFF}, I_{ON} & peak-g_m is done for both the devices as shown in Table 2. The above

Table 2
Device parameters extracted using Silvaco ATLAS-parameter extraction tool [28].

Device	SS	V_{TH}	I_{OFF}	I_{ON}	Peak-g_m
FDSOI without pockets	94.5 mV/dec	0.22 V	6.2×10^{-9} A	6.1 mA	91.9 mS
FDSOI with pockets	82 mV/dec	0.26 V	4.24×10^{-10} A	5.7 mA	89.7 mS

mentioned parameters have been extracted from the parameter extraction tool of Silvaco ATLAS [28]. From the table we can summarize that a substantial improvement in SS (reduced by 13%) and I_{OFF} (reduced by 93%) of FDSOI device with pockets while a slight compromise in I_{ON} and peak-g_m in comparison with FDSOI device without pockets.

To further understand the benefits of adding pockets in S/D region to FDSOI MOSFET, a charge concentration diagram under off-state (V_{GS} = 0 V, V_{DS} = 0 V) and in saturation (V_{GS} = 1.2 V, V_{DS} = 1 V) without considering the back-gate bias (V_B = 0 V) influence for both the devices is presented in Fig. 5. It is elucidated as follows:

(1) Firstly, the devices are kept under off-state as shown in Fig. 5(a) and 5(b). It can be interpreted that the charge concentration is directed towards S/D-channel junctions and not below the gate-oxide predicting

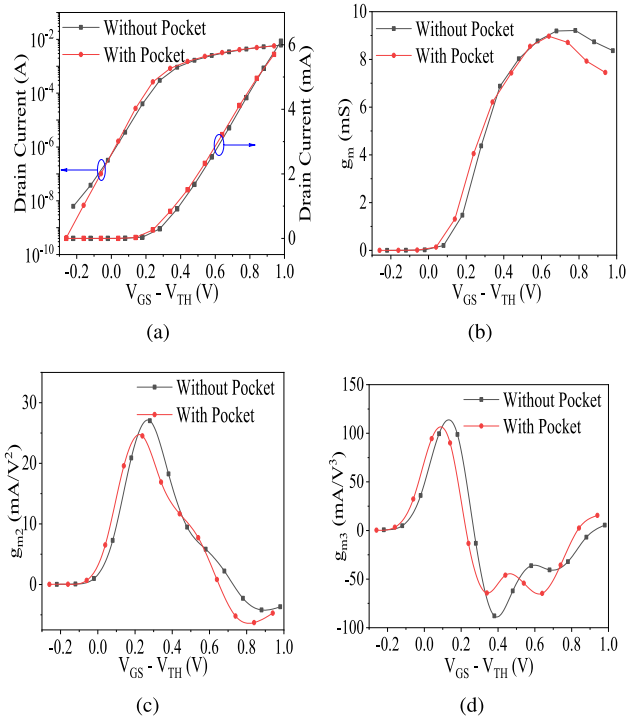

Fig. 4. Transfer characteristics & transconductance coefficients against gate overdrive voltage for FDSOI-GP with and without pockets implant. (a) Transfer characteristics, (b) g_m, (c) g_{m2} and (d) g_{m3} under high drain bias (V_D = 1.0 V).

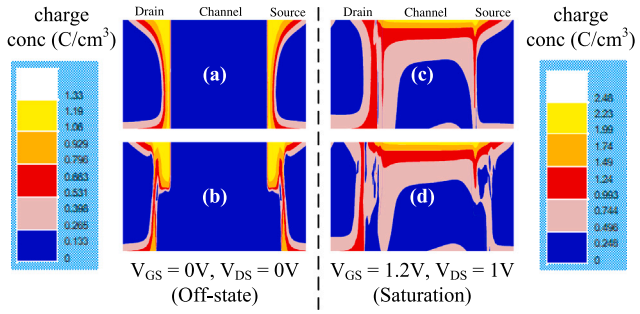

Fig. 5. Charge concentration contours of drain-channel–source regions, respectively across the silicon channel thickness for FDSOI (a) without and (b) with pockets implant in off state, and FDSOI (c) without and (d) with pockets implant under saturation regime.

the off-state behaviour for both the devices. The FDSOI without pockets in Fig. 5(a) can be observed to that the charges are densely concentrated over the entire channel thickness at S/D junctions. Whereas, the charges are having thin charge concentration at the pockets in FDSOI with pockets implant which is transparent from Fig. 5(b) suggesting lower peak electric field under off-state.

(2) Similarly, the devices are kept under saturation as shown in Fig. 5(c) and 5(d). The charge concentration in channel under the gate-oxide region is predicting the formation of strong inversion region. The benefits of pockets can be observed at the junction(s) where a broader charge concentration profile is observed for the FDSOI without pockets implant as shown in Fig. 5(c). Whereas, charges are incapable of accumulating in the FDSOI with pockets implant in Fig. 5(d), owing to the extra room for charges to occupy in the channel predicting lower peak electric field and thereby improved electron mobility under saturation.

The electric field and electron mobility cut-line plots give a comprehensive understanding on the benefits of device with pockets and it

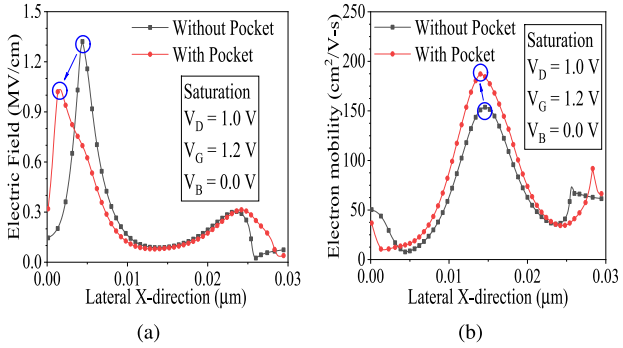

Fig. 6. Cut-line of (a) electric field and (b) electron mobility under saturation regime (V_D = 1.0 V, V_G = 1.2 V, V_S = 0 V).

is plotted in Fig. 6(a) and Fig. 6(b), respectively. The cut-line is drawn across the channel (drain side pocket-channel–source side pocket, respectively) lateral x-direction and 1 nm above the Si-BOX interface to estimate the benefit of adding pockets in S/D regions. The electric field of FDSOI with pockets implant is predicted to show lower peak at the drain-channel junction in comparison with the FDSOI without pockets implant suggesting the rearrangement of accumulated charges is indeed true as presented in the charge concentration contour in Fig. 5. In lieu with the reduction in peak electric field, the electron mobility also improved in the channel region as shown in Fig. 6(b) suggesting that the extra space provided by the pockets help the electrons move more freely, implying the improvement in channel mobility for the FDSOI device with pockets [16,17].

5. Extraction of linearity FoMs considering back-gate bias variation

Since, the FDSOI device with pockets showed improved performance in comparison to the without pockets implant as discussed in Section 4, hence a comprehensive investigation on memoryless or static linearity FoMs [31] is carried out quantitatively for the structure proposed in Fig. 1(b). The linearity FoMs are extracted numerically from the DC transfer characteristics [23], by varying the back gate voltage (V_B) from −1 to +1 V with a +0.5 V step size at high drain bias (V_D = 1.0 V) as shown in Fig. 7(a). It can be interpreted from Fig. 7(a) that the back-gate bias variation has actively shifted the V_{TH} suggesting superior device tuning by utilizing the GP and back-gate bias effect [18,20,32]. The advantage of providing pockets in S/D sides has been briefly investigated in Section 4. Pockets can help in rearranging the accumulated charges generated by higher electric fields that can boost the performance of device by lowering off-currents, peak electric field & increasing channel mobility. The pockets implant combined with GP and back-gate biasing help to achieve better performing devices which can be implemented in low and high power applications [16,17].

5.1. Transconductance coefficients (g_{m1}, g_{m2} & g_{m3})

The coefficients g_{m1}, g_{m2} & g_{m3} are primarily responsible for producing the static non-linearity in small signal operation of the MOSFET and the higher order coefficients g_{m4}, g_{m5}, g_{m6}, etc. are of significance only during the large signal amplitude ($A > 0.2\times V_{DD}$) operation which is not the scope of current work. Henceforth, the investigation is carried out only for g_{m1}, g_{m2} & g_{m3} which are later used for finding the linearity FoMs. They are obtained by differentiating (1) with $V_{GS}(t)$, and given by [36]:

$$g_{mn} = \frac{1}{n!}\frac{\partial^n I_D}{\partial V_{GS}(t)^n} \quad at \quad V_{GS}(t) = 0 \tag{2}$$

where n = 1, 2, 3. The coefficients g_{m1}, g_{m2} & g_{m3} obtained after solving (2) and are plotted against gate overdrive voltage when subjected to

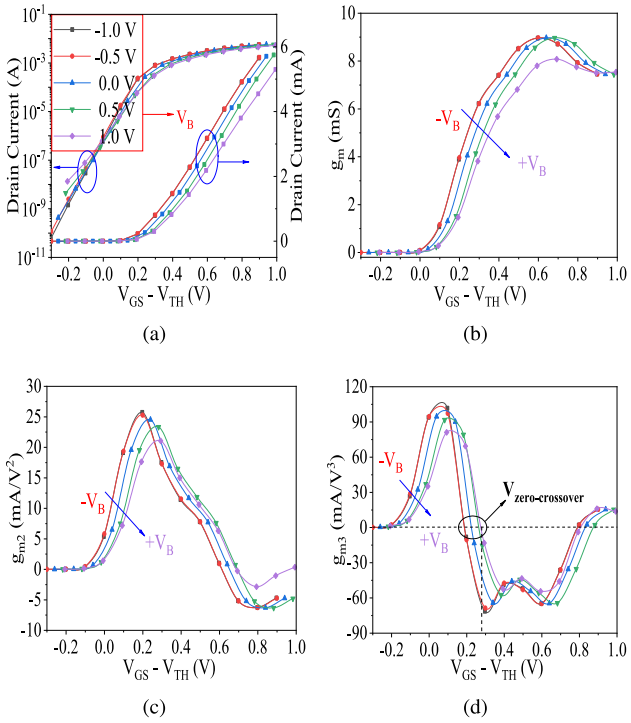

Fig. 7. Transfer characteristics & transconductance coefficients against gate overdrive voltage by varying back-gate bias (V_B). (a) Transfer characteristics, (b) g_m, (c) g_{m2} and (d) g_{m3} under high drain bias (V_D = 1.0 V).

variation in back gate biasing from −1 V to +1 V with a step of 0.5 V under high drain bias (V_D = 1.0 V), which is illustrated in Fig. 7(b), (c) & (d), respectively.

To explain the effects of pockets, GP and V_B effects on the fundamental g_m (= g_{m1}) can be interpreted from (3) as given below [10,37]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = (\mu_{eff}\frac{W}{L_{eff}})(Q_s - Q_d) \tag{3}$$

where μ_{eff} is the effective mobility, L_{eff} is the effective channel length, W is the width of the device (= 1 μm for 2D-TCAD), Q_s&Q_d are source and drain charges (contours presented in Fig. 5 give a fundamental insight toward charge accumulation at S/D-channel regions in off-state and saturation) respectively. The g_m in Fig. 7(b) is observed to be enhanced with increase in gate overdrive voltage and a clear change in g_m for a change in V_B indicating good tuning under high drain potential. Peak g_m is observed at moderate inversion region of the gate overdrive voltages for all V_B suggesting early velocity saturation [16].

By incorporating pockets on either sides of the channel, the accumulated charges rearrange in the pockets as discussed in Fig. 5, which improves the μ_{eff} and fundamental g_m [16,17]. Furthermore, varying back-gate bias for a ground plane FDSOI MOSFET can better tune the device performance. It can be noticed that the V_B variation is having direct influence on I_D which makes tuning of V_{TH} possible with suppressed depletion under BOX in presence of GP [18]. Consequently, the V_B modulation can effectively tune the electric field distribution in the channel leading to a well enhanced and well controlled device for applications like RF, low standby power technology (LSTP) and high performance (HP) [18,20,38].

For g_{m2} the effect of pockets, GP can be interpreted from taking the partial derivative with V_{GS} of (3), we get:

$$\frac{\partial g_m}{\partial V_{GS}} = \frac{\partial^2 I_D}{\partial V_{GS}^2} = (\mu_{eff}\frac{W}{L_{eff}})\frac{\partial(Q_s - Q_d)}{\partial V_{GS}} \tag{4}$$

The g_{m2} is the second order non-linearity transconductance coefficient, it is responsible for causing the second order distortions in the system and it is analytically obtained by taking n = 2 in (2), it is plotted in Fig. 7(c) under high V_D by varying V_B. Please note that the actual value of g_{m2} plotted in Fig. 7 is taken from (2) when n = 2, the expression in (4) is used to explain g_{m2} for the sake of better understanding the physics involved.

In (4) we can interpret that at lower gate voltage (V_{GS}) values, the impact of $(Q_s - Q_d)$ on g_{m2} is higher. And the influence of $(Q_s - Q_d)$ on g_{m2} is nullified at higher V_{GS} values. We can observe the same from Fig. 7(c) at incrementing the gate voltage for high V_D the influence of $(Q_s - Q_d)$ on g_{m2} is significant until the peak-g_{m2}. And, the peak-g_{m2} drops due to a higher gate voltage and drain potential which can provide required $(Q_s - Q_d)$ to gradually drop $\partial g_m/\partial V_{GS}$ with actively tuning the $\partial g_m/\partial V_{GS}$ by varying V_B [10,20].

Similarly, g_{m3} is the third order transconductance coefficient or second order derivative of g_m i.e, $\partial^2 g_m/\partial V_{GS}^2$. It is responsible for causing the third order distortions in a system it can be obtained analytically after solving n = 3 in (2). The solution is plotted against gate overdrive voltage at high V_D as shown in Fig. 7(d). The g_{m3} is observed to have a positive slope in lower gate overdrive values suggesting the device to have higher distortions. The low values of g_{m3} manifests low distortions and the zero-crossover point ($V_{zero-crossover}$) gives the optimum dc bias point of a system. Further increasing the gate overdrive voltage cause the g_{m3} to become lower and tuning of g_{m3} can be observed while V_B is varied. At higher gate overdrive voltages the device is observed to have high g_{m3}. It can be agreed that the device should be operated in between zero-crossover point and moderate inversion regions of the gate overdrive voltages for better control on the distortions and more linear operation of the system [9].

Although, the non-linearity performance of the device can be application specific, finding optimal V_B value to operate the device in a more linear fashion without compromising in device performance can be tricky. For LNA application, it is necessary to operate the device at low power i.e., close to V_{TH}. In the mentioned region, the reduction in peak g_{m2} (from Fig. 7(c)) can be observed at V_B = 1.0 V which signifies more linear behaviour. On the other hand, for PA application, it is imperative to operate the device at high bias condition. Again, another minima for g_{m2} can be seen at V_B = 0.5 V that is making the device more suitable for PA application. Similarly, for g_{m3} to operate the device at zero-crossover (close to V_{TH}), the negative V_B predict lower g_{m3} which can be better suited for LNA application. Whereas, the negative V_B fails to predict lower g_{m3} values under high bias condition, which is required for PA application. Hence, it can be strenuous for a designer to select the optimal V_B condition by comparing trade-off between the distortion terms and performance metrics for a more linear behaviour.

5.2. *Intermodulation Distortion terms (IM_2 & IM_3)*

The intermodulation distortion terms (IM_2 & IM_3) are the integral part of non-linear characteristics exhibited by a transistor in static or memoryless operation during dual tone mode with direct dependency on the input signal amplitude (A). This can cause degeneration of signal in RF/wireless applications which is undesirable. Signal amplitude plays a major role in causing non-linearity in a system which can lead to distortions. Hence, a low constant small signal amplitude of 20 mV (A = 20 mV) is selected in the whole investigation to agree with the distortion expressions presented [10,23,31].

$$IM_2 = 20\log\left(\left|\frac{g_{m2}}{g_{m1}}\right| A\right) \tag{5}$$

$$IM_3 = 20\log\left(\frac{3}{4}\left|\frac{g_{m3}}{g_{m1}}\right| A^2\right) \tag{6}$$

The intermodulation distortion caused by the g_{m2} coefficient which gives dual tone distortions to the fundamental (g_m) is called IM_2 and

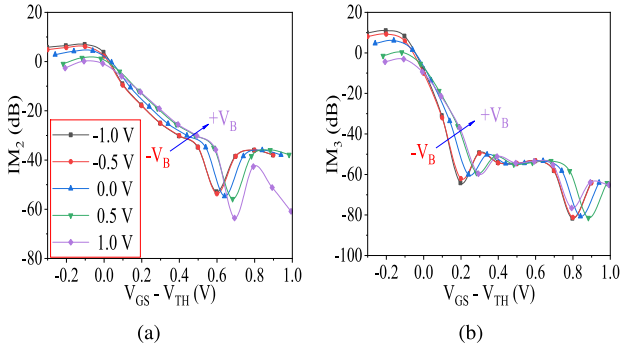

Fig. 8. Intermodulation distortion (a) IM_2 and (b) IM_3 plotted against gate overdrive voltage by varying back gate bias (V_B) under high drain bias (V_D = 1.0 V).

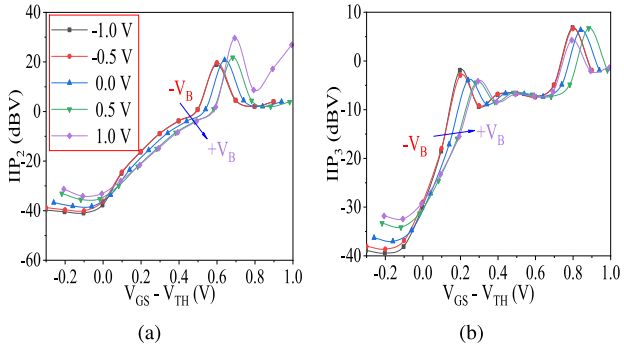

Fig. 9. Input intercept points (a) IIP_2 and (b) IIP_3 plotted against gate overdrive voltage by varying back gate bias (V_B) under high drain bias (V_D = 1.0 V).

is given by (5) [31]. The IM_2 is plotted for high V_D against gate overdrive voltage in Fig. 8(a) while V_B is varied. The IM_2 can be seen to monotonically reduce when increasing the gate overdrive voltage. It can be observed that V_B modulation allows us to find a dip in IM_2 for all V_B, this dip in IM_2 can predict very low distortions in the system [9,10,20,23].

Similarly, the intermodulation distortion caused by the g_{m3} is called IM_3 and is given by (6) [31]. The IM_3 is plotted for high V_D against gate overdrive voltage in Fig. 8(b) while V_B is varied. The degeneracy caused by IM_3 at high V_D can be interpreted by its mobility behaviour. The term $\partial^2 g_m/\partial V_{gs}^2$ gives the dip or minima in IM_3 plot each dip predicts a transition in mobility [9,10]. Mobility of a device can be greatly affected by its transverse electric field when a high drain potential is applied. If the electric field is high then mobility tends to become lower, this can predict a high chance of impact ionization and non-linear performing device which can be mitigated by the pockets as explained in Section 4. This improved mobility in the channel helps in achieving a constant IM_3 between strong and moderate inversion regions. This feature of low distortions and tuning with V_B variation can be well suited for power amplifiers in which the threshold voltage of power amplifier can be changed without compromising on the linearity [1,3,39].

5.3. Input Intercept Points (IIP_2 & IIP_3)

The input intercept points (IIP_2 & IIP_3) have similar context to IM_2 & IM_3 that give dual tone non-linear behaviour. But, the levels of IM_2 & IM_3 are directly dependent on the input signal which increases the complexity in finding their relative values without knowing the input signal amplitude (A). On the other hand, the IIP_2 & IIP_3 detect the whole IM_2 & IM_3 without depending on A. Hence, IIP gives the entire IM_2 & IM_3 independent of the input signal amplitude [9,31].

$$IIP_2 = 20\log\left(\left|\frac{g_{m1}}{g_{m2}}\right|\right) \tag{7}$$

$$IIP_3 = 20\log\left(\sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|}\right) \tag{8}$$

The second-order input intercept point (IIP_2) is defined as the ratio of fundamental to the second-order transconductance coefficient and is given by (7) [31]. The IIP_2 evaluated for high V_D against gate overdrive voltage in Fig. 9(a) while varying V_B. It can be interpreted from (7) that high g_m and low g_{m2} predicts higher IIP_2 values which can improve the device linearity. At maximum g_m (Fig. 7(b)), a peak can be observed in Fig. 9(a) suggesting better linearity at that particular bias point and tuning of the peak is done by varying V_B. For IIP_2 at high V_D the values are increasing gradually due to g_m and g_{m2} being biased at high drain potential by improving μ_{eff} and $(Q_s - Q_d)$ terms which can in turn mitigate the impact ionization phenomena that generally occur at high drain potential without affecting the device performance and improving linearity [9,16–18,20].

The third-order input intercept point (IIP_3) has similar context to IM_3 which dual tone behaviour of IM_3 without depending on the input A. It is defined as the ratio of square-root of fundamental to the third-order transconductance coefficient and is given by (8) [31]. The IIP_3 is plotted against gate overdrive voltage while varying V_B at high V_D in Fig. 9(b). Improved IIP_3 values probe to a more linear system [9]. It can be observed in Fig. 9(b) that the IIP_3 at zero-crossover point followed by strong inversion region shows constant values while varying V_B, which can manifest to better control on linear operation by utilizing the back-gate bias engineering, GP and pockets implant which make it suitable for amplifiers that need to change the gain and do not want to compromise on linearity [16–18,20].

6. Conclusion

In summary, a comparative investigation of FDSOI MOSFET with and without pockets implant is done. The FDSOI MOSFET with pockets implant is observed to have improved channel mobility, reduced peak electric field, rearrangement of accumulated charges, improved SS (reduced by 13%) and I_{OFF} (reduced by 93%) while, a slight compromise in I_{ON} and peak-g_m. Hence, the FDSOI MOSFET with pockets implant has been investigated to check the feasibility to enhance the linearity performance of the device. The investigation predicts that the DC characteristics by varying V_B for high V_D is explicitly used to extract the following linearity FoMs from a memoryless or static characteristics: g_m, g_{m2}, g_{m3}, IM_2, IM_3, IIP_2 & IIP_3. It has been observed that the improvement in the μ_{eff}, reduction in peak electric field & rearrangement of accumulated charges has lead to improvement in fundamental with actively tuning the V_{TH} by varying V_B. From the analysis of $V_{zero-crossover}$, negative back-gate bias values can be preferred to achieve low distortions that can manifest high linearity behaviour for the FDSOI-GP with pockets implant device.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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