A 2.5-2.6 dB Noise Figure LNA for 39 GHz band in 22 nm FD-SOI with Back-Gate Bias Tunability

L. Nyssens[#], M. Rack[#], S. Wane[$], C. Schwan[*], S. Lehmann[*], Z. Zhao[*], L. Lucci[%], J. Lugo-Alvarez[%], F. Gaillard[%], J.-P. Raskin[#], D. Lederer[#]

[#] Université catholique de Louvain, Louvain-la-Neuve, Belgium
[$] eV-Technologies, Colombelles, France
[*] GlobalFoundries, Dresden, Germany
[%] CEA-Leti, Université Grenoble Alpes, Grenoble, France
lucas.nyssens@uclouvain.be

***Abstract* — This paper presents a 2-stage low-noise amplifier (LNA) designed in 22 nm fully-depleted silicon-on-insulator (FD-SOI) technology, covering the N259 and N260 millimeter-wave 5G bands. The prototype features 19.9 dB peak gain, 2.5-2.6 dB noise figure (NF) and 6.6 GHz bandwidth (intersection of 3 dB gain flatness and -10 dB input/output matching), -5.4 dBm third-order input intercept point (IIP3) for a 20.8 mW power dissipation. Modulating the back-gate bias of each stage independently switches the LNA operation mode from a combination of low-noise (0.8 dB variation in NF), high-linearity (~3 dB variation in IIP3) and/or low-power (down to 7.4 mW). Finally, a careful noise contribution analysis of the input matching identifies a 0.58 dB main contribution from the input spiral inductor. EM simulations show that a 0.06 dB improvement in NF can be achieved by using a high-resistivity substrate, if the input inductor design is optimized by stacking several metal layers.**

***Keywords*—Low-noise amplifier, FD-SOI CMOS, millimeter-wave, Back-gate bias, 5G, spiral inductor.**

I. Introduction

The massive deployment of 5G wireless systems, addressing the ever growing demand of high data rate and capacity, requires low-cost, multi-functional and multi-mode front-end modules. Aggressive device downscaling and parasitic optimization has enabled high-performance silicon (Si) technologies for millimeter-wave (mm-wave) applications. Together with its low-cost and high integration of digital and analog circuits, CMOS technologies are great contenders for 5G fully integrated front-end modules.

The low-noise amplifier (LNA) is the most critical block in a receiver. It exhibits trade-offs between important performance parameters, namely noise figure (NF), gain, power dissipation (P_{dc}) and linearity. Fully-depleted silicon-on-insulator (FD-SOI) technologies are particularly suited for mm-wave applications with great f_t, f_{max} and NF_{min} among CMOS technologies [1], [2]. Additionally, the back-gate access represents a unique tuning knob offering more configurability. FD-SOI LNAs have already demonstrated sub-2 dB NF at 28 GHz [3] or wideband LNAs with close to 3 dB NF covering 28 and 39 GHz bands [4]. Despite excellent features of FD-SOI technologies that pushed the trade-off corners to higher performances, designing a sub-3 dB NF LNA at mm-wave frequencies remains challenging. This work presents an LNA designed in 22 nm FD-SOI process covering the N259 and N260 5G bands (39 GHz) [5]. The LNA design procedure is explained in Section II. Section III presents its on-wafer measurements at nominal bias. Section IV provides a detailed analysis of the circuit behavior with back-gate bias tuning. Finally, Section V identifies the main noise contributor in the input matching and explores potential improvement that can be achieved by using a higher resistivity silicon substrate.

II. Circuit Design

The LNA is designed with the cascode common-source with inductance degeneration topology. A simplified schematic is shown in Fig. 1 and a die photo of the fabricated prototype in Fig. 2 (a).

The LNA is designed in GlobalFoundries' 22FDX® technology, with a mm-wave back-end of line (BEOL). This BEOL (Fig. 2 (b)) includes 4 layers with thicknesses greater than 1 µm (JA to LB). The super-low threshold voltage nMOS with high f_t, high f_{max} and low NF_{min} performances is chosen in this design with the nominal gate length of 20 nm. A relaxed contact-poly-pitch (CPP) of 208 nm (2xCPP) enables to boost the f_t and f_{max} performance [6] at the cost of a slightly larger active layout area, which remains negligible at circuit-level, whose total area is dominated by that of the passives. The gate bias of M_1 & M_3 (V_{g1}) of 0.4 V yields lowest NF_{min} with sufficiently large f_t & f_{max} (Fig. 6 (a)). The voltage bias M_2 & M_4 is determined to have equal voltage drop on each device.

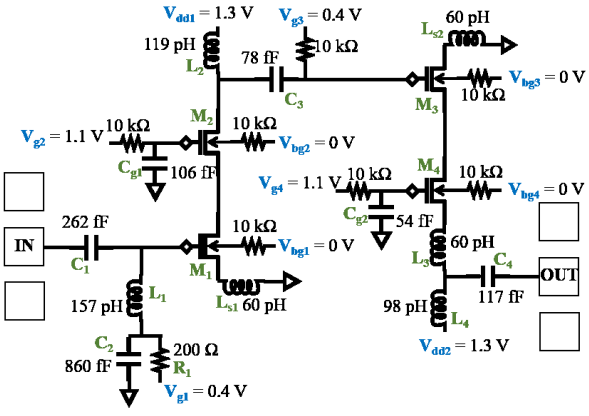

Fig. 1. LNA schematic, with bias and component values.

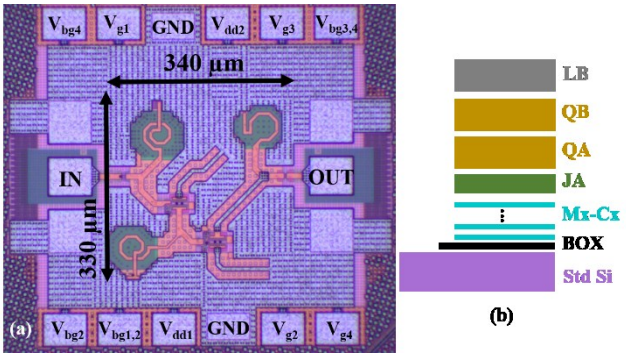

Fig. 2. (a) Die photo of the 39 GHz LNA prototype. Core size of 0.34 x 0.33 mm^2 and 0.6 x 0.62 mm^2 including all pads. (b) MM-wave BEOL in 22FDX®.

The FET's total width is selected based on trade-offs among input matching, noise matching and power dissipation. All FETs have the same dimensions. Linearity performances including third-order input referred intercept point (IIP3) and 1 dB compression point are g_{ds} limited. Therefore, the V_{dd} bias of 1.3 V (V_{ds} = 0.65 V) is selected as a reasonable trade-off between linearity and dissipated power [3].

In LNA design, the gate resistance (R_g) of the common-source FET is one of the major contributions of noise. It can be reduced with special layout techniques. Finger widths spanning from 300 to 500 nm feature the lowest NF_{min} in this technology. In most advanced processes, the lowest metal layer (M1) is used to connect in parallel the poly-Si gates of multiple fingers. Due to the small width and thickness of the M1 interconnect, it adds a significant contribution to the total R_g when a large number of fingers is used. For this reason, a multi-number of vertical fingers are available in this technology, it reduces R_g by decreasing the length of the narrow M1 gate wire that connects fewer fingers horizontally as shown in Fig. 3. The final FET is laid out as a combination of 6 cells of 2 vertical and 10 horizontal gate fingers of 500 nm width (for a total width of 60 µm). The gates of each instance are connected together via the thick JA metal layer for negligible additional gate resistance. The overall FET footprint size is 30 µm, which is < λ/50 at 40 GHz. The NF_{min} and f_t & f_{max} at 39 GHz for different back-gate voltages (V_{bg}) of M_1 including parasitics up to the JA level is shown in Fig. 6 (a). For the nominal bias point given above (when normalized J_d = 1), NF_{min} = 0.86 dB, f_t = 141 GHz, f_{max} = 299 GHz. The dc back-gate contact is connected through a large bias resistor (10 kΩ) to decouple RF and dc signals in a compact way.

The degeneration-inductor (L_{s1}) is used to increase the real part of the input impedance as well as to provide in-band stabilization, at the cost of a small gain reduction. The input matching is realized with a shunt inductor (L_1) and input series capacitor (C_1) that also decouples the RF and dc paths. Such a configuration enables the implementation of ESD protections at the input with large diodes acting as large decoupling capacitors (though these were not implemented in this design). A second stage is added to provide further gain. The interstage matching is implemented with a shunt inductance (L_2) and series capacitance (C_3). The output matching consists of a series inductance (L_3), a shunt inductance (L_4) and series

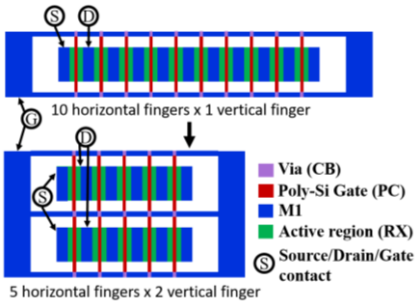

Fig. 3. Sketch of horizontal and vertical gate fingers concept.

capacitance (C_4) for a broader bandwidth. L_1, L_2 and L_4 are implemented as spiral inductors in QB. The others are realized with short pieces of inductive thin-film microstrip lines with the ground plane in JA and signal in LB. All series capacitors are implemented as metal-on-metal lumped capacitors using the top 3 thin metal layers (C3-C5) to reduce parasitic shunt capacitance. An RC network is present at the input matching to provide low frequency stabilization, despite its detrimental effect on total NF (around 0.24 dB, see Section V).

JA ground is used beneath all high-level interconnects and under L_{s1}, L_{s2} and L_3, in order to minimize the ground inductance throughout the whole circuit, thereby avoiding related stability issues that can be critical in single-ended circuits. The parasitics of the FET interconnects and close routing are extracted as a whole block via a combination of local PEX cells (using Calibre xACT) and EM simulations (Keysight Momentum). A full EM simulation is performed including inductors, large-scale interconnects, pads and ground planes. The full EM simulation and other blocks are connected together in order to account for ground impedance, coupling between inductors, pads parasitics, etc. and to ensure a sound simulation concerning circuit stability.

III. Measurements at Nominal Bias

The LNA is measured on-wafer with GSG probes. S-parameters and linearity measurements are performed with a Keysight VNA (PNA-X). Noise measurements are performed from 25 to 50 GHz. Nominal bias conditions are shown in Fig. 1, consuming a current of 8 mA, thus a 10.4 mW P_{dc} for each stage. The measured and simulated S-parameters at nominal bias, shown in Fig. 4 (a), agree well. The LNA exhibits a peak gain of 19.9 dB at 38 GHz with a 3 dB bandwidth from 34.9 GHz to 43.3 GHz. The input and output return losses are below -10 dB across the 36.7-49.5 GHz frequency range. Fig. 4 (b) shows the measured and simulated noise figure. NF measurements agree well with simulations across the whole bandwidth. The LNA achieves a minimum in NF of 2.5 dB at 39 GHz and remains below 3 dB from 34.5 GHz to 48 GHz.

Two input tones with a 100 MHz spacing (39 and 39.1 GHz) and equal power (swept from -30 dBm to -15 dBm) are applied at the LNA input to determine the IP3. The measured output power at the IP3 is shown in Fig. 4 (c). Extrapolation from the lowest power level is used to extract the input referred IP3, which is of IIP3 = -5.4 dBm.

Table 1 compares the performances of the presented LNA with best-in-class CMOS LNAs operating in the 39 GHz band.

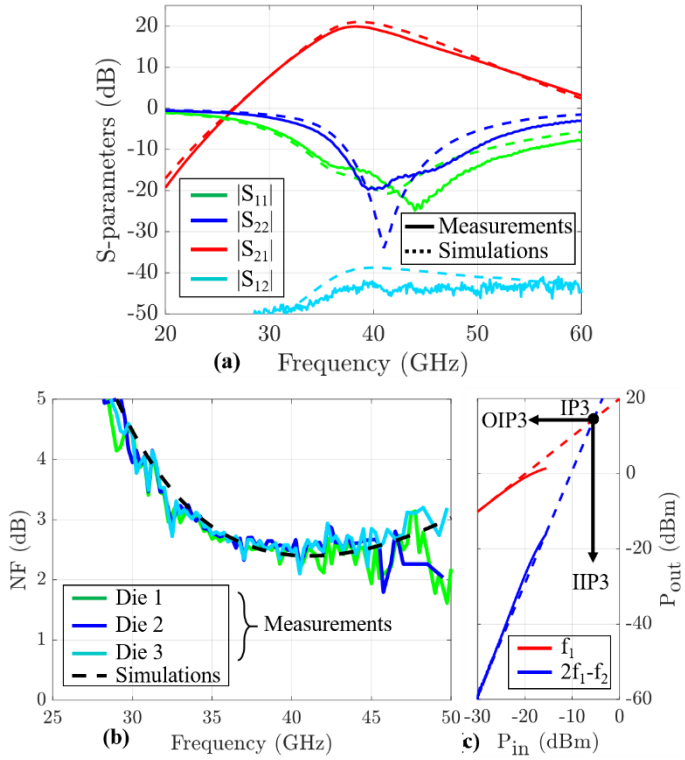

Fig. 4. (a) S-parameters. (b) NF measurements (solid lines) of several runs and dies and simulations (dashed lines). (b) IIP3 measurements. LNA biased in nominal conditions ($V_{g1,3}$ = 0.4 V, $V_{g2,4}$ = 1.1 V, $V_{dd1,2}$ = 1.3 V, V_{bgi} = 0 V).

The proposed LNA has great noise performance, NF < 3 dB in the 37-50 GHz band, and low power consumption, featuring comparable performances with state-of-the-art LNAs in (SOI) CMOS technologies. Although it has similar noise perfomance and total P_{dc} to the LNA in [9], the latter probably features lower IIP3 for several reasons, (i) lower P_{dc} per stage and (ii) increased complexity at output: presence of tunable loads, attenuators and by-pass switch. A second column is added for the low-power mode described in more details in Section IV.

IV. Circuit Behavior with Back-Gate Tuning

With back-gate bias modulation, each stage can change its working mode within the following biases: $V_{g1,3}$ = 0.3 V, $V_{g2,4}$ = 1 V, $V_{dd1,2}$ = 1.3 V and V_{bgi} swept from -0.2 to 2 V, with a corresponding drain current (I_d) and power consumption of 2.2-14 mA and 2.85-18.1 mW, respectively. The back-gate bias range is limited to avoid forward biasing the n-well/p-substrate diode and to prevent reverse breakdown of the diode.

By varying the back-gate biases of stage 1 and 2, one can trade P_{dc} for NF and gain (affected by stage 1 bias) or power for IIP3 and gain (affected by stage 2 bias mainly). Fig. 5 summarizes these trade-offs with data obtained from measurements. Indeed, noise and gain are traded-off for power by biasing the transistors closer to its threshold voltage, thereby lowering f_t & f_{max}, along with larger NF_{min}, but reducing I_d. Fig. 6 (a) shows simulations of f_t, f_{max} and NF_{min} of M_1 with interconnects up to JA. The optimal noise impedance is also modified, which further increases the NF for a constant input matching, mainly when biased close to threshold voltage where the FET characteristics have a sharp transition.

Table 1. Comparison to best-in-class 39 GHz CMOS LNA designs

	This work		[4]		[7]	[8]	[9]
Techno.	22FDX		22FDX		22FDX	45RFSOI	45RFSOI
Freq. (GHz)	36.7-43.3	36.7-42.5	24-43		27.1-29.4 & 37.7-43.9	27-46	37-40
Peak Gain (dB)	19.9	14.8	23	18.2	24.8 & 22.4	21.2	25
NF (dB)	2.5-2.6	3.2-3.4	3.1-3.7	3.4-4.3	3.6-4.9**	2.4-4.2***	2.3-2.85*
P_{dc} (mW)	20.8	7.4	20.5	12.1	13.6	25.5	18.6
IIP3 (dBm)	-5.4	-7.3	-19*	N/A	N/A	-11	-12.9

* graphically estimated. ** dual-band design. 4 dB at 39 GHz.
*** NF > 3 dB above 30 GHz, ~3.8 dB at 39 GHz.

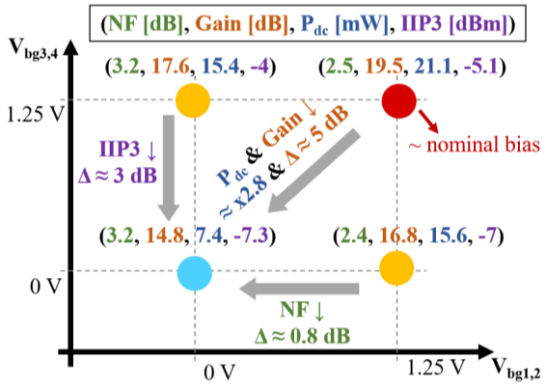

Fig. 5. Summary of LNA measurements at $V_{g1,3}$ = 0.3 V, $V_{g2,4}$ = 1 V, $V_{dd1,2}$ = 1.3 V and $V_{bg1,2}$ and $V_{bg3,4}$ varying from 0 to 1.25 V. A bias of V_{bgi} = 1.25 V yields very close results to the nominal bias detailed in the previous section.

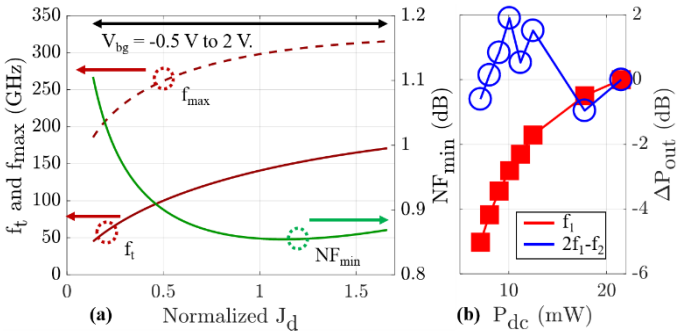

Fig. 6. (a) Simulated f_t, f_{max} and NF_{min} at 39 GHz of the common source FET with parasitics up to JA, V_{gs} = 0.3 V, V_{ds} = 0.65 V and V_{bg} varying from -0.5 to 2 V. (b) 2-tone measurements. Variation of output power at 39 GHz (f_1, red) and 38.9 GHz ($2f_1$-f_2, blue) for V_{bgi} swept from 0 to 1.25 V and P_{in} = -30 dBm.

IIP3 also deteriorates with lower P_{dc}. Indeed, as displayed in Fig. 6 (b), the output power of the 3rd intermodulation product remains roughly constant, while the power of the fundamental decreases due to lower gain at lower I_d.

Overall, back-gate biasing offers a high flexibility in circuit design enabling compensation and correction for process, voltage or temperature variation, besides tunability for different operation modes: low-power, low-noise, high-linearity.

V. NF Contribution Analysis

This section first provides a quantitative analysis through simulations of the contribution of each element in the input matching to the NF_{min} of the circuit. Then, we discuss how NF could be improved by engineering the shunt spiral inductor.

All subsequent figures are given for a simulated frequency of 40 GHz, but the relative numbers are valid for frequencies inside the LNA bandwidth. With separate EM simulations of each element (despite being less accurate than a full EM simulation as described in Section II), we could identify their noise contribution by changing the location of the input port from the FETs gate input toward the pads and checking the increase in NF_{min} each time an element is added.

The circuit without input matching, i.e. the contribution of the cascoded FETs and remaining of the circuitry (interstage matching and second stage) yields a total of 1.52 dB of NF_{min}. The major part is due to the intrinsic NF_{min} of the FETs, though the subsequent matching elements and second stage have a contribution of a few hundreds of mdB due to the limited gain of the first stage. The L_1 spiral inductor adds 0.58 dB, and the R_1-C_2 stabilization network adds 0.24 dB. Finally, the pad and input series capacitor (C_1) add another 0.12 dB to the NF_{min}, yielding a total simulated NF_{min} of 2.46 dB for the overall circuit. The main noise contribution in the input network is from the spiral inductor L_1.

The input spiral inductor is implemented on the QB layer, which is optimized for integration on a standard resistivity (std) substrate (called Ind-S). Its dimensions are given in the inset of Fig. 7. The simulated quality factor is 17.6 at 39 GHz. EM simulations of the same inductor geometry on a quasi-lossless high-resistivity (HR) Si substrate yields a similar quality factor (green line in Fig. 7). Therefore, no improvement in gain or noise figure (small-signal performance) is expected with a more resistive Si substrate. Nevertheless, stacking all thick metal layers available results in an inductor (called Ind-H) with lower metallic losses and, if coupled with a HR substrate, in a 30% improved quality factor (Q = 22.9) as shown in blue lines in Fig. 7. Inserting this inductor in the overall LNA simulation yields a minimum noise figure of 2.38 dB, which represents an improvement of 0.06 dB with respect to the implemented LNA. The much larger improvement in Q for Ind-H when moving from a std to a HR substrate compared to Ind-S is explained by a larger concentration of electric field in the substrate due to the inductor being closer to it.

It is interesting to note that simply improving the substrate RF performance using a high-resistivity substrate does not necessarily enhance the performance of a mm-wave LNA with a conventional design. Whereas, by adopting a different strategy in the design of passive networks, consisting in this case of decreasing the metal resistance by stacking several metal layers, one can achieve a modest improvement in LNA performance with high-resistivity Si substrate.

VI. Conclusion

This paper presented a 22 nm FD-SOI 2-stage LNA covering the N259 and N260 mm-wave 5G bands. The prototype achieves 19.9 (14.8) dB peak gain, 2.5 (3.2) dB minimum NF, 6.6 (5.8) GHz bandwidth and -5.4 (-7.3) dBm IIP3 for a 20.8 (7.4) mW power dissipation in nominal (low-power, respectively) mode. This LNA exhibits similar performances to state-of-the-art LNAs in other (SOI) CMOS technologies [9], narrowing the gap with III-V technologies. The back-gate is an easily accessible knob, which can be used to change the

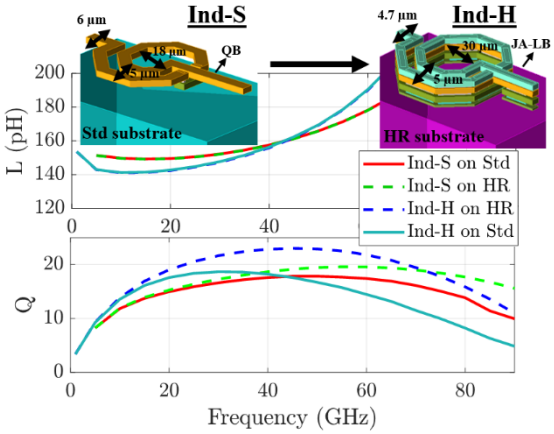

Fig. 7. Simulated L and Q of the shunt input inductance (L_1) on std (solid lines) and HR (dashed lines) substrates. Ind-S is optimized for std substrate and was implemented in the LNA prototype. Ind-H is optimized for HR substrate by stacking JA to LB metal layers.

circuit operation mode, by moving from a combination of low noise (up to ΔNF = 0.8 dB) or high linearity (up to ΔIIP3 = 3.3 dB) to low power mode ($P_{dc,max}/P_{dc,min}$ = 2.8) according to the need. Finally, a detailed analysis of the noise contribution from each element in the input matching is provided. EM simulations show that a 0.06 dB improvement in NF can be achieved when moving from a standard Si substrate to a quasi-lossless high-resistivity substrate, if the input spiral inductor design is optimized by stacking several metal layers.

Acknowledgment

The authors thank GlobalFoundries for chip fabrication and support. This work was partially supported via Beyond5 ECSEL project. L. Nyssens is a research fellow of the FNRS.

References

[1] S. N. Ong *et al.*, "A 22nm FDSOI Technology Optimized for RF/mmWave Applications," in *Proc. RFIC 2018*, 2018, pp. 72-75.

[2] L. H. K. Chan *et al.*, "22nm Fully-Depleted SOI High Frequency Noise Modeling up to 90GHz Enabling Ultra Low Noise Millimetre-Wave LNA Design," in *Proc. RFIC 2019*, 2019, pp. 31-34.

[3] C. Zhang *et al.*, "A Low Noise Figure 28GHz LNA in 22nm FDSOI Technology," in *Proc. RFIC 2019*, 2019, pp. 207-210.

[4] L. Gao and G. M. Rebeiz, "A 24-43 GHz LNA with 3.1-3.7 dB Noise Figure and Embedded 3-Pole Elliptic High-Pass Response for 5G Applications in 22 nm FDSOI," in *Proc. RFIC 2019*, 2019, pp. 239-242.

[5] R. Dilli, "Analysis of 5G Wireless Systems in FR1 and FR2 Frequency Bands," in *Proc. ICIMIA 2020*, 2020, pp. 767-772.

[6] O. Kane *et al.*, "RF characterization and small signal extraction on 22 nm CMOS fully-depleted SOI technology," in *Proc. EUROSOI-ULIS 2019*, 2019, pp. 1-4.

[7] X. Xu *et al.*, "A 28 GHz and 38 GHz Dual-Band LNA Using Gain Peaking Technique for 5G Wireless Systems in 22 nm FD-SOI CMOS," in *Proc. APMC 2020*, 2020, pp. 98-100.

[8] Y. Hu and T. Chi, "A 27–46-GHz Low-Noise Amplifier With Dual-Resonant Input Matching and a Transformer-Based Broadband Output Network," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 6, pp. 725-728, June 2021.

[9] S. Li *et al.*, "A Millimeter-Wave LNA in 45nm CMOS SOI with Over 23dB Peak Gain and Sub-3dB NF for Different 5G Operating Bands and Improved Dynamic Range," in *Proc. RFIC 2021*, 2021, pp. 31-34.