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Impact of substrate resistivity on spiral inductors at mm-wave frequencies

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ABSTRACT

The quality factor (Q) of two inductors for 5–60 GHz applications fabricated in an industrial back-end of line (22FDX® from GlobalFoundries) with thick Cu metal layers on top of several Si substrates of different bulk resistivities is analyzed in this paper. The low frequency RF inductor shows an improvement of up to 44% in Q with a high-resistivity substrate. However, no significant improvement is observed for the high-frequency MMW fabricated inductor. This is identified to be due to lower electric field concentration in the substrate due to the small geometry of this MMW inductor that is realized in the top metal Cu layer. Nevertheless, simulations show that a 30% improvement can be achieved with a low loss substrate when designing a MMW inductor as a stacked coil of all BEOL thick metal layers.

1. Introduction

The ultra-thin buried oxide (UTBB) fully-depleted silicon-on-insulator (FD-SOI) technology exhibits outstanding digital, analog and RF performances for RF and millimeter-wave (mm-wave) applications [1]. Additionally to cutting-edge active devices, these technologies offer rich back-end of line with thick Cu metal layers enabling low-loss passives, including spiral inductors, which are widely used in RF/mm-wave circuits. Due to technological constraints, current UTBB FD-SOI technologies are fabricated on standard (std) Si substrates, which are known to entail RF losses and non-linearity effects [2]. Moving to a high-resistivity (HR) Si substrate improves losses and linearity, but only to some extent, due to parasitic surface conduction (PSC). The latter can be solved using a trap-rich substrate [3] or other interface passivation techniques [4–5].

In the case of spiral inductors, substrate losses reduction is observed on improved quality factor as demonstrated at sub-6 GHz frequencies [6], potentially improving circuit figures of merit such as gain and noise figure in low-noise amplifier [7].

This paper is organized as follow. First, two high frequency (5 to 60 GHz) spiral inductors fabricated on a standard resistivity and a HR substrate are described. Then, we show how the substrate stack for electromagnetic (EM) simulations is tuned to account for PSC in the HR wafer. After, the measured quality factor of the two spiral inductors on different substrates are presented and discussed. Finally, a way of improving the quality factor of the higher frequency inductor on a quasi-lossless substrate is shown via EM simulations.

2. Device description

Two different inductors have been fabricated on an industrial UTBB FD-SOI process (22FDX®), targeting different operating frequencies. These inductors are designed on the 3 μm-thick highest top Cu metal layer of the back-end of line, ~10 μm above the silicon substrate. A sketch of the inductors and their geometrical dimensions are presented in Fig. 1 (a) and (b). The dummy fills are minimized to avoid degrading the inductor quality factors. Metal dummy fills are known to increase capacitive coupling [8] and to entail eddy current [9], which reduces the effective inductance while increasing the effective losses. Combined together both phenomena overall decrease the inductor quality factor and must be minimized for high-quality inductor design. Some special marker layers are commonly available in process design kits to minimize the metal density requirements to achieve high-quality inductors. However, such layers cannot overlap active devices or some passive pcells (such as metal-on-metal capacitors), because the reduced surrounding metal density can lead to large variations in the devices that are not predicted by their design kit model. Therefore, such devices are usually not designed beneath inductors as the large metal density required for these devices would greatly degrade the inductors'

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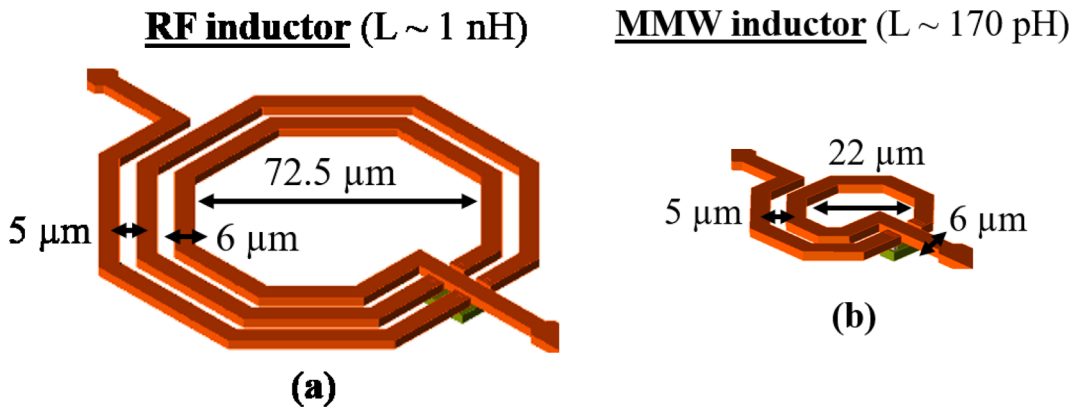

Fig. 1. RF (a) and MMW (b) sketch along with geometrical dimensions.

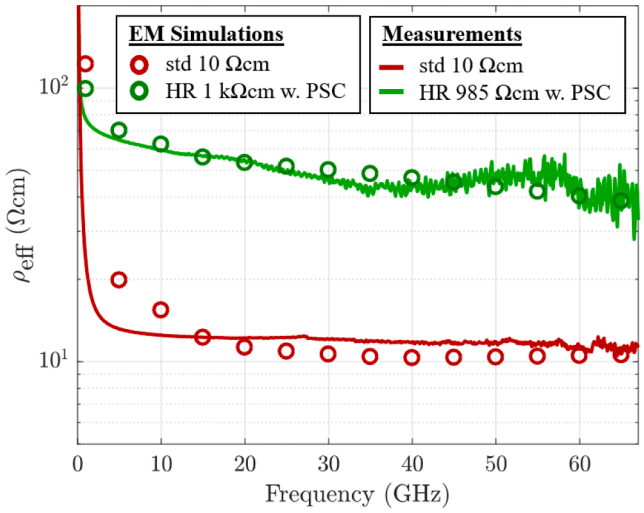

Fig. 2. Effective resistivity versus frequency extracted from measurements and simulations of CPW lines on standard resistivity (red) and HR with PSC effect (green) substrates. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

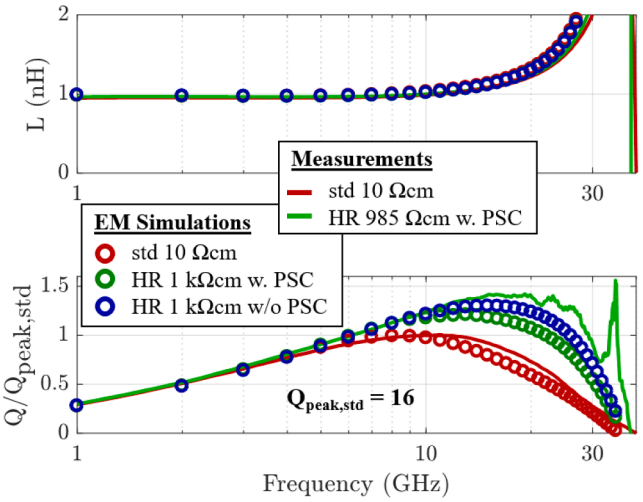

Fig. 3. (a) Inductance (L) and (b) normalized quality factor (Q) of RF inductors on different substrates, with or without interface passivation. Measurements in solid lines, EM simulations in circles.

performance.

In addition to the normal process flow (on a std – 10 Ωcm), the inductors are also fabricated in the 22FDX® node on a HR substrate (HR – 985 Ωcm bulk resistivity), as part of an experimental split process.

3. Substrate stack tuning for PSC effect in EM simulations

In HR wafers, the parasitic surface conduction phenomenon counteracts the benefits of a large bulk substrate resistivity and results in significant RF losses and non-linearity effects (although lower than in std Si substrate) [2]. This PSC effect originates in the presence of fixed charges (generally positive) trapped in the buried oxide (BOX) and generated during manufacturing that induces a thin sheet of highly conductive free carriers (generally electrons) at the silicon – BOX interface. A slight variation in the amount of fixed charges induces a large variation in the thin sheet conductivity (exponential relationship) with a significant effect in RF losses and non-linearity.

Along with the inductors, coplanar waveguide (CPW) lines are designed and fabricated in the bottom metal layers (stacking M1 and M2) to be sensitive to the substrate. The effective resistivity (ρ_{eff}) of the substrates is extracted from these lines (of several lengths for proper pads and parasitic de-embedding) [10] and is used to monitor the substrate RF quality. More details about the CPW lines geometry and results from this experimental split process can be found in [11].

To include this PSC effect in EM simulations, the substrate stack is modified and a thin conductive Si sheet is added between the oxide and the high-resistivity bulk silicon substrate. Due to the absence of a direct measurement of the fixed charges amount at the origin of the PSC effect, the thickness and conductivity of the thin conductive Si sheet (emulating the PSC effect) are determined by fitting EM simulations (using ADS Momentum) of the above CPW lines to their measured effective resistivity as in [12]. Fig. 2 shows the ρ_{eff} extracted from the measured and simulated CPW lines on different substrates. Although a more complex multi-layer stack modeling might give more accurate results, this 2-layer stack is enough for our study.

4. Measurement results

On-wafer measurements are performed from 100 MHz to 67 GHz, using a pair of Ground-Signal-Ground (GSG) probes. A 2-step calibration is performed (Line-Reflect-Reflect-Match calibration on an impedance standard substrate, followed by an on-wafer multi-line Thru-Reflect-Line calibration [13]) to move the reference plane to the DUT vicinity with high accuracy at mm-wave frequencies [14].

The measured S-parameters are transformed in Y-parameters, then the inductance (L) and quality factor (Q) are computed as.

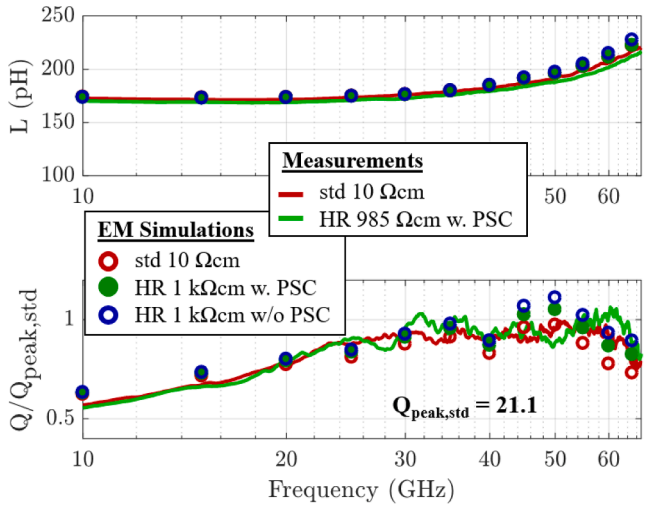

Fig. 4. (a) Inductance (L) and (b) normalized quality factor (Q) of MMW inductors on different substrates, with or without interface passivation. Measurements in solid lines, EM simulations in circles.

$$L = \mathrm{Im}\left(\frac{1}{Y_{11}}\right)\cdot\frac{1}{\omega} \text{ and } Q = \frac{\mathrm{Im}\left(\frac{1}{Y_{11}}\right)}{\mathrm{Re}\left(\frac{1}{Y_{11}}\right)}. \quad (1)$$

Fig. 3 and Fig. 4 show the inductance and normalized quality factor of the RF and MMW inductors. The quality factor is normalized to the measured peak Q of the inductor on the std resistivity substrate. Additionally, electromagnetic simulations using ADS Momentum with different substrate definitions are performed on the inductors and on-wafer calibration structures. The resonance around 35 GHz in Fig. 3 is attributed to probe coupling with its nearby environment that significantly varies between the on-wafer calibration structures and the RF inductor.

A strong improvement is observed for the RF inductor as we move from a std substrate to a HR substrate thanks to a much greater bulk resisitivity. Indeed, the peak Q value is around 1.4 times higher (from 16 to 23) and shifted to higher frequencies. The small mismatch between simulations and measurements of the RF inductor is partially attributed to an overestimation of capacitive coupling, resulting in a lower self-resonant frequency and lower peak Q. As shown in Fig. 3, the PSC effect induces a slight degradation of the quality factor. Even though measurements of these inductors on a HR without PSC effect are not shown here, it can be achieved in practice by using some interface passivation techniques such as the widely used trap-rich substrate [3] or other techniques more suited for FD-SOI technology [4–5].

No significant variation in Q of the MMW inductor is observed for the different substrates. EM simulations show that a very slight improvement should be achieved, but the variation is within the measurement noise that is higher at such high frequencies. The gain in Q as the substrate is changed from a std to a HR with interface passivation (such as the TR substrate for instance) is expected to be smaller for this MMW inductor compared to previously reported studies [6,15] mainly because of its smaller geometry, scaling down with higher operating frequency. Indeed, the smaller geometry of the MMW inductor that is also far away from the substrate (~10 μm) reduces the concentration of electric field (E-field) inside the substrate, thus attenuating the substrate losses effect

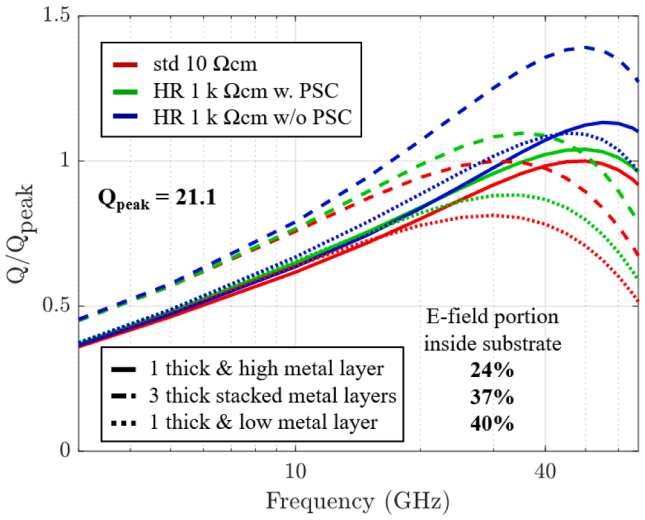

Fig. 5. EM simulations of inductors' Q normalized to the peak Q of the MMW inductor on std substrate (Qpeak = 21.1). 3 inductors are simulated: (i) MMW inductor (solid lines, ~10 μm away from the substrate, ~3 μm-thick metal), (ii) inductor on 3 thick Cu layers (dashed lines, ~2 μm away from substrate, ~7 μm-thick metal), (iii) inductor on 1 metal layer closer to the substrate (dotted lines, ~2 μm away from substrate, ~3 μm-thick metal), on top of three substrates: (i) std (red), HR with PSC (green), HR without PSC (blue). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

on the inductor's Q. The E-field concentration inside the substrate is evaluated via 3D EM simulations (using Ansys HFSS[1]) and represent ~ 24% of the total E-field in the whole structure. A second effect of higher operating frequency is increased metallic losses due to skin and proximity effects, which further reduce the relative impact of substrate losses on the overall inductor losses.

5. Improved MMW inductor

Metallic losses can be decreased by stacking several metal layers. The 22FDX® technology offers up to 11 metal layers, including 3 thick Cu layers. In this section, we investigate via EM simulations the performance of several inductors with the same planar geometry as the MMW inductor, but using different metal layer(s) and substrates. The quality factor of these simulated inductors are shown in Fig. 5. By stacking the 3 thick metal layers, a notable reduction in metallic losses can be achieved (larger Q at low frequencies in dashed lines, where metallic losses dominate the curve). However, the inductor is closer to the substrate and the overall Q quickly drops for the std and HR with PSC substrates. Such an inductor is much more sensitive to losses in the underlying substrate. Indeed, as a consequence of a larger portion of E-field inside the substrate (~37% of the total) a ~ 30% increase in Q (from 21.1 to 29.4) can be achieved with the 3-stacked metal layers by moving from a std substrate to an almost lossless one, e.g. HR with surface passivation of the PSC effect. An additional inductor is simulated (dotted lines), on 1 thick metal layer (same thickness, thus same metallic losses as the MMW inductor) at the same distance from the substrate as the 3-stacked layers inductor (~2 μm). With a similar portion of E-field inside the substrate (~40%), a similar raise (~35%) in Q is achieved by changing the underlying substrate from a std one to a quasi-lossless one, demonstrating the stronger impact of purely substrate losses on the overall Q for

[1] The full wave 3D electromagnetic field simulations performed with Ansys HFSS were conducted in driven modal solution type, with bridge-type lumped ports at the inductor accesses. The grid is composed of up to 46,000 tetrahedra, for a 2 min and 20 s CPU simulation time on a standard desktop.

inductors closer to the substrate.

6. Conclusion

Two inductors (with operating frequency ranges of 5–15 GHz - called RF - and 30–60 GHz - MMW), were fabricated in GlobalFoundries' 22FDX® node on a standard resistivity (10 Ωcm) and a high-resistivity Si substrates (985 Ωcm). Measurements show a ~ 44% improvement in the RF inductor's Q moving from a standard to a HR substrate. No significant improvement is observed for the MMW inductor, due to smaller coil dimensions, thus reduced field concentration in the Si substrate. Nevertheless, simulations show a great improvement in MMW inductor's Q can be achieved (~+30%) when several thick metal layers are stacked to reduce metallic losses on top of a quasi-lossless substrate. It therefore demonstrates the requirement of a high-quality substrate for high Q spiral inductors even at mm-wave frequencies to enable more performing mm-wave circuits.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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