Room-temperature DC-sputtered p-type CuO accumulation-mode thin-film transistors gated by HfO_2

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ABSTRACT:

CuO grown by room-temperature direct current (DC) reactive magnetron sputtering is introduced to realize p-type thin-film transistors (TFTs), with a high-k HfO_2 gate dielectric fabricated by atomic layer deposition (ALD). The devices work in accumulation mode (AM) with two apparent threshold voltages corresponding to the formation of buried channel and accumulation layer, respectively. CuO AM TFT with a channel length of 25 μm exhibits competitive on-off ratio (I_{on}/I_{off}) of 1.3×10^2, subthreshold swing (SS) of 1.04 V dec^{-1}, and field-effect mobility (μ_{FE}) of 1.1×10^{-3} cm^2 V^{-1} s^{-1} at room temperature. By measuring a CuO metal oxide semiconductor (MOS) capacitor at room temperature, a high acceptor doping density (N_A) of $\sim5\times10^{17}$ cm^{-3}, a high positive effective fixed surface charge density (Q_f) of $\sim9\times10^{12}$ cm^{-2} and a low interfacial trap charge density (D_{it}) of $\sim6\times10^{10}$ eV^{-1} cm^{-2} at the HfO_2/CuO interface are estimated. The μ_{FE} extracted from the accumulation regime appears lower than the Hall mobility measured for a similarly processed CuO layer on glass due to the increased hole concentration in CuO TFT, compared to a Hall concentration of $\sim10^{14}$ cm^{-3}, following MOS process. SS appears limited by the decreased channel to gate capacitance (C_{cg}) related to the buried channel in AM TFTs, parasitic capacitance to ground and potentially very high interfacial traps at the non-passivated CuO/air interface.

Metal oxide semiconductors, as the most abundant materials in the earth's crust, are widely used in thin-film transistors (TFTs) because of their good carrier mobilities, low off-current, large-area uniformity and processibility, mechanical stress tolerance, good stability, and low cost.[1-3] Particularly for n-type metal oxides, significant progress has been achieved to fabricate n-type TFTs with excellent electrical performances.[4] However, realization of equally well-performing p-type metal oxides and TFTs still remains challenging because of limited options for p-type oxides, low mobility caused by a high valence band maximum (VBM), and their strict fabrication conditions.[5,6] Few p-type metal oxides like tin oxide,[7] nickel oxide[8] and copper oxide[9] have exhibited good performances in TFTs. Therefore, it is of great interest to study p-type metal oxides, realizing either sensing or memory applications with a single p-type TFT, or p-n junctions and complementary metal oxide semiconductor (CMOS) logic circuits along with n-type counterparts.[6,10]

As one of the most promising candidates, p-type CuO features tunable bandgap from 1.2 to 1.9 eV, high Hall mobility, excellent electrical properties and more stable chemical performance compared to Cu_4O_3 and Cu_2O.[11] Different techniques have been used to fabricate copper oxide TFTs. One of the earliest Cu_2O TFTs was fabricated by pulsed laser deposition (PLD) at high temperatures from 400 to 700 ºC.[9] Room-temperature RF magnetron sputtering was used to fabricate Cu_2O TFTs, showing the possibility to further oxidize Cu_2O to CuO with air annealing.[12,13] More recently, sol-gel processed CuO TFT with a field-effect mobility (μ_{FE}) of 4×10^{-4} cm^2 V^{-1} s^{-1} and an on-off ratio of $\sim10^2$ exhibits good photodetection capabilities.[14] Hypochlorous acid oxidation was used to tune the oxygen concentration in copper oxide, reaching an improved on-off ratio of 4.86×10^4, with a μ_{FE} of 2.83×10^{-3} cm^2 V^{-1} s^{-1}.[3] Atomic layer deposition (ALD) was used to fabricate Cu_2O TFT with an Al_2O_3 surface passivation, showing a μ_{FE} of 1.3×10^{-3} cm^2 V^{-1} s^{-1}.[15] Ni doping can improve the crystalline quality of CuO fabricated by solution-processed method and thus enhance the μ_{FE} to 0.01 cm^2 V^{-1} s^{-1}.[16] Relatively low μ_{FE} from 10^{-4} to 10^{-1} cm^2 V^{-1} s^{-1} have been obtained for most of the copper oxide TFTs related to high contact resistance and interfacial trap states.[17] However, most reported researches focused on SiO_2 gate dielectrics based on standard silicon techniques. Another suitable high-k dielectric, HfO_2, deposited either by anodic formation from Hf[18] or PLD[19], has been rarely studied in CuO TFTs. ALD, as one of the best fabrication methods to produce ultrathin high-quality dielectric, has been rarely studied yet to realize CuO TFTs with HfO_2 gate dielectric.

In this work, p-type CuO TFTs were fabricated on glass. CuO film was deposited by DC magnetron reactive sputtering for material characterizations. High-k gate dielectrics of HfO_2 fabricated by ALD was introduced in CuO TFTs. A MOS capacitor was fabricated to further explore the interfacial properties of CuO TFTs. Related electrical performances were measured for both CuO TFTs and CuO MOS capacitor.

The schematics for the fabrication process of the CuO TFT is shown in Fig. 1. Soda lime glass (SLG) substrate was firstly rinsed by acetone, methanol, isopropanol and deionized water, and dried by N_2. Ti/Au (10/100 nm) was deposited by e-beam evaporation on SLG substrate to form a

bottom gate. A thin layer of Ti helps to enhance the adhesion between Au and SLG. HfO_2 (25 nm) was deposited by thermal atomic layer deposition (TE-ALD, Cambridge Fiji F200) at 200 °C. The deposition rate of HfO_2 by TE-ALD was 1 Å per cycle. P-type CuO (115 nm) was deposited at room temperature for 30 minutes by direct current (DC) reactive magnetron sputtering (ATC Orion 5 Sputter System for AJA International) as detailed in Ref. 23. A constant sputtering power of 50 W was set in the chamber at a sputtering pressure of 10 mTorr with an O_2/Ar ratio of 8/22 sccm. The Au/Ti/Al (100/10/500 nm) source and drain electrodes were deposited by e-beam evaporation. UV reverse lithography and lift-off were used to pattern both the CuO active layer and the top electrode contacts with a channel width (Z) of 270 μm and channel lengths (L) of 25 and 10 μm.

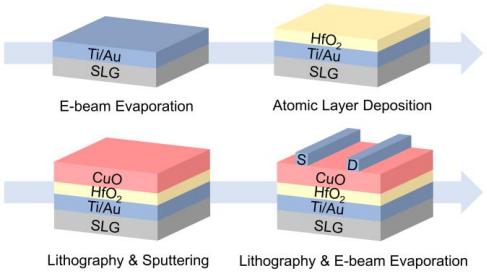

FIG. 1. Schematics for fabrication process and structure of CuO TFT.

The material properties were analyzed by focused ion beam-scanning electron microscopy (FIB-SEM, Zeiss Auriga), X-ray diffraction (XRD, Bruker-D8 Advance diffractometer) with a CuKα radiation (λ=1.5418 Å), and Raman spectroscopy (LabRAM HR, Horiba Scientific). The thicknesses of layers were confirmed by Sentech SE850 ellipsometer, Veeco Dektak 150 and FIB-SEM. The electrical characteristics were measured on a LakeShore CPX probe station connected to Keithley 4200-SCS semiconductor characterization system at room temperature under dark.

In order to determine the material properties, XRD pattern and Raman spectra of the DC-sputtered CuO thin film are shown in Fig. 2. In Fig. 2(a), CuO features a phase of tenorite CuO, with a monoclinic structure in the C2/c(15) space group. The peaks at 2θ values of 32.3º, 35.5º, 38.5º are identical to the reflection planes of (-110), (002), (111). According to the Debye-Scherrer relation, $D = 0.94\lambda/\beta\cos\theta$,[20] where λ is the X-ray wavelength (=1.5418 Å) and β is the half width of maximum peak intensity, crystallite size of CuO can be calculated to be about 29 nm. In Fig. 2(b), Raman peaks of CuO lie around 295, 341 and 628 cm^{-1}, which are close to the values in Ref. 21. The peak at 320 cm^{-1} is related to the SLG substrate and a small hump observed from 500 to 600 cm^{-1} is due to the defects and amorphous phase fraction in CuO.[22]

Well prepared distinct interfaces can be seen clearly by the SEM cross-section view of CuO TFT in Fig. 3(a). Ti/Au bottom gate, HfO_2 gate dielectric, CuO active layer and Au/Ti/Al top electrodes can be observed from bottom to top on SLG substrate. To further investigate the crystal quality, CuO thin film was sputtered on a bare SLG substrate under the same conditions as CuO TFTs. SEM plain view of CuO thin film in Fig. 3(b) shows a triangular grain structure and an estimated grain size of about 30nm, which is consistent with the XRD result. The cross-section view of CuO in Fig. 3(c) shows a columnar growth of CuO. These results reveal better crystal structures and grain growth of CuO sputtered at 10 mTorr with O_2/Ar =8/22 sccm, compared to our previous CuO thin films sputtered at 5 mTorr with O_2/Ar =10/20 sccm.[23]

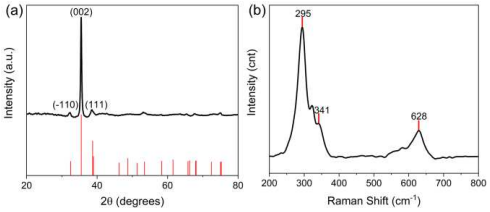

FIG. 2. (a) XRD pattern (JCPDS-45-0937) and (b) Raman spectra of deposited CuO thin film.

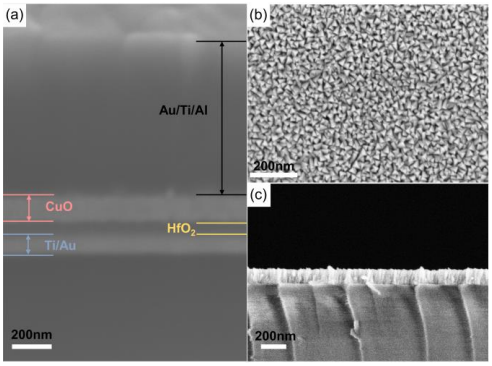

FIG.3. (a) SEM cross-section image of CuO TFT. (b) SEM plain-section and (c) SEM cross-section images of CuO thin film on SLG substrate.

To investigate the electrical properties of CuO/HfO_2 interface, a CuO MOS capacitor (1000×1000 μm^2) was fabricated by the same processes as CuO TFTs with a gate-biased bottom electrode and a grounded top electrode. In Fig. 4(a), measured p-type capacitance versus gate voltage (C_m-V_G) curves at applied active current (AC) frequencies (f) from 5 kHz to 500 kHz are corrected by the methods of Refs. 24, 25 to remove the influence of series resistance (R_s). A clear shift from 5 to 500 kHz caused by the interfacial traps can be

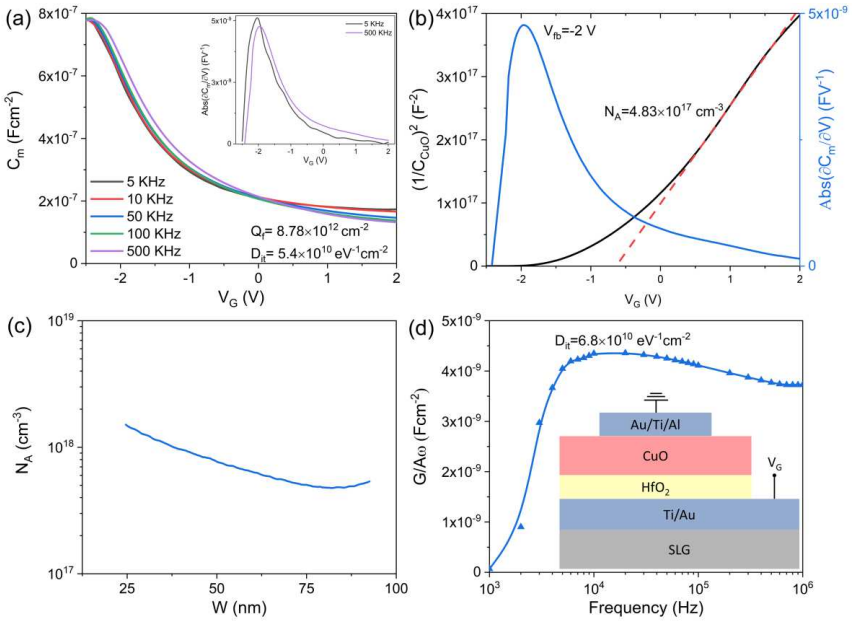

FIG. 4. (a) Corrected C_m-V_G curves from 5 kHz to 500 kHz, the insets are $abs(\partial C_m/\partial V_G)$-$V_G$ curves at 5 and 500 kHz. (b) Calculated $(1/C_{CuO})^2$-V_G, $abs(\partial C_m/\partial V_G)$-$V_G$ and (c) N_A-W curves at 500 kHz. (d) $G/A\omega$ curve from 1 kHz to 1 MHz at 0V, the inset is the schematic of MOS capacitor.

seen from the insets of Fig. 4(a). Interfacial traps can only follow slow quasi-static and lower frequency signals while the higher frequency signals are too fast for the minority carriers and the interfacial traps to respond.[26] Charges induced by interfacial traps are therefore more pronounced at lower frequency and causes a shift of C-V curves. To avoid the influence of interfacial traps when extracting the effective CuO parameters, high-frequency curves are preferred. Therefore, C_m-V_G curve at 500 kHz is used in the analysis of Fig. 4(b) and Fig. 4(c). To analyze it separately, the CuO depletion capacitance (C_{CuO}) is obtained from $C_{CuO} = (C_{ox} \times C_m)/(C_{ox} - C_m)$ where C_{ox} is the theoretical oxide capacitance (7.8×10^{-7} F cm^{-2} for HfO_2 of 25 nm) equal to the maximum capacitance in the accumulation regime of Fig. 4(a). Flat-band voltage (V_{FB}) is extracted to be about -2V from the absolute value of derivative C_m-V_G curve (blue line in Fig. 4(b)). The apparent acceptor doping density (N_A) is extracted from the slope of the linear part in $(1/C_{CuO})^2 - V_G$ curve to be 4.83×10^{17} cm^{-3} (red and black lines in Fig. 4(b)). Next, fixed surface charge density (Q_f) at HfO_2/CuO interface is estimated by:[27]

$$Q_f = C_{ox}\left(\frac{V_{ms}-V_{FB}}{q}\right) \quad (1)$$

where $V_{ms} = (\varphi_m - \varphi_s)/q$ with φ_m as the work function of Au (5.47 eV) and q is the electron charge. Work function of CuO (φ_s) can be estimated by:[26]

$$\varphi_s = \chi_{CuO} + E_g - \left|\frac{kT}{q}\ln\left(\frac{N_A}{N_V}\right)\right| \quad (2)$$

where χ_{CuO} is the electron affinity of CuO (4.07 eV), E_g is the bandgap of CuO (1.6 eV from our previous measurement in Ref. 23), k is the Boltzmann constant, T is the temperature and N_V is the valence band effective density of states of CuO (=5.5×10^{20} cm^{-3}).[28] φ_s is estimated to be 5.49 eV and a calculated positive Q_f of 8.78×10^{12} cm^{-2} is obtained for the capacitor. Even considering deviation in the estimation of φ_s due to slight difference of χ_{CuO} and N_V for specific CuO films, a high positive Q_f of ~10^{13} cm^{-2} remains expected. Such high Q_f repels the hole carriers inside CuO leading to a thick depletion layer at zero gate voltage.[29]

At 500 kHz, the depletion width (W) and the net acceptor concentration (N_A) are obtained in Fig. 4(c) using:[30]

$$N_A = \frac{-2}{q\varepsilon_0\varepsilon A^2\left[d\left(1/C_{CuO}{}^2\right)/d\varphi_{CuO}\right]} \quad (3)$$

$$W = \frac{\varepsilon_0\varepsilon A}{C_{CuO}} \quad (4)$$

where ε_0 is the vacuum permittivity, A is the device area (=0.01 cm^2), φ_{CuO} is the potential at HfO_2/CuO interface (in inversion regime, $\varphi_{CuO} = V_G + Q_{ox}/C_{ox}$) and ε, the CuO permittivity, is assumed to be 18.1.[28] Consistently with to the slope of the $(1/C_{CuO})^2 - V_G$ curve, the minimum N_A is ~5×10^{17} cm^3, and increases towards HfO_2, to a much higher value than in previous Hall measurements on SLG [23] due to high acceptor activation energy and high compensation ratio.[31]

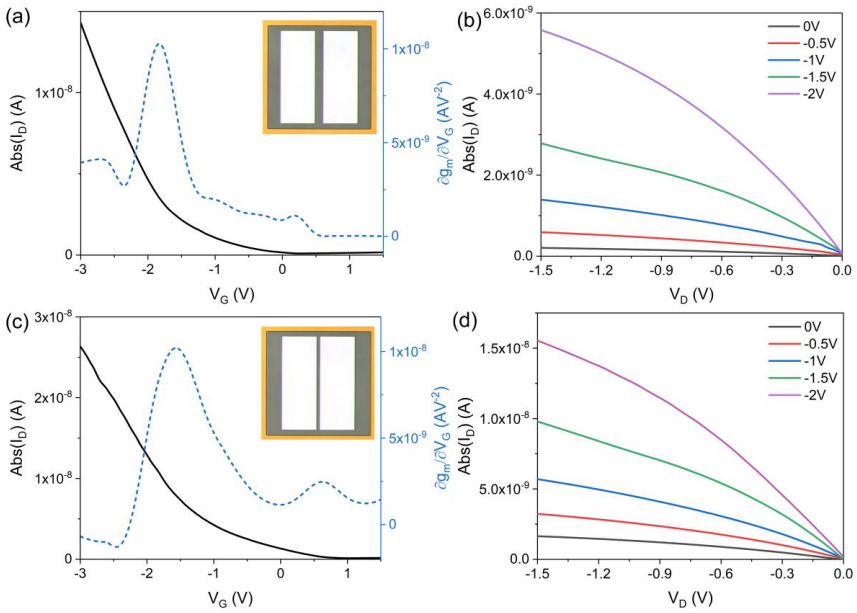

FIG. 5. Transfer I_D-V_G curves (V_D=-1V) and transconductance derivatives (blue dashed lines) of CuO TFTs with channel lengths of (a) 25 μm (c) and 10 μm (Insets are the corresponding top-viewed photographs by optical microscope). Output I_D-V_D curves (V_G=-2 V to 0 V) of CuO TFTs with channel lengths of (b) 25 μm. and (d) 10 μm.

Another important figure of merit is the interfacial trap charge density (D_{it}) at the HfO_2/CuO interface. D_{it} is related to the material and chemical processes in fabrication and can be estimated either by the parallel capacitance, or conductance, variation with V_G, or f, corresponding to the high-low frequency method,[32] or parallel conductance method, respectively. In the high-low frequency method, the interfacial traps respond to variations of input signals only at the low frequency but not at the high frequency. Corresponding D_{it} can be calculated by:

$$D_{it} = \left(\frac{C_{ox}C_{lo}}{C_{ox}-C_{lo}} - \frac{C_{ox}C_{hi}}{C_{ox}-C_{hi}}\right)/q \quad (5)$$

where C_{lo} and C_{hi} are the low and high frequency capacitances. In Fig. 4(a), a clear shift of V_{fb} can be observed due to D_{it}. After removing this shift and extracting D_{it} at a V_G of 0 V, a D_{it} of 5.4×10^{10} eV^{-1} cm^{-2} is obtained at HfO_2/CuO interface. By the conductance method, which is less affected by parasitic elements, D_{it} can be calculated by:[26]

$$D_{it} = \frac{2.5}{q}\left(\frac{G}{A\omega}\right)_{max} \quad (6)$$

where $(G/A\omega)_{max}$ is the height of the peak in $G/A\omega$-f curve, and 2.5 is a correction factor for the peak width statistical fluctuation.[26] The peak value is caused by the maximum energy loss from charge exchange with interface states. In Fig 4(d), G/ω is plotted against ω ($=2\pi f$) at a V_G of 0V and a D_{it} of 6.8×10^{10} eV^{-1} cm^{-2} is extracted at HfO_2/CuO interface, which is close to the calculated value by high-low frequency method. Therefore, D_{it} is estimated to be ~6×10^{10} eV^{-1} cm^{-2}, showing lower value than a D_{it} of 3×10^{13} eV^{-1} cm^{-2} at SiO_2/Cu_2O interface[17] and 6.8×10^{11} eV^{-1} cm^{-2} at HfO_2/Cu_2O[19]. Lower D_{it} in this work compared to SiO_2/Cu_2O and HfO_2/Cu_2O interfaces is due to a better quality of HfO_2/CuO interface than Ref. 17 and 19.

Finally, CuO TFTs with L of 25 and 10 μm are investigated. Their transfer curves (i.e., drain current versus gate voltage, I_D-V_G) at a drain voltage (V_D) of -1 V are reported in Fig. 5(a) and (c), respectively. By extracting the derivatives of transconductance g_m (blue dashed lines in Fig. 5(a) and 5(c)), two main peaks are observed after smoothing, showing accumulation-mode (AM) behaviors of CuO TFTs.[33,34] According to the N_A-W results from C-V measurements, CuO thin film is almost fully depleted at very positive V_G. When lowering V_G, a buried conduction channel is first formed in the middle of the CuO layer, corresponding to the first apparent threshold voltage (V_{th1} as the right peak of the g_m derivative curve, at about 0.2 V in Fig. 5(a) and 0.6 V in Fig. 5(c)). The thickness of the buried channel and hence the related current increase when further lowering V_G, finally forming an accumulation layer below the second threshold voltage ($V_{th2} \approx V_{fb}$, as the left peak of the g_m derivative curve, -1.8 V in Fig. 5(a) and -1.6 V in Fig. 5(c)). Therefore, I_D is dominated by the current in the buried channel or the current in the accumulation layer or both at different V_G.

The output curves (i.e., I_D-V_D) are reported in Fig. 5(b) and (d) with a gate voltage (V_G) varying from 0 V to -2 V,

showing a tendency to saturate with lowering V_D. When a buried channel is formed (V_G between V_{th1} and V_{th2}), the loss of gate control degrades the output conductance in saturation (like it does for the subthreshold slope).[33, 35] When an accumulation layer is formed at a V_G below V_{th2}, the coupling from the V_D still greatly controls the carriers in the accumulation layer due to the quasi-neutral region between the drain electrode and the channel.[33, 35] Therefore, clear saturation regions can be harder to reach in the AM TFTs.

Several parameters are calculated from the transfer curves. The on/off current ratio (I_{on}/I_{off}) is defined as the ratio of maximum to minimum I_D. The field-effect mobility in accumulation layer is expressed by:[36]

$$\mu_{FE} = \frac{L}{WC_{ox}V_D} g_m \quad (7)$$

where g_m is extracted below V_{th2} from -3 to -2 V. In Fig. 5(a), CuO TFT (L=25 μm) shows an I_{on}/I_{off} of 1.3×10^2 and a μ_{FE} of 1.1×10^{-3} cm^2 V^{-1} s^{-1}. In Fig. 5(c), CuO TFT (L=10 μm), shows similar performances, with an I_{on}/I_{off} of 1.7×10^2 and a μ_{FE} of 0.62×10^{-3} cm^2 V^{-1} s^{-1}. Such low μ_{FE} is typical for TFTs based on copper oxides regardless of the deposition techniques due to TFT nonidealities from contact resistance or interfacial traps.[15] Here, compared to a measured Hall concentration of ~10^{14} cm^{-3} for a bare CuO thin film on SLG,[23] N_A of CuO measured in TFTs increases significantly to a minimum of 4.83×10^{17} cm^{-3} following the MOS process. According to the increasing linear tendency of the hole mobility with decreasing hole concentration for CuO,[23] the hole mobility is limited at such high N_A.

The subthreshold swing (SS) that describes the switching quality of TFTs is given by:[27,37]

$$SS = \left(\frac{\partial \log(I_D)}{\partial V_G}|_{max}\right)^{-1} = \frac{kT}{q}\ln 10\left(1+\frac{C_{stot}}{C_{cg}}\right) \quad (8)$$

where C_{cg} is the channel to gate capacitance and C_{stot} is the total substrate capacitance, including trap capacitance at HfO_2/CuO interface ($C_{it1}=qD_{it1}$), trap capacitance at CuO/Air interface ($C_{it2}=qD_{it2}$) and total coupling parasitic capacitance from channel to ground (C_{sub}). Extracting SS of the buried channel around V_{th1}, 1.04 and 1.78 V dec^{-1} are obtained for CuO TFTs with L of 25 and 10 μm, respectively. In this voltage regime, C_{cg} of around 2×10^{-7} F cm^{-2} is extracted from Fig. 4(a). As C_{it1} is about 9.6×10^{-9} F cm^{-2} and C_{sub} is considered low for CuO TFTs on SLG, then the high SS should be explained by D_{it2}, i.e. probably interfacial traps between unpassivated CuO and air, estimated using (8) to be up to 2.04×10^{13} and 3.57×10^{13} eV^{-1} cm^{-2} for CuO with L of 25 and 10 μm, respectively. With top surface passivation, D_{it2} could be decreased and thus SS and μ_{FE} could be improved.[15]

In conclusion, CuO thin film fabricated by room-temperature DC reactive magnetron sputtering shows an excellent crystal growth of tenorite CuO. P-type CuO TFTs fabricated on SLG with a gate dielectric of HfO_2 deposited by ALD demonstrate competitive performances in accumulation mode compared to standard copper oxide TFTs based on silicon techniques.[3,14,15] By characterizing a CuO MOS capacitor, the field-effect mobility appears much lower than in Hall measurements due to a high apparent doping concentration in CuO film and a high Q_f in HfO_2. Subthreshold swing appears limited by the high interfacial traps between CuO and air, and to a lesser extent by a decreased C_{cg} caused by the buried channel dominance in subthreshold and possible parasitic coupling capacitance in a bottom-gate configuration. These results show great potential of CuO TFTs towards future applications in sensors or CMOS logic circuits.

To further optimize CuO TFTs, CuO could be annealed in a controlled ambiance at a temperature compatible with the HfO_2 stability and the top CuO surface could be passivated by Al_2O_3 sputtered in the same chamber after CuO sputtering without exposing the sample to the air.[38] Additionally, reducing the thickness of CuO can be of great interest to improve the TFT performances in a lower-cost way of fabrication. By thickness reduction, the depletion region can be minimized and C_{cg} can be effectively lowered when a buried channel is formed. In such case, the performances of CuO TFTs could be improved, such as the subthreshold wing carrier mobility, carrier velocity, output drain current, short channel effects and impact of doping fluctuation as it was demonstrated in silicon.[39, 40]

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts of interest to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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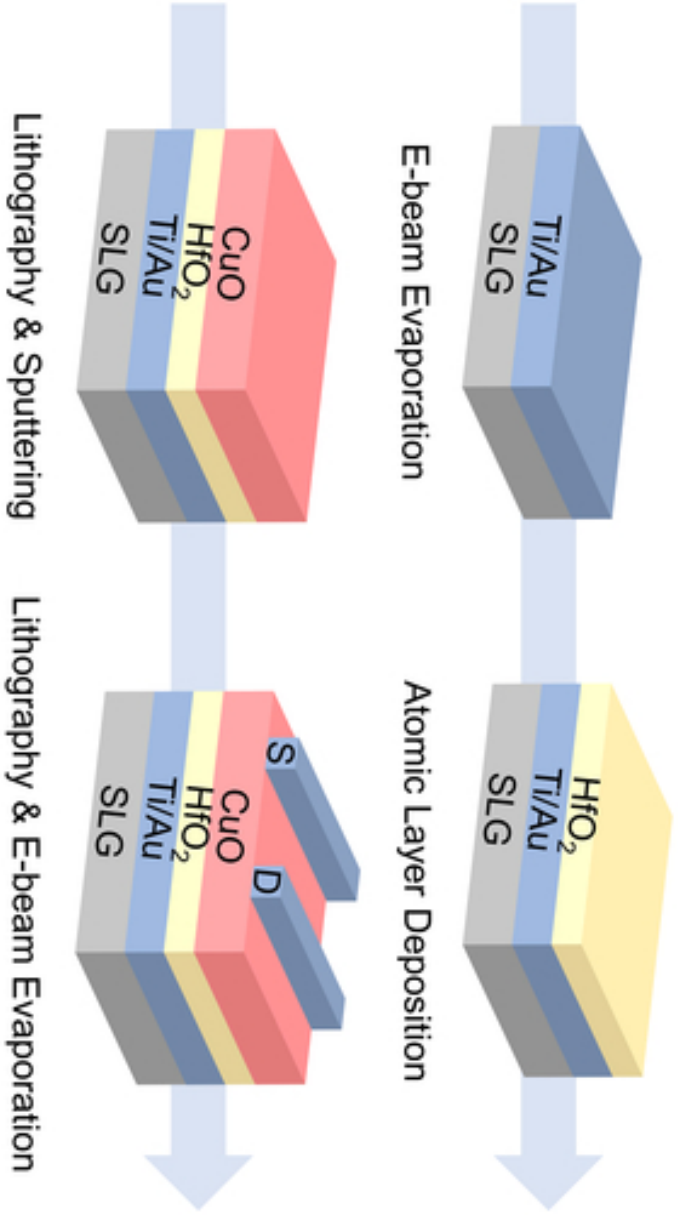

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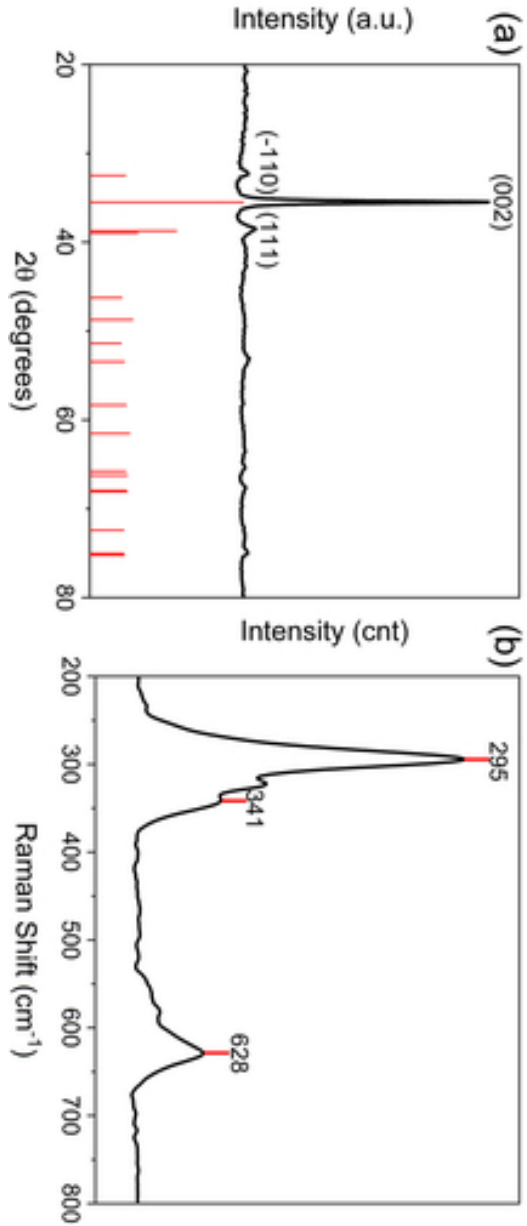

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