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22 nm FD-SOI MOSFET Figures of Merit at high temperatures upto 175 °C

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***Abstract*— This work studies the impact of increase in temperature on the RF and analog figures of merit (FoMs) of 22 nm FD-SOI MOSFETs from room temperature of 25 °C to 175 °C. DC and RF measurements are performed on the MOSFETs to extract the main RF FoMs over temperature. From DC measurements in temperature, the zero-temperature coefficient (ZTC) point and threshold voltage (V_{Th}) reduction on increasing temperature is observed. Through direct on-wafer RF measurements reductions of 21 % in the current-gain cut-off frequency (f_T) and of of 14 % in the maximum oscillation frequency (f_{max}) are observed at 175 °C compared to 25 °C. In particular, the evolution over temperature of transconductance (g_m) appears to be one of the major causes of the degradation in f_T and f_{max}.**

Keywords*— FDSOI, f_T, f_{max}, Figures of Merit (FoMs), high temperature

I. Introduction

22 nm FD-SOI technology from GlobalFoundries is a technology of choice for upcoming RF and high frequency applications. This technology targets a wide variety of applications ranging from IoT/wearables to automotive, millimetre wave radar, 5G communications, etc. The intrinsic f_t and f_{max} of NMOS devices in 22FDX technology are reported to be around 347 GHz and 371 GHz [1], demonstrating excellent results that enable RF and millimetre wave designs. The RF performance of MOSFETs can be evaluated by considering 2 main figures of merit (FoMs): cut-off frequency f_t and maximum oscillation frequency f_{max}. Previously, electronic circuitry exposed to high temperature applications was mainly limited, but this has now broadened to diverse applications. Circuits like automotive electronic circuits located close to the engine for example, are subject to high temperature environment [2]. Additionally, the presence of self-heating in devices causes a rise in temperature simply due to Joule heating from device current during operation. These aforementioned factors motivate the need to observe and correctly quantify the effect of these increased temperatures on the performance of such circuits. In this paper, the effect of increased temperature on the 22 nm FD-SOI MOSFET devices' RF and mm-wave performance metrics (FoMs) of 22 nm FDSOI MOSFETs are presented through on-wafer measurements and extractions.

There is very limited literature on the performance of 22 nm FD-SOI devices at high temperatures. To the authors' best knowledge, the only work [3] studied mainly high frequency performance of FETs in this technology with limited data versus temperature. In our work, the existing study is extended by including detailed results of variation of various FoMs of FETs in this technology versus temperatures up to 175 °C.

II. Experimental details

The devices used in this study are NFETs which originate from the 22 nm FD-SOI technology from GlobalFoundries [1]. The gate length is 20 nm, total width is 60 µm for each of these devices composed of 120 fingers (20 fingers with a multiplicity of 6) of 0.5 µm finger width.

For the RF characterization, S-parameters are measured in a frequency range from 200 MHz to 40 GHz. A PNA-X vector network analyser and two RF |Z| probes of 100 µm pitch are used for these measurements. SOLT (Short-open-load-thru) method is used for calibration at each temperature point separately. De-embedding is done by measuring dedicated Open and Short structures corresponding to each device. The temperature points at which measurements have been carried out are 25 °C, 75 °C,

125 °C and 175 °C respectively. This has been achieved by using a Thermochuck from Temptronic that allows heating up the devices to the desired temperature points with accurate and stable temperature control. The system was kept steady for 30 minutes on reaching each temperature point to aid in stabilizing the temperature of the devices and calibration kit. The back gate was grounded during measurements (V_{bg} = 0 V).

III. Results and Discussion

Fig. 1 shows the I_d-V_g and the g_m-V_g curves in saturation at V_d = 0.8 V at the 4 different temperature points. The Zero Temperature Coefficient (ZTC) point for I_d, defined as the V_g at which I_d remains the same regardless of temperature, is observed to be at a V_g around of 0.62 V (for V_d = 0.8 V). I_d increases with temperature at lower V_g biases, because of reduction in threshold voltage with increasing temperature. However, I_d decreases with increasing temperature at higher V_g biases due to stronger phonon scattering decreasing carrier mobility. These two mechanisms balance each other at the ZTC point resulting in an I_d independent of temperature [4], [5]. A similar ZTC point for transconductance g_m is observed for V_g around 0.38 V, where the g_m remains constant regardless of temperature. Such a bias point could be of great interest for applications where g_m is required to be independent of temperature. With f_T being proportional to g_m, this also relates to a ZTC in f_T (where f_T does not change with temperature) at that corresponding ZTC point for g_m provided that the total gate capacitance $C_{gg,T}$ is relatively independent of temperature as observed in (1).

$$f_T, f_{max} \sim \frac{g_{m,e}}{C_{gg,T}} \quad (1)$$

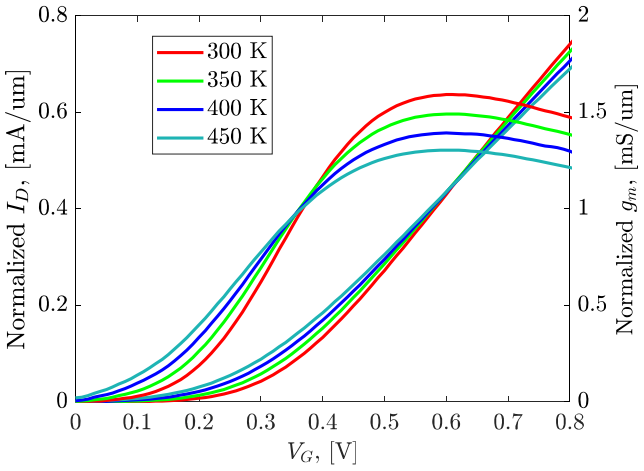

Fig. 1. Normalized drain current I_d and transconductance g_m vs gate voltage V_g at V_d = 0.8 V at different temperatures.

The reduction of threshold voltage V_{Th} with temperature is shown in Fig. 2. The V_{Th} shown here is computed using the second-derivative method from [6] in the linear regime. V_{Th} reduction per unit temperature is found to be 0.6 mV/°C from the measurements over the temperature range of 300 K to 450 K. Such a V_{Th} reduction slope with temperature is a typical value observed in advanced technologies with ultra-thin bodies like UTBB, FinFETs, nanowires etc [7].

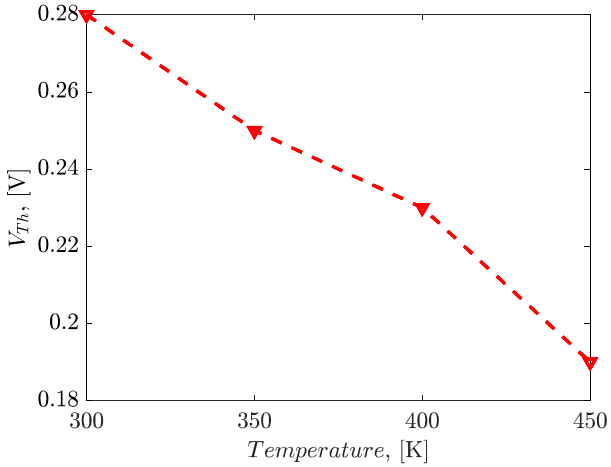

Fig. 2. V_{Th} variation versus temperature.

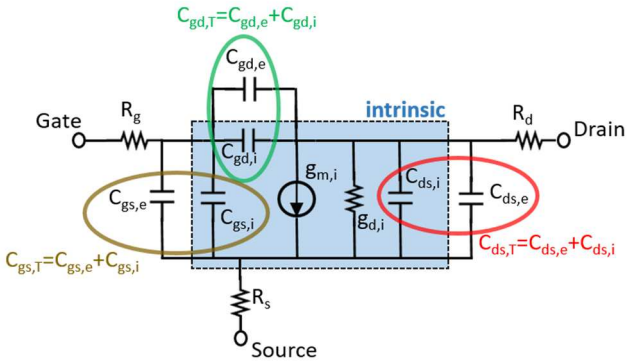

Fig. 3. Small signal equivalent circuit for MOSFET [10].

Regarding the extraction, from the RF measurements, the S-Parameters are converted into Y-parameters. The output conductance (g_d) is computed as the real part of Y_{dd}, transconductance (g_m) is the real part of Y_{dg}. The capacitances can be computed from the imaginary part of Y-parameters. The small signal equivalent circuit (SSEC) for MOSFETs can be represented as shown in Fig. 3. The SSEC elements can be extracted from the S-parameter measurements similar to the procedure described in [11]. Extrinsic parameters refer to the measured values whereas intrinsic parameters refer to the case where the parasitics are removed. Thus, extrinsic parameters $g_{m,e}$, $C_{gd,e}$, $C_{gs,e}$ and $C_{ds,e}$ refer to the measured transconductance, gate-to-drain capacitance, gate-to-source capacitance and drain-to-source capacitance respectively, while $g_{m,i}$, $C_{gd,i}$, $C_{gs,i}$ and $C_{ds,i}$ represent their intrinsic counterparts. R_g, R_d and R_s are the gate, drain and source resistances respectively. In this paper, we focus on the transconductance g_m and the total gate capacitance $C_{gg,T}$ without going into details of the other SSEC elements. Their effect on f_T and f_{max} are discussed. The values of parameters demonstrated in this work are normalized with respect to the total width of the device.

Both the maximum intrinsic and extrinsic transconductances $g_{m,i}$ and $g_{m,e}$ show a degradation of around 24% and 18% going from 300 K to 450 K respectively, as

demonstrated in Fig. 4. The bias condition was V_d = 0.8 V and V_g = 0.6 V (the value of V_g for which $g_{m,max}$ was observed). The degradation in $g_{m,e}$ is related to both R_{sd} variation and mobility degradation with temperature whereas the degradation in $g_{m,i}$ is related to mobility degradation only. As R_{sd} variation is weaker than that of mobility, the degradation in $g_{m,i}$ is stronger than that of $g_{m,e}$.

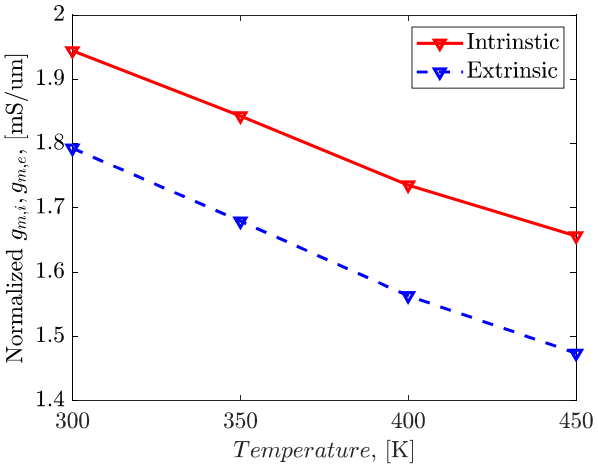

Fig. 4. Variation of maximum normalized intrinsic and extrinsic transconductance $g_{m,i}$ and $g_{m,e}$ with temperature at V_d = 0.8V and V_g corresponding to $g_{m,max}$.

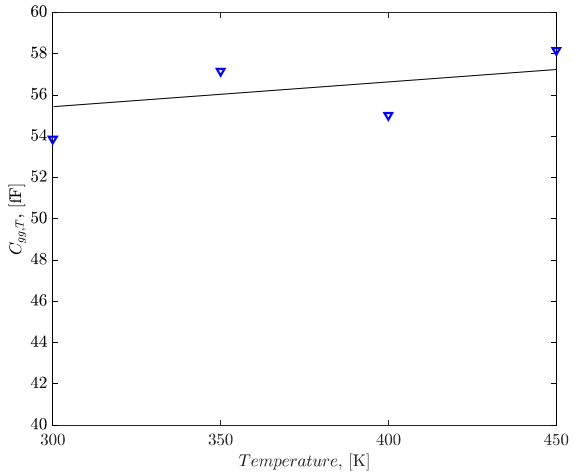

Fig. 5. Variation of total gate capacitance $C_{gg,T}$ with temperature at $V_g = V_d$ = 0.8V.

In Fig. 5, the variation of total gate capacitance $C_{gg,T}$ versus temperature is demonstrated. $C_{gg,T}$ extracted is found to be mostly steady over the temperature range of 300 to 450 K, varying by only a few fF which is within the extraction precision.

Two of the main parameters of interest, the RF FoMs, the f_T and f_{max} are found to degrade with temperature as seen in Fig. 6 and Fig. 7 respectively. f_T and f_{max} are computed from the extrapolation of the current gain H_{21} and unilateral gain to 0 dB respectively at V_d = 0.8 V and V_g = 0.6 V (that corresponds to maximum g_m). Qualitatively, referring back to (1), f_T is proportional to $g_{m,e}$. This is seen from the trends observed in Fig. 6 for f_T as f_T degrades in a similar manner to g_m as expected. Following up from this, f_{max} is seen to be degrading with temperature as well. On going from room temperature to 450 K, a reduction of 22% and 14% can be observed for f_T and f_{max} respectively.

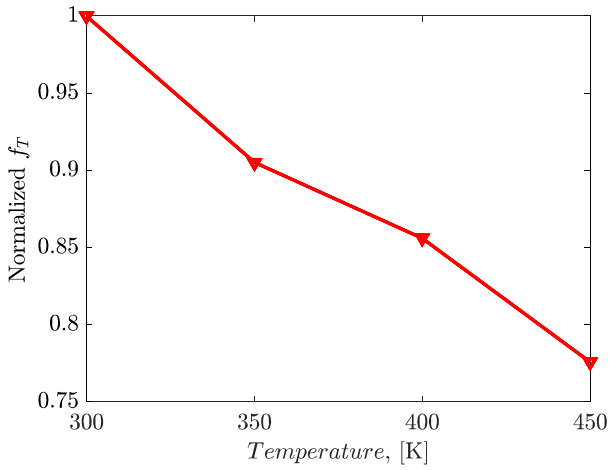

Fig. 6. Variation of normalized current-gain cut-off frequency f_T with temperature at V_d = 0.8 V and V_g corresponding to $g_{m,max}$.

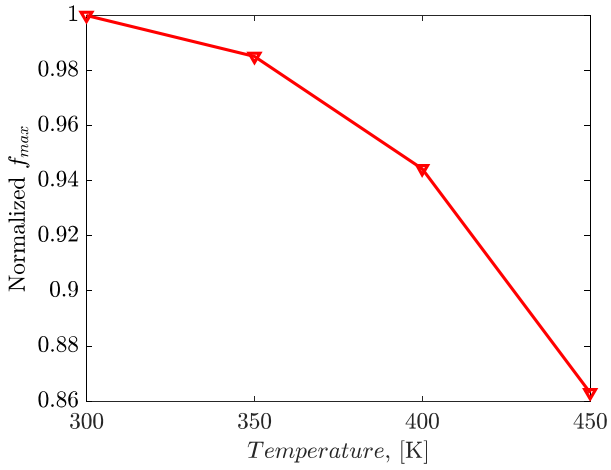

Fig. 7. Variation of normalized maximum oscillation frequency f_{max} with temperature at V_d = 0.8 V and V_g corresponding to $g_{m,max}$.

IV. Conclusion

The effect of temperature rise on the RF FoMs from measurements of MOSFETs in 22 nm FDSOI technology was studied in this work. The ZTC points for I_d and g_m were observed from the IV characteristics with temperature. V_{Th} was seen to reduce by 0.6 mV/°C over the temperature range of 300 to 450 K. For the RF FoMs, around 21% reduction in f_T and 14% reduction in f_{max} was observed when temperature is increased from 300 K to 450 K. Additionally, the behaviour of transconductance g_m and gate capacitance C_{gg} with temperature was also investigated. The degradation in g_m with temperature was found to be one of the major factors for the reduction in the aforementioned FoMs.

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