Impact of Device Shunt Loss on DC-80 GHz SPDT in 22 nm FD-SOI

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***Abstract*—In this paper, shunt admittance parameters of FET devices for RF switch applications at mm-wave frequencies are investigated. These parameters complement the well know series elements R_{on} and C_{off} that are widely used to benchmark devices for switch applications. It is shown that at mm-wave frequencies and beyond, the shunt FET elements can be responsible for significant loss, and devices with the lowest $R_{on}C_{off}$ metric may in fact not be the best ones suited to high-frequency switch implementation. This is demonstrated in this paper, which compares 20 nm long SLVT and BFMOAT devices in the 22FDX® technology from GLOBALFOUNDRIES. While the SLVT presents an $R_{on}C_{off}$ metric of 100 fs, it is outperformed by the BFMOAT device that has an $R_{on}C_{off}$ of 160 fs, because the BFMOAT device reduces parasitic shunt loss, i.e. the real part of device shunt admittance, which cannot be compensated for by passive matching networks, and degrades the switch's insertion loss. After analyzing the shunt loss contribution to switch performance and demonstrating that a BFMOAT-based design is preferable over an SLVT design in the high-end of the mm-wave spectrum, the performance of a fabricated and measured DC-80 GHz SPDT device is presented. This design showcases the BFMOAT device's excellent characteristics for mm-wave switch applications by achieving competitive results. At 60 GHz it presents 2.1 dB insertion loss, 25 dB isolation, a P_{1dB} of 19.9 dBm and an IIP3 of 33.6 dBm, for a total area of 0.014 mm².**

Keywords— $R_{on}C_{off}$, shunt parasitic loss, switch, SPDT, ultra-wideband, millimeter-wave IC, 5G front-end, FD-SOI, UTBB

I. INTRODUCTION

The well-known transistor figure of merit for RF switch applications is the $R_{on}C_{off}$ product. For a single device in switch configuration (RF-floating gate node) R_{on} is the series device resistance between source and drain when biased in an on-state regime, and is inversely proportional to transistor width W. C_{off} is the series device capacitance when biased in an off-state regime, and is proportional to transistor width W.

At RF frequencies (i.e., below a few tens of GHz), the *series* terms R_{on} and C_{off} are quite sufficient to describe a device technology for switch applications. Shunt capacitance C_{sh} terms can be neglected at RF, since the $j\omega C_{sh}$ admittance is quite low, and any parasitic C_{sh} can be compensated for using passive matching circuits. This is not the case for any shunt conductance terms G_{sh}, that will always be a source of additional degradation in switch insertion loss (IL), regardless of any passive matching scheme.

In the 22FDX® node from GLOBALFOUNDRIES, the SLVT device presents an $R_{on}C_{off}$ metric of the order of 100 fs [1,2], but is outperformed by the BFMOAT device for mm-wave switch applications [2,3], even though the BFMOAT's $R_{on}C_{off}$ is substantially higher at around 160 fs.

In this paper, we expose the origin of BFMOAT's higher performance results despite a significantly larger $R_{on}C_{off}$. This figure of merit is then shown to be insufficient in general for benchmarking devices for switch applications in the high mm-wave spectrum and beyond. Finally, a wideband DC-80 GHz SPDT module was fabricated and measured demonstrating the BFMOAT device's quality for mm-wave switch applications.

II. SHUNT LOSS ANALYSIS

A. Impact on a Single FET

The mm-wave SLVT and BFMOAT NFET devices from GLOBALFOUNDRIES' 22FDX® node are depicted in Fig. 1a. The SLVT incorporates a back-gate (BG) electrode below the thin (20 nm) buried oxide. For switch applications, applying a positive bias to the BG results in a more conductive channel in the on-state and to a lower value of R_{on}. For this reason, SLVT devices are preferred at low frequencies (roughly below 30 GHz) [2,3]. The BFMOAT device sacrifices the BG functionality for reduced shunt losses G_{sh} to the ground reference node. Both devices include a P-type substrate-tap ring (Sub) to include shunt parasitics in the mm-wave models.

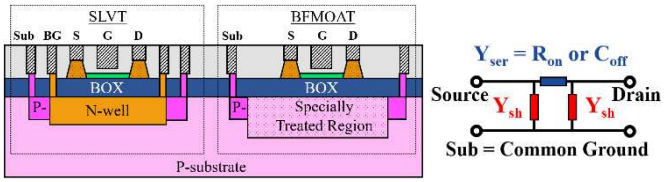


Fig. 1. a: Simple representation of the SLVT and BFMOAT NFETs. b: Simple two-port equivalent circuit pi-model between source and drain.

Fig. 1b illustrates that R_{on} and C_{off} are both series elements of the two-port pi-model of a FET in switch configuration.

To highlight the impact of G_{sh} a single FET is simulated in a two-port configuration between source and drain. The simulation setups for both the SLVT and BFMOAT are depicted in Fig. 2, where the substrate terminal of both FETs is defined as the common ground node of the two ports. The gate and back-gate are biased through large resistances, and these nodes can be considered as RF floating. Both FETs are 20 nm long, are referenced to the C3 (5th) metal layer, and have five fingers ($N_f = 5$), each with a width of $W_f = 5$ µm.

Fig. 3 then plots the results pertaining to each FET. The raw S-parameters are plotted, and so are the equivalent circuit elements of the two-port model (see Fig. 1b). Both on- and off-states are simulated. The on-state is achieved by applying 0.9 V to the gate (V_g) and 3 V to the back-gate (V_{bg}), while in the off-state $V_g = -0.9$ V and $V_{bg} = 0$ V.

The R_{on} element (extracted as $\Re\{-1/Y_{21}\}$) determines the low frequency loss, however the real part of the shunt admittance $G_{sh} = \Re\{Y_{sh}\}$ increases with frequency and is responsible for substantial additional loss in the SLVT device,

where $Y_{sh}=Y_{11}-Y_{21}$ (=$Y_{22}-Y_{21}$ in a symmetrical device). This is demonstrated through the results of Fig. 3c which shows that S_{21} appreciably decreases above approximately 30 GHz. Fig. 3e shows that the power transfer coefficient $|S_{21}|^2$ reduces by 11% over the considered frequency range, and that only 2% of this is due to reflection by increased mismatch (see $|S_{11}|^2$). This indicates that the $|S_{21}|^2$ reduction in frequency is mainly attributable to increased losses in the network.

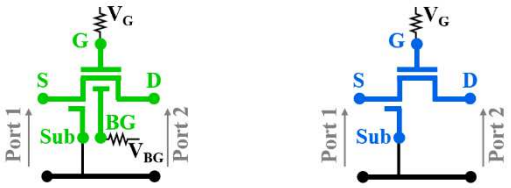


Fig. 2. Schematic of the two-port simulated FETs for switch performance evaluations. Left: SLVT. Right: BFMOAT. The results are plotted in Fig. 3.

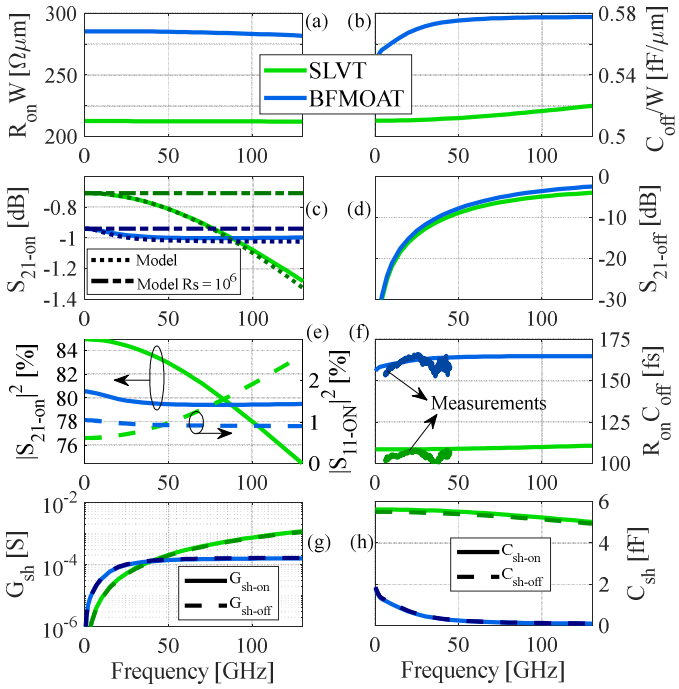


Fig. 3. Loss and equivalent circuit (pi-model) analysis of an SLVT and a BFMOAT FET simulated in a two-port (switch) configuration, as per Fig. 2. Both devices are referenced to the C3 (5th) metal plane and have W_f = 5 µm and N_f = 5 (for a total width of $W = N_f W_f$ = 25 µm).

Fig. 3g shows that the G_{sh} term of the BFMOAT devices saturates at a value of around 150 µS, which it reaches at around 30 GHz. This explains the 1% degradation in $|S_{21}|^2$ at 30 GHz. The SLVT's G_{sh} term reaches 1 mS at 110 GHz, and continues to increase with frequency. This term is responsible for the 9% increase in power loss in the SLVT.

Fig. 3h shows that the SLVT presents higher C_{sh} than the BFMOAT. Though this makes it harder to design ultra-broadband SLVT-based switches compared to BFMOAT-based ones, the C_{sh} parasitic can be compensated for in any given band using passive matching networks. This is not the case for the parasitic G_{sh} term, which will always be a source of additional loss.

The extracted G_{sh} and C_{sh} elements depend little on the bias state of the transistor (i.e. they are roughly the same in the on- and off- states: $G_{sh\text{-}on} \approx G_{sh\text{-}off}$ and $C_{sh\text{-}on} \approx C_{sh\text{-}off}$).

Let S_{21on} be the analytical formulation for the device's full insertion loss (defining $G_{on} = 1/R_{on}$):

$$S_{21on} = \frac{2G_{on}Y_0}{(Y_{sh}+Y_0)(Y_{sh}+Y_0+2G_{on})} \approx S_{21ser}K \quad (1)$$

$$S_{21ser} = \frac{2G_{on}}{Y_0+2G_{on}} \quad (2)$$

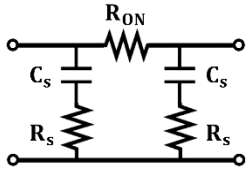
$$K = \frac{Y_0}{G_{sh}+Y_0} \quad (3)$$

It can be approximately written as a product of S_{21ser}, which is the insertion loss when neglecting shunt elements (i.e. when $G_{sh} = 0$) by the factor K, which accounts for the power dissipated in G_{sh} in parallel with the port admittance Y_0.

At 130 GHz the SLVT presents a shunt conductance of G_{sh} ≈1.2 mS to ground, which is a significant proportion of the Y_0 = 20 mS port load, and justifies entirely the |K| = 0.51 dB higher power loss (equivalent to 9% in $|S_{21}|^2$) compared to lower frequencies, as demonstrated by the fitting of the simple equivalent model in Fig. 3c. The dotted-line curves of Fig. 3c were obtained from the model represented here below, with Table 1 listing the lumped values associate to the two devices.

Table 1. Parameters of the simple on-state models used in Fig. 3 (dashed lines).

Model	R_{on} [Ω]	C_s [fF]	R_s [Ω]	K [dB]
SLVT	8.5	4.7	82	-0.51
BFMOAT	11.4	1.7	5530	-0.07



This simple model demonstrates well the impact of the real part of the shunt admittance on the overall loss from the two FETs (R_s = 5.5 kΩ for the BFMOAT and 82 Ω for the SLVT), and fits well (to the first order) to the simulated $S_{21\text{-}on}(f)$ curves (full PDK models).

Fig. 3c further shows that at lower frequencies the loss in the on-state is well accounted for by the series term (R_{on}) only (see model dashed-line curves with R_s set to 10^6). This corresponds to the S_{21ser} parameter, without shunt device loss.

It is then concluded that the well-known $R_{on}C_{off}$ FoM is insufficient to characterize switch performance at high-end mm-wave frequencies (when effects related to shunt substrate impedance are non-negligible). Indeed, both R_{on} and C_{off} are purely series elements of the full two-port device pi-model and the current FoM does not include additional losses related to the shunt admittance of the switch equivalent circuit.

Table 1 highlights that high values of R_s are desirable to avoid large shunt loss factors K. In fact, low R_s values can be tolerated if the C_s elements are low. In the 22FDX® technology under consideration, the C_s terms are quite high due to a very thin relative to buried oxide layer (20 nm).

Measurements of the SPDT devices from [3] enabled the extraction of $R_{on} = \Re\{-1/Y_{21}\}$ and $C_{off} = \mathcal{I}\{-Y_{21}\}$ of both types of FET, and the results are superimposed on the data of Fig. 3f. These measurements agree well to the simulated data and serve to experimentally confirm the $R_{on}C_{off}$ value of around 100 fs for the SLVT and of around 160 fs for the BFMOAT. Due to the presence of the shunt branch FET stacks, the Y_{sh} parameters could not be extracted from those full-SPDTs.

B. *Impact on a Series-Shunt SPDT*

Full SPDT switches were also simulated based on both types of FET, implemented using the broadband series-shunt topology, as depicted in Fig. 4. A stack of three transistors (all 20 nm-long) was used in each branch (N_{stk} = 3) targeting 20 dBm of input power 1-dB compression point (P_{1dB}) [3].

When the switches are in the on-state, the control voltages are set to [V_{g1}, V_{bg1}] = [0.9, 3] V and [V_{g2}, V_{bg2}] = [-0.9, 0] V. In the off-state, they are set to [V_{g1}, V_{bg1}] = [-0.9, 0] V and [V_{g2}, V_{bg2}] = [0.9, 3] V.

The designs were made to have the same device sizes in the series branches and to achieve similar isolation levels over the entire band. For both designs, each series FET was implemented using $W_{f\text{-}ser}$ = 5 µm and $N_{f\text{-}ser}$ = 15. In the SLVT-based design, each FET of the shunt branches is implemented with $W_{f\text{-}sh}$ = 3 µm and $N_{f\text{-}sh}$ = 10, while in the BFMOAT-based SPDT they are set to $W_{f\text{-}sh}$ = 3 µm and $N_{f\text{-}sh}$ = 30. This enables almost identical isolation curves to be attained for both designs, as shown in Fig. 5b, which then permits us to analyze solely the on-state performance while comparing the two types of SPDTs fairly.

In order to compare the S_{21} curves, the (lossless) matching circuits depicted in Fig. 4 are adapted at each frequency point in order to achieve reflection coefficients S_{ii} at each port lower than -25 dB in the on-state (so that we may ignore any lack of power transfer through the switch due to mismatch, and focus solely on the S_{21} data).

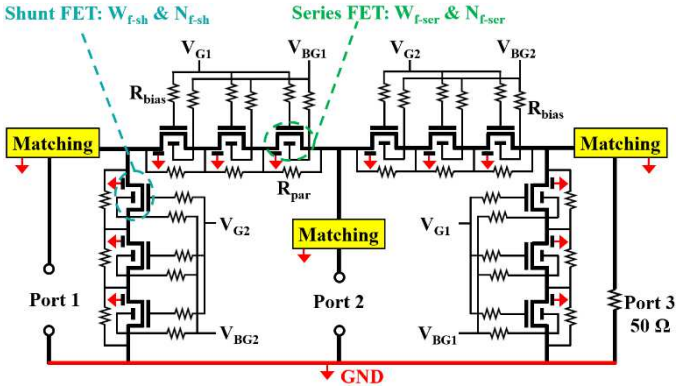


Fig. 4. Schematic of the designed SPDT switches.

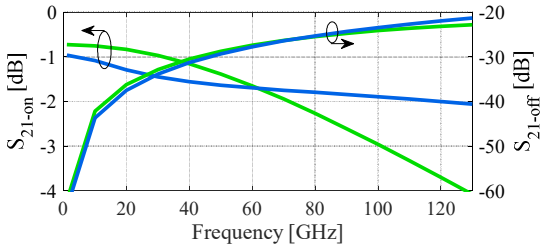


Fig. 5. Simulated $S_{21\text{-}on}$ and $S_{21\text{-}off}$ of the SLVT-based and BFMOAT-based SPDTs of Fig. 4. The lossless matching circuits are adapted at each frequency point in order to achieve reflection coefficients S_{ii} at each port lower than -25 dB in the on-state. Pre-layout data referenced to the C3 (5^{th}) metal layer.

The results from Fig. 5a demonstrate additional loss in the SLVT-based SPDT above 70 GHz –despite lower R_{on} (and $R_{on}C_{off}$) metrics than the BFMOAT devices– due to shunt loss terms in the individual FETs of the full SPDT.

III. Measurements of a DC-80 GHz BFMOAT SPDT

To demonstrate the BFMOAT's performance for high mm-wave switch modules, a DC-80 GHz SPDT was designed, fabricated and measured based on the wideband series-shunt topology (Fig. 4). The design is performed with probe access to two ports, with the third port (second throw) loaded to 50 Ω using an on-chip mm-wave precision integrated resistor.

A. *Design Parameters*

The design was performed to achieve minimal on-state insertion loss while maintaining at least 20 dB of isolation in the off-state at 80 GHz. Including EM post-layout simulations and open-pad de-embedding, this was achieved during the design process for the following choice of parameters: $W_{f\text{-}ser}$ = $W_{f\text{-}sh}$ = 3 µm and $N_{f\text{-}ser}$ = $N_{f\text{-}sh}$ = 15. The gate lengths of all FETs were set to the minimum allowable value of 18 nm.

B. *Results*

The SPDTs were fully characterized under small-signal conditions using an on-wafer set-up employing a pair of GSG Infinity probes from FormFactor and a 130 GHz PNA vector network analyzer (N5291A) from Keysight. The acquired raw S-parameters are corrected with a Load-Reflect-Reflect-Match calibration performed on an Impedance Standard Substrate.

The simulated and measured S-parameter results labelled as 'full-device' in Fig. 6 (red curves) are the raw data, as measured/simulated including the coplanar GSG landing pad structures for the on-wafer probes. Data from a measured open structure was used to de-embed the GSG probe pads from the measured device, and data from the EM-simulated open structure was used to de-embed the full post layout simulation (which includes the GSG pads). These de-embedded results are also plotted in Fig. 6 (as the blue curves).

Fig. 7 is a photograph of the measured device, and the dashed lines illustrate its reference planes after open de-embedding. The feed lines from those planes to the active part are 50 µm-long TFMS lines of 50 Ω characteristic impedance. After open-de-embedding, these lines (implemented in the QB (10^{th}) metal layer) are considered as part of the SPDT.

The core area of the SPDT is highlighted in Fig. 7 and is roughly 130 µm x 110 µm.

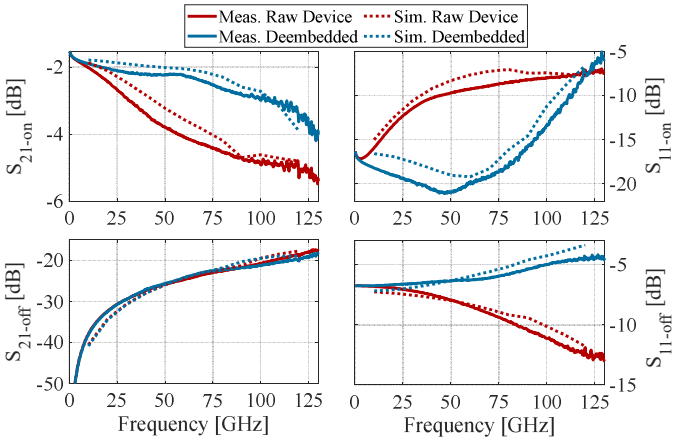


Fig. 6. Simulated and measured $S_{ij\text{-}on}$ and $S_{ij\text{-}off}$ of the fabricated BFMOAT-based SPDT.

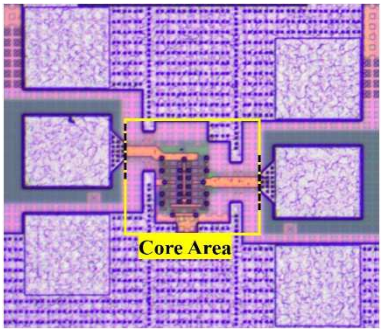


Fig. 7. Photograph of the fabricated DC-80 GHz BFMOAT-based SPDT.

Good agreement is achieved between the post-layout simulations and the measured data. The isolation spec is well met and is higher than 20 dB from DC to 80 GHz. The device's insertion loss is less than 2.2 dB up to 60 GHz, and is 2.6 dB at 80 GHz. The large-signal FoMs of the switch were simulated at 60 GHz, and a P_{1dB} value of 19.9 dBm and an IIP3 of 33.6 dBm were obtained.

Table 2 benchmarks these results against the published state-of-the-art SPDTs covering frequencies close to 60 and/or 80 GHz, and demonstrates the competitiveness of the presented DC-80 GHz BFMOAT-based series-shunt switch.

IV. Conclusion

In this paper, *shunt* parasitics were shown to be non-negligible contributors to FET performance for mm-wave switch applications and complement the well-known $R_{on}C_{off}$ figure of merit for FET benchmarking, as $R_{on}C_{off}$ contains information only on the *series* Y-parameter Y_{21}. While the imaginary parts of shunt admittances can be compensated for with matching circuits, the real parts cannot, and will always be a source of S_{21} degradation in all of the most common switch topologies. The importance of shunt loss was demonstrated by analyzing how a BFMOAT device from GlobalFoundries' 22FDX® outperforms an SLVT as a mm-wave switch despite having a significantly larger $R_{on}C_{off}$.

Finally, a wideband DC-80 GHz SPDT was designed and fabricated to showcase the BFMOAT's low shunt-parasitic performance. On-wafer measurements demonstrate this SPDT to be competitive over this band, with an insertion loss of 2.6 (2.1) dB at 80 (60) GHz, and an isolation of 25 (21) dB at 80 (60) GHz, for a of P_{1dB} = 19.9 dBm and IIP3 of 33.6 dBm.

Acknowledgments

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Table 2. State-of-the-art mm-wave SPDT modules operating close to 60 and/or 80 GHz.

Work	Technology	Topology	Frequency [GHz]	Insertion Loss [dB]	Isolation [dB]	P_{1dB} [dBm]	IIP3 [dBm]	Area w/o pads [10^{-3} mm²]
[4]	130 nm CMOS	Series-shunt	57-66	4.5-5.8	24-26	4.1	-	220
[5]	130 nm CMOS	λ/4-shunt	50-70	2	32	13-14*	23	125
[6]	130 nm CMOS	Matching-network	57-66	< 2.0	> 21.1	13.8*	-	20
[7]	90 nm CMOS	λ/4-shunt	50-70	< 2.0	> 27	13.5	22.5	275
[8]	65 nm CMOS	Traveling Wave	17-100	2.8-4.5	> 15	17	-	420 $ 200 $$
[9]	180 nm SiGe	Transformer	90	22.7	14	13.8	23.8*	43
[10]	800 nm InP DHBT	λ/4-shunt	90-170	3.0-5.0	42-55	> 15	-	950 $ 650 $$
[11]	100 nm Tri-Gate GaN HEMT	λ/4-shunt	68-134	1.1-2.1	17.6-21.5	> 25	-	308
[12]	50 nm InGaAs mHEMT	λ/4-shunt	50-75	1.0-1.6	31.6-32.8	> 22	-	348
		λ/4-shunt	72-110	1.0-1.6	28.5-31.4	> 19	-	216
[13]	45 nm SOI	Series-shunt	DC-60	2.5	22	7.1	18.2	40
This work	22 nm FD-SOI	Series-shunt	DC-80	2.1 @60 GHz 2.6 @80 GHz	25 (60 GHz) 21 (80 GHz)	19.9* (60 GHz)	33.6* (60 GHz)	14

*Simulated data. $Including pads. $$Estimate excluding pads.