g_m/I_D-derivative Method for Threshold Voltage Extraction in Junctionless MOSFETs

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***Abstract*— In this work, we validate an applicability of the g_m/I_D-derivative method for the threshold voltage extraction in junctionless MOSFETs using numerical simulations, analytical modeling and experimental data. We show that this technique is more accurate than the traditionally used dg_m/dV_g method.**

Keywords—junctionless MOSFETs; threshold voltage; transconductance-to-current ratio.

I. Introduction

Junctionless (JL) MOSFETs, featuring excellent scalability along with simplified fabrication process, are presently recognized as very promising candidates for further CMOS scaling [1]-[3]. Though electrical characteristics of JL MOSFETs are similar to those of inversion-mode MOSFETs, the operation of both types of the devices is not the same. For this reason, the conventional techniques commonly used for electrical characterization of inversion-mode MOSFETs are often inapplicable (or misleading) in the case of JL devices. Therefore, there is a need in the development of the techniques for the electrical characterization and parameter extraction of JL devices.

A critical parameter of the JL MOSFET is the threshold voltage (V_{TH}), which characterizes the transition from full depletion to bulk conduction regime. Thus, an accurate and reliable V_{TH} extraction is crucial for JL device characterization and modeling. Since in bulk conduction regime, the mobile charge (Q_m) varies non-linearly with the gate voltage (V_g), linear extrapolation techniques, including the *Y*-function method [4], are not applicable for extracting V_{TH} in JL devices. In JL MOSFETs, V_{TH} is usually defined from the position of the lower-V_g peak of the transconductance derivative or second derivative of the drain curent, $dg_m/dV_g \equiv d^2I_D/dV_g^2$, which is assumed to coincide with that of d^2Q_m/dV_g^2 [5]. However, as shown in our previous work [6], the peak position of dg_m/dV_g in inversion-mode MOSFETs is affected by V_g-dependent mobility and series resistance effects. These parasitic effects are particularly important for JL MOSFETs.

Previously, we have proposed the $d(g_m/I_D)/dV_g$ method for extracting V_{TH} in inversion-mode MOSFETs, in which V_{TH} is defined from the V_g value at the minimum of the $d(g_m/I_D)/dV_g$ versus V_g function [7]. This method is based on the same theoretical V_{TH}-criterion as the dg_m/dV_g method; however, it is much less sensitive to the parasitic effects of the V_g-dependent mobility and series resistance [6]. In this work, we analyze an applicability of the $d(g_m/I_D)/dV_g$ method for extracting V_{TH} in JL MOSFETs and its advantages compared to the dg_m/dV_g method.

II. Simulation and Modeling Results

Noting that, for the constant mobility (μ) and a very low drain voltage ($V_D<kT/q$), d^2I_D/dV_g^2 is equivalent to d^2Q_m/dV_g^2, and $d(g_m/I_D)/dV_g$ is equivalent to $[-d^2[\ln(Q_m)]/dV_g^2]$, we performed simulations of d^2Q_m/dV_g^2 and $-d^2[\ln(Q_m)]/dV_g^2$ as a function of V_g for JL MOSFETs with different geometries and device parameters.

Fig.1 shows results of 3-D classical numerical simulations [8] for d^2Q_m/dV_g^2 and $d^2[\ln(Q_m)]/dV_g^2$ versus V_g in n-channel tri-gate 100-nm-long nanowire (NW) JL silicon-on-insulator (SOI) MOSFETs with two different doping levels, $N_D=1\times10^{19}$/cm^3 and $N_D=5\times10^{18}$/cm^3. The simulated devices feature the NW width W_{NW}=15 nm, the NW height H_{NW}=8 nm, the gate oxide thickness t_{ox}=1.3 nm, the buried oxide thickness t_{BOX}=145 nm, and the gate work function Φ_m=4.7 eV. Fig. 2 presents d^2Q_m/dV_g^2 and $d^2[\ln(Q_m)]/dV_g^2$ versus V_g obtained by 1-D classical simulations for symmetrical double-gate (DG) JL SOI MOSFETs with $N_D=5\times10^{18}$/cm^3 and different Si film thicknesses (t_{Si}=10 nm, 15 nm, and 20 nm).

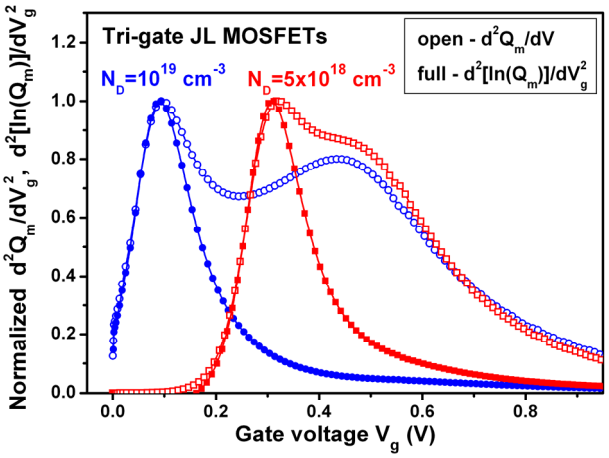

Fig. 1. Normalized d^2Q_m/dV_g^2 and $d^2[\ln(Q_m)]/dV_g^2$ versus V_g in tri-gate 100-nm-long NW JL MOSFETs with two different doping levels, obtained by 3-D classical numerical simulations [8] (W_{NW}=15 nm, H_{NW}=8 nm, t_{ox}=1.3 nm, t_{BOX}=145 nm, Φ_m=4.7 eV).

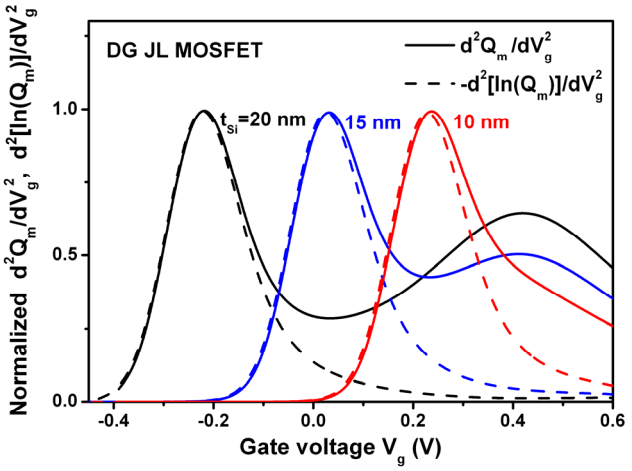

Fig. 2. Normalized d^2Q_m/dV_g^2 and $d^2[\ln(Q_m)]/dV_g^2$ versus V_g in symmetric DG JL MOSFETs with different Si film thicknesses, obtained by 1-D classical numerical simulations (N_D=5×10^{18} /cm^3, t_{ox}=1.3 nm, Φ_m=4.7 eV).

As can be seen from Fig. 1 and Fig. 2, in JL MOSFETs with different geometries and device parameters, the position of the maximum of $-d^2[\ln(Q_m)]/dV_g^2$, being for constant μ and very low V_D identical to $d(g_m/I_D)/dV_g$, coincides with the position of the lower-V_g peak of d^2Q_m/dV_g^2, being identical to d^2I_D/dV_g^2.

In addition, it has been found that the position of the maximum of $[-d^2[\ln(Q_m)]/dV_g^2]$ also coincides with the peak position of $d^2\varphi_s/dV_g^2$ and $d^2\varphi_m/dV_g^2$, where φ_s and φ_m are the potentials at the surface and in the middle of the Si film (Fig. 3). From the foregoing simulation results it can be concluded that the peak position of $[-d(g_m/I_D)/dV_g]$ can be used for the V_{TH} extraction in JL MOSFETs, similar to that of $dg_m/dV_g \equiv d^2I_D/dV_g^2$.

The above conclusion has been confirmed by an analytical modeling. An analytical modeling has been performed for long-channel symmetrical DG JL MOSFETs on the assumption of constant mobility and a very low V_D. It shows that upon the above assumptions, in depletion region in the long-channel JL MOSFETs operating in bulk conduction regime, $d(g_m/I_D)/dV_g$ differs from d^2Q_m/dV_g^2 only by a constant factor. Thus, the position of the extremums of both functions should be the same, which is in a complete agreement with foregoing results of numerical simulations.

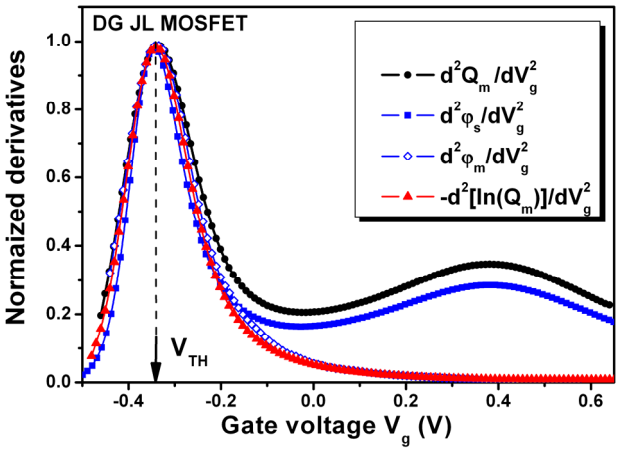

Fig. 3. Normalized d^2Q_m/dV_g^2, $d^2\varphi_s/dV_g^2$, $d^2\varphi_m/dV_g^2$ and $d^2[\ln(Q_m)]/dV_g^2$ versus V_g in symmetrical DG JL MOSFET, obtained by 1-D classical numerical simulations (N_D=5×10^{18} /cm^3, t_{Si}=20 nm, t_{ox}=2 nm, Φ_m=4.7 eV).

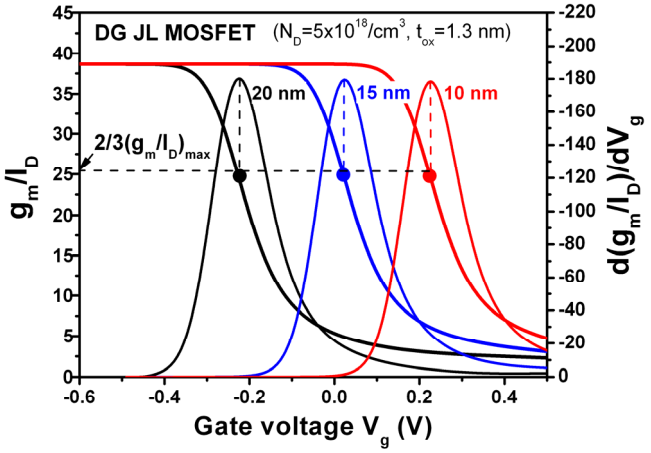

Fig. 4. Results of numerical simulations of g_m/I_D vs. V_g function and its derivative in long-channel symmetrical DG JL MOSFETs with different silicon film thicknesses on the assumption of μ=const and V_D<kT/q (N_D=5×10^{18} /cm^3, t_{ox}=1.3 nm, Φ_m=4.7 eV).

Furthermore, from analytical modeling it has been found that the value of g_m/I_D at the point of min$[d(g_m/I_D)/dV_g]$ or max$[d^2Q_m/dV_g^2]$ is equal to 2/3 of the maximum g_m/I_D value. This is in a good agreement with simulation results in Fig. 4 and is similar to that in inversion-mode MOSFETs [9]. It can be used as an alternative method for the V_{TH} extraction in JL MOSFETs from the g_m/I_D vs. V_g curve with the V_{TH} criterion of max$[d^2Q_m/dV_g^2]$. However, the V_{TH} extraction using $(g_m/I_D)_{max}$ is not always applicable and reliable [9].

Fig. 5 shows numerical simulation results for d^2Q_m/dV_g^2, d^2I_D/dV_g^2 and $[-d(g_m/I_D)/dV_g]$ in DG JL MOSFETs assuming mobility increase with V_g, as is typical for JL devices due to Coulomb scattering at ionized impurities [10], [11]. One can see that in the case of mobility increase with V_g, the position of the d^2I_D/dV_g^2 peaks is shifted with respect to that of d^2Q_m/dV_g^2 towards higher V_g values; the lower mobility value at V_{TH}, the larger this shift.

In JL devices with thin or relatively low doped bodies, featuring two closely located humps of d^2Q_m/dV_g^2, mobility increase with V_g can result in high distortion of d^2I_D/dV_g^2, transforming it in one-hump curve (Fig. 6). At the same time, the peak position of $-d(g_m/I_D)/dV_g$ in Fig. 5 and Fig. 6 remains essentially unaltered and coincides with that of the lower-V_g peak of d^2Q_m/dV_g^2.

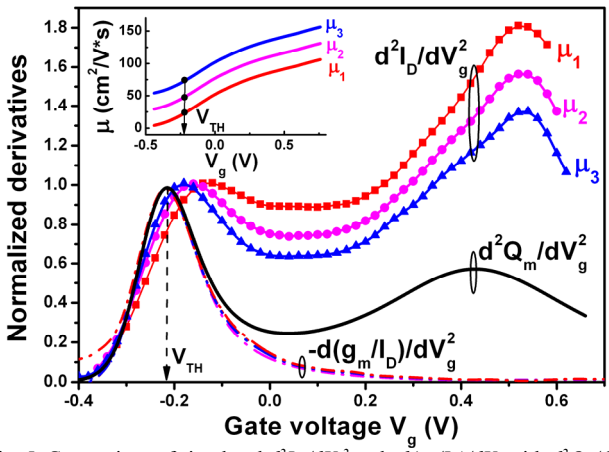

Fig. 5. Comparison of simulated d^2I_D/dV_g^2 and $-d(g_m/I_D)/dV_g$ with d^2Q_m/dV_g^2 in the long-channel DG JL MOSFET assuming mobility variation with V_g shown in the inset (N_D=5×10^{18}/cm^3, t_{ox}=1.3 nm, t_{Si}=20 nm, Φ_m=4.7 eV).

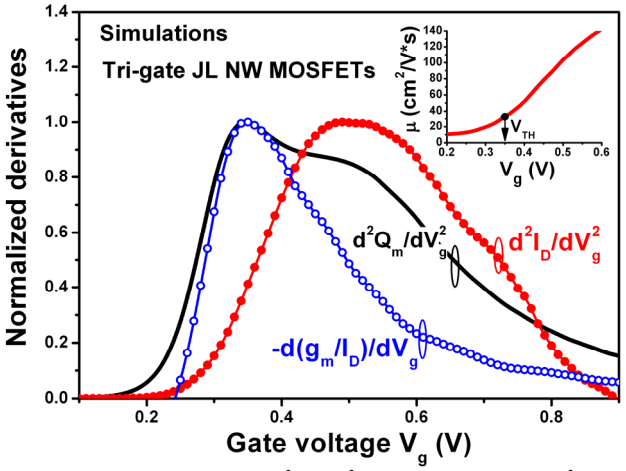

Fig. 6. Comparison of simulated d^2I_D/dV_g^2 and $-d(g_m/I_D)/dV_g$ with d^2Q_m/dV_g^2 in the long-channel triple-gate NW JL MOSFET, assuming μ increasing with V_g, as shown in the inset (N_D=5×10^{18}/cm^3, H_{NW}=8 nm, W_{NW}=20 nm, t_{ox}=1.3 nm, Φ_m=4.7 eV)

From the foregoing simulation results it follows that the $d(g_m/I_D)/dV_g$ method can be used for the evaluation of V_{TH} in JL MOSFETs, and that it is more accurate than the d^2I_D/dV_g^2 method.

III. Experimental Results

To verify the above findings experimentally, we compared the results of V_{TH} extraction in tri-gate nanowire (NW) JL MOSFETs by d^2I_D/dV_g^2 and $d(g_m/I_D)/dV_g$ methods with results of the gate-to-channel capacitance derivative $dC_{gc}/dV_g \equiv d^2Q_m/dV_g^2$ method (which is unaffected by V_g-dependent mobility).

The measured devices are triple-gate NW JL MOSFETs fabricated at CEA-Leti using (100) SOI wafers with a 145-nm-thick buried oxide and a 10-nm-thick silicon film. The phosphorus channel implantation was performed on non-patterned wafers with target doping concentration $N_D \approx 10^{19}$/cm^3. The real effective doping concentration in the channel region evaluated by the method proposed in [12] was found to be $N_D \approx 5\times10^{18}$ cm^{-3}. The gate stack consisted of HfSiON with equivalent oxide thickness EOT=1.3 nm and a TiN gate electrode. Details of the device fabrication process can be found in [13].

The measurements were performed on tri-gate multi-fin NW transistors with the nanowire height $H_{HW}=t_{Si}$=10 nm and nanowire widths W_{NW} varied from 20 nm to 190 nm. Gate-to-channel capacitance measurements were performed at f=300 kHz. Drain current measurements used in this study were performed at V_D=10 mV. All measurements were carried out at room temperature and with grounded substrate.

Fig. 7 presents the comparison between experimental V_{TH} extractions by dC_{gc}/dV_g, d^2I_D/dV_g^2 and $d(g_m/I_D)/dV_g$ methods for 10 µm-long JL NW MOSFETs with three different NW widths. It can be seen that, as expected from the previous analysis, the $d(g_m/I_D)/dV_g$ method yields V_{TH} values very close to those obtained by the dC_{gc}/dV_g method, being unaffected by the V_g-dependent mobility, whereas the d^2I_D/dV_g^2 method yields noticeably higher V_{TH} values than dC_{gc}/dV_g, namely, by ≈100 mV for W_{NW}=20 nm, ≈125 mV for W_{NW}=40 nm, and ≈250 mV for W_{NW}=190 nm.

According to simulation results in Fig. 5 and Fig. 6 and analytical modeling presented in [6], the discrepancy between V_T extractions by the d^2I_D/dV_g^2 and dC_{gc}/dV_g methods is related to the mobility increase with V_g around V_{TH} due to impurity Coulomb scattering. The larger discrepancy between the methods in JL MOSFETs with larger W_{NW} can be explained by the lower mobility at V_{TH} in wider devices. The latter is confirmed by the mobility results obtained by the split-CV technique [10], [11]. Thus, the experimental results confirm that in JL MOSFETs, the $d(g_m/I_D)/dV_g$ method for the V_{TH} extraction is much more accurate than the d^2I_D/dV_g^2 method.

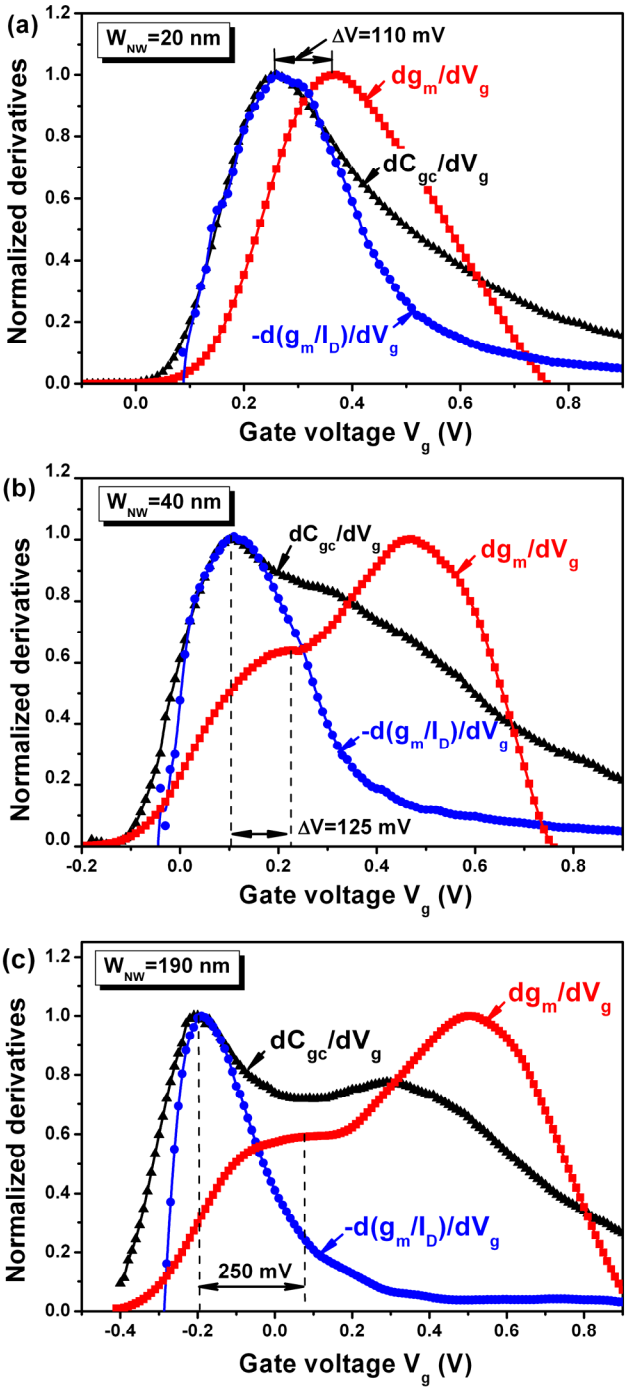

Fig. 7. Comparison between experimental V_{TH} extraction by dC_{gc}/dV_g, d^2I_D/dV_g^2 and $d(g_m/I_D)/dV_g$ methods for 10 µm-long JL NW MOSFETs with different NW widths: (a) W_{NW}=20 nm; (b) W_{NW}=40 nm; (c) W_{NW}=190 nm.

In [14] it has been demonstrated that series resistance effects in JL MOSFETS (which are enhanced with reducing the channel length) shift the peak positions of d^2I_D/dV_g^2 to lower V_g values. Thus, the series resistance has the effect opposite to the mobility variation related to Coulomb scattering. Therefore, one can expect a smaller difference between the methods in short devices.

IV. CONCLUSIONS

Using numerical simulations, analytical modeling, and experimental data, we have demonstrated that the threshold voltage in JL MOSFETs can be extracted from the derivative of the tranconductance-to-current ratio in respect to the gate voltage, $d(g_m/I_D)/dV_g$. We have shown that the $d(g_m/I_D)/dV_g$ method satisfies the same physical criterion as the d^2I_D/dV_g^2 method. However, the $d(g_m/I_D)/dV_g$ method is much more accurate than the d^2I_D/dV_g^2 method due to its lesser sensitivity to the gate-voltage-dependent mobility.

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