Back-gate bias Effect on the MOSFET-C CMOS UTBB Performance by Circuit Simulations

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***Abstract*— This work investigates the on-resistance and harmonic distortion (HD) of Ultra-Thin Body and Buried Oxide (UTBB) fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFETs for a typical process (TT) working in the triode regime, of interest for MOSFET-C filter applications. Circuit simulations of the DC characteristics of n- and p-type MOSFETs in a large temperature range (-25ºC–150ºC) allow to identify the interest of the back-gate bias to compensate the shift of the on-resistance and 3rd - order HD with the temperature.**

Keywords- UTBB-FDSOI; Harmonic Distortion; MOSFET-C filter

I. INTRODUCTION

Ultra-Thin Body and Buried oxide (BOX) Fully Depleted Silicon on Insulator (UTBB FDSOI) CMOS technology is engineered for low-power operation. Thin silicon body improves the electrostatic integrity [1] and allows the channel to be undoped so that significant variability reduction is achieved [2]. Thin BOX device enables implementing back-gate biasing schemes for tuning device characteristics [1]. UTBB technology was also shown to be promising for analog and RF applications [2] such as Internet of Things (IoT) and 5G [3].

In this work, we investigate the potential use of UTBB transistors for the implementation of MOSFET-C filters where high dynamic range and low-power operation are of concern [4]. In such circuit, the resistor of active RC filters is replaced with a MOS transistor operating in triode region [4] using the gate bias to maintain the On Resistance (Ron) constant under temperature and process variations, in order to fix the RC filter specifications. In UTTB, back-gate bias tuning further enables the modulation of the threshold voltage (Vth) [3], and hence variability mitigation and Ron control. The MOSFET nonlinear I–V behavior nevertheless generates harmonic distortion (HD) and deteriorates the whole system performance. This is a major specification in this case [5]. Fully-differential circuits are commonly used to suppress even-order distortions, so that the 2nd-order harmonic distortion (HD_2) becomes a function of mismatches between the transistors and the third-order harmonic distortion (HD_3) dominates [3].

In this paper, circuit simulations of typical-process (TT) UTBB FDSOI n- and p-MOSFETs are used to investigate the impact of sweeping front-gate bias V_{GS} at different constant back-gate biases V_{BG} to fix Ron at different temperatures and minimize HD_3.

II. SIMULATION DETAILS

The studied UTBB FDSOI n- and p-MOSFETs are based on the state-of-art 28 nm FDSOI platform of ST-Microelectronics [6]. Equivalent gate oxide, Si body and BOX thicknesses are 1.3 nm, 7 nm and 25 nm respectively. An industrial Spice compact model [7] was used to simulate DC transfer and output UTBB characteristics. DC simulations are known to be sufficient to predict Ron and HD_3 performance for the low-frequency MOSFET-C circuits of relevance here. Different bias and temperature conditions corresponding to the practical circuits were considered such as: temperature, T from -25 to +150°C, $|V_{GS}|$ above V_{th} (i.e. 0.42 V and -0.51 V for n- and p-MOSFET, respectively) from 0.55 to 1.10V, V_{BG}=-0.30–0.5 V, drain voltages V_{DS}=-0.25 to 0.25 V. Gate lengths (L) for n- and p-MOSFETs were 9.0 and 2.7 µm, respectively and width (W) for both MOSFETs was 900 nm. Under such conditions, a Ron in the range of 50-100 kΩ can be achieved as required in the target application.

III. RESULTS AND DISCUSSION

Fig. 1 shows Ron for the n- (dashed lines) and p-MOSFET (solid lines) at selected operation conditions. Those values are extracted from DC output characteristics as Ron=1/gd, where gd is the output conductance obtained by $gd=\delta I_{DS}/\delta V_{DS}|_{VGS=const}$, around V_{DS}=0 V. As can be expected, Ron is decreased by sweeping V_{GS} and V_{BG} towards stronger inversion and then, by increasing mobility at lower temperature. By tuning V_{GS} (i.e. applying a ΔV_{GS}) for constant V_{BG}, Ron can be kept constant versus the whole T range. This validates the suitability of the devices for the tuning of the target circuits. The required ΔV_{GS} tuning range depends on the choice of nominal bias point ($|V_{GS}|$ and V_{BG}) at room temperature (RT). It increases when driving the transistor in stronger inversion. The circuit designer will determine it for minimal HD and adapt the nominal Ron by optimizing W and L [8]. Note that a Zero-Temperature-Coefficient (ZTC) Ron exists in all cases,

but can hardly be used in practice due to process variations, dynamic range (i.e. low gate bias) and HD_3 considerations.

The HD_3 was extracted in a fast way through the Integral Function Method (IFM) [5], which only needs device DC characteristics. The IFM has been validated in the frequencies range of interest [4,5]. Therefore, drain current (I_{DS}) as a function of V_{DS} was considered at different fixed V_{GS} and V_{BG} required to keep the device in the triode region of the output characteristic. The HD values were then obtained for a given signal amplitude (Va) around a DC bias point (Vo). In order to evaluate the worst case, we use Va=100 mV and Vo=0 V, providing a 200 mVpp signal amplitude, which can be considered as representative for operation of low-voltage UTBB circuits.

Fig. 2 shows the typical ν-like shape of the HD_3 as a function of V_{GS} at different V_{BG} and temperatures for the n- and p-type MOSFETs, respectively. As discussed in [4], considering the RT curves at V_{BG}=0 V in both transistors, the HD_3 at low voltage is dominated by the body-related effect (η), while at high voltage, the mobility effect dominates due to the increase of the carrier scattering (θ). At an intermediate voltage, the body and mobility effects compensate producing a minimum of HD_3 [4]. We observe that, if a negative V_{BG} is applied to the n-MOSFET, HD_3 increases due to the increase of V_{th}, while pushing the channel toward the front-gate interface causes a body effect decrease and mobility decrease. However, if a positive V_{BG} is applied to the n-MOSFET, HD_3 decreases due to the increase of the mobility (positive V_{BG} attracts channel centroid to the bottom Si/BOX interface [1]). Similar behaviour is observed on p-MOSFET for opposite V_{BG} values, except for slightly higher HD_3 values compared with n-MOSFET which could be due to the shorter p-MOSFET length required for the same Ron range due to the lower mobility value. At low temperature (T=-25 ºC), V_{th} and body effect increase; as a result, HD_3 increases and its local minimum shifts to higher voltages. Nevertheless, this shift can be partially compensated if a positive V_{BG} bias is applied to the n-MOSFET or negative for the p-MOSFET, thanks to the mobility increment. At high temperatures (T=150 ºC), both V_{th} and mobility decrease, as a result HD_3 decreases and a shift of its minimum is observed towards lower voltages. However, since HD_3 can be increased by increasing V_{th} and body effect through applying negative V_{BG} bias to the n-MOSFET or positive for the p-MOSFET, a partial compensation can still be obtained.

An important observation is the existence in all cases of a voltage range ΔV_{GS} in which Ron is kept constant and HD_3 kept below -60 dB to satisfy MOSFET-C circuit requirements. The intersections of such HD_3 constraint versus Ron and $|V_{GS}|$ ranges are summarized in Table II for all temperatures and V_{BG}. The Ron top (resp. bottom) edge is obtained for the lowest (resp. largest) $|V_{GS}|$ yielding HD_3 below -60dB by interpolating between

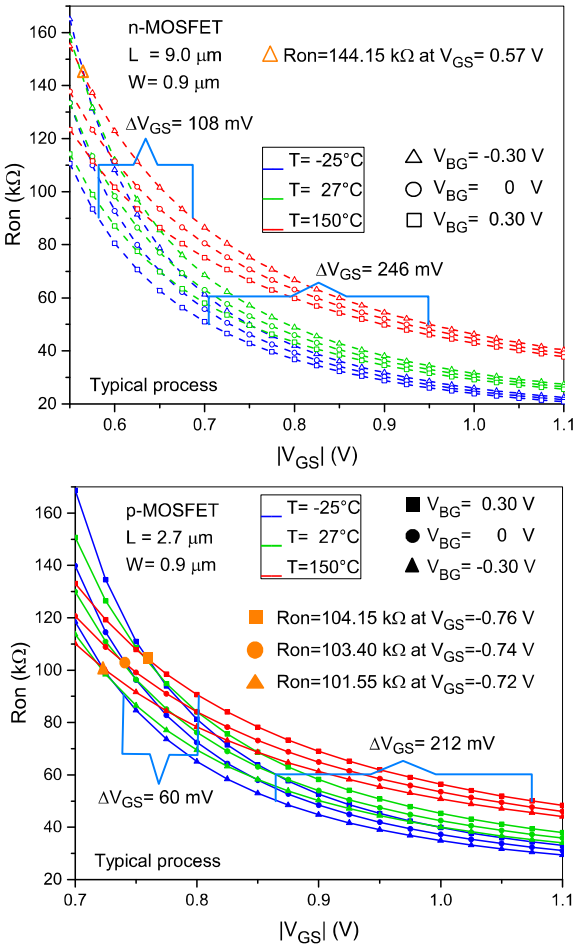

Figure 1. Ron versus V_{GS} at different temperatures and V_{BG} for a n-MOSFET (top) and a p-MOSFET (bottom). ΔV_{GS} range required to keep Ron constant at 90kΩ and 50kΩ when varying V_{BG} and Temperature are also showed.

measured data. The table shows that this constraint can be satisfied in acceptable ranges of V_{GS} and Ron in all cases for both MOSFETs.

More specifically,

- For the n-MOSFET, the harshest constraint is met at low T and negative V_{BG}, with V_{GS} = 0.651V and Ron=78.35 kΩ. Such Ron can be kept constant up to the highest T by applying a ΔV_{GS} of 87 mV. This constraint can be relaxed and HD_3 lowered to -70dB by using a positive V_{BG} for a constant Ron of about 60 kΩ and a ΔV_{GS} of 190 mV.
- For the p-MOSFET, a very narrow ΔV_{GS} tuning range is allowed at low T and positive V_{BG}. However, it lies close to the ZTC point, so that an even smaller ΔV_{GS} of 48 mV is sufficient to keep Ron constant at about 100kΩ. Varying V_{BG} to a negative value relaxes the constraint and favors a HD_3 lower by a few dB at Ron of about 80 kΩ.

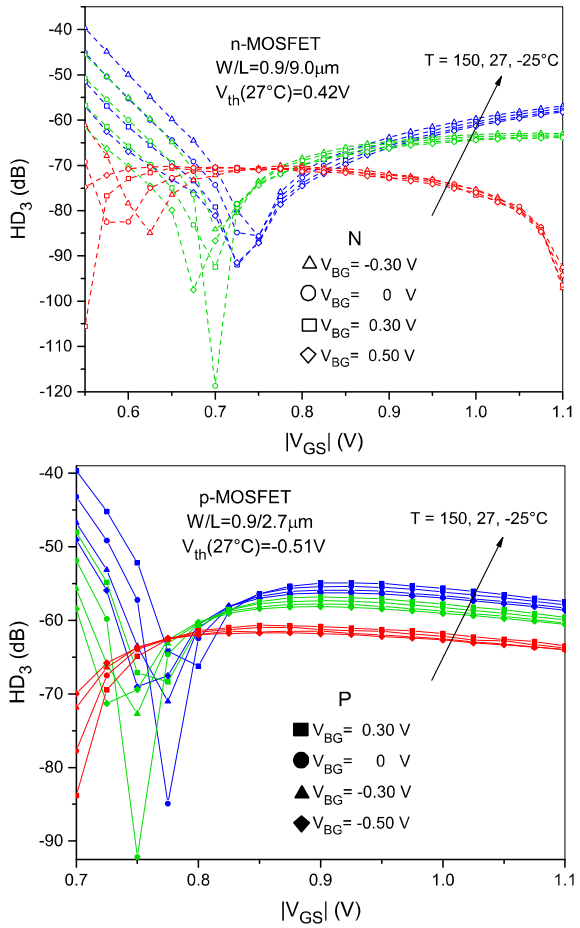

Figure 2. HD_3 versus V_{GS} at different temperatures and V_{BG} for a n-MOSFET (top) and a p-MOSFET (bottom).

In all cases, a final tuning of the nominal Ron can be performed by adapting W and L. Note that the ZTC Ron values are not appropriate since corresponding to too high HD_3 values for T=-25 and 27 ºC.

Finally, it is worth to point out that even though the considered MOSFETs are large and wide, a gate leakage current (I_{GS}) of at least 2 orders of magnitude below I_{DS} were observed for both n- and p-MOSFETs even at the maximum $|V_{GS}|$ of this technology (i.e. 1.1 V), which allows to discard the impact of I_{GS} with regards to HD_3.

IV. Conclusion

The Ron and HD_3 performances of UTBB FDSOI n- and p-MOSFETs were simulated at different temperatures and found suitable for MOSFET-C filter designs. The effect of the back-gate bias was analyzed at different temperatures. Application of positive back-gate bias to n-MOSFET or negative bias to p-MOSFET allows to reduce HD_3 as well as to compensate the reduction of the temperature, whereas reversed back bias has to be applied at high temperatures. For the considered Ron range of 50 to 100 kΩ, the longer n-MOSFET appears more favorable to reduce the HD_3 below -60dB.

TABLE I. Intersection of HD_3 = -60dB and $|V_{GS}|$ and corresponding Ron for that $|V_{GS}|$ vs temperature and V_{BG}

MOS-FET	Temperature (ºC)	V_{GB} (V)	HD_3≤-60dB range			
			Ron top edge (kΩ)	V_{GS} left edge (V)	Ron bottom edge (kΩ)	V_{GS} right edge (V)
N	-25	-0.3	78.35	0.651	26.36	0.990
		0	79.79	0.625	24.41	1.011
		0.3	84.67	0.591	23.01	1.024
	27	-0.3	96.71	0.626	27.41	1.100
		0	97.98	0.600	26.45	1.100
		0.3	103.67	0.567	25.53	1.100
	150	-0.3	154.90	0.550	40.31	1.100
		0	137.70	0.550	39.01	1.100
		0.3	123.40	0.550	37.76	1.100
P	-25	0.3	99.94	0.766	73.09	0.821
		0	95.02	0.752	67.62	0.814
		-0.3	89.59	0.741	62.57	0.809
	27	0.3	118.93	0.753	80.72	0.809
		0	111.09	0.724	74.32	0.806
		-0.3	107.36	0.710	68.00	0.806
	150	0.3	133.20	0.700	48.30	1.100
		0	120.70	0.700	46.10	1.100
		-0.3	110.10	0.700	44.04	1.100

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