Improving MOSFET Piezoresistive Strain Gauges Limit of Detection Using Lock-In Principle

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***Abstract*—In this work, we present a way to improve piezoresistive MOSFET strain gauges using Lock-In principle. This reduces the influence of 1/f-noise, showing a Limit of Detection (LoD) reduction from 474 (42) $\mu\epsilon$ for current measurements to 40.5 (15) $\mu\epsilon$ for Lock-In measurements at 10 μA (100μA) bias. This 1/f-noise reduction also allows for using more efficiently averaging, leading to a 50-fold improvement from 387 (30) $\mu\epsilon$ for current measurements to 7.8 (2.4) $\mu\epsilon$ for Lock-In, with 100 samples averaging.**

***Index Terms*—strain, sensor, piezoresistive effect, lock-in, MOSFET, Limit of detection**

I. Introduction

Silicon strain sensors have a very high sensitivity compared to their metallic counterparts [1]. They are used to measure strain directly, for example in structural health [1] or motors/turbines torque monitoring [2], or as an intermediate means to detect other mechanical stimuli, as in the case of piezoresistive Atomic Force Microscopes [3], or even pressure sensors [4]. MOS transistors piezoresistivity magnitude being comparable to lightly-doped bulk-silicon [5], recent works have proposed to use MOS transistors as strain gauges to reduce power consumption or for high temperature applications [6], [7]. Apart from sensitivity, the challenge for these sensors is to succeed in reducing the intensity of their intrinsic electrical noise, to improve their Limit of Detection. Since thin gauges are mainly affected by thermal noise and low-frequency 1/f noise [8], the use of the Lock-In principle has already been introduced to reduce noise in the case of Wheatstone bridge sensors [9].

In this study, we propose to apply a small modulated signal on the gate of a PMOS transistor that is demodulated at the output (Lock-In principle), to reduce the 1/f noise impact and enhance its limit of detection as strain gauge. This has not been explored yet, to the best of our knowledge. We first quickly detail the analytical expressions necessary for understanding the principle before presenting our experiments and results. Results show an 50-fold improvement in terms of LoD between current and Lock-In measurements, depending on bias conditions and moving average filter applied.

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II. Methodology

A. Sensitivity definition

The sensor under study is based on the piezoresistive effect of silicon, which sees its mobility vary when a stress is applied, as it has already been demonstrated [10], and more particularly on the piezoresistivity of PMOS transistors, which exhibit better piezoresistive performances compared to NMOS and which have already been used in various sensors [6], [7]. This PMOS piezoresistivity is expressed according to the following relationship [5]:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \mu}{\mu} = -(\pi_l \sigma_l + \pi_t \sigma_t) \tag{1}$$

where I_D is the current flowing through the transistor, as seen on fig.1, μ is the holes mobility in the case of a PMOS, σ_l

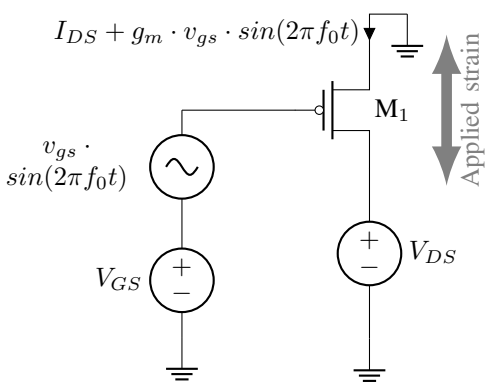

Fig. 1. PMOS transistor used as a strain gauge with modulated small signal gate voltage.

and σ_t are the longitudinal and transverse stresses referring to the transistor channel, and π_l and π_t are the longitudinal and transverse piezoresistive coefficients. The mobility variation can also be expressed with regards to strain(ϵ) by using the gauge factor (GF) [11]. This leads to a sensitivity (S) of the current regarding to the strain that is expressed as:

$$S_{I_D} = \frac{\Delta I_D}{\Delta \epsilon} = I_D \cdot GF \tag{2}$$

The transconductance of a MOS transistor, which expresses the relationship between the variation of I_D and the small signal applied to the gate, v_{gs}, is expressed according to:

$$g_m = \frac{dI_D}{dv_{gs}} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{th}) \tag{3}$$

where C_{ox}, W, L and V_{th} are respectively the capacitance, the width, the length of the gate oxide and the threshold voltage of the transistor. Since this depends directly on the mobility, it is expected that an applied strain will also influence this g_m with an equivalent gauge factor, leading to an equivalent expression for the sensitivity:

$$S_{g_m} = \frac{\Delta g_m}{\Delta \epsilon} = g_m \cdot GF \tag{4}$$

B. Limit of Detection

Limit of Detection, expressed in units of strains, is proportional to the ratio between the noise and the sensitivity [4]:

$$LoD = \frac{3N}{S} \tag{5}$$

where N is the standard deviation that relates to the system noise power, which is mainly composed of thermal noise and $1/f$ noise.

C. Lock-In Principle

The Lock-In principle is used by applying a small signal, at frequency f_0, to the gate of the transistor and by multiplying the measured output current by the same AC signal to demodulate it. The signal, s_{demod}, after demodulation is [9] :

$$\begin{aligned} s_{demod} &= \big(I_D + g_m v_{gs} sin(2\pi 0t)\big) \times sin(2\pi f_0 t) \\ &= \frac{g_m v_{gs}}{2} + I_D sin(2\pi f_0 t) + \frac{g_m v_{gs}}{2} sin(4\pi f_0 t) \end{aligned} \tag{6}$$

And after filtering with an adequate low-pass filter to only keep low frequencies ($f << f_0$) :

$$s_{out} \cong \frac{g_m v_{gs}}{2} \tag{7}$$

This principle allows to get rid of the 1/f noise if f_0 is larger than the noise corner frequency, f_c, between 1/f and thermal components. This allows for drastically reducing the noise power. It is also allowing for only having to manage uncorrelated white thermal noise that can be greatly reduced using moving average filter. As the current and transconductance gauge factors are equivalent, the Lock-In should make it possible to greatly reduce the noise power and therefore increase the performance of the sensors in terms of LoD.

III. Experiment

A. Experimental Set-up

The tested device is a PMOS transistor, made in UMC180 technology, with 8.5 μm gate width and 5 μm gate length. It stands on a bare die, thinned down to $50\mu m$ by grinding of the substrate and glued on an aluminum tensile specimen thanks to M-bond 200 adhesive from Vishay. Mechanical stimuli are applied thanks to a home-made four-points bending setup and electrical measurements are made using a MFLI from Zurich Instruments. The MFLI is a state of the art Lock-In amplifier

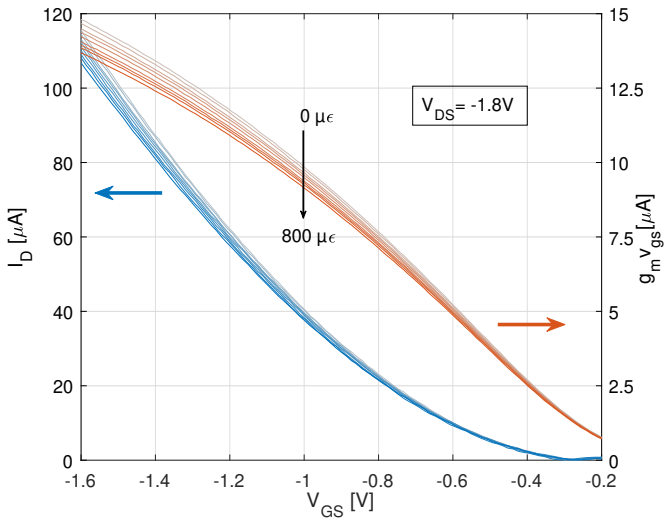

Fig. 2. $I_D - V_{GS}$ (blue) and $g_m v_{gs} - V_{GS}$ (orange) curves under increasing strain conditions, going from 0 $\mu\epsilon$ to 800$\mu\epsilon$.

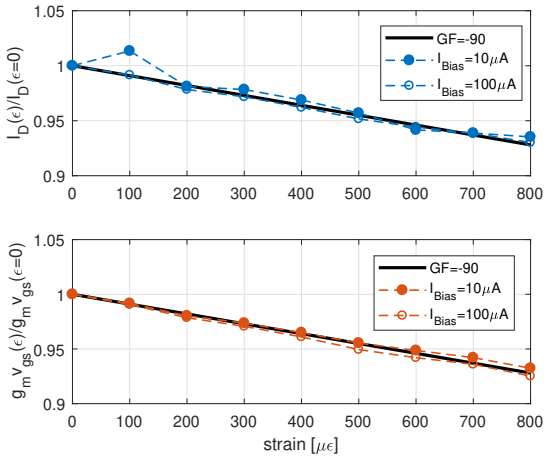

Fig. 3. Relative variations of I_D (blue), current measurement, and $g_m.v_{gs}$ (orange), Lock-In measurement, to applied strain. Black solid lines show the linear regressions for the two curves, leading to a -90 GF

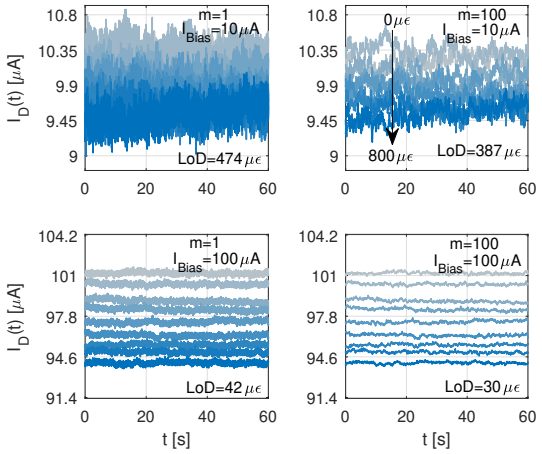

Fig. 4. Current transient measurements: two biases, 10 and 100 μA, and averaging conditions, 1 and 100 points. Sampling rate is $837Hz$.

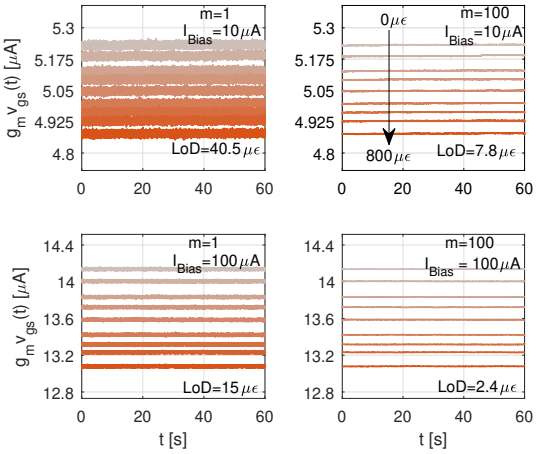

Fig. 5. Lock-In transient measurements: two biases, 10 and 100 μA, and averaging conditions, 1 and 100 points. Sampling rate is $837Hz$.

that contains internal oscillators and allows digital modulation-demodulation and filtering. We use it to control the V_{GS} and V_{DS} bias voltages, to apply the small-signal v_{gs} excitation and to measure, demodulate and filter the output current, in both current and Lock-In measurements.

We carried out measurements at different levels of strain, ranging from 0 to 800 $\mu\epsilon$. At each step of strain, we made I_D-V_{GS} and $g_m v_{gs} - V_{GS}$ curves for V_{GS} ranging from -1.6V to -0.2V, in saturation region of the transistor ($V_{DS} = -1.8V$). For each strain step, we also performed a 60 seconds transient measurements with $10\mu A$ and $100\mu A$ biases, to extract the PSD, the noise power, the LoD, and to observe the influence of a moving average filter.

Regarding $g_m v_{gs} - V_{GS}$ curves, we used a small signal excitation voltage v_{gs} of 100 mV at 100 kHz. For both, current and Lock-In, measurements, the MFLI digital low-pass filter was set to 354.5 Hz thanks to a 4^{th} order low-pass filter, and the sampling rate was set to 837Hz, avoiding aliasing.

B. Results

The different I_D-V_{GS} and $g_m v_{gs} - V_{GS}$ curves are presented in fig. 2. It can be seen that the curves decrease monotonically with strain. The curves behave like conventional transistors in saturation, for which the mobility would vary. By linear regression, for the two levels of current we can observe in fig. 3 that the gauge factor for both curves is -90, confirming that current and transconductance are similarly affected by strain.

Regarding the transient measurements, in fig. 4 and 5, we observe the gain in terms of LoD thanks to the Lock-In principle. We can therefore decrease the LoD from 474 to 40.5 $\mu\epsilon$ for a 10 μA bias, i.e., a ten-fold improvement. Using a 100 points moving average, we further decrease the LoD from 387 to 7.8 $\mu\epsilon$, a fifty-fold improvement, taking advantage of the white nature of the noise on the AC signal. For a 100 μA bias, the gain is also visible, but smaller, allowing for reducing from 14 to 5 $\mu\epsilon$, i.e. a three-fold improvement, and from 10 $\mu\epsilon$ to 0.8 $\mu\epsilon$ with a 100 points moving average, a ten-fold improvement.

The distribution of the spectral power density is represented in fig. 6 , for the $100\mu A$ bias, showing a significant difference: the current measurements is mainly affected by a $1/f$ noise in the considered frequency band, since the PSD of the Lock-In measurements behaves as a white noise, explaining the Lock-In measurements advantage.

IV. Conclusion

By applying the Lock-In principle between the gate signal of a PMOS transistor, used as a piezoresistive strain gauge, and its current, we have shown that it is possible to greatly improve its LoD. Thanks to the Lock-In, we drastically decreased the impact of the $1/f$ noise, reducing the standard deviation of the signal and enabling moving average filter usage. We therefore improved this PMOS strain gauge Limit of Detection of a strain variation by a factor of 50 (resp. 10),at $10\mu A$ (resp. $100\mu A$) bias current.

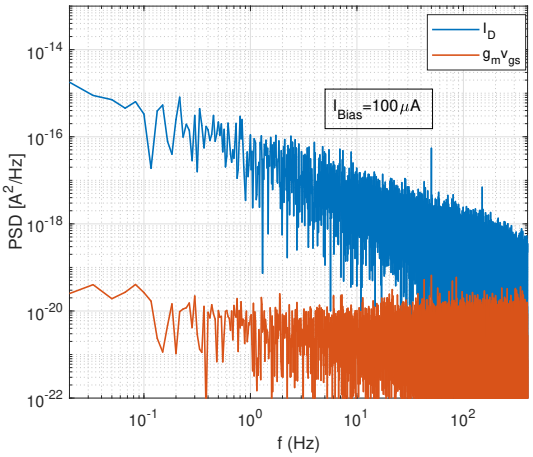

Fig. 6. Noise PSD for current (blue) and Lock-In (orange) signal measurements for a $100\mu A$ bias current, no strain.

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