Comprehensive Analytical Comparison of Ring Oscillators in FDSOI Technology: Current Starving Versus Back-Bias Control

Maxime Schramme, *Graduate Student Member, IEEE*, Léopold Van Brandt, Denis Flandre, *Senior Member, IEEE*, and David Bol, *Senior Member, IEEE*

***Abstract*— Back-bias control is a new degree of freedom brought by fully-depleted silicon-on-insulator (FDSOI) CMOS technologies, which can be used to control the oscillation frequency of voltage-controlled ring oscillators (VCROs). The resulting VCRO architecture is called a back-bias-controlled oscillator (BBCO). This paper compares it with the conventional current-starved ring oscillator (CSRO) topology in terms of power consumption and phase noise figure-of-merit (FoM), while taking practical design constraints of process-voltage-temperature (PVT) robustness and frequency tuning range into account. The proposed comprehensive analysis takes advantage of relevant and compact analytical models, as well as extensive pre-layout simulation results. The comparison is made at four different target oscillation frequencies, which are representative of frequency synthesis for WiFi/Bluetooth/LPWAN wireless communications and of clock generation for smartphone/Internet-of-Things processors: 300 MHz, 868 MHz, 2.45 GHz, and 5.18 GHz. In 28-nm FDSOI technology, the results demonstrate that BBCOs can intrinsically reach 1.69 to 4.63× lower minimum power consumption and slightly better FoM values than CSROs.**

***Index Terms*— Voltage-controlled ring oscillator (VCRO), current starving, back-bias control, fully-depleted silicon-on-silicium (FDSOI), ultralow power (ULP), phase noise.**

I. Introduction

THE advent of the Internet-of-Things (IoT) imposes several requirements on the design of its sensor nodes, among which the necessity to operate at ultralow power (ULP) and ultralow voltage (ULV) [1]. The challenge usually lies in preserving similar performance levels while consuming less power. Thanks to their simplicity, compactness, speed, flexibility, and low power, *ring oscillators* (ROs) are widely adopted [2]–[4], for instance inside phase-locked loops (PLLs) for processor clock generation or wireless-communication frequency synthesis. This is especially true for sub-GHz frequencies, for which inductance-capacitance (LC) counterparts cannot be efficiently integrated due to the large silicon area required to achieve a high inductor value [4], [5].

To control the RO frequency and obtain a *voltage-controlled ring oscillator* (VCRO), several techniques exist. For instance, the frequency can be modified by tuning the supply voltage [6] or the load capacitors [7]. However, the most conventional technique is called *current starving* [3], [4] and is thus investigated in this work. As its name suggests, this technique controls the RO frequency by varying the current flowing in the delay stages constituting the oscillator. In *fully-depleted silicon-on-insulator* (FDSOI) CMOS technologies, *back-gate biasing* is an interesting alternative to control the RO frequency through the tuning of its transistors threshold voltage V_{th}, as done in [8]–[10], for example. Also called *back biasing*, back-gate biasing is the FDSOI counterpart of body biasing in conventional bulk technologies, but is much more effective to tune the transistor threshold voltage and has a larger voltage span [11]–[13].

This paper compares back-bias-controlled oscillators (BBCOs) to conventional current-starved ring oscillators (CSROs), with a focus on the corresponding power consumption and on the trade-off between power and phase noise. The comprehensive analysis proposed here relies on relevant and compact analytical models derived from conventional RO theory, as well as extensive pre-layout simulation results applied to the particular 28-nm FDSOI technology node. Practical design constraints, such as process-voltage-temperature (PVT) robustness and frequency tuning range, are also taken into account. This work is structured as follows. Section II introduces the RO architectures under study and presents the hypotheses made in this paper. Then, Section III explains our analysis methodology applied to simple uncontrolled ROs, which are used as starting examples. Section IV follows with a comparison of current starving and back-bias control, for a target oscillation frequency of 2.45 GHz. An extension to 300 MHz, 868 MHz, and 5.18 GHz target frequencies is also provided, to broaden the discussion. These frequency values are representative of a broad range of applications, ranging from frequency synthesis for WiFi/Bluetooth/LPWAN wireless communications to clock generation intended for smartphone/IoT processors. The mathematical developments needed to support the proposed analysis are gathered in the appendix.

Manuscript received December 7, 2021; accepted January 16, 2022. Date of publication February 1, 2022; date of current version April 28, 2022. This work was supported in part by the National Foundation for Scientific Research of Belgium (FRS-FNRS), in part by the Fonds Européen de Développement Régional (FEDER), and in part by the Wallonia within the Wallonie-2020.EU Program. This article was recommended by Associate Editor A. Worapishet. *(Corresponding authors: Maxime Schramme; David Bol.)*

The authors are with the ICTEAM Institute, Université Catholique de Louvain (UCLouvain), 1348 Louvain-la-Neuve, Belgium (e-mail: maxime.schramme@uclouvain.be; david.bol@uclouvain.be).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2022.3144527.

Digital Object Identifier 10.1109/TCSI.2022.3144527

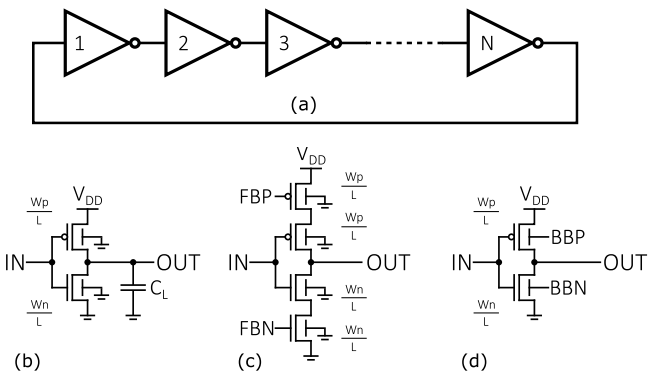


Fig. 1. (a) Schematics of a single-ended N-stage RO and three different kinds of inverting stages in FDSOI technology using LVT flipped-well devices: (b) uncontrolled, (c) current-starved, and (d) back-bias-controlled inverter.

II. Ring Oscillator Architectures

This section presents the three RO architectures studied in this paper and the corresponding hypotheses. The focus is on simple single-ended ring architectures, but the analysis described in this work could be extended to more sophisticated topologies, such as differential and multi-path topologies.

As shown in Fig. 1, a simple single-ended inverter-based N-stage RO is composed of an odd number N of inverting delay elements with a supply voltage V_{DD} [2]. Different types of inverting cells result in different RO architectures. An *uncontrolled RO* is composed of simple inverters [Fig. 1(b)], possibly loaded with additional capacitors. A *current-starved ring oscillator* (CSRO) uses current-starved inverters [Fig. 1(c)] and features two frequency control nodes, FBN and FBP. Finally, a *back-bias-controlled oscillator* (BBCO) is made of back-bias-controlled inverters [Fig. 1(d)] and its two control voltages are the back-gate voltages, BBN and BBP.

Each of these architectures has numerous design parameters available (i.e. number of stages, transistor sizes, voltages). For clarity in the subsequent analysis and for simulation efficiency, several hypotheses are made in this work to decrease the number of free parameters while enabling a fair objective comparison.

As mentioned in the introduction, the RO comparison presented in this paper uses pre-layout SPICE simulation results. They are obtained with steady-state analysis (SST and SSTNOISE) from Eldo simulator piloted by Matlab. In order to have back-bias control capability, the 28-nm FDSOI CMOS technology from STMicroelectronics is selected. Only low-V_{th} (LVT) flipped-well devices are used, to be able to scale down the supply voltage more aggressively. Concerning the sizes, the same gate length L is used for all the transistors of a given VCRO, for layout regularity concern. The width ratio W_p/W_n between PMOS and NMOS devices is set to 2.5 for matched rising/falling edges. The width of all NMOS transistors W_n is fixed to 200 nm. Instead of the transistor width, the device multiplier M (equal to the number of devices placed in parallel) is used to increase the inverter current. This can be implemented at the layout level with multiple fingers.

Also, in practice, VCROs are usually controlled by only one control node instead of two, which assumes a *symmetrical biasing*. For the CSRO topology, FBN is used as primary control and FBP is defined as its symmetrical voltage with respect to V_{DD} [14]:

$$FBP = V_{DD} - FBN. \tag{1}$$

This can simply be generated with a current mirror branch as in [15] for instance. Both FBN and FBP have a voltage range comprised between 0 V and V_{DD}.

For BBCOs, BBN is the main control voltage and BBP has an opposite value (symmetrical to BBN with respect to the ground level):

$$BBP = -BBN. \tag{2}$$

This means BBP is negative, and is usually generated with on-chip charge pumps [8], [10]. The voltage range of BBN (resp. BBP) goes from 0 V to +3 V (resp. from 0 V to −3 V) [13].

With all these assumptions in hand, the number of degrees of freedom for each RO architecture considered in this work reduces to 6: the supply voltage V_{DD}, the number of stages N, the optional added loading capacitor value C_L, the transistors gate length L, the device multiplier M, and the control voltage FBN or BBN.

A. VCROs Oscillation Frequency

The oscillation frequency f_0 of an N-stage VCRO can be obtained as follows [16]:

$$f_0 = \frac{I}{N\ V_{DD}\ C}, \tag{3}$$

where C denotes the total capacitance seen at the output of each inverting stage (sum of the intrinsic parasitic capacitance of the transistors and the added loading capacitor C_L). Equation (3) assumes a perfect current matching between NMOS and PMOS devices as well as a perfect capacitance matching among the N inverting stages. Note that the device multiplier M does not appear in (3) and does not affect the oscillation frequency, because both I and C (in absence of loading capacitors) are proportional to M. This is also discussed in Section III-B.

The oscillation frequency of VCROs is tuned through the variation of the delay element current I, which is a function of FBN for CSROs and of BBN for BBCOs:

$$\text{RO: } I = \beta\ \left(V_{DD} - V_{th,0}\right)^2, \tag{4}$$

$$\text{CSRO: } I(FBN) = \beta\ \left(FBN - V_{th,0}\right)^2, \tag{5}$$

$$\text{BBCO: } I(BBN) = \beta\ \left(V_{DD} - V_{th,0} + \gamma_b BBN\right)^2. \tag{6}$$

In Equations (4)-(6), the term β regroups the devices' dimensions W and L, the mobility and the gate-oxide capacitance per unit of area, γ_b is the body factor parameter which takes values around 70-85 mV/V in 22/28-nm FDSOI technology [11], [13], [17], and $V_{th,0}$ designates the zero-bias threshold voltage. Second-order effects, such as V_{th} roll-of, drain-induced barrier lowering (DIBL), and velocity saturation, are neglected in this work.

For both the CSRO and BBCO topologies, an increase of their oscillation frequency is obtained through the increase

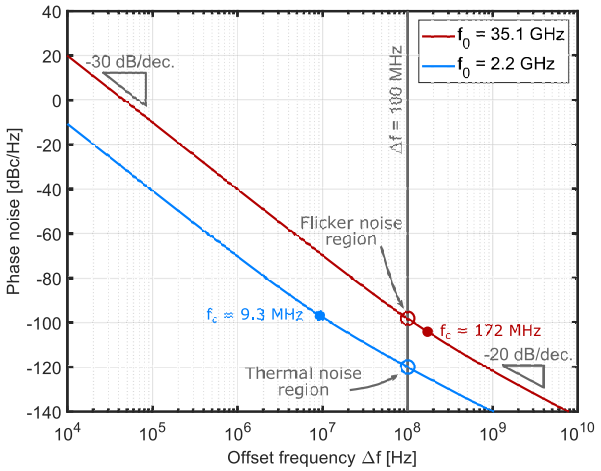


Fig. 2. Simulated phase noise spectra for 3-stage ROs supplied at 1 V, respectively oscillating at 2.2 GHz ($L = 300$ nm) and 35.1 GHz ($L = 30$ nm). The 100-MHz offset frequency line, respectively, intersects these profiles in their thermal and flicker noise regions.

of the stages' current, resulting from the increase of their respective control voltage. The main difference between both architectures thus lies in the way the current increases with the control voltage: CSROs act on the gate-to-source voltage FBN of the header/footer transistors, while BBCOs act on the decrease of the threshold voltage $V_{th} = V_{th,0} - \gamma_b BBN$ of the inverting transistors by the use of forward back biasing through BBN.

B. Phase Noise and Figure-of-Merit

The developments carried out in the next sections focus particularly on the trade-off existing between power and phase noise experienced by all kinds of oscillators [16], [18]–[22]. The following phase noise *figure-of-merit* (FoM) quantifies this trade-off [22]:

$$\text{FoM} = \mathcal{L}(\Delta f) + 20\log_{10}\left(\frac{\Delta f}{f_0}\right) + 10\log_{10}\left(\frac{P}{1\text{mW}}\right). \quad (7)$$

The quantity $\mathcal{L}(\Delta f)$ is the oscillator phase noise value (in dBc/Hz), taken in the thermal noise region, i.e. at a sufficiently high offset frequency Δf from the oscillation frequency f_0. The corresponding power consumption is P (in mW). The lower the FoM value (in dBc/Hz), the better the oscillator phase noise performance.

In this work, the offset frequency Δf is fixed to 100 MHz, to be well above the thermal/flicker-noise corner frequency f_c. Indeed, the FoM formula of (7) is only valid in the $1/f^2$ region of the phase noise spectrum, resulting from the up-conversion of thermal noise. Besides, the flicker noise contribution can be filtered out when corresponding VCROs are used within second-order PLLs with a sufficiently high bandwidth [23], [24]. Fig. 2 represents two examples of RO phase noise profiles, respectively obtained at 2.2 and 35.1 GHz of oscillation frequencies. It shows that the chosen 100-MHz offset frequency line respectively intersects the aforementioned phase noise profiles in their thermal and flicker noise region. For the frequencies targeted in this work, the FoM is computed from the thermal region of corresponding phase noise spectra, thanks to this choice of 100-MHz of offset frequency.

It is interesting to see that the FoM cannot be infinitely improved, some theoretical limits exist depending on the oscillator architecture. For LC oscillators, the best achievable FoM, which mostly depends on the inductor quality factor, can easily achieve values lower than −180 dBc/Hz [22]. For single-ended inverter-based ROs as the ones studied in this paper, the *theoretical best achievable FoM* value is −165 dBc/Hz [22] (also demonstrated in Appendix A). One goal is thus to determine which of the studied VCRO architecture goes closest to this FoM limit.

III. Ring Oscillator Analysis

This section presents an analysis of the uncontrolled RO depicted in Fig. 1(b), in order to get more intuition about the impact of its parameters on power consumption, phase noise and corresponding FoM. The uncontrolled RO is used as a preliminary example to describe the analysis framework used in this work, which is then applied to the CSRO and BBCO topologies in Section IV. With the hypotheses made in Section II and as the uncontrolled RO has no control voltage, only 5 degrees of freedom are left: the supply voltage V_{DD}, the number of stages N, the load capacitor value C_L, the transistor length L, and the device multiplier M. All of them have an influence on the RO frequency, except for M as shown with (3) and discussed in Section III-B. It is thus useful to determine which of these parameters is the best tuning knob to achieve a given target oscillation frequency while minimizing the FoM value. This is explained in Section III-A. The effect that the remaining parameter M has on power consumption, phase noise, and FoM is studied in Section III-B. Finally, the uncontrolled RO is optimized for a target frequency of 2.45 GHz and the different steps of the analysis are summarized in Section III-C.

A. Gate Length Scaling: The Best Way to Slow Down an RO

In the context of this paper, the fastest uncontrolled RO is obtained at maximal supply voltage ($V_{DD} = 1.0$ V), with minimal length value ($L = 30$ nm), with minimal number of stages ($N = 3$), and without any additional loading capacitors ($C_L = 0$ fF). The corresponding oscillation frequency is around 35 GHz and its FoM value is -158.4 dBc/Hz. This point is highlighted in black in Fig. 3. From that point, by decreasing V_{DD} or by increasing L, N or C_L, the oscillation frequency can be lowered to the desired target frequency (300 MHz, 868 MHz, 2.45 GHz, or 5.18 GHz in this work). Fig. 3 shows the evolution of the phase noise FoM value when slowing down the RO with each of these parameters separately. The theoretical FoM limit of −165 dBc/Hz is also added.

As shown in Appendix A, the FoM expression of a single-ended inverter-based N-stage RO supplied by V_{DD} can be written as:

$$\text{FoM} = \underbrace{2000 k_B T \left(1 + \frac{2\gamma V_{DD}}{V_{DD} - V_{th,0}}\right)}_{\text{Thermal}} + \underbrace{250 \frac{\mu \kappa_f V_{DD}}{N L^2} \frac{1}{\Delta f}}_{\text{Flicker}}, \quad (8)$$

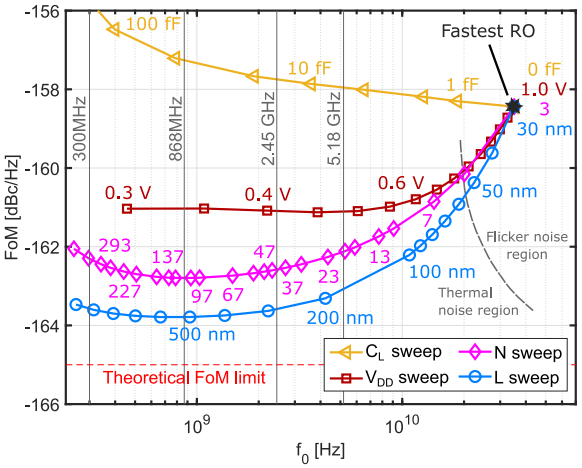


Fig. 3. Evolution of phase noise FoM with oscillation frequency. Each curve represents a different way of slowing down a 3-stage RO with maximal supply voltage, minimal transistor length and without loading capacitors.

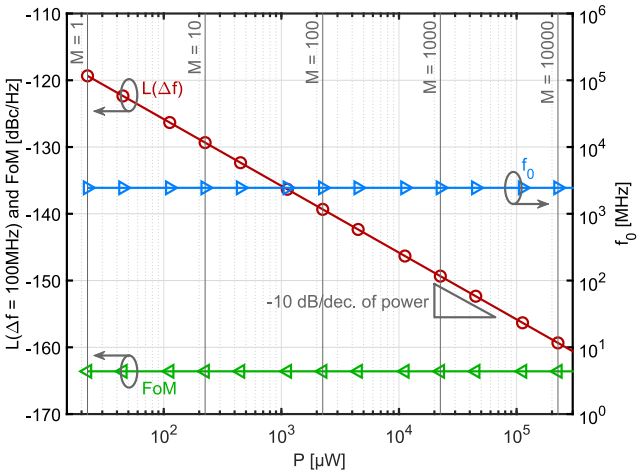


Fig. 4. Effect of the device multiplier M on the oscillation frequency, the power consumption, the phase noise level and the corresponding FoM of a 2.45-GHz RO (3 stages, with gate lengths of 283 nm, and supplied at 1.0 V).

where the FoM is in linear scale (unlike in (7)). The unknown parameters of the formula are properly defined in the appendix. Note that this formula does not take into account second order effects (such as V_{th} roll-off, DIBL, or velocity saturation), assumes an operation in strong inversion, and supposes a purely dynamic power consumption. Nonetheless, it can still be useful to validate some observations made from the results of Fig. 3.

At very high oscillation frequencies in Fig. 3 (right side), the phase noise taken at a 100-MHz offset frequency is dominated by flicker noise and the corresponding FoM value decreases with V_{DD} or when increasing L or N. These trends are confirmed by Eq. (8) (right term). At lower oscillation frequencies in Fig. 3 (left side), around the target frequency values of this work (300 MHz to 5.18 GHz), the phase noise at 100-MHz offset is dominated by thermal noise. The corresponding FoM stays relatively independent from L or N, as can once again be predicted from Eq. (8) (left term). The FoM plateau observed when decreasing V_{DD} cannot be predicted by (8) as the strong inversion hypothesis might not hold for V_{DD} values below 0.4 V.

The impact of the loading capacitor is also not well captured in (8), because a C_L increase slows down the stages' transitions and increases the time during which both the NMOS and the PMOS transistors are on. A short circuit power thus adds to the purely dynamic power consumption assumed to develop (8) and this can only degrade the FoM. Using loading capacitors to slow down an RO thus appears inefficient. This is the reason why loading capacitors are totally avoided in the remaining part of the paper (thus removing one degree of freedom). This also means that any additional parasitic capacitance (i.e. coming from interconnect routing) should impact negatively both the oscillation frequency, the power, and the corresponding FoM. Parasitic capacitances should thus be minimized and their impact should be carefully assessed with post-layout simulations. This falls out of the scope of this work.

From Fig. 3, it is also clear that the most efficient way to slow down an RO is by upsizing the length L, as it gives the most important FoM improvement which goes closer to the theoretical limit. Consequently, in the remaining part of the paper, the length L is used to fine tune the oscillation frequency to the desired target value.

B. Impacts of the Device Multiplier M

In this part, the effect that the device multiplier M has on power, phase noise and corresponding FoM is studied. Intuitively, using M devices in parallel takes more area and increases both the inverter stage current and parasitic capacitances by a factor M. Consequently, the oscillation frequency at the first order does not vary (as mentioned in Section II-A), whereas the power increases with M. Moreover, spending more power for the same oscillation frequency decreases the phase noise by the same factor. Ultimately, the phase noise FoM thus stays constant. These considerations are confirmed in Fig. 4. The parameter M can thus be used to directly *trade phase noise for power and area* at constant frequency and FoM. It can thus be chosen a posteriori and is fixed ($M = 1$) for the remaining part of this work, as we focus on reaching the lowest power or best FoM at the target frequency.

C. Proposed Ring Oscillator Optimization Process

The uncontrolled RO is now left with only three free parameters, namely the supply voltage V_{DD}, the numbers of stages N, and the gate length L. This part optimizes the RO for a target frequency of 2.45 GHz, for different number of stages N and different supply voltage values V_{DD}. For each configuration, the gate length L is adjusted to reach the desired target frequency.

Fig. 5(a) shows the transistor gate length value required for 2.45-GHz operation, as a function of the supply voltage and for different number of stages. Each point of the figure can be seen as a different 2.45-GHz RO design. As can be expected, to compensate for the speed decrease when decreasing the supply voltage or increasing the number of stages, the required length decreases as well. We show in Appendix B that the

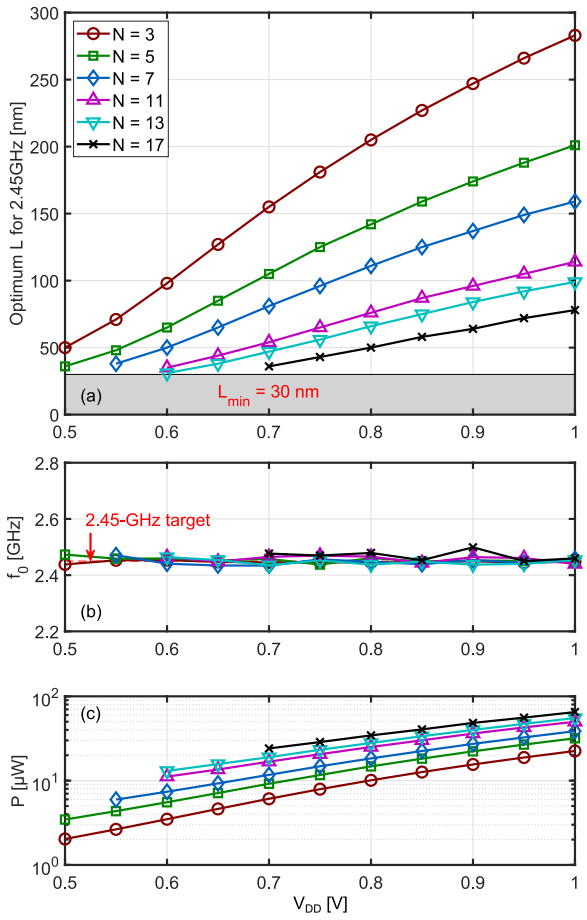


Fig. 5. Effect of the number of stages and the supply voltage on: (a) the required gate length for 2.45-GHz operation, (b) the RO oscillation frequency, and (c) the power consumption. Each point represents a different 2.45-GHz RO design, characterized by a given number of stages N, a given supply voltage V_{DD}, and a given transistor gate length L.

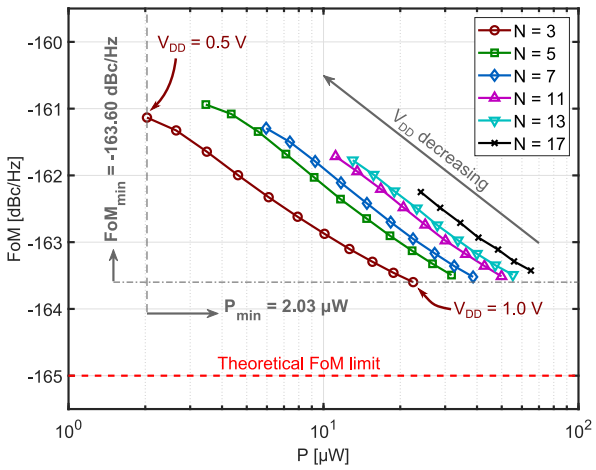


Fig. 6. Effect of the number of stages and the supply voltage on the phase noise FoM of 2.45-GHz uncontrolled ROs. Each point represents a different 2.45-GHz RO design, characterized by a given number of stages N, a given supply voltage V_{DD}, and a given transistor gate length L.

required L is inversely proportional to $\sqrt{N}$ at a fixed supply voltage V_{DD}, and proportional to $(V_{DD} - V_{th,0})/\sqrt{V_{DD}}$ at a fixed N value. The results of Fig. 5(a) are in good agreement with these predictions. As can be observed in Fig. 5(b), the corresponding oscillation frequency is well (yet coarsely) tuned to the target frequency. The corresponding power consumption is given in Fig. 5(c). It increases with both the supply voltage and the number of stages. As shown again in Appendix B, the power is proportional to $\sqrt{N}$ at a fixed supply voltage V_{DD}, and to $V_{DD}^{3/2}(V_{DD} - V_{th,0})$ at a fixed number of stages N.

Computing the FoM value for each of these different 2.45-GHz ROs, and relating it to the power consumption, leads to Fig. 6. Each curve corresponds to a different number of stages N, while each point on a curve corresponds to a different supply voltage value V_{DD}. ROs with 3 stages appear to be the best, as they can achieve lower power values at fixed FoM, or better FoM values at fixed power level. Two *fundamental limits* appearing in Fig. 6 characterize the uncontrolled RO topology for 2.45 GHz operation: the lowest achievable power $P_{\min}$, and the best achievable power/phase noise compromise $\text{FoM}_{\min}$. As reported, power levels as low as 2.03 μW and FoM values as low as -163.6 dBc/Hz can be reached.

It is interesting to see that the analytical FoM expression developed in Appendix A and recalled in (8) can also be used to predict the FoM evolution of Fig. 6, with respect to N and V_{DD}, respectively. For instance, increasing the number of stages N only shifts the curves towards higher power values, without impacting (at first order) the FoM value. Assuming thermal noise only, the formula in (8) confirms this observation as the FoM is in theory independent from N. In addition, if we look for instance at the case $N = 3$ (red curve), moving from 0.5 V to 1 V of V_{DD} improves the FoM by 2.5 dB (from -161.1 to -163.6 dBc/Hz). Using (8) with thermal noise only and assuming $\gamma = 2/3$ and $V_{th,0} = 0.35$ V, the FoM reduction can be estimated as follows and shows a good agreement with the simulation results:

$$\Delta\hat{\text{FoM}} \approx 10\ \log_{10}\left(\frac{1+\dfrac{2\gamma}{1-V_{th,0}}}{1+\dfrac{\gamma}{0.5-V_{th,0}}}\right) = -2.51\ \text{dB}. \quad (9)$$

The general VCRO sizing methodology used in this section is summarized in Fig. 7. For a set of chosen design parameters values (i.e. supply voltage, number of stages), the oscillation frequency is obtained from simulation as a function of gate length values. Then, to reach a specific target frequency, the required length value L is determined by interpolation. This results in a single VCRO design point, properly sized for the target frequency. In order to obtain its performance, a second simulation is performed and extracts the oscillation frequency, the power, and the phase noise value, from which the corresponding FoM can be derived. The next section uses this procedure with CSRO and BBCO topologies in order to compare them fairly in terms of $P_{\min}$ and $\text{FoM}_{\min}$.

IV. Current Starving Versus Back-Bias Control

Compared to an uncontrolled RO, the CSRO and BBCO architectures feature an additional degree of freedom: their control voltage. This tuning knob allows to stay functional on a broader range of operating conditions, thanks to a fine adjustment of the frequency. In this work, we define the *functionality*

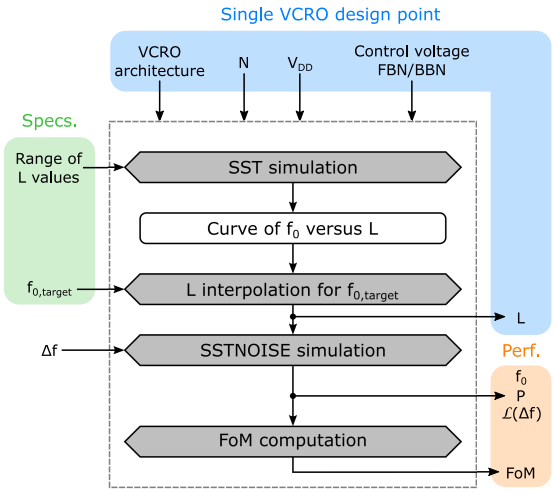


Fig. 7. Sizing methodology used for the design of ROs in nominal conditions (TT 25°C). Simulations of SST (steady-state) and SSTNOISE types are performed with Eldo and piloted with Matlab. In practice, parallelism is used to speed up the simulations.

of an RO as its ability to correctly generate the desired target frequency. This section compares the design of CSROs and BBCOs, taking into account the effect that *process-voltage-temperature* (PVT) variations have on their functionality. Slow NMOS/slow PMOS (SS) and fast NMOS/fast PMOS (FF) are considered instead of typical NMOS/typical PMOS (TT) process, with ±5% supply voltage variation, and temperatures ranging from 0 to +55°C. A brief comparison of the transfer function of CSROs and BBCOs is provided in Section IV-A. The effects of PVT variations on the VCROs functionality are then studied in Section IV-B. A comparison of their corresponding P_{min} and FoM_{min} follows and is carried out at 2.45 GHz in Section IV-C, before extending the methodology to 300 MHz, 868 MHz, and 5.18 GHz in Section IV-D.

A. VCROs Transfer Functions: Gain, Range, and Linearity

The VCROs studied in this work differ by the type of control they use. As described in Section II, CSROs are controlled by the front-gate voltage FBN, while BBCOs are controlled by the back-gate voltage BBN. Their corresponding transfer functions, i.e. the oscillation frequency versus the control voltage, thus possess significant differences. Intuitively, the tuning of the CSRO's frequency involves the gate-to-source transconductance g_m, while for BBCOs it involves the body-to-source transconductance g_{mb}. The link between these two quantities is γ_b, the body factor of (6) whose value is small and lies in the 70-to-85 mV/V range in 22/28-nm FDSOI technology [11], [13], [17]:

$$g_{mb} = \gamma_b \; g_m. \tag{10}$$

We can thus expect a lower *frequency gain* for BBCOs. Figures 8 and 9 respectively depict the transfer function of a CSRO and a BBCO, both oscillating at 2.45 GHz. They confirm the aforementioned expectation. Indeed, CSROs can easily achieve frequency gain values of 8 GHz/V while the BBCOs reach lower gains of around 400 MHz/V. The analytical developments of Appendix C demonstrate that the

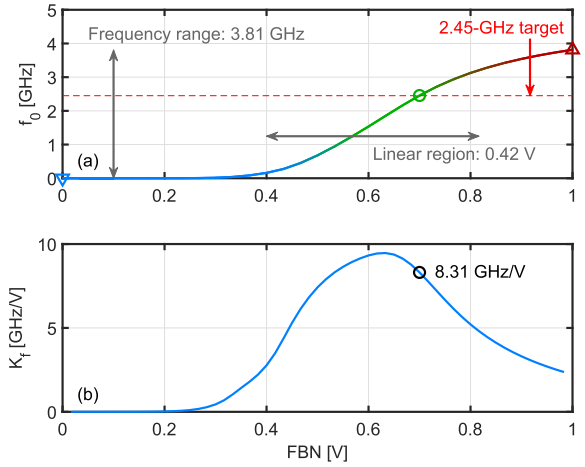


Fig. 8. Characteristics of a 2.45-GHz CSRO with nominal control voltage of $FBN = 0.7\ V$: (a) transfer function and (b) frequency gain.

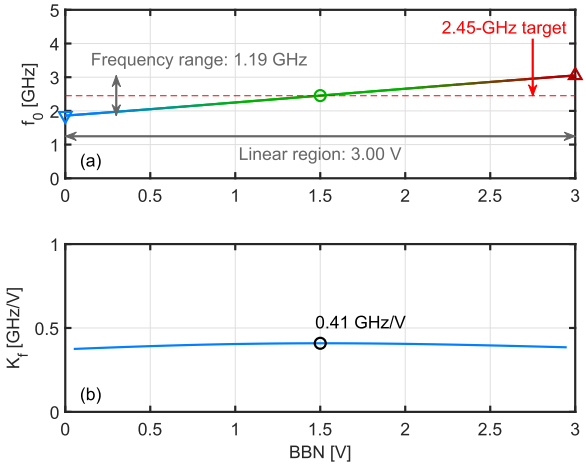


Fig. 9. Characteristics of a 2.45-GHz BBCO with nominal control voltage of $BBN = 1.5\ V$: (a) transfer function and (b) frequency gain.

BBCO gain is indeed at least $1/\gamma_b \approx 13\times$ lower than the CSRO counterpart. As a consequence, BBCOs have also a lower *frequency range* than CSROs, despite the larger voltage range of BBN (limited to +3 V) compared to FBN (limited to V_{DD}).

Another observation that can be made from figures 8 and 9 concerns the *linearity* of the VCRO transfer functions. Compared to BBCOs, the CSROs exhibit a highly non linear transfer function. Appendix C again confirms this observation using a Taylor series expansion of the oscillation frequency formula. It is demonstrated that the first non-linear term is $1/\gamma_b^2 \approx 169\times$ lower for BBCOs with respect to CSROs.

Both the frequency gain and the linearity are important points to consider for designers. For instance, the linearity in the transfer function is important in the domain of RO-based ADCs [17], [25], while a high and stable gain is necessary when implementing PLLs.

B. Impacts of PVT Variations on the VCROs Frequency Range

The choice of the nominal control voltage value is important in the design of VCROs, as it impacts both the oscillator frequency range and its PVT compensation capability.

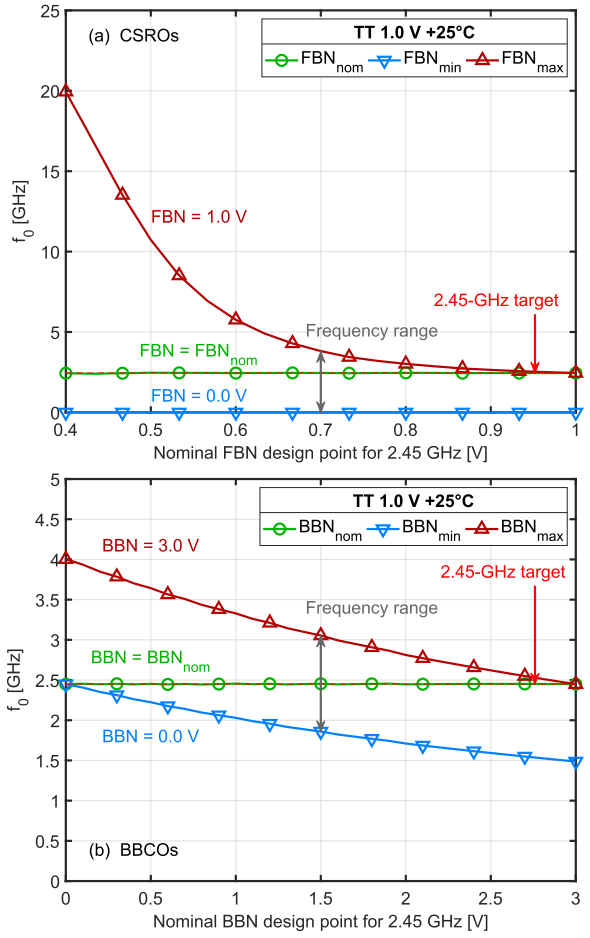


Fig. 10. Frequency range comparison of 3-stage CSROs (a) and BBCOs (b) in typical conditions, as a function of their nominal control voltage. All these VCROs are nominally designed for 2.45 GHz at 1.0 V supply voltage.

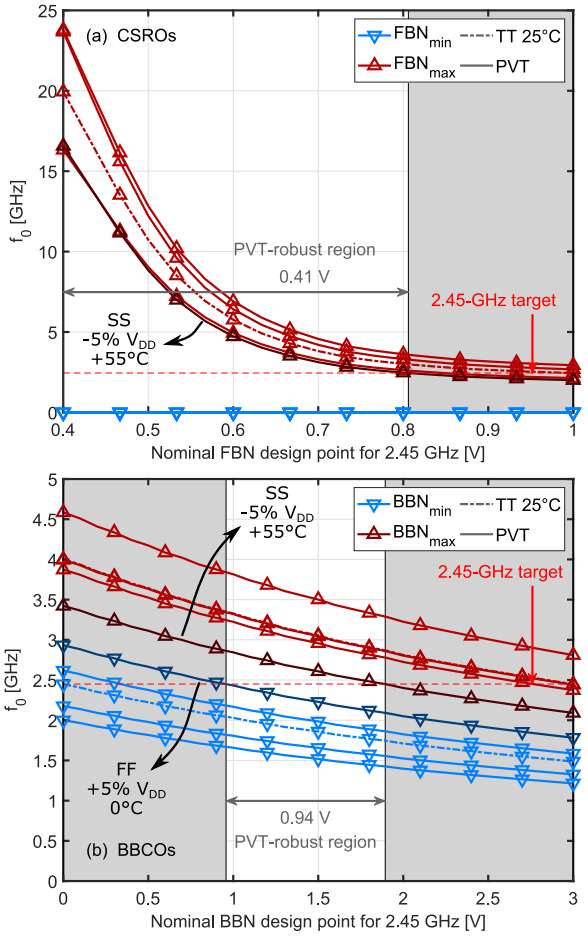


Fig. 11. Frequency range comparison of 3-stage CSROs (a) and BBCOs (b) in PVT corners as a function of the nominal control voltage. All these VCROs are nominally designed for 2.45 GHz at 1.0 V supply voltage. The PVT variations reduce the range of available nominal control voltage values.

Fig. 10 shows the oscillation frequency of CSROs [Fig. 10(a)] and BBCOs [Fig. 10(b)] as a function of their nominal control voltage. All these oscillators feature 3 stages and are sized for 2.45-GHz operation in nominal conditions (TT 25°C) and at 1.0 V supply voltage following the procedure of Fig. 7. Each point on the x-axis thus corresponds to a different oscillator design (with a particular control voltage and a particular gate length value). As can be seen in Fig. 10, each of these oscillators has a 2.45-GHz nominal frequency (green circles) when operated at the nominal control voltage for which they have been designed for. Increasing (resp. decreasing) the control voltage allows to speed up (resp. slow down) the oscillators. The spread between maximal (red triangles, obtained at maximal control voltage) and minimal frequency (blue triangles, corresponding to minimal control voltage) determines the VCROs frequency range. As discussed in Section IV-A, the CSRO topology achieves a higher frequency range thanks to a higher frequency gain with respect to its BBCO counterpart.

With variations of the PVT conditions, the speed of the VCROs is changed. As can be seen in Fig. 11, the nominal frequency limits (dashed lines) of the VCROs are shifted upwards or downwards, depending on the PVT conditions. This impacts the VCROs functionality, as illustrated with the gray shaded areas. Indeed, an oscillator designed with a too high nominal control voltage might not be able to compensate the frequency decrease resulting from slow operating conditions (SS, $-5\%\ V_{DD}$). Similarly, a VCRO which has a too low nominal control voltage might not be able to compensate fast operating conditions (FF, $+5\%\ V_{DD}$). The PVT variations forces the use of control voltage values closer to mid-range and limits the range of possible nominal control voltage values. It is important to notice also that, due to *temperature effect inversion* [26]–[28], the effect of temperature is not the same at high or low supply voltage and depends also on the VCRO topology (due to transistor stacking). That is why we consider four extreme corners (instead of two). For information, in the example shown in Fig. 11 for 1-V supply voltage, the two limiting PVT corners are FF, $+5\%\ V_{DD}$, 0°C (in dark blue) and SS, $-5\%\ V_{DD}$, +55°C (in dark red).

For the remaining part of this work, to verify the functionality of a given VCRO design under extreme PVT variations, the methodology of Fig. 12 is followed. The design to verify is put under fast conditions (FF, $+5\%\ V_{DD}$) using minimum control voltage. The corresponding oscillation frequencies are obtained from simulations at two extreme temperatures (0°C and +55°C), to be compared to the target. The same

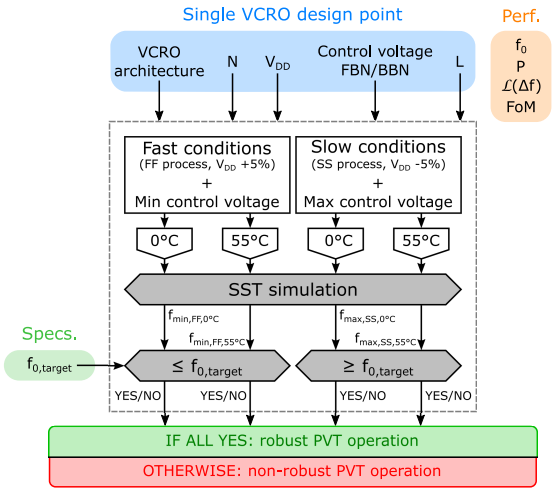


Fig. 12. Methodology used to verify the design of ROs under extreme PVT variations. Simulations of SST (steady-state) type are performed with Eldo and piloted with Matlab. In practice, parallelism is used to speed up the simulations.

TABLE I

RANGE OF DESIGN PARAMETER VALUES USED FOR THE COMPARISON OF FUNDAMENTAL LIMITS OF CSROS AND BBCOS

Parameters	Units	Min	Max	Resolution
V_{DD}	V	0.3	1.0	0.05
N	–	3	17	prime numbers
L	nm	30	500	1
FBN	V	0	V_{DD}	$V_{DD}/30$
BBN	V	0	3	0.1

procedure is applied with slow conditions (SS, -5% V_{DD}) and maximum control voltage. The VCRO is considered to have robust PVT operation if its ability to generate the target frequency is preserved under all four aforementioned PVT conditions.

C. Comparison of CSROs and BBCOs at 2.45 GHz

In this part, using the sizing methodology of Fig. 7, several CSROs and BBCOs are designed for 2.45 GHz, at several supply voltage values and with different number of stages. For each of these design points, the oscillator functionality is verified under PVT variations with the procedure of Fig. 12. Each design parameter is limited to a fixed range of values, and swept with a fixed resolution, as shown in Table I.

Fig. 13 compares the obtained phase noise FoM and power consumption. Performance in nominal (light crosses) and after verification in extreme conditions (bold circles) are shown, for both the CSRO [Fig. 13(a)] and BBCO topologies [Fig. 13(b)]. The two fundamental limits $P_{\min}$ and $\text{FoM}_{\min}$ are highlighted, for both nominal and non-nominal cases. As can be observed, ensuring functionality under extreme PVT conditions tends to degrade these limits. This is linked to the discussion of Section IV-B that showed that PVT variations forces the use of mid-range nominal control values.

Several conclusions can be drawn from this comparison made at 2.45 GHz. In terms of lowest achievable power, $P_{\min}$,

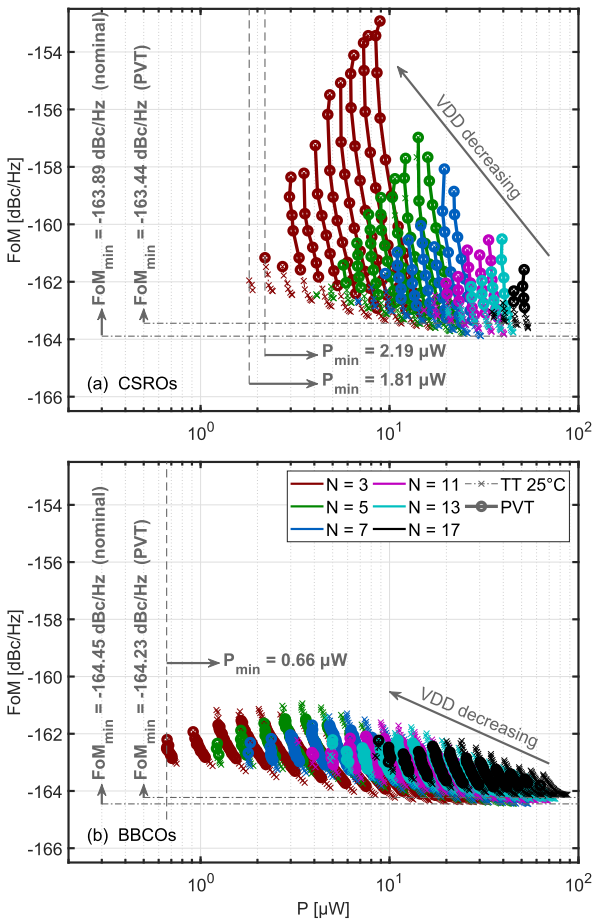


Fig. 13. Comparison of 2.45-GHz CSROs (a) and BBCOs (b) in terms of phase noise FoM and power consumption, in nominal conditions and under PVT variations. All these oscillators differ by the number of stages N (different curve colors), the nominal supply voltage V_{DD} (different curves), and the nominal control voltage FBN/BBN (different points of a curve). Corresponding oscillation frequency is tuned to 2.45 GHz using the transistor gate length L.

BBCOs can go as low as 0.66 μW, while CSROs are limited to 2.19 μW (1.81 μW if considering nominal conditions only). In other words, BBCOs outperform CSROs by a factor 3.31×. This is explained by the fact that BBCO can operate at a lower supply voltage (down to 0.3 V), as they avoid the stacking of transistors and benefit from a threshold voltage reduction through their back-bias control. BBCOs also benefit from the lower number of devices they are made of, which limits the number of noise sources and parasitics. In terms of best achievable power/phase noise trade-off, $\text{FoM}_{\min}$, both architectures are very close (within 1 dB), with values around -164 dBc/Hz. Compared to its CSRO counterpart, the BBCO topology exhibits a lower vertical spread in its FoM levels, which seem thus less sensitive to the choice of nominal control voltage. This can be explained by the lower frequency gain of BBCOs, as previously discussed in Section IV-A and in Appendix C. For both architectures, the fundamental limits $P_{\min}$ and $\text{FoM}_{\min}$ are respectively achieved with the lowest number of stages ($N = 3$) and at the highest supply voltage ($V_{DD} = 1$ V).

An additional way to compare both architectures is illustrated in Fig. 14, where only the optimum VCROs with robust

TABLE II

COMPARISON OF FUNDAMENTAL LIMITS FOR CSROS AND BBCOS AT FOUR DIFFERENT TARGET OSCILLATION FREQUENCIES AND VALIDATED UNDER EXTREME PVT VARIATIONS (FF/SS PROCESS, ±5% VOLTAGE VARIATION, AND 0°C/+55°C TEMPERATURE). CORRESPONDING DESIGN PARAMETERS (N, V_{DD}, FBN/BBN, L) AND PHASE NOISE LEVELS ($\mathcal{L}$ AT AN OFFSET FREQUENCY Δf OF 100 MHZ) ARE ALSO PROVIDED

			P_{min}		FoM_{min}	
f_0	Metrics	Units	CSRO	BBCO	CSRO	BBCO
300 MHz	P	µW	0.14	**0.08**	8.86	14.24
	FoM	dBc/Hz	-160.84	-160.98	-163.15	**-163.84**
	$\mathcal{L}(\Delta f)$	dBc/Hz	-112.60	-110.63	-133.06	-135.83
	N	–	3	3	11	11
	V_{DD}	V	0.40	0.30	0.95	0.90
	FBN	V	0.29	-	0.79	-
	BBN		-	1.00	-	1.90
	L	nm	32	55	261	493
868 MHz	P	µW	0.63	**0.24**	21.65	34.69
	FoM	dBc/Hz	-160.80	-161.86	-163.69	**-164.45**
	$\mathcal{L}(\Delta f)$	dBc/Hz	-110.03	-106.89	-128.26	-131.10
	N	–	3	3	13	11
	V_{DD}	V	0.50	0.30	1.00	1.00
	FBN	V	0.38	-	0.80	-
	BBN		-	1.30	-	1.80
	L	nm	38	45	122	287
2.45 GHz	P	µW	2.19	**0.66**	22.51	28.23
	FoM	dBc/Hz	-161.16	-162.51	-163.44	**-164.23**
	$\mathcal{L}(\Delta f)$	dBc/Hz	-106.73	-103.06	-119.21	-120.94
	N	–	3	3	5	3
	V_{DD}	V	0.55	0.30	1.00	1.00
	FBN	V	0.42	-	0.80	-
	BBN		-	1.80	-	1.80
	L	nm	31	39	116	344
5.18 GHz	P	µW	6.52	**1.41**	35.93	59.15
	FoM	dBc/Hz	-161.18	-162.41	-162.84	**-163.69**
	$\mathcal{L}(\Delta f)$	dBc/Hz	-105.06	-99.66	-114.15	-117.09
	N	–	3	3	5	5
	V_{DD}	V	0.65	0.30	1.00	1.00
	FBN	V	0.50	-	0.77	-
	BBN		-	2.00	-	1.80
	L	nm	31	31	60	147

PVT operation are kept to obtain Pareto-optimal fronts. This figure clearly shows the advantages of the BBCO topology over its CSRO counterpart, as at a fixed power level it achieves better FoM values, and at a fixed FoM level it consumes less power.

D. Extension of the Comparison to Other Target Frequencies

Table II summarizes the results obtained at 2.45 GHz, and extends them to 300-MHz, 868-MHz, and 5.18-GHz target frequencies. The CSRO and BBCO topologies are compared in terms of the values of P_{min} and FoM_{min} they can achieve, and their corresponding design parameters are also provided. Fig. 15 graphically shows the evolution of the fundamental limits with respect to frequency.

The conclusions previously drawn at 2.45 GHz hold both at higher and lower frequencies. BBCOs reach significantly lower P_{min} values. The power reductions range from a factor 1.69× at 300 MHz to a factor 4.63× at 5.18 GHz with respect to CSRO counterparts [Fig. 15(a)]. In addition, BBCOs achieve slightly better FoM_{min} values than CSROs (still within 1 dB) [Fig. 15(b)]. Back biasing is thus an efficient frequency tuning knob and is well suited for ULP/ULV applications.

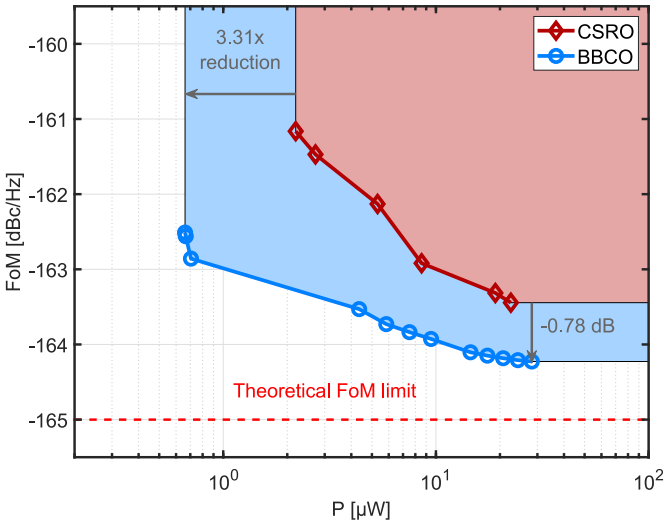


Fig. 14. Comparison of FoM Pareto-optimal fronts as a function of the power consumption for 2.45-GHz CSROs and BBCOs whose functionality is verified under PVT variations.

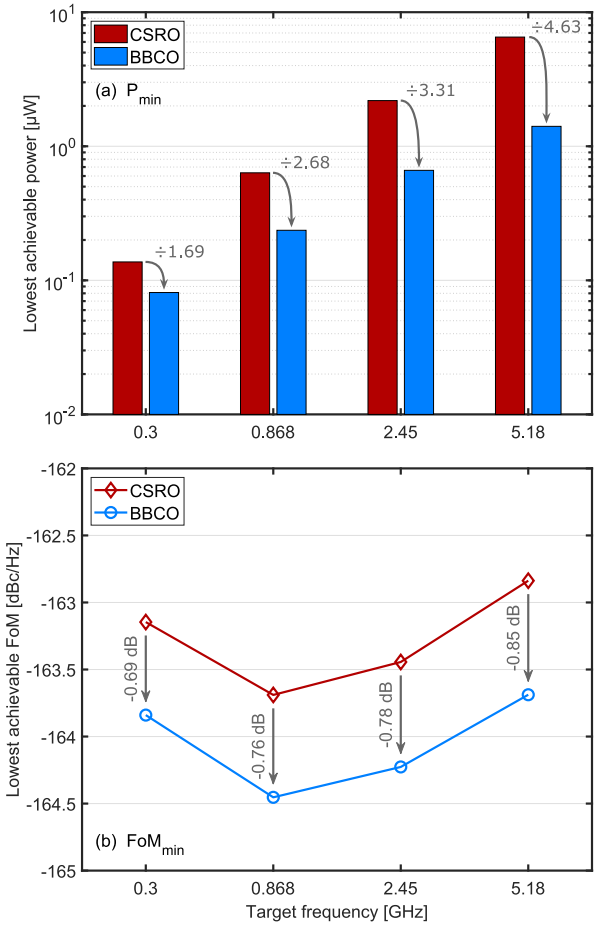


Fig. 15. Comparison of CSROs and BBCOs in terms of (a) P_{min} and (b) FoM_{min} fundamental limits, while ensuring PVT robustness.

V. Conclusion

In this paper, extensive simulation results supported by compact analytical models are used to analyze and compare two types of VCROs: conventional CSROs and FDSOI-enabled BBCOs. At fixed oscillation frequency, oscillators can be characterized by two fundamental limits: the minimum achievable power $P_{\min}$ and the best power/phase noise trade-off $\text{FoM}_{\min}$ they can intrinsically achieve. In this paper, we objectively characterize these fundamental limits for CSROs and BBCOs built in 28-nm FDSOI technology and oscillating at four different target frequencies: 300 MHz, 868 MHz, 2.45 GHz, and 5.18 GHz. The chosen frequency values are representative of frequency synthesis for WiFi/Bluetooth/LPWAN wireless communications and of clock generation for smartphone/IoT processors. The impact of PVT variations on the VCROs functionality is also taken into account.

Compared to the conventional current starving technique, a VCRO frequency tuning based on back biasing offers many advantages: in 28-nm FDSOI technology, BBCOs reach 1.69 to 4.63× lower $P_{\min}$ than their CSRO counterparts and offer slightly better $\text{FoM}_{\min}$ values. These improvements are related to the low degree of transistor stacking, yielding a lower device count and therefore reduced associated noise/parasitics, as well as to the threshold voltage reduction induced by forward back biasing. These features help the BBCO topology to operate at lower supply voltages, and thus lower power. Therefore, back-bias control appears to be an excellent tuning knob for VCROs targeting ULP/ULV applications, such as wake-up radios [29], for instance.

Despite the discussed advantages, the use of back biasing in VCROs also raises some design challenges. For instance, if a symmetrical biasing is used as assumed here, BBCOs need a negative control voltage BBP, whose range can go down to −3 V. It is usually generated on-chip with charge pumps as in [8] and [10], whose power overheads and impacts on the phase noise performance of the BBCOs should be carefully evaluated, in comparison to current mirrors typically needed for CSROs. The lower frequency gain value obtained with BBCOs is also an important design metric to take into account, for instance in PLL design. Let us mention that asymmetrical control strategies could be chosen, for both current-starved and back-bias techniques. They may lead to different benefits and disadvantages at the system level, that must be properly assessed in future works.

Appendix
Mathematical Developments

This appendix gathers the mathematical developments needed to support analytically the simulation-based observations made in this work. Appendix A gives an analytical expression for the FoM of an RO. Appendix B derives formulas for the oscillation frequency as well as for the power consumption of ROs. Appendix C compares the linearity and the frequency gains of CSROs with respect to BBCOs.

A. Phase Noise FoM of an Inverter-Based RO

As the focus of this work is on the phase noise FoM, it is useful to obtain its analytical expression for a single-ended inverter-based RO topology. The FoM definition of (7) can be rewritten in linear scale, as done here:

$$\text{FoM} = \mathcal{L}(\Delta f)\left(\frac{\Delta f}{f_0}\right)^2\left(\frac{P}{1\text{mW}}\right), \tag{11}$$

with $\mathcal{L}(\Delta f)$ the phase noise level being this time expressed in linear scale. Neglecting the static and short circuit power contributions, the RO power is purely *dynamic* and is defined as:

$$P = N\ C\ f_0\ V_{DD}^2 = I\ V_{DD}, \tag{12}$$

where I designates the charge/discharge current of an inverting stage. Only one stage transitions at a time.

In [16], the phase noise spectrum induced by the *thermal noise* of an N-stage inverter-based RO supplied by V_{DD} is expressed as:

$$\mathcal{L}_{wn}(\Delta f) = \frac{2k_BT}{I}\left[\frac{2\gamma}{V_{DD}-V_{th,0}} + \frac{1}{V_{DD}}\right]\left(\frac{f_0}{\Delta f}\right)^2, \tag{13}$$

with k_B the Boltzmann constant, T the temperature in Kelvin, and $V_{th,0}$ the zero-bias threshold voltage of the devices. The γ coefficient is equal to 2/3 for long-channel devices in saturation and takes higher values for short-channel devices [21]. Equation (13) assumes matched currents, threshold voltages, and an equal noise contribution between NMOS and PMOS devices.

The phase noise spectrum induced by *flicker noise* of an N-stage RO is also obtained in [16] and expressed as:

$$\mathcal{L}_{1/f}(\Delta f) = \frac{1}{8NI^2}\ S_i^{1/f}(\Delta f)\ \left(\frac{f_0}{\Delta f}\right)^2, \tag{14}$$

where $S_i^{1/f}(f)$ denotes the flicker noise current power spectral density (PSD). For long-channel devices in saturation, it is obtained from the flicker noise PSD referred to the gate voltage $S_v^{1/f}(f)$ as follows:

$$S_v^{1/f}(f) = \frac{\kappa_f}{C'_{ox}WL}\ \frac{1}{f}, \tag{15}$$

$$S_i^{1/f}(f) = g_m^2\ S_v^{1/f}(f) = 2I\ \frac{\mu\kappa_f}{L^2}\ \frac{1}{f} \propto \frac{1}{L^3}\ \frac{1}{f}. \tag{16}$$

The parameter κ_f is a process-dependent constant [22], C'_{ox} is the gate-oxide capacitance per unit of area, W and L are the devices dimensions, and μ designates the devices mobility. Note that in FDSOI technology, the flicker noise current PSD also has a $1/L^3$ dependence, as verified with simulations and confirmed in [30]. The conclusions drawn at the end of this section thus hold for FDSOI as well.

The phase noise induced by the flicker noise of an RO becomes:

$$\mathcal{L}_{1/f}(\Delta f) = \frac{1}{4NI}\ \frac{\mu\kappa_f}{L^2}\ \left(\frac{f_0^2}{\Delta f^3}\right). \tag{17}$$

Equation (17) assumes matched parameters and equal flicker noise current PSDs between NMOS and PMOS devices.

The total phase noise is naturally obtained by summation of thermal and flicker noise contributions:

$$\mathcal{L}(\Delta f) = \mathcal{L}_{wn}(\Delta f) + \mathcal{L}_{1/f}(\Delta f). \tag{18}$$

Combining Equations (11)-(13), (17), and (18) results in the following final FoM expression in linear scale:

$$\text{FoM} = \underbrace{2000 k_B T \left(1 + \frac{2\gamma V_{DD}}{V_{DD} - V_{th,0}}\right)}_{\text{Thermal}} + \underbrace{250 \frac{\mu \kappa_f V_{DD}}{N L^2} \frac{1}{\Delta f}}_{\text{Flicker}}. \tag{19}$$

Assuming that $V_{DD} - V_{th,0} = V_{DD}/2$ and $\gamma = 2/3$ as done in [22], the theoretical best achievable FoM value for a single-ended RO is thus -165 dBc/Hz at room temperature and in absence of flicker noise.

Different dependences with respect to the RO parameters are observed for Equation (19), depending on the noise contribution considered. At the first order, the thermal noise contribution in (19) is independent of the number of stages N, the gate length L, and the capacitance C seen at the output of each stage, but increases when decreasing the supply voltage V_{DD}. The flicker noise contribution of (19) is at the first order independent of C, and decreases with L, V_{DD}, or when increasing N. These analytical trends are compared to simulation results in Section III-A and Section III-C. A good agreement between analytical and simulation data is generally observed, despite the first order nature of Equation (19).

B. Oscillation Frequency and Power of an Inverter-Based RO

This section obtains analytical expressions for the oscillation frequency and for the power consumption of inverter-based ROs.

Assuming a perfect current matching between NMOS and PMOS devices as well as a perfect capacitance matching among the inverting stages, the oscillation frequency f_0 of an N-stage RO supplied by V_{DD} can be expressed as in [16]:

$$f_0 = \frac{I}{N\ V_{DD}\ C}, \tag{20}$$

where C denotes the total capacitance seen at the output of each inverting stage. In absence of explicit loading capacitor at the output of each inverting stage, it is proportional to W, L, and C'_{ox}:

$$C \propto C'_{ox}\ WL. \tag{21}$$

The stages' current I taken in strong inversion equals:

$$\begin{aligned} I &= \beta \left(V_{DD} - V_{th,0}\right)^2 \\ &= \frac{1}{2}\ \mu C'_{ox} \frac{W}{L}\ \left(V_{DD} - V_{th,0}\right)^2. \end{aligned} \tag{22}$$

Plugging (21)-(22) into (20) yields the following relation:

$$f_0 \propto \frac{\left(V_{DD} - V_{th,0}\right)^2}{N\ V_{DD}\ L^2}. \tag{23}$$

The corresponding power consumption P, already defined in (12), becomes:

$$P = \frac{1}{2}\ \mu C'_{ox} \frac{W}{L} \left(V_{DD} - V_{th,0}\right)^2\ V_{DD}. \tag{24}$$

In Section III-C, several ROs are built with different numbers of stages N and supplied at different supply voltage values V_{DD}. Their gate length L is tuned to make them all oscillate at a fixed frequency of 2.45 GHz. Equations (23)-(24) can explain the evolution of the corresponding power consumption when varying N at fixed V_{DD} or vice versa. As the comparison is made at a fixed oscillation frequency f_0, we have from (23):

$$\text{At fixed } V_{DD}\text{: } L \propto \frac{1}{\sqrt{N}}, \tag{25}$$

$$\text{At fixed } N\text{: } L \propto \frac{(V_{DD} - V_{th,0})}{\sqrt{V_{DD}}}. \tag{26}$$

In these conditions, the power of (24) becomes

$$\text{At fixed } V_{DD}\text{: } P \propto \sqrt{N}, \tag{27}$$

$$\text{At fixed } N\text{: } P \propto V_{DD}^{3/2}\ (V_{DD} - V_{th,0}). \tag{28}$$

These trends are in good agreement with the results of figures 5 and 6 in Section III-C.

C. Frequency Gain and Linearity of VCROs

This section compares the frequency gain values and the linearity of the transfer functions of BBCOs and CSROs.

The RO oscillation frequency definition was given in (23). It is recalled here for convenience and adapted to the case of VCROs:

$$f_0(x) = \frac{I(x)}{N\ V_{DD}\ C}, \tag{29}$$

where x designates the VCRO control voltage used to tune the oscillation frequency through the variation of the stages' current I. In the context of this work, x thus corresponds to FBN for a CSRO and to BBN for a BBCO. Assuming a strong inversion regime, the current I has thus the following form:

$$I(V_{GS}, V_{BS}) = \beta \left(V_{GS} - V_{th,0} + \gamma_b V_{BS}\right)^2, \tag{30}$$

where β regroups the devices' dimensions, the mobility and the gate-oxide capacitance per unit of area, γ_b is the body factor parameter with typical values ranging from 70 to 85 mV/V in 22/28-nm FDSOI technology [11], [13], [17], and V_{GS} and V_{BS} respectively designate the transistors' gate-to-source and body-to-source voltages.

Applying a Taylor series expansion of the second order to (29) around a nominal control voltage x_* yields to:

$$f_0(x) \approx f_0(x_*) + k_1(x - x_*) + k_2(x - x_*)^2. \tag{31}$$

The parameter k_1 is the VCRO frequency gain while k_2 is the first non-linear term. Their values depends on the type of control that is chosen, and thus on the VCRO topology.

After derivation of (29) with respect to x, the resulting frequency gain expressions for a CSRO and a BBCO are respectively given by:

$$k_{1,CSRO} = \frac{2\ \beta}{N V_{DD} C}\ \left(FBN - V_{th,0}\right), \tag{32}$$

$$k_{1,BBCO} = \frac{2\ \gamma_b\ \beta}{N V_{DD} C}\ \left(V_{DD} - V_{th,0}\right). \tag{33}$$

As can be observed, there is at least a factor $1/\gamma_b \approx 13\times$ of frequency gain decrease for BBCOs compared to CSROs. Similar developments were conducted in [17] and lead to the same observation.

A similar comparison can be made with the non-linear term k_2, which is obtained after a double derivation of (29). For CSROs and BBCOs respectively, it can be shown that:

$$k_{2,CSRO} = \frac{\beta}{NV_{DD}C}, \tag{34}$$

$$k_{2,BBCO} = \frac{\gamma_b^2\ \beta}{NV_{DD}C}. \tag{35}$$

The ratio of these two quantities is equal to $1/\gamma_b^2 \approx 169$, which means that, all other things being similar, BBCOs have a more linear transfer function than their CSRO counterparts.

These analytical developments confirm the observations made in Section IV-A from the results of figures 8 and 9. The conclusions also hold if weak inversion is assumed for (30) instead of strong inversion.

ACKNOWLEDGMENT

The authors would like to thank Dr. Cecilia Gimeno for the fruitful discussions and collaborations about the phase noise simulation methodologies.

REFERENCES

[1] D. Bol, G. de Streel, and D. Flandre, "Can we connect trillions of IoT sensors in a sustainable way? A technology/circuit perspective," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2015, pp. 1–3.

[2] B. Razavi, "The ring oscillator [a circuit for all seasons]," *IEEE Solid StateCircuits Mag.*, vol. 11, no. 4, pp. 10–81, 2019.

[3] M. Moghavvemi and A. Attaran, "Recent advances in delay cell VCOs [application notes]," *IEEE Microw. Mag.*, vol. 12, no. 5, pp. 110–118, Aug. 2011.

[4] J. Jalil, M. Bin Ibne Reaz, and M. A. M. Ali, "CMOS differential ring oscillators: Review of the performance of CMOS ROs in communication systems," *IEEE Microw. Mag.*, vol. 14, no. 5, pp. 97–109, Jul. 2013.

[5] V. Issakov, "The state of the art in CMOS VCOs: Mm-Wave VCOs in advances CMOS technology nodes," *IEEE Microw. Mag.*, vol. 20, no. 12, pp. 59–71, Dec. 2019.

[6] A. Elshazly, R. Inti, B. Young, and P. K. Hanumolu, "Clock multiplication techniques using digital multiplying delay-locked loops," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1416–1428, Jun. 2013.

[7] L. Kong and B. Razavi, "A 2.4 GHz 4 mW integer-N inductorless RF synthesizer," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 626–635, Mar. 2016.

[8] G. de Streel *et al.*, "SleepTalker: A ULV 802.15.4a IR-UWB transmitter SoC in 28-nm FDSOI achieving 14 pJ/b at 27 Mb/s with channel selection based on adaptive FBB and digitally programmable pulse shaping," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1163–1177, Apr. 2017.

[9] M. Schramme, C. Gimeno, A. Cathelin, D. Flandre, and D. Bol, "A 2.5-GHz clock recovery circuit based on a back-bias-controlled oscillator in 28-nm FDSOI," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 478–481, 2020.

[10] D. Bol *et al.*, "SleepRunner: A 28-nm FDSOI ULP cortex-M0 MCU with ULL SRAM and UFBR PVT compensation for 2.6–3.6-μW/DMIPS 40–80-MHz active mode and 131-nW/kB fully retentive deep-sleep mode," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2256–2269, Jul. 2021.

[11] R. Carter *et al.*, "22 nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *IEDM Tech. Dig.*, 2016, p. 2.

[12] T. Skotnicki *et al.*, "UTBB FDSOI: Evolution and opportunities," in *Proc. 45th Eur. Solid-State Device Res. Conf.*, 2015, pp. 76–79.

[13] A. Cathelin, "Fully depleted silicon on insulator devices CMOS: The 28-nm node is the perfect technology for analog, RF, mmW, and mixed-signal system-on-chip integration," *IEEE Solid-State Circuits Mag.*, vol. 9, no. 4, pp. 18–26, Fall 2017.

[14] P. Mroszczyk and P. Dudek, "Tunable CMOS delay gate with improved matching properties," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2586–2595, Sep. 2014.

[15] M. Bolt, E. Cantatore, M. Socha, C. Aussems, and J. Solo, "Matching properties of MOS transistors and delay line chains with self-aligned source/drain contacts," in *Proc. Int. Conf. Microelectronic Test Struct.*, Mar. 1996, pp. 21–25.

[16] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[17] J. Ahmadi-Farsani, V. Zuniga-Gonzalez, T. Serrano-Gotarredona, B. Linares-Barranco, and J. M. de la Rosa, "Enhanced linearity in FD-SOI CMOS body-input analog circuits—ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 10, pp. 3297–3308, Oct. 2020.

[18] T. C. Weigandt, B. Kim, and P. R. Gray, "Analysis of timing jitter in CMOS ring oscillators," in *Proc. IEEE Int. Symp. Circuits Syst.-(ISCAS)*, May 1994, pp. 27–30.

[19] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.

[20] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1999.

[21] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.

[22] N. Da Dalt *et al.*, *Understanding Jitter and Phase Noise: A Circuits and Systems Perspective*. Cambridge, U.K.: Cambridge Univ. Press, 2018.

[23] F. Gardner, *Phaselock Techniques*. Hoboken, NJ, USA: Wiley, 2005.

[24] D. C. Lee, "Analysis of jitter in phase-locked loops," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 11, pp. 704–711, Nov. 2002.

[25] R. Dekimpe *et al.*, "SleepRider: A 5.5 μW/MHz cortex-M4 MCU in 28 nm FD-SOI with ULP SRAM, biomedical AFE and fully-integrated power, clock and back-bias management," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

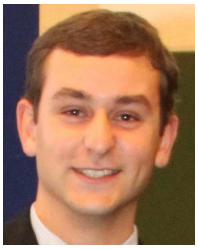
[26] D. Bol, C. Hocquet, D. Flandre, and J.-D. Legat, "The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2010, pp. 522–525.

[27] A. Calimera, R. I. Bahar, E. Macii, and M. Poncino, "Reducing leakage power by accounting for temperature inversion dependence in dual-Vt synthesized circuits," in *Proc. 13th Int. Symp. Low Power Electron. Design-(ISLPED)*, Aug. 2008, pp. 217–220.

[28] Y. Pu *et al.*, "Misleading energy and performance claims in sub/near threshold digital systems," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 625–631.

[29] P.-H. Wang *et al.*, "A dual-mode Wi-Fi/BLE wake-up receivers," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1288–1298, Apr. 2021.

[30] P. Kushwaha *et al.*, "A unified flicker noise model for FDSOI MOSFETs including back-bias effect," in *Proc. IEEE Int. Conf. Electron., Comput. Commun. Technol. (CONECCT)*, Mar. 2018, pp. 1–5.



Maxime Schramme (Graduate Student Member, IEEE) received the M.Sc. degree in electrical engineering from UCLouvain, Louvain-la-Neuve, Belgium, in 2016, where he is currently pursuing the Ph.D. degree in microelectronics. He fully exploits the back-gate biasing capability of FDSOI technology to reduce power, increase circuit speed, ensure good performance, and/or compensate process-voltage-temperature variations. In this context, his current research focuses on the design of ultralow power clock generation and frequency synthesis.

Léopold Van Brandt was born in Belgium, in 1995. He received the B.S. and M.S. degrees in electrical engineering from the Université Catholique de Louvain, Louvain-la-Neuve, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree in nanoelectronics. His current research interests include, but are not limited to, characterization and modeling of the noise in nonlinear devices and circuits; circuit simulation theory; analytical study of analog circuits, digital logic gates, and oscillators; and efficient assessment of the reliability of SRAM cells. The interplay between research and education is one of his major concerns.

Denis Flandre (Senior Member, IEEE) received the M.S. degree in electrical engineering, and the Ph.D. and Research Habilitation degrees from UCLouvain, Louvain-la-Neuve, Belgium, in 1986, 1990, and 1999, respectively. His doctoral research was on the modeling of silicon-on-insulator (SOI) MOS devices for characterization and circuit simulation, and his post-doctoral thesis was on a systematic and automated synthesis methodology for MOS analog circuits. Since 2001, he has been a full-time Professor with UCLouvain. He has organized or lectured many short courses on SOI technology, devices, and circuits in universities, industrial companies, and conferences. He is also the Co-Founder of CISSOID, a spin-off company of UCL focusing on SOI and high-reliability integrated circuit design and products. He is also a Scientific Advisor of three other start-ups, such as INCIZE (semiconductor characterization and modeling for design of digital, analog/RF, and harsh environment applications), e-peas (energy harvesting and processing solutions for longer battery life, increased robustness in all IoT applications), and VOCSens (smart gas sensing solutions from edge to cloud). He is involved in the research and development of SOI MOS devices, digital and analog circuits, and sensors, MEMS and solar cells, for special applications, more specifically ultra low-voltage low-power, microwave, biomedical, radiation-hardened, and high-temperature electronics and microsystems. He has authored or coauthored more than 1000 technical articles or conference contributions. He is the co-inventor of 12 patents. He has participated or coordinated numerous research projects funded by regional and European institutions. He has been a member of several EU networks of excellence on high-temperature electronics, SOI technology, nanoelectronics, and micro-nano-technology. He has received several scientific prizes and best paper awards.

David Bol (Senior Member, IEEE) received the Ph.D. degrees in engineering science from the Université Catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 2004 and 2008.

In 2005, he was a Visiting Ph.D. Student with the CNM National Centre for Microelectronics, Sevilla, Spain, in advanced logic design. In 2009, he was a Post-Doctoral Researcher with intoPIX, Louvain-la-Neuve, in low-power image processing. In 2010, he was a Visiting Post-Doctoral Researcher with the UC Berkeley Laboratory for Manufacturing and Sustainability, Berkeley, CA, USA, in life-cycle assessment of the semiconductor environmental impacts. He is currently an Associate Professor with UCLouvain. In 2015, he participated in the creation of e-peas semiconductors in Louvain-la-Neuve. He also leads the Electronic Circuits and Systems (ECS) Group focused on ultra-low-power design of integrated circuits for the IoT and biomedical applications, including computing, power management, sensing, and wireless communications. He is engaged in a social-ecological transition in the field of ICT research. He co-teaches four M.S. courses on digital, analog, and mixed-signal ICs; sensors; and systems; with two B.S. courses, including the course on sustainable development and transition. He has authored or coauthored more than 120 technical articles and conference contributions, and holds three delivered patents. On the private side, he pioneered the parental leave for male professors in his faculty to spend time connecting to nature with his family.

Prof. Bol (co-)received four best paper/poster/design awards in IEEE conferences (ICCD 2008, SOI Conference 2008, FTFC 2014, and ISCAS 2020). He serves as a Reviewer for various journals and conferences, such as IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS. Since 2008, he has been presenting several invited papers and keynote tutorials in international conferences, including a forum presentation at IEEE ISSCC 2018.