Assessment of RF compact modelling of FD SOI transistors

Martin Vanbrabant
Institute of Information and Communication Technologies, Electronics and Applied Mathematics
Université catholique de Louvain
Louvain-la-Neuve, Belgium
martin.vanbrabant@uclouvain.be

Lucas Nyssens
Institute of Information and Communication Technologies, Electronics and Applied Mathematics
Université catholique de Louvain
Louvain-la-Neuve, Belgium
lucas.nyssens@uclouvain.be

Valeriya Kilchytska
Institute of Information and Communication Technologies, Electronics and Applied Mathematics
Université catholique de Louvain
Louvain-la-Neuve, Belgium
valeriya.kilchytska@uclouvain.be

Jean-Pierre Raskin
Institute of Information and Communication Technologies, Electronics and Applied Mathematics
Université catholique de Louvain
Louvain-la-Neuve, Belgium
jean-pierre.raskin@uclouvain.be

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***Abstract*—In this work, the compact model for FD SOI transistors and its limitations are assessed by comparing Spectre simulations to experimental measurements in a wide range of frequencies. The impact of two phenomena, namely self-heating (SH) and substrate effect (SE), on the frequency response of output conductance and capacitance and their respective modelling are studied. This work shows that the present version of compact model is not sufficient to accurately model the experimentally observed transitions in the output conductance and capacitance frequency response related to these two phenomena.**

Keywords— UTBB, FDSOI, self-heating, thermal impedance, substrate effect, Spectre simulations.

I. Introduction

Ultra-thin body and buried oxide (UTBB) fully depleted (FD) Silicon-on-Insulator (SOI) technology is widely considered as one of the main contenders for the technology downscaling to 20 nm and beyond [1-2]. This technology offers outstanding electrostatic control, very low mismatch, high performance in terms of low-power, high-speed, as well as attractive analog and RF figures of merit (FoMs) [3-5]. However, due to lower thermal conductivity of the buried oxide w.r.t silicon, FD SOI MOSFETs are more subjected to self-heating than their bulk counterparts [6]. While BOX thinning can ease heat evacuation towards Si substrate, it also enhances the electrical coupling through the Si substrate [7-8]. Both dynamic self-heating and substrate effect (that is drain to source coupling through the back-gate node or Si substrate) are known to induce a transition in the Y-parameters over frequency [7-9]. Furthermore, in advanced technologies self-heating characteristic frequency shifts towards higher frequency [10] and as a result both self-heating and substrate effect related transitions appear in a similar frequency range [11]. Therefore, proper separation and modelling of these two phenomena are crucial to get a good physical insight and accurate device simulations.

In [11] we proposed a methodology to separately extract self-heating and substrate effect using measurements at the zero temperature coefficient (ZTC) point. More recently we experimentally studied the back-gate network extraction free from dynamic self-heating by performing the small-signal parameter extraction based on the isothermal Y-parameters, i.e. not affected by dynamic self-heating [12].

In this paper, the output conductance and capacitance frequency responses from Spectre simulations are compared with wideband measurements in order to assess the compact model accuracy. We show that the compact model does not reproduce accurately the measurements because: (i) the impact of self-heating is modelled via a simple first-order thermal network; (ii) the contribution of the substrate effect on the output conductance does not appear in the expected frequency range. Thus, it motivates future developments of new models capturing the complexity observed in the measurements.

II. Results

A. Wideband measurements

An FD SOI super-low threshold voltage (SLVT) nMOSFET from 22FDX® [13] featuring a gate length of 20 nm, finger width of 0.5 µm, 20 fingers and a multiplicity of 6 for a total width of 60 µm, is measured on-wafer from 100 kHz to 10 GHz. The measurement details as well as de-embedding procedures are described in [12].

Fig. 1 shows the $C_{dd}(f)$ (extracted as $Im(Y_{22})/\omega$)) and $g_d(f)$ (extracted as $Re(Y_{22})$) for different front gate biases, V_g when dynamic self-heating is present (solid lines) and when it is removed (dashed lines). More details about the SH removal procedure can be found in [12].

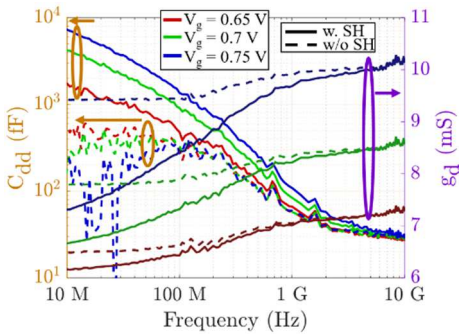

Fig. 1. Output capacitance (C_{dd}) and conductance (g_d) versus frequency for different front-gate biases, V_d = 0.8 V and V_{bg} = 0 V. Solid lines correspond to the original measurements including self-heating; dashed lines represent the measurements from which dynamic SH is removed [12].

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B. Spectre simulations

The simulated device is an FD SOI SLVT nMOSFET with the same dimensions as the measured device. The same DC biases as in experiments are applied to the device terminals. The device is simulated with its reference plane at the same level (M1) as the de-embedded measurements.

Figs. 2 and 3 show, respectively, the simulated output conductance and capacitance for different front-gate biases with (solid lines) and without self-heating model (dashed lines). When the self-heating model is enabled, a transition between 10 MHz and 100 MHz is clearly observed in the output conductance frequency response. However, the transition due to dynamic self-heating in the measurements in Fig. 1 spreads over a larger frequency range until around 1 GHz, which highlights a first discrepancy between the compact model and measurements.

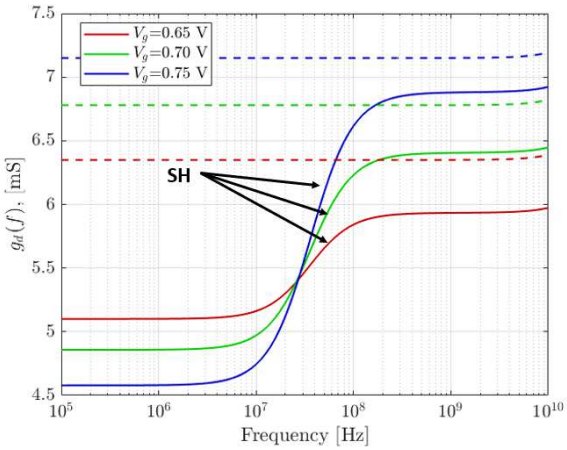

Fig. 2. Simulated output conductance (g_d) versus frequency for different front-gate biases V_g, V_d = 0.8 V and V_{bg} = 0 V. Spectre simulations with self-heating option enabled in solid lines and with self-heating option disabled in dashed lines.

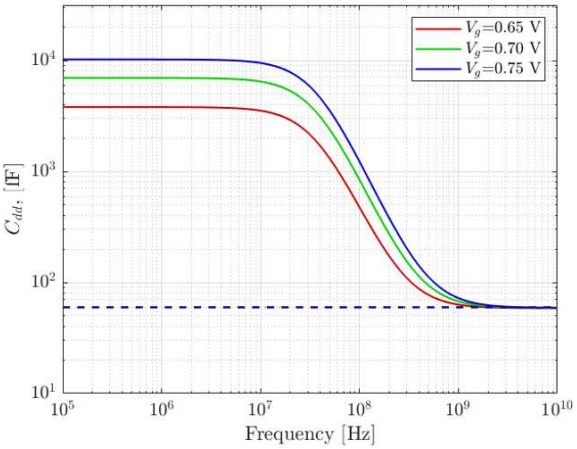

Fig. 3. Simulated output capacitance (C_{dd}) versus frequency for different front-gate biases V_g, V_d = 0.8 V and V_{bg} = 0 V. Spectre simulations with self-heating option enabled in solid lines and with self-heating option disabled in dashed lines.

Following the method detailed in [11], the thermal impedance is extracted. As shown in Fig. 4, a simple first-order thermal network is sufficient to model the simulated thermal impedance implemented in the compact model and accurately capture the SH transition present in the simulated output conductance frequency response. However, it is known from experimental data [11] that higher-order (at least third-order or fourth-order) thermal networks are necessary to fit the thermal impedance and model the transition in the output conductance as shown in Fig. 5 [11]. Therefore, although the compact model captures the global thermal effect using a simplistic approach associated with a first-order thermal model, it lacks precision and physical insight on the different heat evacuation paths that co-exist in real devices (via BOX, via gate, via source/drain and vias, …) and their associated thermal time constants. This could limit the model flexibility to correctly predict the effect of bias, temperature and geometry on the self-heating related frequency response of the output conductance and capacitance.

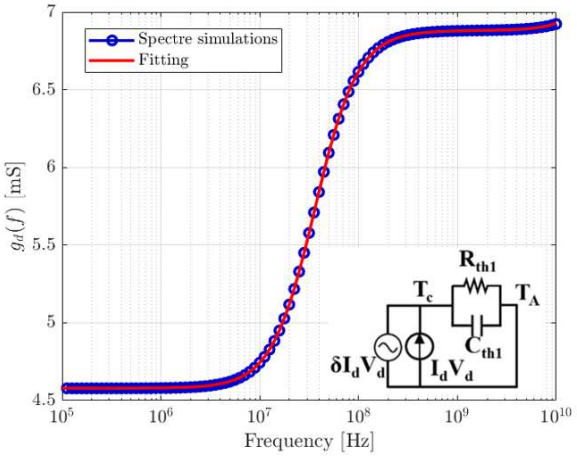

Fig. 4. Output conductance (g_d) versus frequency for V_g = 0.75 V, V_d = 0.8 V and V_{bg} = 0 V. Spectre simulations in blue circles and fitted model with first-order thermal network in red line.

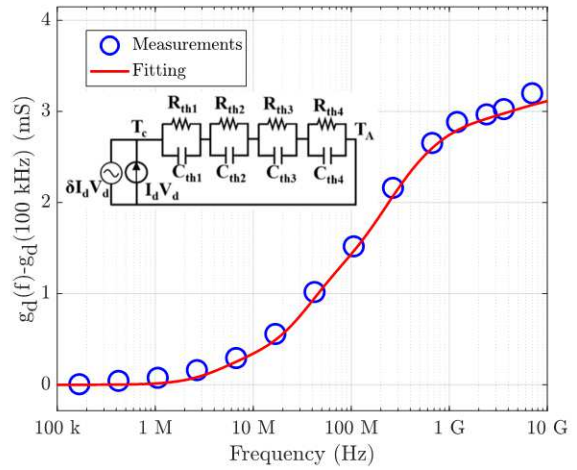

Fig. 5. Output conductance (g_d) versus frequency for V_g = 0.75 V, V_d = 0.8 V and V_{bg} = 0 V. Measurements in blue circles and fitted model with fourth-order thermal network in red line [11].

Furthermore, Fig. 2 also shows that contrarily to measurements, the simulated output conductance with and without SH model does not match at higher frequencies (i.e. above 1 GHz), although the dynamic self-heating free conditions should be reached. This difference is slightly larger at lower Vg. The origin of this difference is most probably related to the static self-heating component modelled via temperature rise which is a function of the power dissipated by the device at fixed bias conditions T = f(P)= f(Id,Vd). Then, one of the hypotheses could be that temperature in simulations is overestimated with respect to real SH measurements.

Moreover, from Fig. 2 one can see that the transition related to the substrate effect (i.e. due to the source/drain coupling through the substrate) does not appear in the 100 kHz – 10 GHz range of the simulated output conductance. Contrarily to the observation from the measurements in Fig. 1, the Spectre simulated output conductance is "flat" over the whole simulated frequency range when self-heating option is disabled (dashed lines in Fig. 2). Introducing an RC network connected to the back-gate contact can however be used to emulate this transition related to the substrate effect as shown in Fig. 6.

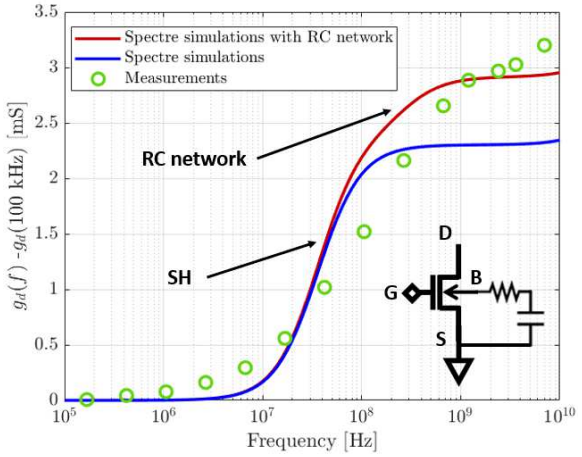

Fig. 6. Output conductance (g_d) versus frequency for V_g = 0.75 V, V_d = 0.8 V and V_{bg} = 0 V. Spectre simulations with (red) and without (blue) RC network connected to the back-gate contact. Measurements in green circles.

III. Conclusion

In this work, we studied the impact of self-heating and substrate effect on the output conductance and capacitance frequency responses through Spectre simulations. A detailed comparison with experimental results highlighted that both phenomena are not well captured by the current version of the compact model. First, self-heating is modelled with a first-order thermal network characterized by a narrow frequency range which is not sufficient to represent the more complex SH distributed transition observed in the measurements. Then, the transition related to the substrate effect does not appear in the 100 kHz – 10 GHz contrarily to what is observed in the measurements. Physical understanding of these different phenomena and the development of accurate models with sufficient complexity are therefore essential for device simulations and circuits performance prediction in a wide range of temperatures and frequencies for various bias conditions.

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