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Temperature-dependent performance of Schottky-Barrier FET ultra-low-power diode

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ABSTRACT

In this paper, for the first time, we apply the ultra-low-power (ULP) diode concept with Schottky Barrier (SB) transistors and analyze their performance in comparison to standard CMOS, using calibrated TCAD mixed-mode simulations. The negative impedance characteristics obtained in reverse mode with SB devices are shown to offer more stable current characteristics compared to CMOS, especially as a function of temperature. The origin of this behavior manifests itself in the fact that carriers tunneling through the barrier by field emission and carriers overcoming the barrier by thermionic emission both contribute to the total device current. This enables superior current performance over temperature. This enables ultra-low-power memory application over a larger temperature range, or with a denser cell area.

1. Introduction

The demand for ultra-low-power (ULP) circuit drives worldwide interest, notably for Internet of Things (IoT) applications. In one such direction, CMOS technology downscaling has led to a reduction of V_{DD} (supply voltage) minimizing the operating power dissipation. The V_T (threshold voltage) of the MOSFETs is reduced as well to maintain adequate overdrive ($V_{DD} - V_T$) for high speed. The aggressive downscaling results in an exponential increase of subthreshold leakage. The reduction of the static power dissipation has become a major concern for the IC industry. In this context, the ULP design concept proposed by Levacq et al. [1] offers CMOS composite diodes with ultra-low-leakage behavior, i.e. a p-type MOSFET is connected in series with the n-type one such that when the composite structure is switched off, the n-MOSFET (resp. p) gate-to-source voltage becomes negative (resp. positive), thereby reducing the off-leakage current and hence static power consumption (Fig. 1).

The concept has been successfully applied towards implementation in rectifiers for energy harvesting [2], charge-pumps for power voltage management, latches in dynamic logic circuits [3] or high-speed adders [4] and low-V_{DD} SRAMs, in CMOS nodes from 1 µm to 28 nm, with record energy efficiency [5,6]. The modeling, process dependence and temperature behavior or the structure have been discussed in details towards design optimization.

In this paper, we analyze the usage of Schottky Barrier (SB) transistors for ULP diode and latch implementations, using simulations with the state-of-the-art Synopsys TCAD framework [7]. We show that ULP diodes can exploit the SB device well-known benefits at low voltage when compared to CMOS, while the higher off current of SB transistors linked to their ambipolar characteristic can be suppressed by the ULP concept.

2. Simulation setup

The paper is organized as follows: Section 2 gives detailed information of the simulation setup. In Section 3 the simulation results of CMOS vs. SB-FET ULP diodes and latches are compared and discussed as a function of voltage and temperature ranges. Furthermore, analysis of the performance boost origin is presented. Section 4 concludes the paper.

The TCAD simulations (Synopsys toolchain) have been calibrated on experimental CMOS and SB devices with the settings of [8–10,12,13] obtained from the simulated structures by process simulations and parameters shown in Table 1. As a result, we have developed individual FET models with well calibrated DC I-V curves [12] which enable trustful mixed-mode circuit simulations.

Within the TCAD simulation environment the following models were activated: Fermi distribution of carriers, incomplete dopant ionization

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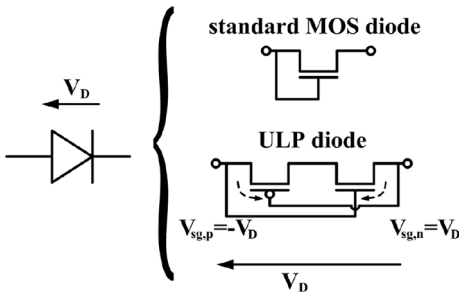


Fig. 1. Standard n-MOS diode and ULP CMOS diode architectures with forward I-V definitions adapted from [1].

Table 1
Geometry and material parameters in the TCAD simulation [7] for 300 K. Parameters from references [7,15–17].

	SB-FET	MOS		
L_{ch}	200	200	[nm]	effect. channel length
T_{ch}	≈ 20	≈ 20	[nm]	channel thickness
W_{ch}	1 (n-SB-FET), 10 (p-SB-FET)	1 (n-MOS), 2 (p-MOS)	[μm]	channel width
T_{ox}	1.8	2.5	[nm]	oxide thickness
N_B	10^{15}	10^{18}	[1/cm^3]	substrate doping
$N_{S,D}$	-	10^{20} (peak)	[1/cm^3]	Source/drain doping
N_{RG}	10^{18} (peak)	-	[1/cm^3]	Retrograde doping
ϵ_{ch}	11.7	11.7	[–]	channel permittivity
ϵ_{ox}	7	7	[–]	oxide permittivity
$\phi_{Bn,p}$	0.27 (ErSi, p-SB-FET), 0.22 (PtSi, n-SB-FET)	-	[eV]	SBH electrons
A_n^{**}	112	-	[A/cm$^2K^2$]	elec. Richardson constant
A_p^{**}	32	-	[A/cm$^2K^2$]	hole Richardson constant
m_n^*	0.19	-	[–]	electron effective tunneling mass
m_p^*	0.49	-	[–]	hole effective tunneling mass

and its effect on mobility, doping density effect on mobility, high electric field effect on mobility, mobility degradation at interfaces, bandgap narrowing effect on carrier intrinsic density in terms of old Slotboom model, lattice temperature, nonlocal tunneling at metal–semiconductor interfaces. Schottky Barrier Lowering effects (SBL) are not considered within this simulation because of convergence issues. It should be noted, that even without SBL, tunneling through the barrier is included. However, it is to be expected from previous TCAD simulations that the currents with SBL would be slightly higher, for both on- and off-currents [13].

However, the reason to skip SBL effects in this work is twofold. Firstly, single device simulations have shown that in the range of biases used for the ULP diodes, the impact of SBL was very low. Secondly, one cannot extract the correct current components of each device within mixed-mode simulations, which need to be performed for the ULP circuitry as proposed by [1]. Detailed information for the single device extraction of the SBL current can be found in [14]. Here, we want to show that in principle the performance of SB-FET ULP diode can be beneficial.

Figs. 2(a) and 2(b) present the simulated structures for the classical n-MOS/p-MOS and n-SB-FET/p-SB-FET, respectively. The simulation settings of previous calibrated devices were applied to the device simulations with the physical models for individual device I-V curves and next mixed-mode simulations for ULP circuits.

3. Results

3.1. I-V characteristics

Fig. 3 shows the drain current (I_d) vs. gate voltage (V_g) characteristics, for different drain-to-source voltage (V_{ds}), of the n-MOS & p-MOS and n-SB-FET & p-SB-FET simulations, respectively, at the room temperature (RT) of 300 K, focusing on subthreshold operation of highest relevance for the ULP diodes. It should be pointed out, that comparisons of simulation with experimental FD SOI CMOS [8–10] over temperature show a fairly good agreement. Furthermore, comparisons of simulation with experimental SB-FET devices [12] for low temperature show a very good agreement. One may ask if SB-FETs can promise a good memory application as compared to conventional CMOS? One can clearly observe that I_{on} and I_{off} of n-MOS and p-MOS are far better than for n-SB-FET and p-SB-FET. This is why the ULP structure of Flandre et al. [1] is investigated to reduce the leakage by operating the devices at a negative V_{gs} voltage.

3.2. ULP temperature behavior

There are visible differences between a typical behavior of classical MOSFETs and SB-FETs for different bias conditions. In the OFF-regime, the higher the V_{ds}, the higher the leakage current in both device types and the lower the V_{gs} voltage corresponding to the onset of the ambipolar current in the SB-FETs. In the ON-regime/state, the p-SB-FET has low drive current but as discussed later, for ULP diode applications as e.g. memory cells this regime is not of importance.

However, the target here is a similar on-current for n- and p-type device at low supply voltage $V_{DD} \approx 0.4$ V. In case of the SB technology this led to a scaling up of the channel width W for the p-SB-FET, causing increased I_{off}. Furthermore, because of this symmetry of currents for both simulations the intersection between n-channel and p-channel characteristics is V_g approx. 0 V. In the subthreshold range the SB-FET shows a slightly steeper transition between the OFF and ON regions than the standard MOSFET.

In Fig. 4(a) the steep ON-switching of a SB-FET ULP diode at even lower bias than the CMOS ULP diode can be seen in the range from 0 to 300 mV, but not beyond threshold voltage due to current limitation in SB-FET by the tunneling mechanism. In reverse operation, the SB-FET ULP diode demonstrates a bell-shaped characteristic similar to what has been demonstrated in CMOS [1–6] previously. These curves also mimic the I-V behavior of resonant-tunneling diodes. Our simulation results fairly follow the qualitative trends measured over voltage and temperature, highlighting the negative resistance behavior in reverse operation, between −0.5 V and 0 V, while the quantitative differences result from different dimensions and threshold voltages in published experiments and our simulations.

The negative resistance region can be used to minimize the off-leakage current of diodes but also generate a latch effect for memory applications as will be discussed below. In such a case, the figures of merit are the peak and valley currents in reverse mode, as well as their ratios (PVR), dependence on temperature and bias conditions. Please also note that the simulated CMOS bell-shaped curve is very similar to what was measured in practice regarding current amplitudes, PVR, and their corresponding bias voltages [5,6].

3.3. Temperature dependence and physical interpretation

In Figs. 4(b) and 4(c) the different peak and valley currents of each ULP diode are shown for a temperature range of 230 K to 375 K. In Figs. 5(a), 5(b) and 5(c) the extracted current in peak and valley operation point and PVR is plotted for the same temperature range.

As one may observe, in Fig. 5(a) the peak results for V_D in CMOS from −33 mV to −51 mV and SB-FET from −27 mV to −52 mV. The valley

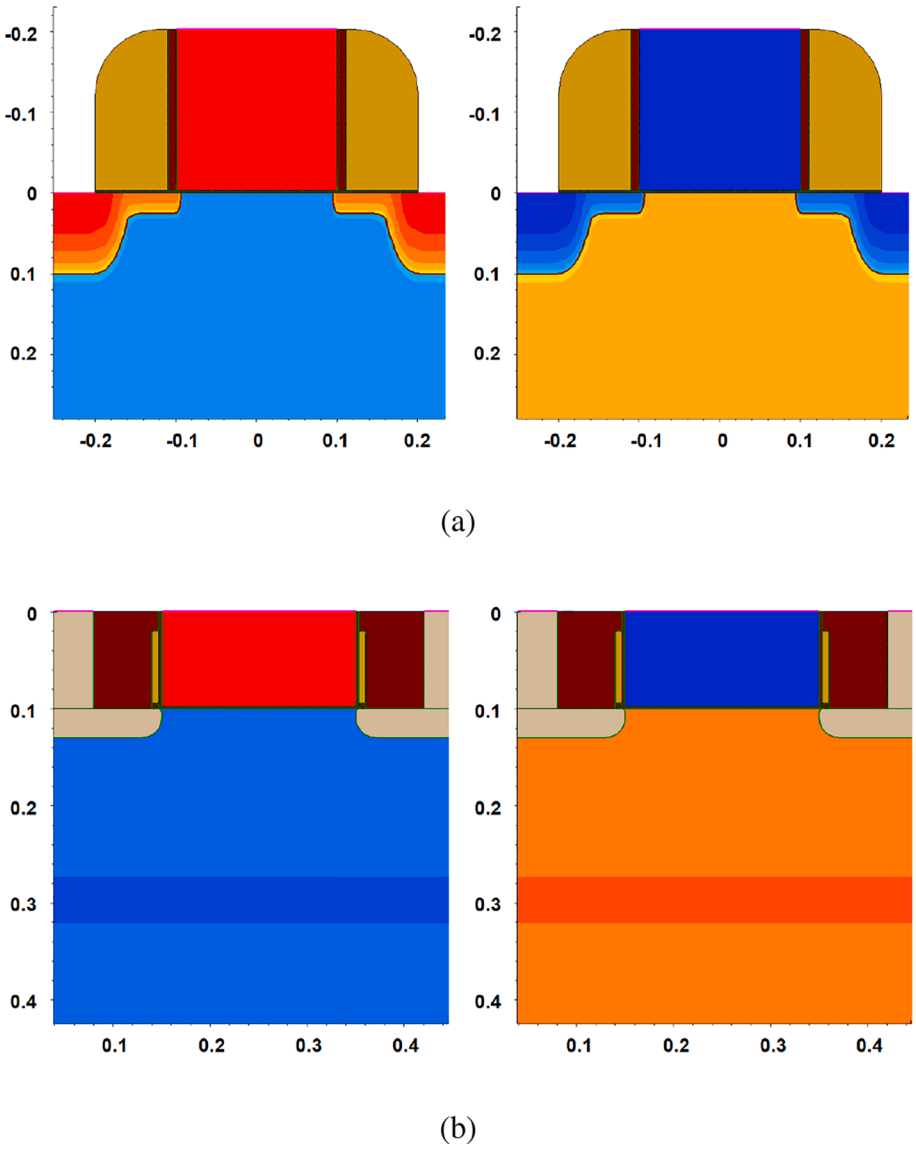


Fig. 2. (a) n-MOS (blue substrate)/p-MOS (orange substrate) TCAD device structures. (b) n-SB-FET (blue substrate)/p-SB-FET (orange substrate) TCAD device structures.

in Fig. 5(b) varies for V_D in CMOS from −500 mV to −558 mV and SB-FET from −318 mV to −606 mV.

For SB-FET ULP diode, the peak current is between two and three orders of magnitude higher compared to the CMOS ULP diode, see Fig. 5 (a). It is also remarkable to note that the peak current of the SB diode at low temperature keeps higher than that of the CMOS diode at RT. This will ensure functionality of the SB latches at low temperatures, as in practical applications has been demonstrated for the CMOS diode above RT.

On the other hand, the SB-FETs ULP valley current is between four and one orders of magnitude higher compared to the CMOS ULP diode as one can observe in Fig. 5(b). This is because for the SB-FET ULP diode the ambipolar current has to be taken into account. The extracted temperature dependences from 300 K to 375 K of peak and valley currents for both CMOS and SB-FET diode are summarized in Table 2.

For the classical CMOS ULP diode the amount of peak degradation, i.e. the decrease of peak current with lower temperature is much higher than in the counterpart with SB contacts. For the case of CMOS, the transistors are operated in deep subthreshold and the drain-to-source leakage current can be expressed as [11]:

$$I_{ds} = qDN_{sd}t_{ch}\frac{W}{L}\cdot\exp\left(-\frac{\psi_b}{kT/q}\right)\cdot\left(1-\exp\left(-\frac{V_{ds}}{kT/q}\right)\right) \quad (1)$$

with diffusion coefficient D of carriers, source/drain doping concentration N_{sd}, channel thickness t_{ch} and height of the potential barrier ψ_b which the carriers have to overcome by thermionic emission for entering the channel region. In case of $V_{ds} \gg kT/q$ and by defining a factor $A = qDN_{sd}t_{ch}W/L$ we obtain

$$I_{ds} = A\cdot\exp\left(-\frac{\psi_b}{kT/q}\right). \quad (2)$$

The temperature dependence is dominated by the exponential part. We obtain for the current in log scale:

$$\log I_{ds} = \log A - \frac{1}{\ln(10)}\cdot\frac{q\psi_b}{kT}. \quad (3)$$

Finally, we get for the inverse slope of the temperature dependence of the subthreshold current

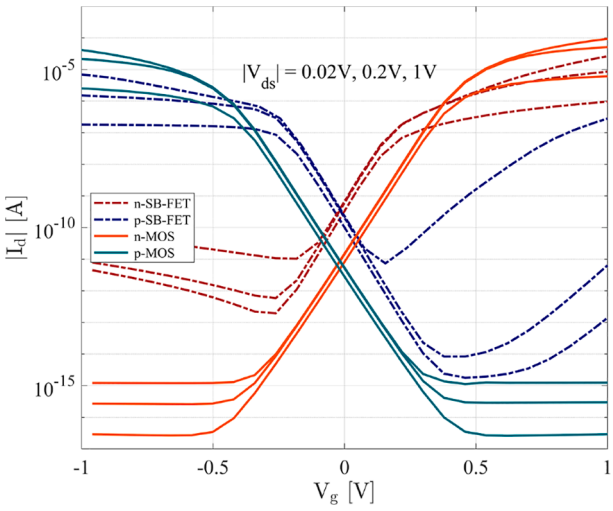


Fig. 3. $I_d - V_g$ curves of CMOS with n-MOS $L_{ch} = 200$ nm, $W_{ch} = 1\,\mu$m & p-MOS with $L_{ch} = 200$ nm, $W_{ch} = 2\,\mu$m, SB-FET with n-SB-FET $L_{ch} = 200$ nm, $W_{ch} = 1\,\mu$m & p-SB-FET with $L = 200$ nm, $W_{ch} = 10\,\mu$m, for different V_{ds}.

$$\frac{dT}{d\log I_{ds}} = \frac{kT^2}{q\psi_b}\ln(10). \tag{4}$$

The height of the potential barrier can be related to the gate bias by the following equation [11]:

$$\psi_b = -\frac{V_{gs} - V_T}{\eta}, \tag{5}$$

where η captures the impact of the gate bias on the barrier height depending on the capacitances per gate area of the gate oxide (C'_{ox}) and the depletion region in the channel (C'_{dep}):

$$\eta = 1 + \frac{C'_{dep}}{C'_{ox}}. \tag{6}$$

The subthreshold swing of the device is given by

$$S = \eta\frac{kT}{q}\ln(10) \tag{7}$$

revealing from the swing of $S \approx 78$ mV/dec a factor $\eta \approx 1.3$ at 300 K.

According to Fig. 4(b), for CMOS ULP diode demonstrates a peak at $V_D \approx 0.05$ V. Because of symmetry of p- and n-channel transistors we obtain for the n-channel device in a circuit according to Fig. 1 a gate-to-source bias of $V_{gs} \approx -0.025$ V. Having a threshold voltage of $V_T \approx 0.44$ V we obtain from (5) $\psi_b \approx 0.36$ V. According to (4) this results in an inverse slope of ≈ 49 K/dec at $T = 300$ K. This is close to the value of ≈ 50 K/dec which for CMOS ULP diode has been extracted from the simulations (refer to Table 2).

The valley appears from Fig. 4(b) at a voltage $V_D \approx 0.5$ V, obtaining in a similar way $\psi_b \approx 0.53$ V and an inverse slope of ≈ 34 K/dec in agreement with the simulation results.

For SB-FET ULP diode, in Fig. 4(c) one can observe with higher temperature a shift of the valley to lower V_D. From Table 2 it is obvious that the temperature dependence of both peak and valley currents is less (higher inverse slope) than for CMOS ULP diode. However, depending on the operation point the current in a SB-FET can be dominated by tunneling/field emission (FE) or thermionic emission (TE). In order to elaborate further, from TCAD simulation we extracted the inverse slope also for cases having only thermionic or only field emission current. According to the results shown in Table 2, in peak operation the inverse slope of ≈ 79 K/dec is dominated by thermionic emission current. This is in agreement to the bias point of $V_{gs} \approx -0.025$ V we find for the n-SB-

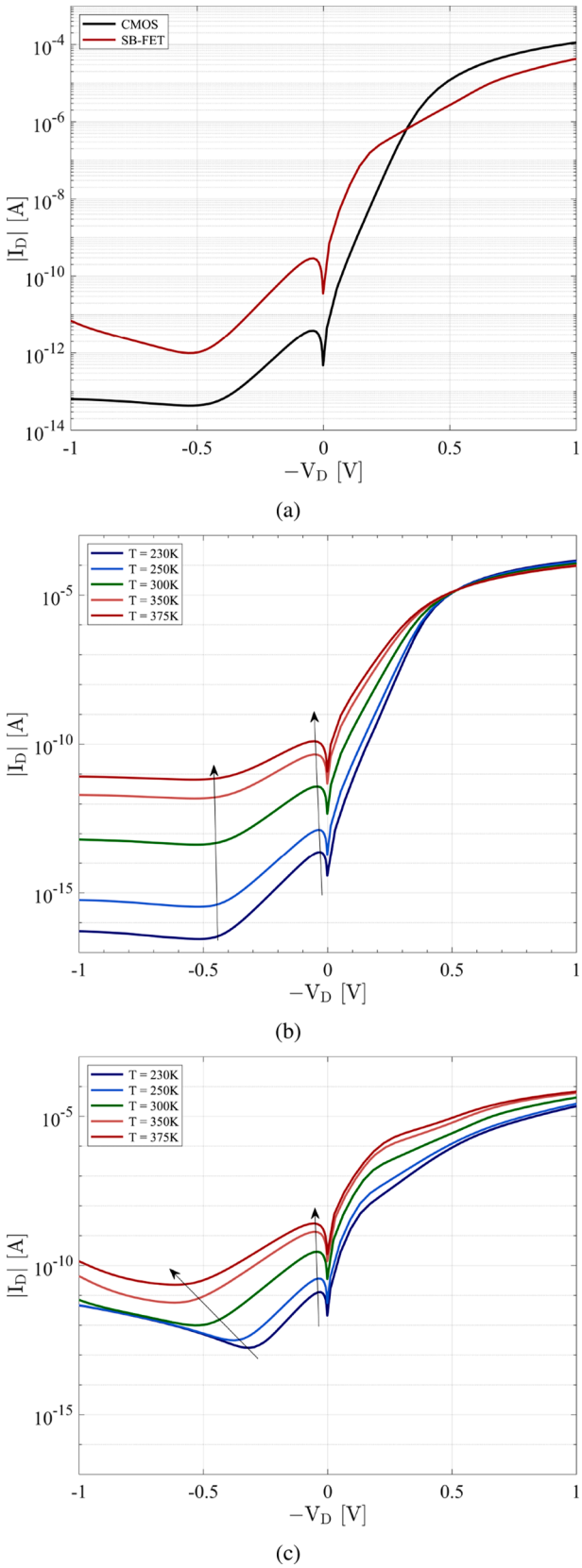
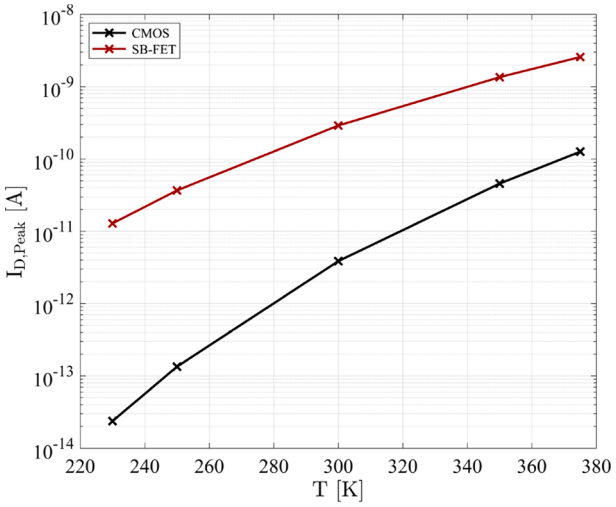
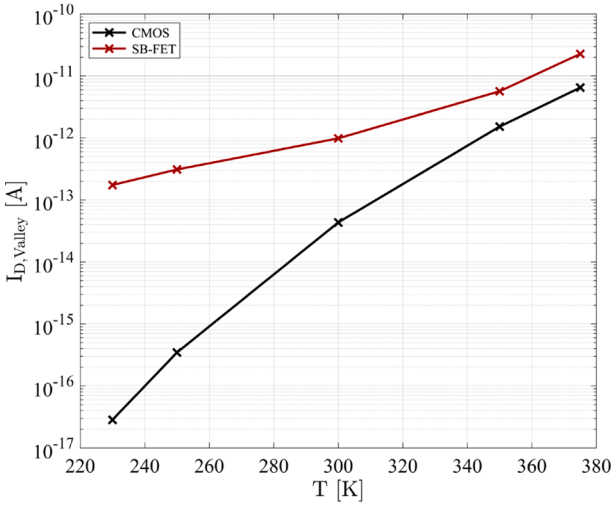


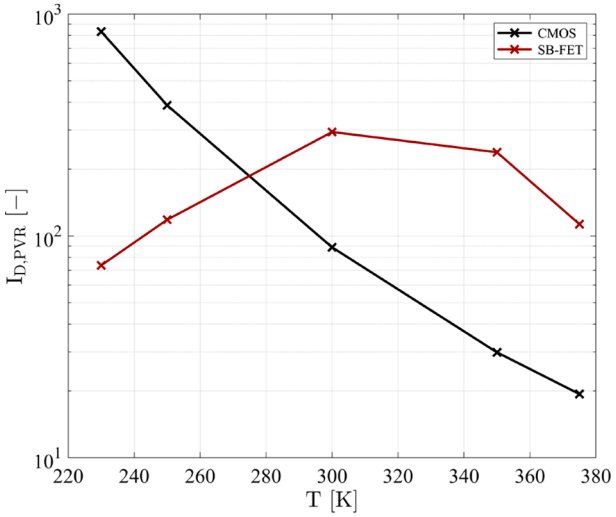
Fig. 4. (a) $I_D - V_D$ of CMOS ULP vs. SB-FET ULP at RT. (b) $I_D - V_D$ curves of CMOS ULP diode and (c) $I_D - V_D$ curves of SB-FET ULP diode vs. temperature.



(a)



(b)



(c)

Fig. 5. (a) Peak and (b) valley I_D of CMOS vs. SB-FET ULP diode in reverse mode. (c) Peak-to-valley ratio $I_{D,PVR}$.

Table 2
Peak and Valley inverse slopes for 300 K to 375 K for CMOS ULP and SB-FET ULP components.

	Peak	Valley
CMOS ULP	≈ 50 K/dec	≈ 34 K/dec
SB-FET ULP	≈ 79 K/dec	≈ 55 K/dec
SB-FET ULP TE only	≈ 79 K/dec	≈ 61 K/dec
SB-FET ULP FE only	≈ 130 K/dec	≈ 53 K/dec

FET in peak operation at $V_D \approx 0.05$ V. In this case, Fig. 7 shows the transistor is in the OFF state, far away from ambipolar operation.

Evaluating again Eq. (4), now with a barrier height of $\psi_B \approx 0.25$ eV we obtain an inverse slope of ≈ 72 K/dec, which is close to the TCAD results. Taking into account that the effective Schottky barrier height is the barrier the carriers have to overcome for thermionic emission, this value for ψ_B reasonable. It is close to the values $\phi_{Bn,p}$ defined for p- and n-SB-FET in Table 2.

If the SB-FET ULP diode is operated at valley point, then the contribution of tunneling current increases. Fig. 6 gives a detailed view of current contributions at $T = 300$ K. For the case of thermionic and field emission (TEFE) the electron current density plot including field emission contribution shows an increase of carrier injection with respect to electron thermionic emission (TE) only, especially at the rounded corner of the drain, which can be attributed to the higher electric field in this region. This is indicated by the contour level within the plot. The warmer the coloring, the higher the current density. Furthermore, the tunneling generation rate (TGR) illustrates tunneling of carriers all along the drain boundary, clearly indicating the onset of ambipolar current conduction.

Fig. 7 illustrates the bias dependence of the current contributions at different temperatures and gives insight to the physical origin of the valley formation and its shift with temperature. Current contribution by thermionic emission decreases with higher bias V_D. This results in a lower inverse slope of ≈ 61 K/dec (refer to Table 2) in valley operation compared to peak operation. The behavior can be attributed to a higher potential barrier the carriers from source have to overcome in valley operation than in peak operation.

In contrast, field emission current shows an increase with V_D, and this results in forming of the valley in the total current plot. The tunneling current shows a different temperature dependence than thermionic emission current [12]. Consequently, different temperature dependencies of both current components result in a shift of the valley point to a lower bias with decreasing temperature. At $T = 300$ K we obtain an inverse slope of ≈ 55 K/dec. As can be seen in Fig. 5(b), this value is further improved with lower temperature.

The SB-FETs have a slightly lower SS than the FETs, and also lower I_{on}/I_{off} ratio. Moreover they suffer from the ambipolar current. However, on another hand, the SB-FET ULP diodes demonstrate lower temperature variation in the reverse bias range. Then, in all cases, the SB-FET ULP diode outperforms the CMOS version in the whole temperature range from the application point of view.

In [6], the problem of too low current in the ULP structure for the SRAM cell application is indeed clearly emphasized with standard MOSFET implementation when operating at lower temperatures, since the reverse current drastically reduces, so that the SRAM read failure and delays increases, see Fig. 4(b). Trying to solve that, by e.g. lowering the MOS threshold voltage V_T, will yield too much power consumption under the higher temperatures. Our study shows that thanks to their lower temperature dependence, SB-FETs offer a better compromise towards optimization. As mentioned, there is margin to scale down the SB-FET by a factor of 5, hence the area and the power consumption.

The peak-to-valley-ratio in Fig. 5(c) for the current I_D demonstrates a more robust behavior of the SB-FET ULP diode over temperature. Especially, for the higher temperatures the degradation of the SB-FET

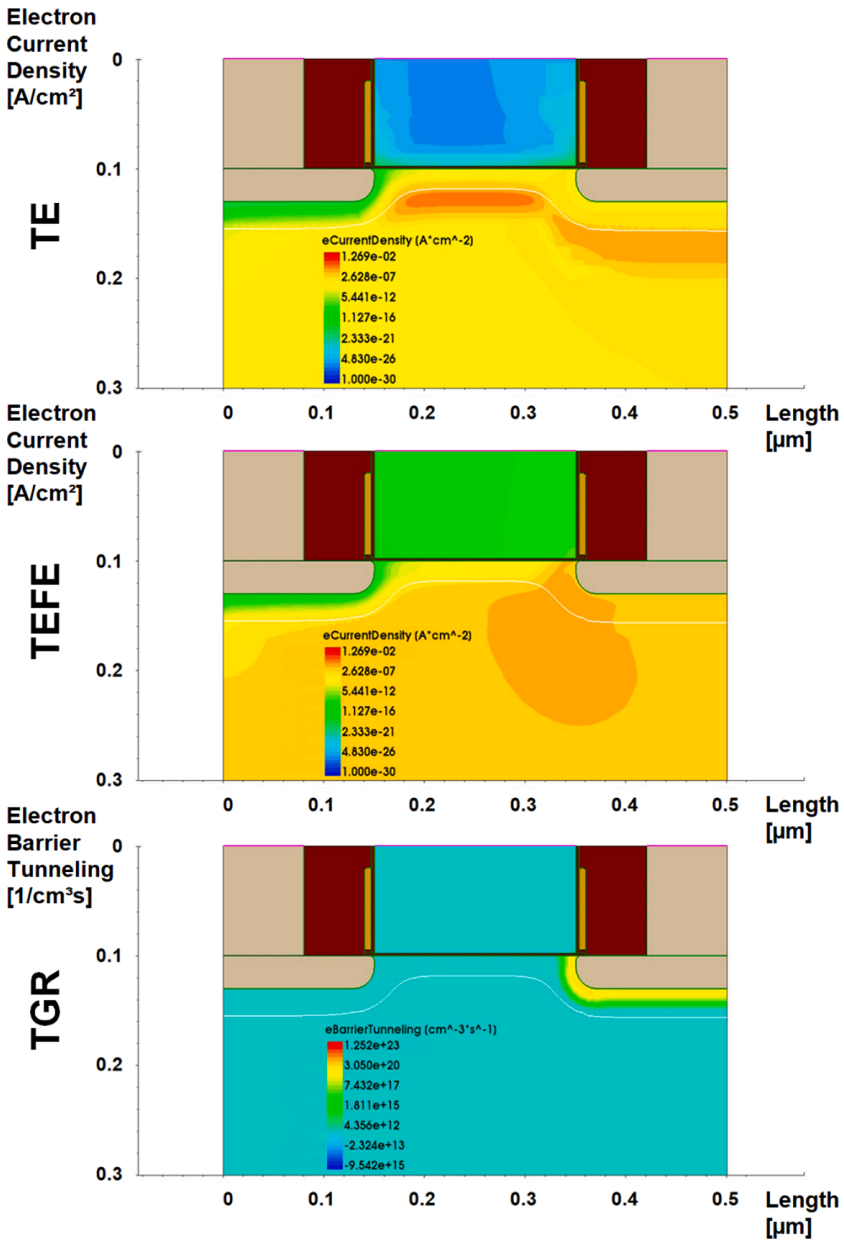


Fig. 6. p-SB-FET current densities at valley operation point $V_D \approx 0.5$ V.

ULP diode is 3*x* (reference is RT), whereas for CMOS ULP diode it is 8*x* when an adaptive V_D circuit scheme is used to follow the valley shift. The lesser dependence of the PVR to temperature could be used to more easily, and hence better optimize the design (i.e. choice of dimensions, *W*).

According to Fig. 5(a), in CMOS diode a low peak current is critical at low temperature, whereas low PVR is critical at high temperature. In SB diode, a low *T* design would stay robust in the whole temperature range provided that an adaptive supply voltage is used. This finally allows for the ULP peak current a reduction of the SB-FET's widths (*W*) by a factor of 5, bringing the minimum *W* of the p-SB-FET equal to CMOS and that of the n-SB-FET to minimum *W*, and hence, the SB-FET leakage current close to that of CMOS. Otherwise, higher regenerative current peaks result in higher static power consumption.

3.4. Application towards memory cells

Further investigations were performed on the ULP bistable memory cell as shown in Fig. 8 adapted from [1]. Here, we combine two ULP diodes (D1 and D2) and an input MOS switch to realize a ULP bistable circuit. The current difference $I_{D2} - I_{D1}$ is represented as a function of the voltage V_x applied at the intermediate node, see Fig. 9a. It sums up the negative resistance behavior of the two superposed ULP diodes. If we apply a voltage V_{in} between 0 and half of V_{DD} through the closed switch, and next open the switch to leave *C* floating, the current difference will discharge *C* towards 0 V, writing a 0-logic stable state. A logic 1 can be similarly obtained applying a voltage V_{in} above half of V_{DD}. Furthermore, there exists one metastable state at the mid point.

We finally apply the transistor results to the memory concept of Fig. 8. In Figs. 9b and 9c we compare the CMOS and SB-FET ULP Memory characteristics. Here, for fully visualizing maximum and minimum, as well as positive and negative currents, as a function of *T*, we use a logarithmic current scale defined as

$$y = sign(x) \cdot (log10(1 + abs(x)/(10^C))) \quad (8)$$

where the scaling constant *C* determines the resolution of the data

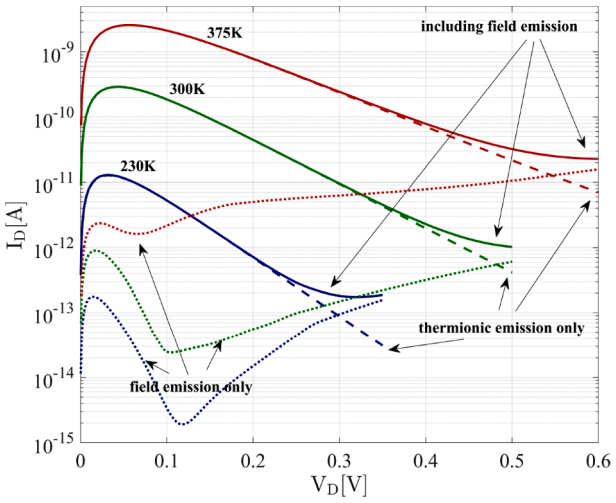


Fig. 7. SB-FET ULP diode (n-SB-FET and p-SB-FET devices) electron and hole currents with and without tunneling (field emission) over temperature for various $|V_D|$.

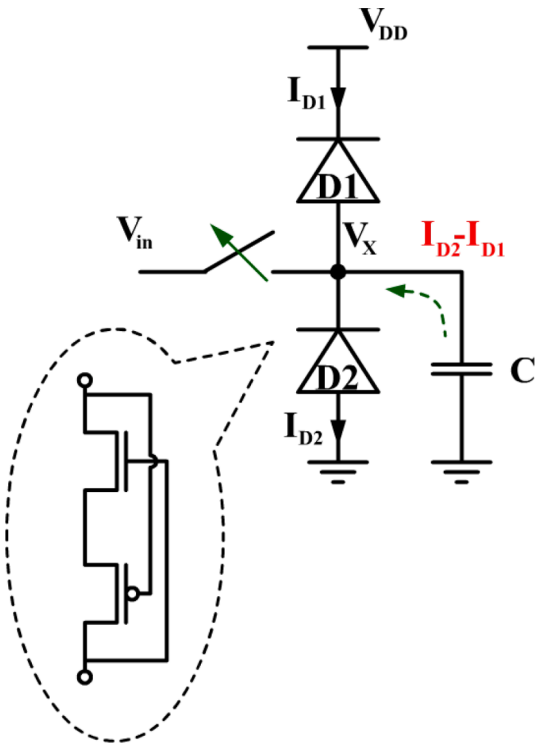


Fig. 8. ULP bistable memory cell adapted from [1].

around zero. The smallest order of magnitude shown on either side of zero will be $10^{ceil(C)}$ according to [18].

In CMOS, it has been shown that the current is high enough at high temperature to yield a functional SRAM, but not at low temperature [6]. From the comparison of both it is obvious, that the SB-FET ULP SRAM shows a 20*x* higher current and hence higher stability at low temperature. This could be retained even if the SB-FET widths are scaled down by a factor of 5, thus making the p-SB-FET the same size than in CMOS, but the n-SB-FET 5 times smaller, hence yielding a much smaller memory area.

However, as discussed in [5,6], the ULP bistable memory cell can be used to build a 7- or 8-transistor SRAM cell, but with better power x delay performance than conventional 6-T ones. As in [5,6], the ULP

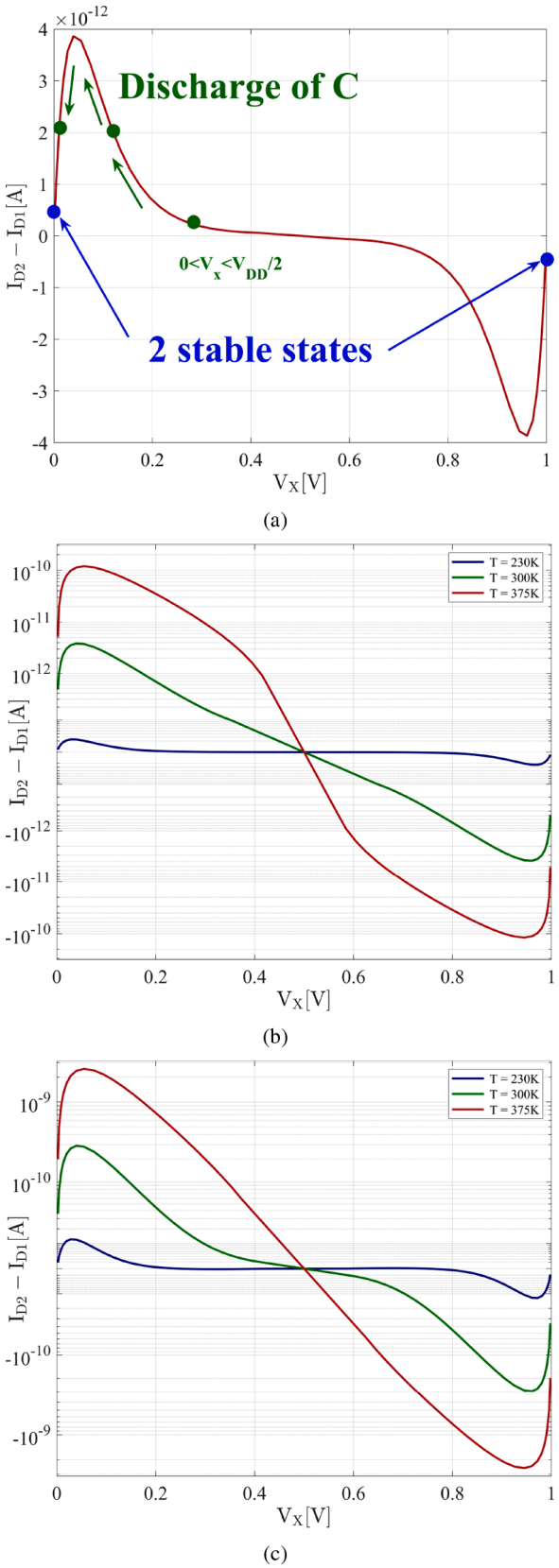


Fig. 9. CMOS ULP Memory at RT with n-MOS $L_{ch} = 200$ nm, $W_{ch} = 1$ µm & p-MOS with $L_{ch} = 200$ nm, $W_{ch} = 2$ µm at (a) RT and (b) over T. (c) SB-FET ULP Memory with n-SB-FET $L_{ch} = 200$ nm, $W_{ch} = 1$ µm & p-SB-FET with $L_{ch} = 200$ nm, $W_{ch} = 10$ µm.

SRAM will operate from the conventional supply voltage, for all write, hold and read operations. Given that the technology, dimensions and current–voltage curves of the ULP diodes are similar to the ones reported in [5], we would expect them competitive with standard SRAM from the same technology node.

4. Conclusion

For the first time, the ULP diode concept was applied to SB-FET transistors to mitigate their ambipolar leakage current. Using calibrated TCAD mixed-mode simulations, the SB-FET ULP diode is shown to offer superior performance in comparison to standard CMOS with regards to the bell-shaped I-V characteristics in reverse mode, of interest to design ULP latch circuits and SRAM cells notably.

This has been related to the better performance of the SB-FETs in weak inversion, and as a function of temperature. Compared to the CMOS counterpart, the SB-FET ULP diode can provide a peak current less degraded at low temperature, a valley current less degraded at high temperature and all together a more robust (i.e. constant) peak-to-valley ratio from 230 K to 375 K. As discussed in [5,6], the ULP SRAM ultra-low-power and speed performances depend on the worst-case values of, respectively, the I_{valley} and I_{peak} of the ULP diode that are obtained respectively, at the highest and lowest temperature conditions. Our results indicate that these can be equivalent or better in SB-FETs than in CMOS transistors, with all respects.

The origin of this behavior manifests itself in the fact that the field emission current and the thermionic emission current prevail in different bias ranges. Both components intersect at a certain bias and create the valley. This valley is stabilized over temperature by both players contrary to a classical CMOS ULP diode in which no field emission is present. It enables this superior current performance of the SB-FET ULP diode concept over temperature.

The results finally offer a possibility to design the SB-FET ULP diode with I-V curves compatible with the operation of memory cells, using about 30% less area than in standard CMOS including real design rules and interconnects [19].

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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