# Micrometer-thin SOI Sensors for E-Skin Applications

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***Abstract*—Ultra-thin silicon-on-insulator-based sensors are presented, featuring a thickness of less than 20 µm, as new integrable items for wearable physical and physiological ultra-low-power applications. Depending on the Si thickness, the back contact realization and the bias conditions, they can be optimized for thermal sensing or optical sensing in the UV-VIS light band. A lateral PIN diode with a transparent graphene back gate shows a maximum responsivity of 0.18 A/W at 390 nm wavelength, and a high sensitivity of ~2.28 mV/°C at fixed 0.01 µA low bias current, whereas a vertical PN strip diode with an Al back contact extends the optical responsivity to the visible range (with e.g. 0.24 A/W at 555nm wavelength when biased at -2 V) and achieves a high-temperature sensitivity using constant reverse voltage method.**

***Keywords—Flexible electronics, Ultra-thin, Silicon-on-insulator, Wearable sensors, Temperature sensors, Optical sensors, Graphene gate***

## I. Introduction

Thin, flexible, low-power, possibly wireless and energy autonomous health monitoring wearable sensors offer new functionalities for artificial electronic skins or e-skins [1]. Crystalline semiconductors like silicon show varied properties with temperature, illumination or strain, and are already used as for example, piezoresistive sensors for force mapping of hip-prostheses [2], or monitoring of UV or temperature skin exposure [3, 4] (Fig. 1). Thermal burns cause second-degree skin damages starting at 44°C if applied during 6 h, while at 70°C, damage occurs in less than 1 s [5]. Sunburns may directly damage skin DNA or cells, producing pain symptoms with often hour delays. Monitoring light and temperature body exposure during long periods of time, at low power, is then of utmost interest.

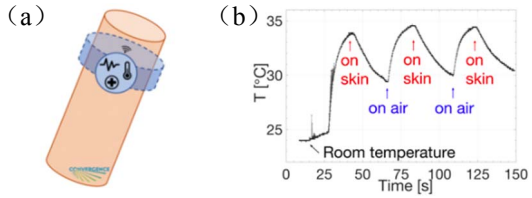


Fig. 1. (a) Flexible wearable concept for human body monitoring, and (b) Measurements of a temperature wrist with the lateral PIN diode of section II.A (distance from arm is varied over time to prove functionality).

This work was supported by the Micro+ project co-funded by the European Regional Development Fund (ERDF) and Wallonia (Belgium), the FRS-FNRS Convergence project (Belgium), the National Natural Science Foundation of China No. 61705065, the Hunan Provincial Natural Science Foundation of China No. 2020JJ4214.

In order to develop and validate technologies adequate for such applications and requirements, the present paper compares (i) different processing alternatives and (ii) performances of experimental Si temperature and light sensors thinned down to a few µm, providing potential flexibility capabilities beyond standard Si-based devices.

## II. Fabrication Alternatives

Two wafer-level processing approaches have been used to evaluate the capabilities of silicon-on-insulator (SOI) technologies to deliver high-performance, stable and robust devices, with final thickness of less than 20 µm at die level.

### *A. Fabrication for ultra-thin lateral sensor*

First sensors were manufactured using X-fab 1.0-µm SOI CMOS technology that monolithically integrates diodes, MOSFETs, micro-hotplates… on thin membranes (typically of a few mm$^2$) after post-CMOS MEMS processing [6, 7]. A such on-membrane lateral PIN diode for temperature and light sensing has been previously reported [7, 8]. It features a multilayer stack comprising 560-nm thick $Si_3N_4$ for passivation, 2.5-µm $SiO_2$ for stress-relief, 300-nm polysilicon as implantation mask, 25-nm $SiO_2$ gate dielectric for MOSFETs, 250-nm Si active layer and 1.0-µm $SiO_2$ buried oxide or BOX, as depicted in Fig. 2 (a). However, due to the interface traps created by the etching of back Si substrate using DRIE, the device performance can only be stabilized and optimized by adding an Al back gate below the BOX and annealing the final structure at high temperature [8]. Best achieved temperature sensitivity is ~ 2.25 mV/℃ at 0.02 µA low forward constant current and high back gate bias, up to 200 ℃ [7]. For optical sensing, a maximum responsivity of 0.1 A/W is achieved at 590nm with the Al backside optical reflector and electrical gate. However, the CMOS polysilicon gate, used as implantation mask for the intrinsic region of the diode, lead to unnecessary high absorption for wavelength below 450 nm and dramatically reduced the diode optical response in the ultraviolet range [8].

To achieve ultra-thin-die singulation and solve the problems of defect creation and non-transparent back gate, the process was extended to isotropic etching with xenon difluoride ($XeF_2$) of the whole back Si substrate, followed by the transfer of a graphene gate on the BOX, as shown in Fig. 2 (b). Dies can be mounted on thin PCB with holes for back-side illumination or with a back-side conductor for graphene biasing [9]. When irradiated through the transparent back gate,

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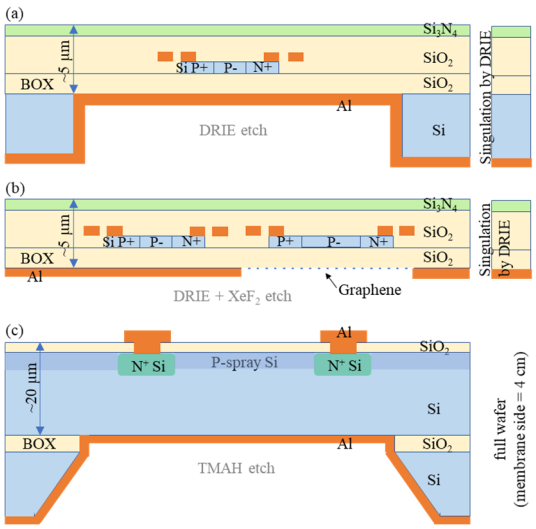


Fig. 2. Schematic cross-sections of SOI sensors: (a) ultra-thin lateral PIN diode with Al gate, (b) ultra-thin lateral PIN diode with graphene gate, (c) micrometer-thin strip diode with Al contact.

a high UV optical responsivity of 0.18 A/W has been achieved at 390 nm wavelength. In the present paper, the thermal sensing performance will be added.

### *B. Fabrication for micrometer-thin vertical sensor*

To increase the responsivity of the SOI sensors in the visible range, the Si thickness must be greatly increased and a vertical diode structure is preferred. As shown in Fig. 2 (c), strip detectors were initially fabricated on 3-inch p-type double-side polished SOI wafers, with a BOX thickness of 400 nm and a top silicon thickness of 20 µm, for radiation detection [10]. In this work, the thermal and optical sensing performances have further been studied. The top silicon layer acts as the thin active membrane after etching the bottom silicon substrate below the detector, up to a quasi-full-wafer-level area of 4.5 x 4.5 $cm^2$.

Firstly, a wet-thermal oxide of 300 nm was grown as a hard mask for the backside thinning, and a wet-thermal oxide of 50 nm was grown as a protection layer on the frontside to reduce the silicon damages caused by the implantation. For N+ strip implantation, $10^{21}$ $cm^{-3}$ arsenic doping concentration was achieved at the oxide/silicon interface. The length, width and depth of the $N^+$ strips are 1.5 cm, 30 µm and 1 µm, respectively. A p-spray boron implantation process is typically performed at the silicon surface between the $n^+$-strips in order to insulate them, without requiring an extra photolithographic mask. For reliability purposes, an additional 250 nm oxide layer was deposited through Plasma Enhanced Chemical Vapor Deposition (PECVD) process, and contact holes then be etched to enable the metallic contact to the implanted strips. Strips were then metallized by depositing a 200 nm Al/Si (1%) layer to reduce spiking effect. In order to protect the device from its environment, a nitride passivation layer (not shown in the Fig. 2 (c)) of 200 nm was deposited by PECVD over the whole frontside surface.

Secondly, the thinning step was performed. The backside oxide was etched over the active area with a BHF solution for 6 min. Afterwards, the bulk silicon was etched in a 5% TMAH bath at 95 ℃ for about 10 hours. For the BOX release, a RIE with a CHF3 plasma was performed for 25 min. Finally, the back metallization consists of a 250 nm thick aluminum layer which was finally annealed at 432 ℃ for 30 min.

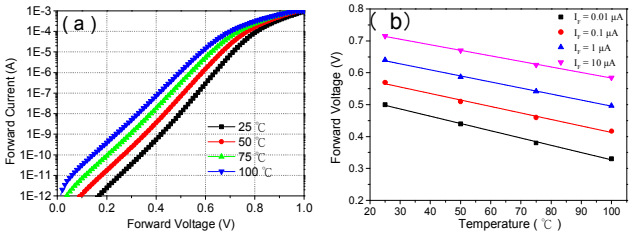


Fig. 3. (a) Forward current characteristics and (b) Forward voltage ($V_F$) at different temperature from 25 to 100 °C of SOI lateral PIN on membrane diode gated by graphene under 0V gate voltage.

TABLE I. LINEARLY STABILIZED THERMAL SENSITIVITY

| Sensitivity (mV/℃) | 0.01 µA | 0.1 µA | 1 µA | 10µA |
|---|---|---|---|---|
| [7], $V_G$= 0 V | / | -1.94 | -1.74 | -1.56 |
| This work, VG = 0 V | -2.28 | -2.04 | -1.90 | -1.74 |

In summary, the different sensors all benefit from the SOI technology to thin them down to the BOX layer by the TMAH, DRIE or $XeF_2$ etching technique which present advantages such as CMOS compatibility and high Si:$SiO_2$ selectivity.

## III. TEMPERATURE SENSING WITH GRAPHENE-GATED SOI LATERAL PIN DIODE

Working under reverse voltage mode, our ultra-thin SOI lateral PIN diode exhibited enhanced photodetection characteristics compared to standard SOI lateral PIN diode when introducing graphene as the back gate [9]. Additionally, the same diode can be used for thermal sensing when biased under forward voltage mode.

In Fig. 3 (a), the current characteristics under 0 V gate voltage and forward voltage sweep from 0 to 1 V are presented from room temperature (25 ℃) up to 100 ℃, considering that e-skins may have to detect hazardous temperatures in excess of 45 °C. The forward current increases with temperature as expected, with the increased intrinsic carrier concentration in Si. To quantify the performance of the diode, the thermal sensitivity is calculated by formula (1)

$$-\mathrm{d} = \frac{V_{F2}-V_{F1}}{T_2-T_1} \quad (1)$$

where -d is the slope of Forward voltage ($V_F$)-Temperature (T) curve. In Fig. 3 (b), $V_F$ has been extracted at different temperatures with constant forward current ($I_F$) of 0.01, 0.1, 1 and 10 µA.

The corresponding thermal sensitivity is calculated from the linear fit of $V_F$-T curves and compared, in Table 1, with the best results reported for on-membrane SOI Lateral PIN diode gated by Al in [7]. The thermal sensitivity slightly decreases with increasing forward current due to parasitic series resistance of the junction in higher forward voltage mode [11]. In this work, the diode gated by graphene at 0 V shows a greatly improved and more stable sensitivity of 1.74-2.28 mV/°C at lower forward currents of 0.01-1 µA, from room temperature up to 100 °C. This record value for SOI based PIN diodes is probably related to the smooth defect-free processing using $XeF_2$ and graphene transfer, compared to DRIE and Al deposition.

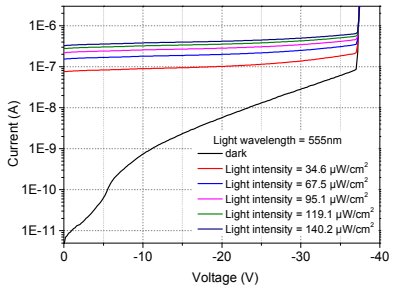


Fig. 4. Dark and Photo current of the Micrometer-thin strip sensor versus reverse voltage under varied light intensities at a wavelength of 555 nm.

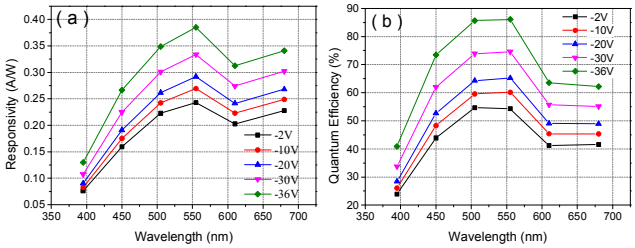


Fig. 5. (a) Responsivity and (b) Quantum efficiency spectra of the strip sensor at varying bias voltages.

## IV. MICROMETER-THIN SOI STRIP VERTICAL DIODE

### A. Optical sensing performance

I-V curves of the vertical strip sensor were measured under illumination using LEDs with wavelengths of 395, 450, 505, 555, 610 and 680 nm, and low light intensities ranging from 34.6 to 140.2 μW/cm$^2$. The curves under dark and 555 nm light with varied intensities are plotted in Fig. 4 demonstrating a significant and linear response with the intensity.

The responsivities and quantum efficiencies (QE) are calculated in the visible spectrum from 395nm to 680nm under different reverse voltages from -2 V to -36 V, which indicates that the device has high response performance throughout the visible spectrum as shown in Fig. 5. The sensor achieves its highest responsivity of 385 mA/W and a corresponding QE of 86% at 555 nm with a bias of -36 V close to avalanche breakdown. The high reverse bias below avalanche voltage increases the width of the depletion layer with an electric field that will cause photogenerated carriers to be efficiently collected. Under a low bias voltage of -2 V better suited for wearable electronic skin applications, its responsivity and QE at 555nm still reach high values of 243 mA/W and 54%, respectively.

Compared with the previous Al-gated and graphene-gated ultra-thin lateral sensors using the same reverse biased voltage of -2 V [8,9], the present micrometer-thin vertical strip sensor shows a lower responsivity at 390 nm, in the blue, but a much better responsivity in the green and red (Table II) in direct relation with the increased absorption depth caused by inner vertical junction and thicker silicon substrate.

### B. Temperature sensing performance

To limit the current increase in the vertical strip diode to low values, especially at high temperature, we used a constant reverse bias voltage for thermal sensing, instead of the constant forward current method.

TABLE II. OPTICAL RESPONSIVITIES OF DIFFERENT SOI SENSORS IN VISIBLE SPECTRUM. (WORKING VOLTAGE = -2V)

| *Sensor type* | *Thickness* | *Irradiating side* | *Highest Responsivity* |
|---|---|---|---|
| [8], Lateral PIN, Al gate | ~5 μm | Frontside | 100 mA/W @ 590 nm |
| [9], Lateral PIN, Graphene gate | ~5 μm | Backside | 110 mA/W @ 490 nm |
| This work, Strip vertical N+/p-substrate diode, Al contact | ~20 μm | Frontside | 243 mA/W @555 nm |

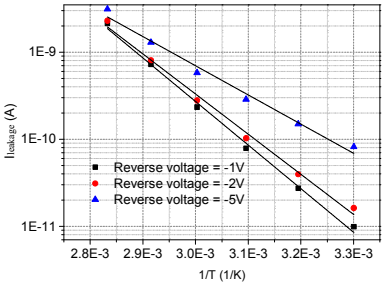


Fig. 6. 1/T dependence of leakage current at various reverse biases of the micrometer-thin strip sensor.

The reverse leakage current $I_{leakage}$ increases with temperature following [11]:

$$I_{leakage} \cong KT^r e^{(-qV_g/kT)} \quad (2)$$

q is the electron charge, k the Boltzmann's constant, T the absolute temperature, $V_g$ the extrapolated energy gap at absolute zero temperature, K a constant that depends on geometric factors like the area of the p–n junction, and r a process dependent parameter with a value of ~ 3.5 for silicon. As the terms K, r and $V_g$ are independent of temperature, a linear relationship between the log of $I_{leakage}$ and 1/T can be obtained in the reverse constant voltage mode from (2).

The temperature variations of the leakage current measured at constant voltage of -1 V, -2 V and -5 V are presented in Fig. 6, The leakage current increases exponentially in the temperature range from 30 to 80 ℃, which shows a high thermal sensing stability of the micrometer-thin strip sensor. Especially when the device is biased at -1 V, the fitted straight line as shown in Fig. 6 has a very high slope, which indicates a very high thermal sensitivity of the strip sensor, while the value of leakage still remains much smaller than the photocurrent (Fig. 4).

## CONCLUSIONS

We demonstrated working prototypes of very thin, potentially bendable, thermal and optical SOI sensors based on the full thinning of underlying substrate and the realization of a back contact for stable measurements and high performance. In particular, the $XeF_2$ thinning of Si substrate till the BOX and the transfer of a graphene back gate do not affect the chip quality (on the contrary to DRIE and Al back gate) and deliver higher performance in temperature and UV/blue sensing than the reference die. To extend the optical sensing to the visible range, a vertical strip diode has been tested with thicker SOI active layer, TMAH substrate etching and Al back contact. The chips from the two approaches are compatible with direct board assembly paving the way towards the development of hybrid flexible electronics into a soft polymeric e-skin, possibly autonomous with passive RFID and energy harvesting solutions.

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