Digital Substrate Noise Coupling into Trap-Rich HR-SOI Substrate

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1. Abstract

The influence of substrate noise coupling on the RF performance of FD SOI MOSFET built on top of commercial high-resistivity (HR)-SOI and trap-rich (TR)-SOI substrates is investigated when a digital noise signal is injected in the vicinity of the transistors. A crosstalk reduction of more than 20 dBm is achieved with TR-SOI substrate when noise frequency varies from 500 kHz to 50 MHz.

2. Introduction

The continuous downscaling of CMOS technology has stimulated the trend to integrate radio-frequency (RF) analog circuits with baseband digital circuitry to realize system-on-chip (SoC) solutions onto Si [1]. Despite its advantages thanks to a higher integration level, hybrid systems fabricated on Si substrates face the problem of analog performance degradation due to the impact of digital switching noise, called substrate noise coupling [2]. Voltage variation into silicon substrate is induced by CMOS digital integrated circuits. The noise propagates to the area of sensitive analog/RF circuits and interferes with their operation. In bulk CMOS technology, the physical area of sensitive devices is overlaid by deep n-well or surrounded by guard rings for isolation [3], [4]. SOI technology presents the major advantage of providing high resistivity capabilities which are mandatory for high performance RF integrated circuits [5], leading to substantially reduced substrate RF losses and crosstalk [6]. However, oxidized HR-Si wafers suffer from parasitic surface conduction due to fixed oxide charges which attract free carriers at the Si/SiO_2 interface, hence creating a highly conductive layer which reduces the substrate effective resistivity, increases substrate losses [7], and crosstalk [8]. The introduction of a trap-rich passivation layer underneath the buried oxide has been proved as the most effective technique to reduce PSC effect while being compatible with SOI wafer fabrication and with the important thermal budget of standard SOI CMOS process [9].

In this paper, we experimentally study the reduction of digital substrate noise coupling effect and its impact on FD SOI MOSFET behavior fabricated on top of standard or trap-rich HR-SOI UNIBOND wafers provided by SOITEC.

3. Experimental Results

2 µm-long Fully-depleted (FD) MOS transistors are fabricated using a standard CMOS process [10] on commercial 200 mm SOI wafers. The cross-section of the FD SOI MOSFET is shown in Fig. 1, having 400 nm BOX, 80 nm for the thin active silicon film and 25 nm for the gate oxide thickness, all lying on HR-Si with and without a trap-rich layer underneath the BOX. The propagation of substrate noise through HR-SOI and TR-SOI is investigated by measuring the frequency spectra at the MOSFET's drain when a clock noise is injected in the vicinity of the transistors via a metallic pad 350 µm away from the device.

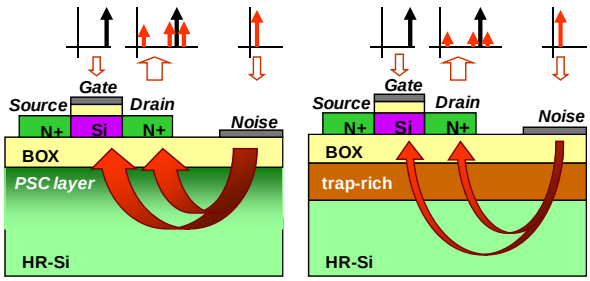


Fig. 1: *Digital substrate noise injected close to a FD SOI MOSFET on HR-SOI and TR-SOI wafers*

3.1. Digital substrate noise reduction on TR-SOI

The FD SOI MOSFET is biased in saturation mode (V_{GS} = 2 V and V_{DS} = 1.5 V), and an input RF signal f_c = 900 MHz is applied at its gate. Fig. 2 shows the directly coupled noise for 500 kHz noisy test square signal (5 V peak-to-peak) is applied. Although it was expected that at such low frequencies the BOX layer of the SOI technology provides a high isolation level, the presence of a highly conductive surface layer at the BOX/HR-Si interface leads to coupling and propagation of the large noise signal. However, in the case of TR-SOI the directly coupled noise signal level is highly reduced. The largest noise peak, at 500 kHz, is -50.2 dBm for HR-SOI while it is reduced to -81.2 dBm for the TR-SOI.

3.2. Impact of the injected noise on FD SOI MOSFET

The impact of DSN is not limited to the direct coupling

of the noise signal but it can also generate mixing products combined to the signal of operation of the analog device. When a digital noise is injected near the active device, we observe N harmonics at f_c - Nf_{noise} and f_c + Nf_{noise} as shown in Fig. 3. The generation of these mixing products of the RF input and the noise signal at the RF output can be explained by the substrate noise coupled at the back-gate of the FD SOI transistor which modulates the active zone. As it can be seen this mixing products are well attenuated when a trap-rich layer is introduced underneath the BOX. In fact, as it can be seen in Fig. 3b, the noise signal falls by more than 22 dBm compared with the HR-SOI wafer when a 500 kHz square signal of 5 V peak-to-peak is injected.

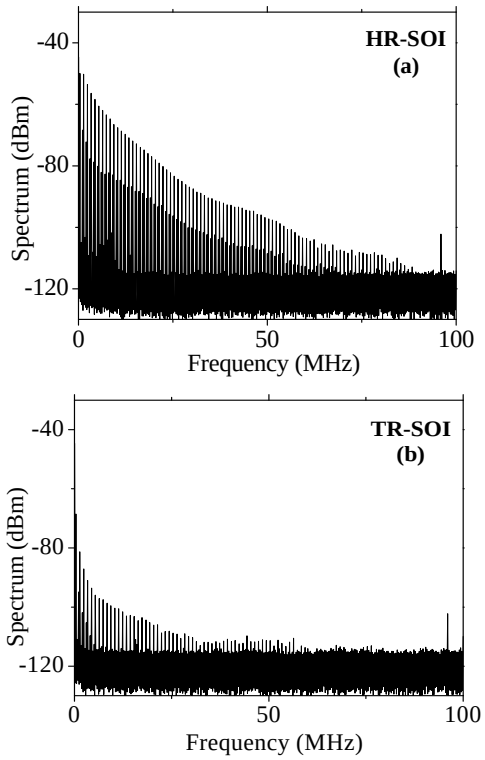
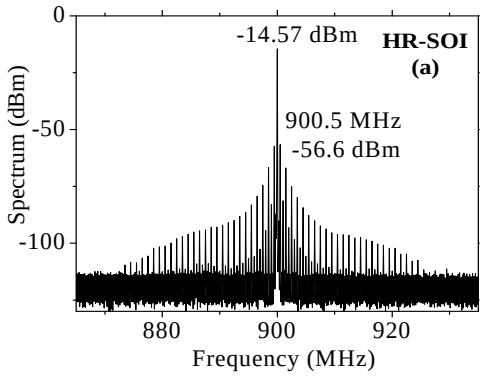


Fig. 2: *Frequency spectrum of measured noise signal on (a) HR-SOI and (b) TR-SOI wafers (clock frequency = 500 kHz, V_{pp}= 5 V).*



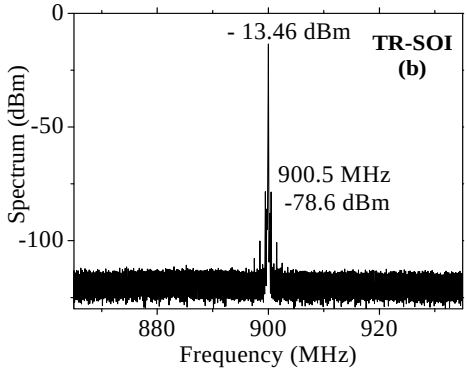


Fig. 3: *Output spectrum around 900 MHz for a FD SOI MOSFET on (a) HR-SOI and (b) TR-SOI.*

Table 1 shows the detected power levels of the mixing products due to the noise signal on both HR-SOI and TR-SOI when the frequency noise varies from 500 kHz up to 50 MHz. A reduction of more than 20 dBm is obtained with TR-SOI in comparison with HR-SOI. This result confirms the efficiency of commercially available TR-SOI substrate to reduce the noise coupling between digital and sensitive analog/RF parts on the same chip.

Table 1: *Harmonic levels at 900 MHz ± Nf_{noise} for HR-SOI and TR-SOI wafers.*

Freq. (MHz)	HR-SOI (dBm)	TR-SOI (dBm)
0.5	-56.6	-78.6
1	-56.05	-85.49
10	-68.67	-101.82
50	-79.76	-99.39

4. Conclusion

The efficiency of the trap-rich HR-SOI technology to reduce DSN is demonstrated. TR-SOI wafers provide an adequate level of isolation while reducing the coupling through the substrate at clock frequencies and maintaining HR properties. TR-SOI can be considered as an excellent solution for the co-integration of digital, analog and RF ICs on the same chip.

Acknowledgment

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