SOI FinFET compact model for RF circuits simulation

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***Abstract* — A methodology to properly establish an accurate SOI FinFET compact model through SPICE simulator is presented. This compact model is implemented in Verilog-A to simulate the performance of RF circuits based on SOI FinFET technology. It predicts well static behavior of the transistor and circuit, as well as their small-signal RF behavior by modeling the intrinsic capacitances and also the effects of the gate resistance and the extrinsic gate capacitances. Finally, the comparison between the simulated and measured performance of a Low Noise Amplifier demonstrates the validity and the capabilities of this compact model to simulate the dc and RF behavior of RF circuits.**

***Index Terms* — RF circuits, LNA, FinFETs, Compact model, Verilog-A.**

I. Introduction

Thanks to the better electrostatic control of the channel with its three-gate architecture, which reduces the Short Channel Effects (SCE), SOI FinFETs became attractive for very high frequency applications. In this context, accurate RF modeling is of first importance, which can be made based on the definition of the small-signal lumped equivalent circuit [1]. Hence a compact model that considers internal capacitances as well as external parasitic elements, such as three-dimensional (3D) capacitances, gate resistance and source/drain resistances, becomes crucial for this purpose. Recently, an analytical compact model for SOI Symmetric Doped Double Gate MOSFETs (SDDGM) was implemented in Verilog-A, where its applicability for SOI FinFETs was demonstrated in [2] as well as its capability to reproduce the small-signal parameters from dc characteristics [1]. The SDDGM compact model considers the doping concentration of the silicon layer from lowly to highly doped, which provides good agreement with numerical calculation of the potentials. Field dependent mobility as well as SCE, such as DIBL, channel length modulation and velocity saturation, are included.

In this context, an extension of the Verilog-A implementation is proposed with the aim of correctly determining the behavior of the SOI FinFETs in high frequency domain through SPICE simulations. Comparisons with experimental data of stand-alone transistors are done to check the validity of the compact RF modeling. SOI FinFETs with 250 and 500 nm of channel length (L) composed of 50 gate fingers (N_{finger}) controlling 9 fins (N_{fin}) each were built at IMEC, Leuven, Belgium. The transistors with fin height (H_{fin}) and fin width (W_{fin}) of 60 and 32 nm, respectively, were measured. Also, the transistors are characterized by a fin spacing (S_{fin}) of 328 nm and a extension length to the source and drain contact (L_{ext}) of 145 nm. The gate stack is formed by 2 nm equivalent oxide thickness (EOT), 5 nm of TiN metal and 100 nm-thick polysilicon (T_{poly}). Extraction of the small-signal parameters are performed according to [3].

After validation of the SOI FinFET compact model, the static and RF performance of a Low Noise Amplifier (LNA) is simulated in SPICE. The important impact of the 3D extrinsic capacitances and gate resistance on LNA RF performance is clearly demonstrated.

II. Small-Signal equivalent circuit

Fig. 1 shows the FinFET equivalent-circuit, where the intrinsic elements C_{gsi}, C_{gdi}, C_{dsi}, g_{di} and g_{mi} are bias dependent, whereas extrinsic capacitances C_{gse}, C_{gde} and C_{dse} originate from the overlap between the source and drain regions and the thin gate oxide, and the fringing electric field between contacts. Also, the bias independent extrinsic series resistances R_{ge}, R_{se} and R_{de} are included.

According to [1], the impedance matrix is given by $Z_{\Sigma} = Z_e + Y_{\pi}^{-1}$, where the admittance matrix (Y_{π}) is:

$$Y_{\pi} = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ g_{mi} - j\omega C_{gd} & g_{di} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \quad (1)$$

where C_{gs}, C_{gd} and C_{ds} are the sum of the extrinsic and intrinsic capacitances as: $C_{gs} = C_{gsi} + C_{gse}$, $C_{gd} = C_{gdi} + C_{gde}$ and $C_{ds} = C_{sdi} + C_{dse}$ and Z_e is the extrinsic resistances matrix. Changes in technological parameters (e.g. oxide thickness) or bias conditions impose the need to execute the whole extraction of the small-signal equivalent circuit,

therefore a compact model becomes crucial to determine these parameters for any variation.

III. Small-Signal Model

The proposed methodology to correctly model the small-signal parameter of a SOI FinFET considers the three following steps: (A) matching between experimental I-V curves and the modeled drain current, here normalized charges at drain and source are determined, q_{nd} and q_{ns} respectively; (B) calculation of the 3D extrinsic capacitances including external fringing field effects as presented in [4]; (C) determination of the intrinsic capacitances using the normalized charges q_{nd} and q_{ns} which can be calculated and fitted with measured values after removing the calculated extrinsic capacitances. The complete small-signal compact model has been validated with available experimental data and also finite-element numerical simulations to cover a wide range of bias conditions and FinFET geometries.

A. Drain current model

Considering the first step, the drain current model has to match with experimental I-V curves and its expression is:

$$I_{DS} = I_0\left[\frac{q_{ns}^2 - q_{nd}^2}{2} + 2\left(q_{ns} - q_{nd}\right) - q_b \ln\left(\frac{q_{ns}+q_b}{q_{nd}+q_b}\right)\right] \quad (2)$$

where $I_0 = 2\mu_{eff}\phi_t^2 W/L\, C'_{ox}$, q_b is the normalized depleted charge, ϕ_t is the thermal voltage, C'_{ox} is the oxide capacitance per unit area and μ_{eff} is the effective mobility, which considers the effects of the lateral and transversal electric fields according to [1]. Fig. 2 (top) shows the comparison between the experimental and modeled transfer and output characteristics, whereas Fig. 2 (bottom) shows the comparison for the transconductance and conductance. Fair agreement is demonstrated in each case, where the total source-drain extrinsic resistance (R_{SD}) is included.

B. Extrinsic Capacitances (C_{gge})

Overlap and fringing field effects between the gate electrode and the silicon film are modeled by C_{gse} and C_{gde}. Those fringing capacitances include internal (C_{fint}) and external (C_{fext}) coupling fields. The external fringing capacitance is constant and originates from the 3D FinFET structure, whereas the internal fringing capacitance is bias dependent due to the charge variation in the channel close to the source or drain regions. A new semi-analytical model for the external capacitances has been developed [4] and is now implemented in SDDGM compact model. The external capacitance compact model takes into account the source/drain electrodes and has 5 components that describe the different electrical couplings in the structure by $C_{fext}=N_{fin}(C_1+C_2+C_3+C_4+C_5)$, where C_1 to C_5 are described in [4] and have dependence with FinFET geometry (L_{ext}, S_{fin}, W_{fin}, L, T_{poly} and H_{fin}). The internal fringing capacitances C_{fint} are taken into account as in [1].

C. Intrinsic Capacitances (C_{ggi})

Considering the normalized charges q_{nd} and q_{ns} calculated by the drain current model, analytical expressions for the intrinsic capacitances are obtained according to [1]. Hence, C_{gsi}, C_{gdi} and C_{sdi} are calculated and the total gate to gate capacitance is given by $C_{gg} = C_{gs} + C_{gd}$, where:

$$C_{gs} = C_{gsi} + \underbrace{C_{f\,\mathrm{int}} \cdot \left\{1 - \tanh\left[20\left(V_G - V_t\right)\right]\right\} + C_{fext}}_{C_{gse}} \quad (3)$$

$$C_{gd} = C_{gdi} + \underbrace{2C_{f\,\mathrm{int}} + C_{fext}}_{C_{gde}} \quad (4)$$

where V_t the threshold voltage. Fig. 3 shows the comparison between simulated and modeled capacitances at different bias conditions and a fair agreement is observed.

The mobility degradation, series resistances and recombination models were modulated to get a good matching between the measured I-V curves and the simulations. Also, modeled capacitances and measured ones are compared, and in order to extract the intrinsic parameters from the measured devices, it is necessary to remove R_{SD} and C_{gge} (= C_{gse} + C_{gde}) as described in [1]. Table I summarizes the obtained results.

IV. Low Noise Amplifier

In order to validate the small-signal model, a LNA is implemented in SPICE simulator. In Fig. 4 (left) the schematic view of the LNA and its measurement setup [5] are presented. Since a trans-impedance topology was chosen, high power consumption but wide band can be achieved, as well as no coils and no couplings are necessary, which allows focusing on the FinFET device behavior. V_{DD} is set to 1.2 V and the current consumption of the LNA is fixed close to 25 mA for both gate lengths. To fulfill the current consumption specification the total gate width of the transistors composing the LNA are W_{M1} = 2,325 μm and W_{M2} = 273 μm for the 500 nm-gate length FinFETs, whereas they are W_{M1} = 5,014 μm and W_{M2} = 3,326 μm for the 250 nm-long FinFETs.

Fig. 4 (right) shows the simulated associated power gain for the two channel lengths, where a comparable maximum gain is obtained in both cases. The gate resistance R_{ge} is taken into account in these simulations through the Wu's model [6]. It is worth to point out that the cut-off frequency of the simulated LNA circuit (f_{C_LNA}) is slightly higher for the LNA with shorter gate length FinFET (250 nm). Additionally, Fig. 4 (right) shows the power gain of experimental SOI 75 nm-long FinFET LNA circuit reported by Knoblinger [5]. The f_{C_LNA} of their LNA is only slightly higher than our simulated values for

much longer FinFET channel length. This observed saturation of the LNA cut-off frequency is related to the excess of parasitic capacitances which are relatively more important for shorter devices as was demonstrated in [3].

In order to evaluate the degradation coming from the external capacitances on the LNA behavior, 250 nm-FinFET LNA is simulated in neglecting C_{fext}. Fig. 4 (right) depicts the result of this simulation, where higher f_{C_LNA} as well as power gain are obtained. Additionally, considering the other parasitic extrinsic effects that degrade the RF performance, simulations with R_{ge} reduced by a factor 2 and 5 are made. This artificial reduction of the parasitic elements allows us to simulate the intrinsic performance of the LNA. As a consequence, the minimization of C_{fext} and R_{ge} becomes mandatory in order to achieve higher f_{C_LNA} and gain.

V. Conclusions

An extended Verilog-A implementation of the SDDGM compact model for SOI FinFETs in a SPICE simulator is presented. Fair agreement with dc characteristics as well as with extracted small-signal intrinsic parameters of modeled and measured RF SOI FinFETs is demonstrated. Simulated RF performance of LNA based on a FinFET technology show good agreement with measured data presented in the literature. This methodology provides an efficient way to determine the analog and RF performance of SOI FinFET RF circuits.

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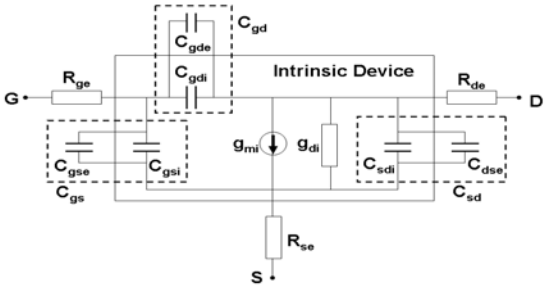

Fig. 1. Small-signal equivalent circuit model of SOI FinFET.

Table I. Comparison of the small-signal parameters predicted by the model and extracted from wideband S-parameters measurements [1].

	Model		Measurements	
Gate length	500 nm	250 nm	500 nm	250 nm
g_{mi} / g_{di} (mS)	23/0.72	40/1.1	24.7/0.81	34.3/2.8
C_{gsi} / C_{gdi} (fF)	353/17.1	160/12	360.1/17.3	152.6/8
f_T (GHz)	9.88	37	10.4	34

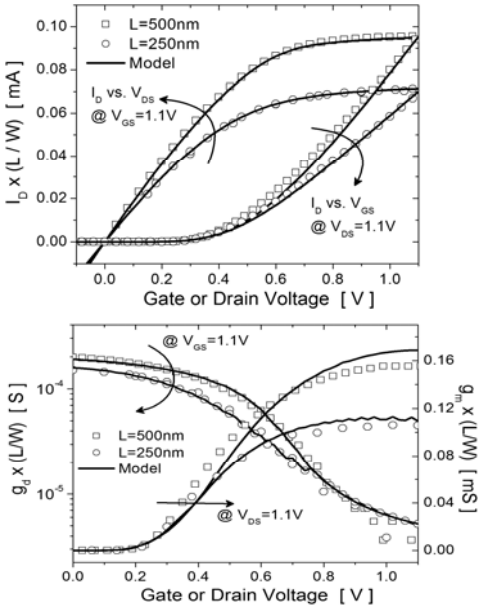

Fig. 2. I-V characteristics (top) as well as transconductance and conductance (bottom).

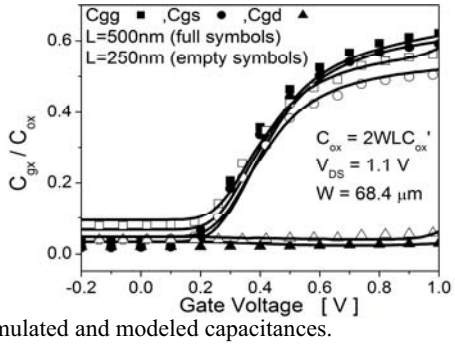

Fig. 3. Simulated and modeled capacitances.

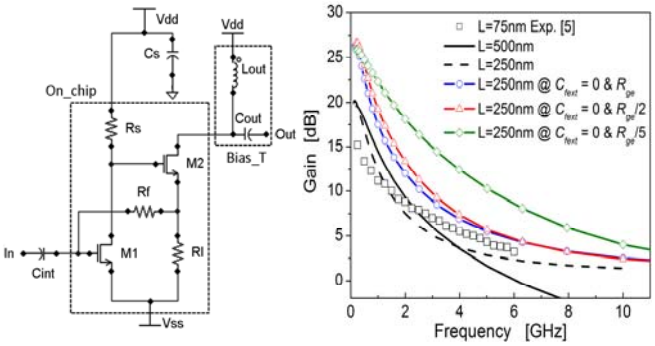

Fig. 4. Schematic of the LNA and its measurements setup (left). Simulated power gain of LNA (right).