Fringing Gate Capacitance Model for Triple-Gate FinFET

S. Salas[1], J. C. Tinoco[2], A. G. Martinez-Lopez[1], J. Alvarado[3] and J.-P. Raskin[4]

[1] Centro de Investigación en Micro y Nanotecnología, Universidad Veracruzana, Veracruz, México
[2] Depto. de Ing. en Telecomunicaciones, Facultad de Ingeniería UNAM, México D.F.
[3] Centro de Investigación en Semiconductores, BUAP, Puebla, Mexico
[4] Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, Louvain-la-Neuve, Belgium

***Abstract* — In this paper, a semi-analytical extrinsic gate capacitance model for Triple Gate FinFET, based on three-dimensional numerical simulations, is presented. The model takes into account the source/drain electrode and contact areas. It includes 5 capacitance components that describe the different fringing electrical couplings that exist inside the FinFET structure. The semi-analytical model accurately calculates the total extrinsic gate capacitance as function of the main geometrical parameters of Triple-Gate FinFET.**

***Index Terms* — FinFETs, Extrinsic Capacitance, Fringing Gate Capacitance, Fringing Electric Field.**

I. Introduction

These last years, FinFET has demonstrated to be a promising candidate to pursue the downscaling of CMOS technology, thanks to their superior control of the short channel effects (SCE). Very recently, an Intel microprocessor based on the 22-nm node FinFET technology has been successfully fabricated [1]. Nowadays, FinFET is not anymore a scientific curiosity but a technology of choice on the semiconductor market. Nevertheless, due to their three-dimensional (3-D) structure, FinFETs show high parasitic resistances and capacitances which lead to strong degradation of their analog and RF performance [2]-[3]. Thus, there is still room for improvement and especially concerning the reduction of the total extrinsic gate capacitance (C_{gge}).

The RF model of FinFETs is made based on the well-known small-signal equivalent circuit (SS-EC) and implies the accurate determination of all the intrinsic and extrinsic parameters. In this context, a compact model with the aim to determine the DC and intrinsic RF parameters was demonstrated [4]. In order to provide high-quality SS-EC, there is an urgent need to accurately model the extrinsic capacitances which are strongly dependent on the FinFET geometry. Recently, Wu and Chan [2] developed a semi-analytical model to describe total extrinsic gate capacitance of double-gate FinFETs. Fig. 1a shows a schematic representation of the structure used and identifies the main FinFET geometrical parameters. Three capacitance components associated to the FinFET structure were considered, as Figs. 1b to 1d show: (i) C_1 is the capacitance component from the top of the gate electrode to the top of the source/drain (S/D) fin extension; (ii) C_2 is the capacitance component from the side of the gate electrode to the top of the S/D fin extension and (iii) C_3 is the capacitance from the side of the gate electrode to the internal side of the S/D fin extension. In the Wu's model, the S/D electrode regions are not considered and thus some important parasitic capacitances are not modeled while they are not negligible.

In this paper, based on 3-D numerical simulations, a semi-analytical model for the extrinsic gate capacitances of Triple-Gate FinFETs is presented. This model includes the S/D electrode and contact areas in order to overcome the limitations of previous models and thus provide a complete and accurate modeling of the total extrinsic gate capacitance valid for a wide range of FinFET geometries.

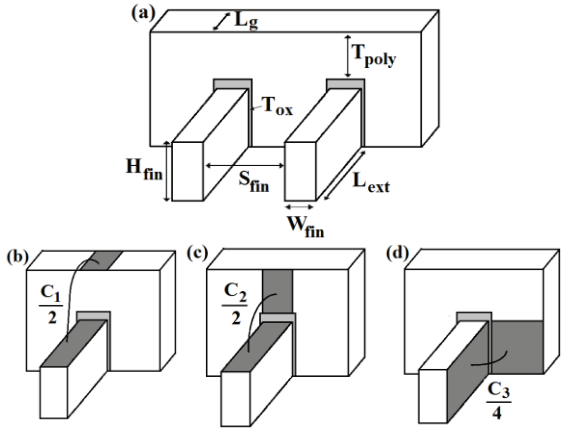


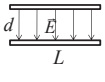
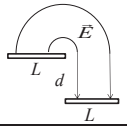
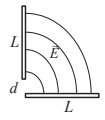
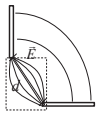
Fig. 1. (a) FinFET schematic representation used in the Wu´s model [2]. (b), (c) and (d) schematic representations of the different capacitance components associated to the 3-D structure.

II. The Compact Model

In the 3-D FinFET structure we can identify some typical capacitor structures, as shown in Table I [5]: (i) parallel-plate capacitor, (ii) perpendicular-plate capacitor, (iii) flat-plate non-parallel capacitor, and (iv) fringing field capacitive component.

Including the S/D contact areas and based on the classical capacitance formulations presented in Table I, we propose a compact model with five extrinsic capacitance components as illustrated in Fig. 2.

TABLE I
SIMPLE CAPACITANCE EXPRESSIONS

Structure	Expression	Structure	Expression
	(i) $C = \varepsilon \frac{L}{d}$		(iii) $C = \frac{\varepsilon}{\pi} ln\left(1+\frac{L}{d}\right)$
	(ii) $C = \frac{2\varepsilon}{\pi} ln\left(1+\frac{L}{d}\right)$		(iv) $C_{fr} = \frac{\varepsilon}{2\pi} ln\left(\frac{\pi l}{d}\right)$

C_1 component (Fig. 2a) can be represented as flat-plate non-parallel structure. It exhibits dependence with L_g, L_{ext}, W_{fin}, T_{poly}, and T_{ox}, and can be expressed as:

$$C_1 = \frac{\varepsilon_{ox}}{\pi} W_{fin}^{\alpha 1} L_{ext}^{\alpha 2} \left(a_1 - a_2 T_{poly}^{\alpha 3}\right) \ln\left(1+\frac{0.5L_g}{T_{poly}+T_{ox}}\right) \ln\left(1+\frac{L_{ext}}{T_{ox}}\right) \quad (1)$$

where a_1, a_2, $\alpha 1$ $\alpha 2$ and $\alpha 3$ are fitting parameters.

Similarly, Fig. 2b shows that C_2 can be represented as perpendicular-plate structure and exhibits dependences with T_{poly}, T_{ox}, L_{ext} and W_{fin}.

$$C_2 = \frac{2\varepsilon_{ox}}{\pi} W_{fin}^{\beta 1} \left\{ b_1 T_{poly}^{\beta 2} \ln\left(1+\frac{L_{ext}}{T_{ox}}\right) \ln\left(1+\frac{T_{poly}}{T_{ox}}\right) + W_{fin}\left(b_2 + b_3 \exp\left(-\frac{T_{poly}}{b_4}\right)\right) \ln\left(\frac{\pi W_{fin}}{T_{ox}}\right) \right\} \quad (2)$$

where b_1, b_2, b_3, b_4, $\beta 1$ and $\beta 2$ are fitting parameters.

C_3 component has to be divided in two parts when the S/D contact area is considered, as Fig. 2c shows: (i) the C_{3a} which is the same that was considered in the Wu´s model and (ii) a new C_{3b} component which corresponds to the direct coupling between the side of the gate electrode and the internal side of the S/D contact region like a parallel-plate capacitor. Thus, C_3 can be expressed as $C_3 = C_{3a} + C_{3b}$, where:

$$C_{3a} = \frac{4\varepsilon_{ox}}{\pi} H_{fin}^{\gamma 1} \left\{ \begin{array}{l} \left(d_1 S_{fin}^{\gamma 2} + d_2\right) \ln\left(1+\frac{L_{ext}}{T_{ox}}\right) \ln\left(1+\frac{0.5S_{fin}-T_{ox}}{T_{ox}}\right) + \\ \left(d_3 S_{fin}^{\gamma 3} + d_4\right) \ln\left(\frac{\pi H_{fin}}{T_{ox}}\right) \end{array} \right\} \quad (3)$$

$$C_{3b} = \frac{4\varepsilon_{ox}}{\pi} \left[0.66\pi H_{fin}^{\gamma 1} \left(\frac{0.5S_{fin}-T_{ox}}{L_{ext}}\right) \left(d_5 S_{fin}^{\gamma 4} + d_6\right) + d_7 \right] \quad (4)$$

where d_1-d_7 and $\gamma 1$-$\gamma 4$are fitting parameters.

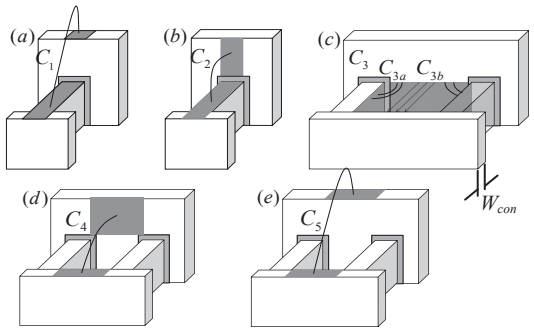


Fig. 2. Schematic representations of the five capacitance components, C_1-C_5, considered in our proposed compact model.

Additionally, two new capacitance components C_4 and C_5 appear, when the S/D contact region is included as shown in Figs. 2d and 2e. C_4 corresponds to the capacitance from the side of the gate electrode located above the fin spacing and the top of the S/D contact region. This component corresponds to a perpendicular-plate capacitor with also a fringing component from the S/D contact edge and the gate electrode, and exhibits dependences with of T_{poly}, L_{ext}, S_{fin} and W_{con}. Thus, C_4 can be expressed as:

$$C_4 = \frac{2\varepsilon_{ox}}{\pi} S_{fin}^{\tau 1} \left(t_1 + t_2 exp\left(-\frac{T_{poly}}{t_3}\right)\right) \left(ln\left(1+\frac{W_{con}}{L_{ext}}\right) ln\left(1+\frac{T_{poly}}{T_{ox}}\right)\right) + \frac{\varepsilon_{ox}}{\pi-2} ln\left(\frac{\pi}{2}\right) S_{fin}^{\tau 1} \left(t_4 + t_5 exp\left(-\frac{T_{poly}}{t_6}\right)\right) \quad (5)$$

where $\tau 1$, t_1, t_2, t_3, t_4, t_5 and t_6 are fitting parameters.

The last capacitance component to be considered is C_5, which corresponds to the capacitance from the top of the gate electrode to the top the S/D contact region. This component corresponds to a flat-plate non-parallel capacitor with also a fringing component from the edge of the gate electrode to the S/D contact region and exhibits dependences with L_{fin}, L_{ext}, S_{fin} and W_{con}. Thus, C_5 can be expressed as:

$$C_5 = 1.5 \frac{\varepsilon_{ox}}{\pi} S_{fin}^{\varphi 1} \left(f_1 + f_2 L_{ext}^{\varphi 2}\right) \left(ln\left(1+\frac{0.5L_g}{\sqrt{\left(T_{poly}+T_{ox}\right)^2 + \left(L_{ext}\right)^2}}\right) \right) \times \left(ln\left(1+\frac{W_{con}}{\sqrt{\left(T_{poly}+T_{ox}\right)^2 + \left(L_{ext}\right)^2}}\right) \right) \quad (6)$$

where f_1, f_2, $\varphi 1$and $\varphi 2$ are fitting parameters.

Finally, because RF transistors consist of multi-fin devices, the total gate capacitance per gate finger is defined by the sum of the whole components expressed by (1)-(6) as:

$$C_{gge}=2N_{fin}\left(C_1+C_2+C_3+C_4+C_5\right) \quad (7)$$

where N_{fin} is the number of fins.

III. Simulations

3-D finite-element numerical simulations were performed in order to verify the developed semi-analytical compact model as well as to determine the values of the fitting parameters. Simple structures were used to analyze each capacitance component, finally the full FinFET structure was used to verify the total gate capacitance. Table II summarizes the obtained fitting parameters.

IV. Results

Figs. 3a and 3b show the comparison between the total extrinsic gate capacitance C_{gge} obtained from the compact model and from numerical simulations vs. L_{ext} and H_{fin}, respectively, and for various S_{fin} values.

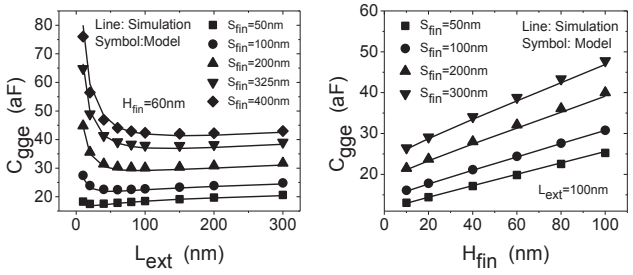


Fig. 3. (a) C_{gge} vs L_{ext} and (b) C_{gge} vs H_{fin}; for various S_{fin} and T_{poly} = 100 nm, T_{ox} = 2 nm, L_g = 40 nm, W_{fin} = 50 nm and W_{con} = 50 nm.

Figs. 4a and 4b show the comparison between C_{gge} calculated with the compact model and results from the numerical simulations vs. W_{fin} and L_g, respectively, and for various S_{fin} values.

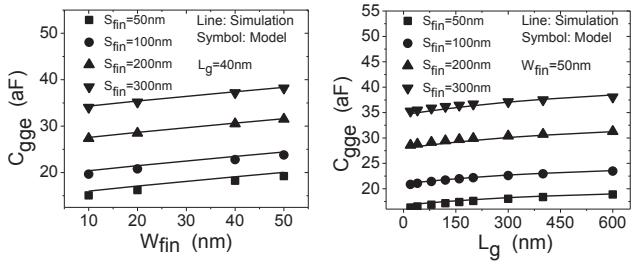


Fig. 4. (a) C_{gge} vs W_{fin} and (b) C_{gge} vs L_g; for various S_{fin} and T_{poly} = 100 nm, T_{ox} = 2 nm, H_{fin} = 60 nm, L_{ext} = 100 nm and W_{con} = 50 nm.

V. Conclusions

A semi-analytical model for extrinsic gate capacitance of Triple-Gate FinFET is presented. The model considers the S/D contact region and includes five capacitance components. It is based on simple capacitor structures and describes the dependences with the main geometrical FinFET parameters: L_{ext}, W_{con}, S_{fin}, W_{fin}, L_{fin} and H_{fin}. The compact model has been validated for a wide range of FinFETs dimensions. Simulation results show optimization paths to decrease the impact of extrinsic capacitances, such as the reduction of fin spacing S_{fin}, the S/D fin extension L_{ext} as well as by increasing the fin aspect ratio (H_{fin}/W_{fin}). The proposed compact model is of great interest for designers considering FinFET technology for high-speed digital and RF applications.

TABLE II
Summary of Fitting Parameters

Parameter	Value	Parameter	Value
a_1	2.54	$\gamma 3$	0.96
a_2	2.26×10^{-8}	$\gamma 4$	-0.67
$\alpha 1$	0.44	t_1	4.06×10^{-3}
$\alpha 2$	0.64	t_2	6.41×10^{-3}
$\alpha 3$	- 1.07	t_3	211.4×10^{-9}
b_1	0.236	t_4	0.154
b_2	80.12	t_5	- 0.09
b_3	2.54×10^{3}	t_6	121.53×10^{-9}
b_4	82.35×10^{-9}	$\tau 1$	0.757
$\beta 1$	0.42	f_1	6.95×10^{-5}
$\beta 2$	0.55	f_2	22.05
$\gamma 1$	0.84	$\varphi 1$	0.336
$\gamma 2$	0.32	$\varphi 2$	0.834
d_1	$6.03 - 4.95\times10^{6}\ (0.5S_{fin} - T_{ox})$		
d_2	$16\times10^{3}\ (0.5S_{fin} - T_{ox})$-0.019		
d_3	$4.03\times10^{10}\ (0.5S_{fin} - T_{ox})$-$4.9\times10^{4}$		
d_4	$0.079-6.46\times10^{4}\ (0.5S_{fin} - T_{ox})$		
d_5	$0.44(0.5S_{fin} - T_{ox})-5.635\times10^{-7}$		
d_6	$0.077-6.27\times10^{3}\ (0.5S_{fin} - T_{ox})$		
d_7	$1.05\ (0.5S_{fin} - T_{ox})+3.94\times10^{-8}$		

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References

[1] M. Bohr and K. Mistry, "INTEL´s revolutionary 22-nm Transistor Technology", 2011, www.intel.com.

[2] W. Wu and M. Chan, "Analysis of geometry-dependent parasitics in multifin Double-Gate FinFETs", *IEEE TED*, vol. 54, no. 4, pp. 692-698, April 2007.

[3] J. C. Tinoco *et al*., "Impact of extrinsic capacitances on FinFETs RF performance", *SiRF 2012*, pp. 73-76.

[4] J. Alvarado *et al.* "Compact Small-Signal Model for RF FinFETs", *ICCDCS 2012*.

[5] D. Goren, "On-chip interconnect-aware design and modeling methodology, based on high bandwidth transmission line devices", *DAC 2003,* pp. 724-727.