Engineered substrates: The foundation to meet current and future RF requirements

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***Abstract* — The increasing demand for wireless data bandwidth and the rapid adoption of LTE and LTE Advanced standards push radio-frequency (RF) IC designers to develop devices with higher levels of integrated RF functions, meeting more and more stringent specification levels. The substrates on which those devices are manufactured play a major role in achieving that level of performance [1]. In this paper, Soitec and UCL explain the value of using RF-SOI substrates and more especially the new generation of Soitec widely adopted eSI™ (enhanced Signal Integrity) substrate to achieve the RF IC performance requested to address the LTE Advanced smart phone market.**

***Index Terms* — Silicon-on-Insulator (SOI), high resistivity Si substrate, trap-rich layer, high frequency, wireless applications, LTE.**

I. Introduction

Growing usage of multimedia applications associated with consumers' desire for ultimate mobility experience has created significant market changes:

i. More mobile devices: The number of smart phones will grow at a compound annual growth rate (CAGR) of 12.7 percent between 2013 and 2018 (Source: IDC [2]).
ii. More mobile users: The number of mobile subscriptions worldwide exceeds world population since 2014 and will reach 9.2 billion by 2019. More than 65% of the world population will be covered by LTE in 2019 versus 25% today (Source: Ericsson [3]).
iii. More multimedia applications: Driven by video streaming, TV, social media and content sharing, etc., data traffic continues to grow at a 61%CAGR (Fig. 1 [4]).

To respond to this data traffic demand, faster mobile throughput is required. Carrier Aggregation (CA) of bands and multi input multi output (MIMO) techniques are the main hardware techniques in handset to increase capacity. For example, in LTE Release 8, theoretical maximum data rate with 20 MHz bandwidth is 150 Mbs download / 50 Mbs upload. In LTE Release 12, theoretical maximum data rate with 3x20 MHz bandwidth is 1.2 Gbs download with 4x4 MIMO and 0.6 Gbs upload with 2x2 MIMO.

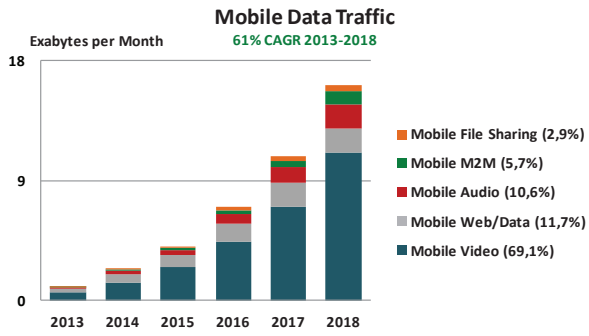

Fig. 1. Cisco VNI Mobile, February 2014 [4].

Common flagship devices are today using carrier aggregation in receive mode with 4 receivers (MIMO received on) and one transmitter operating simultaneously. Most stringent linearity requirements are then required on most critical Front End Module blocks such as main antenna switches, swapping switches, antenna tuners. IIP3 requirements up to 90 dBm are foreseen to handle some specific cases (Table 1). For example, carrier aggregation of Band 17 & 4 when Band 17 Tx third harmonic fall into Band 4 Receive.

To address high volume market at competitive cost and meet linearity requirements demand, since 1992 Soitec and UCL has been cooperating to enable a standard CMOS compatible silicon wafer with nearly perfect RF performance: RF Silicon-on-Insulator (RF-SOI).

978-1-4799-7375-0/15/$31.00 ©2015 IEEE

Network	Linearity (IIP3 in dBm)
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90

Table 1. Intel Mobile, "Challenges for Radios due to Carrier Aggregation requirements", Larry Schumacher, Nov. 2012 [5].

II. RF-SOI SUBSTRATE – BEST PERFORMANCE-COST TRADE-OFF

RF-SOI foundries are constantly improving devices performance. A typical figure of merit used for switches is Ron x Coff. We have seen 20% Ron x Coff performance improvement per year for the last 8 years.

The main challenges for RF SOI substrate is to reduce its contribution to the non-linear behaviour of the RF IC compared with an ideal substrate (fully dielectric). When measuring the same RF IC onto different substrates from ideal to very nonlinear substrates, substrate target specifications must fall into the "IC limited" zone (Fig. 2).

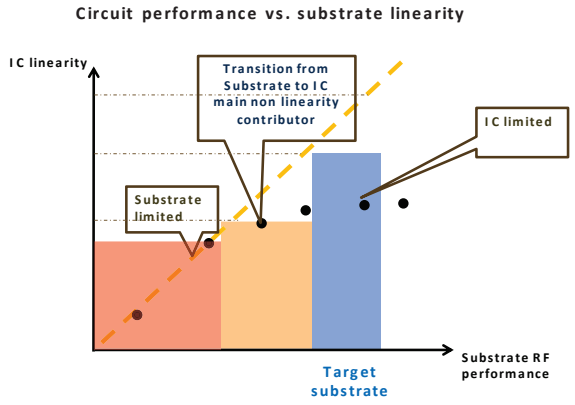

Fig. 2. Circuit performance versus substrate non-linearity.

Since 2008, by offering the best cost, area and performance to the market, RF-SOI has progressively displaced GaAs and Silicon-on-Sapphire technologies, becoming the mainstream technology for antenna switch with more than 85% market share (Yole, February 2014, [6]), being available in all foundries.

RF-SOI wafers share the same challenges as the circuits and devices to meet IIP3 requirements: never be the limiting performance factor.

Beyond performance, RF-SOI offers a unique advantage to further reduce board area by integrating all front end module devices on the same die.

III. ESI SUBSTRATE PERFORMANCE

In 1997, UCL presented pioneering work on the RF performance of high-resistivity (HR) SOI substrate material. The great interest of HR SOI substrate to reduce RF losses as well as crosstalk in Si-based substrates was demonstrated [7]. It has been demonstrated in [8] that HR-Si must present an effective resistivity as high as 3 kΩ.cm to be considered low loss for RF applications. However, oxidized HR-Si substrate suffers from parasitic surface conduction (PSC) due to fixed oxide charges which attract free carriers near the Si/SiO_2 interface, thereby reducing the substrate effective resistivity (ρ_{eff}) of the wafer by more than one order of magnitude compared with the bulk nominal resistivity.

In 2005, UCL presented the possibility of creating HR SOI substrates characterized with an effective resistivity as high as 10 kΩ.cm (Fig. 3) thanks to the silicon surface modification below the buried oxide (BOX) of a high resistivity SOI substrate. The surface modification consists in the introduction of a high density of defects called traps at the BOX / HR-Si handle substrate [9]. Those traps originate from the grain boundaries in a thin (300 nm-thick) polysilicon layer. This high-resistivity characteristic, which is conserved after a full CMOS process, translates to very low RF insertion loss (< 0.15 dB/mm at 1 GHz) along coplanar waveguide (CPW) transmission lines and purely capacitive crosstalk (Fig. 4) similarly to quartz substrate.

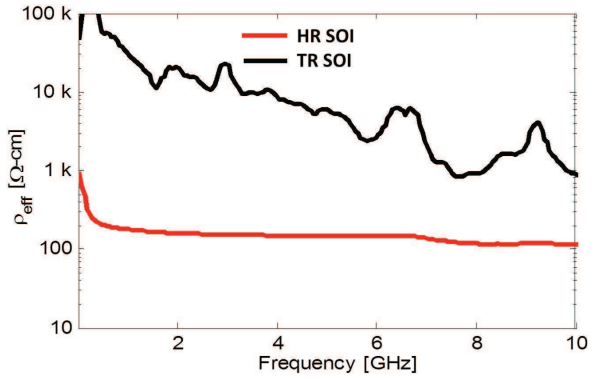

Fig. 3. Measured effective resistivity of a high-resistivity SOI substrate (HR SOI) and a trap-rich (TR SOI, i.e. eSI TR-SOI from Soitec) HR SOI substrate presenting both of them a handle Si substrate characterized by a nominal resistivity of 10 kΩ.cm. While TR SOI presents an effective resistivity of around 10 kΩ.cm, the value of the HR SOI without traps is actually only of 200 Ω.cm.

It has been demonstrated that the presence of a trapping layer does not alter the DC or RF behavior of SOI MOS transistors [10]. Besides the insertion loss issue along interconnection lines, the generation of harmonics in the Si-based substrates has been investigated [11]. UCL demonstrated that harmonics level originated from the

substrate is reduced by at least 20 dB moving from standard resistivity SOI substrate (~ 10 Ω.cm) to high resistivity SOI (~ 1 kΩ.cm), and more importantly an additional drop of 40 dB is achieved with the innovative trap-rich HR SOI (TR SOI) substrate, as illustrated in Fig. 5. This low harmonic level is comparable with insulating substrate. The improvement of the HR SOI substrate with the introduction of defects brings also clear benefits for the integration of passives, such as the quality factor of spiral inductors [12], tunable MEMS capacitors [12], as well as for the reduction of the substrate noise (crosstalk) between devices integrated on the same chip (Fig. 6).

Fig. 7 presents the noise signal amplitude recorded at the drain electrode of the transistor when the injected noise signal frequency varies from 500 kHz up to 50 MHz and a dc voltage of 0 or -10 V is applied on the noise signal pad. A deep depletion is formed under the BOX when a negative dc bias is added to the clock frequency, therefore the coupled noise decreases by 10 dB comparing with its level at 0 V for HR-SOI substrate whereas there is no change for eSI TR-SOI.

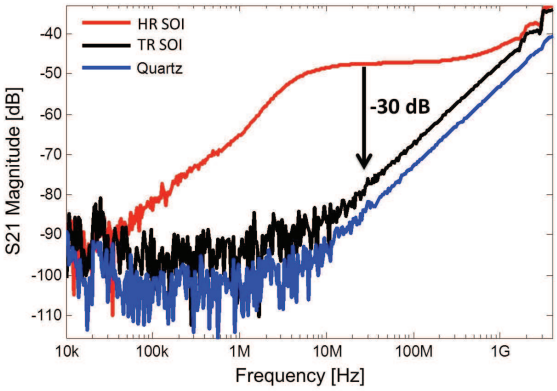

Fig. 4. Measured crosstalk response for the basic test structure on quartz and HR based-Si substrates with (TR SOI, i.e. eSI TR-SOI from Soitec) and without (HR SOI) 300 nm-thick polysilicon trap-rich layer. The distance *d* between the disturbing input and the output device is 50 µm.

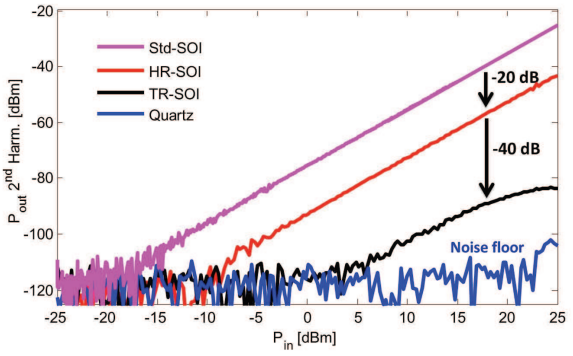

Fig. 5. Measured harmonic distortion along a CPW line lying on standard SOI (~ 10 Ω.cm) and HR based-Si substrates (~ 10 kΩ.cm) with (TR SOI, i.e. eSI TR-SOI from Soitec) and without (HR SOI) trap-rich layer. Identical CPW transmission line has been measured on top of a quartz substrate to quantify the harmonic measurement noise floor.

UCL and Soitec have been working together to identify the technological opportunities to still further improve the high-frequency performance of commercially available HR-SOI substrates. Thanks to the introduction of an engineering substrate handle based on the Prof. Raskin's discovery, Soitec has ramped up in early 2012 a new flavor of HR-SOI called eSI™, for enhanced Signal Integrity substrate with a measured effective resistivity beyond 3 kΩ.cm. Thanks to the introduction of eSI, the RF SOI substrate can really be considered as a lossless Si-based substrate. Beyond switch, eSI RF-SOI technology opens the path to further system integration in the Front End Module space as well as even more complex mixed signal System-on-Chip (SoC) [13]. In February 2014, Qualcomm has announced the first smart phone having adopted its RF360 solution. Qualcomm unveiled that their "RF360 is based on CMOS and SOI technology". As pointed out by several press releases published this year, the demand for the newly developed HR-SOI is booming and it is becoming the major material for high-performance RF applications. All major foundries in the field of RF applications have adopted the newly developed HR SOI substrate.

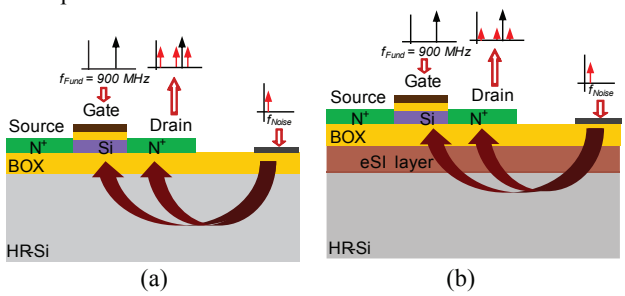

Fig. 6. Substrate noise reduction test

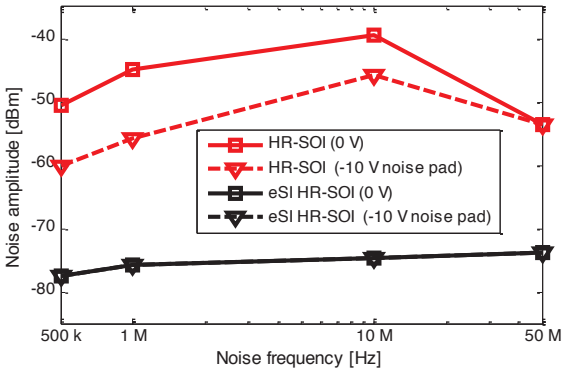

Fig. 7. Cross-section of FD SOI MOSFET with noise pad on a (a) HR-SOI and (b) eSI TR-SOI wafer, (c) Power levels recorded at the transistor drain electrode when biased in saturation and lying on either

HR-SOI or eSI TR-SOI wafers when a noise signal is fed into the noise pad and no RF signal is applied to the gate.

The linearity performance of eSI wafers provided by Soitec is presented in Fig. 8 for the first and new substrate generation namely eSI90.

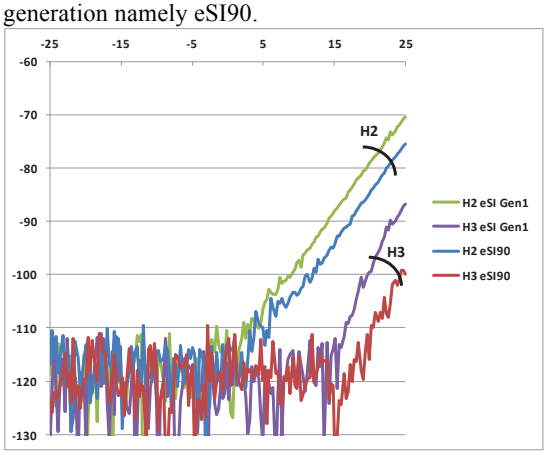

Fig. 8. Linearity performance of commercially available eSi substrates from Soitec.

New generation eSI products meet required specifications in terms of losses, coupling and non-linearities to push further the RF ICs performance limit.

IV. Next Challenges Served by SOI

Pushed by still more data demanding video applications, linearity requirements will continue to be even more stringent, dual carrier upload being the next technological implementation driving current substrate innovations. Beyond its demonstrated market adoption on RF Front End Module, RF-SOI is close to be in 100% of the worldwide smart phone. In parallel, digital Fully Depleted SOI (FD-SOI) is also being adopted by bringing the best cost-performance trade-off at 28 nm and beyond for mobile digital devices such as application processors. It offers up to 10x lower consumption compared with standard bulk CMOS thanks to its capability to operate at much lower supply voltage and lower biasing current for equivalent processing performance. Combining advanced CMOS process with optimized SOI substrate will enable RF and digital integration for advanced SoC integration. SOI is then very well positioned to serve future 5G standards and IoT applications such as wearables that will respectively run on higher bands than today's 4G and will require drastic power consumption reduction.

Acknowledgement

The authors wish to acknowledge Didier Basso, Laurent Marinier, Cédric Malaquin, Christophe Didier and Communication & Power Product Engineering teams of Soitec for their strong support.

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