Self-Heating in 28 nm Bulk and FDSOI

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1. Abstract

In this work self-heating and its effect on device parameters are compared in 28 nm technology bulk and FDSOI MOS devices. It is found that the thermal resistance is ~3.4 times higher and the temperature rise is ~2.5 times higher in FDSOI than in bulk. However, in spite of stronger self-heating, FDSOI devices outperform bulk over a wide frequency range. Moreover, device parameters degradation with temperature is attenuated in FDSOI transistors.

2. Introduction

FDSOI and bulk technologies are two competing approaches to the planar CMOS process at the 28 nm node. FDSOI offers better control of short channel effects, improved variability due to the absence of doping and a possibility of dynamic threshold voltage using a ground plane. However, FDSOI imposes very strict requirements on Si layer thickness uniformity thus increasing the cost of starting wafers. In addition, the standard CMOS process has to be somewhat adapted to be compatible with FDSOI technology. Though, these adaptations are minimal. In turn, bulk technology has been in development for several decades and is standard for the semiconductor industry. However, the bulk technology is close to its limit due to short channel effects.

Improved performance, higher speed and lower power consumption in FDSOI devices were demonstrated in [1]. Many FDSOI-specific issues such as process adaptation, models and design libraries were successfully solved during the last years [2]. The only technological concern which has not been addressed yet is self-heating which is expected to be stronger in FDSOI than in bulk.

Indeed, both technologies are expected to induce self-heating due to geometrical confinement and high power densities in short transistors. Self-heating in FDSOI is expected to be aggravated due to thin Si film with poorer thermal properties than Si bulk and by a presence of the buried oxide (BOX) that limits removal of the Joule heat from the device channel to the substrate. However, in a MOSFET several thermal paths exist and their relative importance to heat dissipation is an open question. Therefore, this work is focused on comparison of self-heating in bulk and FDSOI devices, a timely issue for designers and compact model developers.

3. Experimental Details

Devices studied in this work come from 28LP and 28FDSOI processes by STMicroelectronics. Bulk and FDSOI MOSFETs with gate lengths L_g from 30 to 150 nm were studied in this work. More details on the process can be found in [1]. Bulk devices feature a thin SiGe layer for performance enhancement.

Measured transfer characteristics of the studied FDSOI and bulk devices are plotted in Fig. 1 in linear and saturation regimes.

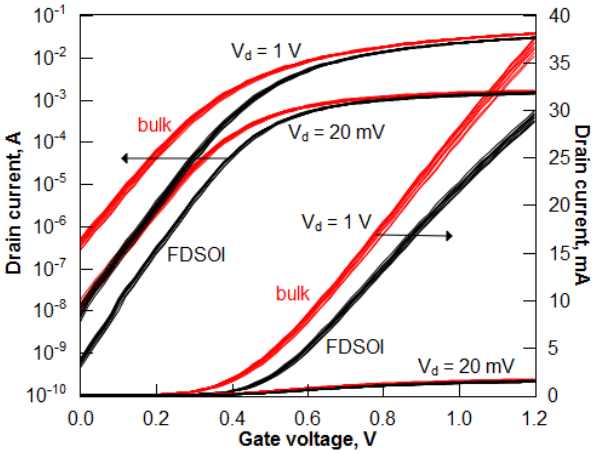


Fig. 1: *Transfer characteristics of the studied bulk and FDSOI MOSFETs in linear (V_d = 20 mV) and saturation regimes (V_d = 1 V).*

Self-heating was characterised using the RF method [3]. Due to finite thermal capacitance of a transistor, the self-heating effect is frequency dependent. An increase of frequency results in suppression of dynamic self-heating. Therefore, at a certain frequency, device temperature ceases to follow voltage oscillations and only static self-heating remains. The output conductance difference at this frequency and at low frequency can be linked to the device thermal resistance and hence its average temperature rise. In order to extract the self-heating figures of merit, S-parameters must be measured in a wide frequency range, converted to Y-parameters and de-embedded using open structures. In addition to S-parameters, complementary current-voltage measurements at different ambient temperatures are required. The thermal resistance is then extracted as [4]:

$$R_{th} = \frac{\Delta g_d}{(I_d + V_d g_{dT}) \partial I_d / \partial T}, \quad (1)$$

where Δg_d is the output conductance difference at low and at high frequencies, g_{dT} is the output conductance at

high frequency, V_d is the drain voltage, I_d is the drain current and $\partial I_d/\partial T$ is the drain current dependence on the ambient temperature obtained from hot-chuck measurements.

4. Results and Discussion

4.1. Self-heating parameters

The thermal resistance R_{th} was extracted in bulk and FDSOI devices. It is plotted in Fig. 2 and benchmarked against experimental data for various technologies [5]–[8] as a function of the gate length. The benchmarked technologies are UTB and UTBB devices with various BOX thicknesses as well as 28 nm FDSOI and bulk devices. The main parameters of the compared devices are listed in Table 1. As seen from Fig. 2, R_{th} in bulk devices is lower than in FDSOI even in FDSOI devices of longer L_g up to 228 nm. This can be attributed to enhanced heat removal from the channel to the substrate in bulk devices compared with FDSOI. In FDSOI, BOX with low thermal conductivity impedes effective heat dissipation. Furthermore, thermal conduction in the thin Si film is two orders of magnitude lower than in bulk Si [9]. R_{th} in the bulk devices is lower than in any of benchmarked SOI devices. The temperature rise due to self-heating at V_g and V_d of 1 V is ~32 K in bulk and ~87 K in FDSOI.

Fig. 3 shows the frequency dependence of the absolute values of $1/\mathrm{Imag}(Z_{th})/\omega$, which expresses the effective thermal capacitance C_{th}, where ω is the angular frequency. Larger C_{th} in bulk can be attributed to bigger silicon volume available for the generated heat storage.

Table 1: *Key parameters of the devices compared in Fig. 2.*

Symb.	Technology	Ref.	t_{BOX}, nm	t_{Si}, nm
□	UTBB	[5]	10	8
+	UTBB	[6]	25	7.5
×	UTBB	[6]	10	7
○	UTB	[7]	145	10
✳	28 nm FDSOI	[8]	25	7
△	28 nm FDSOI	this work	25	7
△	28 nm bulk	this work	-	-

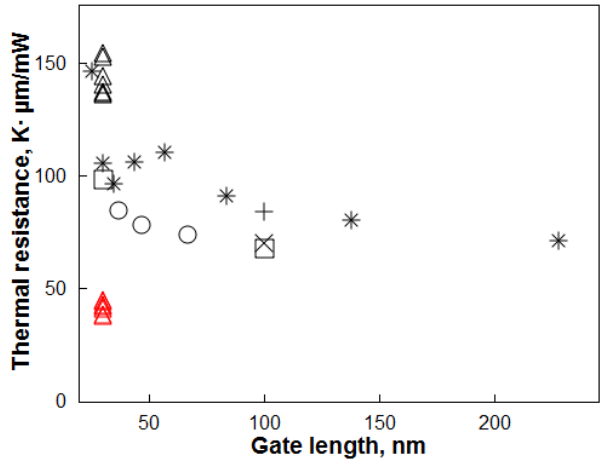


Fig. 2: *Thermal resistance in devices of various technologies. Device details are listed in Table 1.*

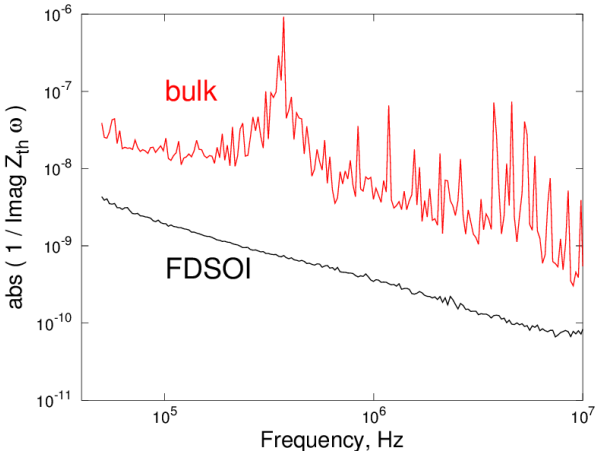


Fig. 3: *Absolute values of the equivalent thermal capacitance $1/\mathrm{Imag}(Z_{th})/\omega$ as a function of frequency.*

4.2. Effect of self-heating on device performance

Self-heating is frequency dependent due to finite R_{th} and C_{th} of a device. This results in the frequency dependence of the transconductance g_m and output conductance g_d. Their variations in the range from 50 kHz to 4 GHz are shown in Fig. 4 and Fig. 5. The data are shown as measured (non-normalised) and normalised to their value at 50 kHz in order to emphasise the effect of frequency variation. Slightly higher g_m in bulk devices (Fig. 4) can be due to a thin SiGe layer employed to boost the performance, a smaller series resistance R_{sd} or interface effects. Mobility boosters are also employed in the next FDSOI nodes. Better control of short channel effects in FDSOI results in reduced g_d compared with bulk (Fig. 5). The variation of g_m and g_d is translated in the frequency dependent voltage gain as shown in Fig. 6. In bulk and FDSOI, the change of g_d due to self-heating is much stronger than the change of g_m (32% and 5% in FDSOI, respectively). Thus the gain frequency variation is dominated by g_d.

Stronger self-heating clearly manifests itself in a larger variation of device analogue figures of merit in FDSOI compared with bulk. The change of g_d is ~32% in FDSOI and ~8% in bulk (Fig. 5). Nevertheless, the main

conclusion drawn from Fig. 4, Fig. 5 and Fig. 6 is that in spite of stronger thermal effects, FDSOI outperform bulk in the entire frequency range. This observation is confirmed for devices with different gate lengths in Fig. 7 and Fig. 8.

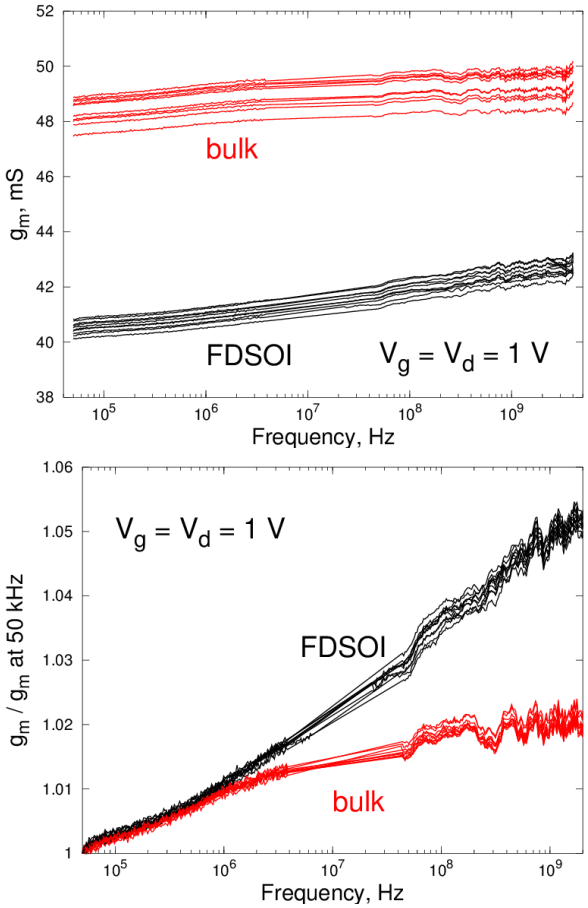
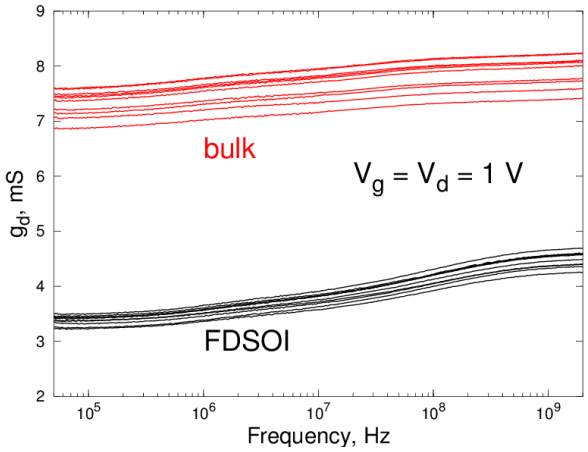


Fig. 4: *Variation of non-normalised (top) and normalised (bottom) g_m with frequency in bulk and FDSOI devices at $V_g = V_d = 1.0$ V.*



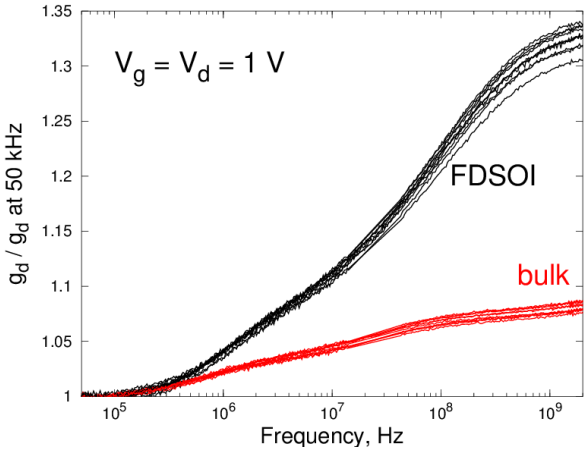


Fig. 5: *Variation of non-normalised (top) and normalised (bottom) g_d with frequency in bulk and FDSOI devices at $V_g = V_d = 1.0$ V.*

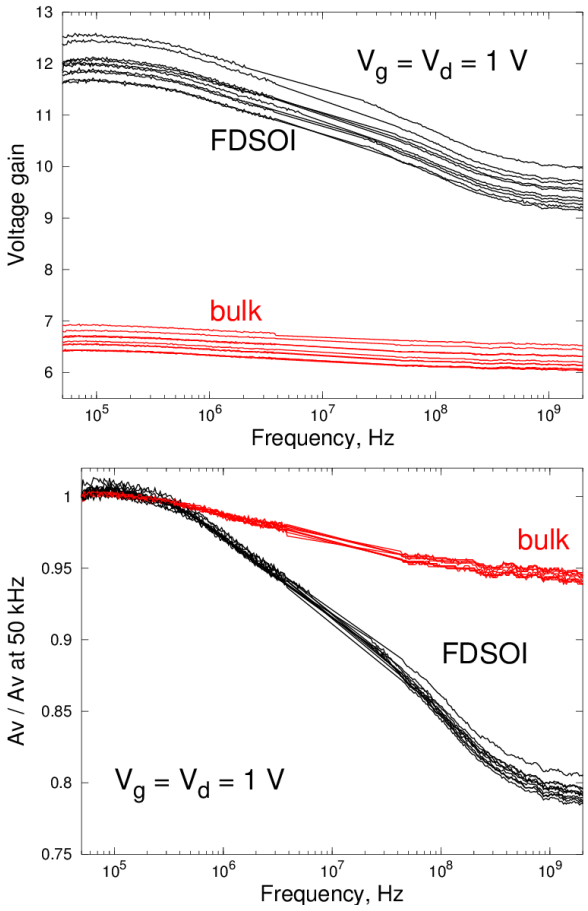


Fig. 6: *Variation of non-normalised (top) and normalised (bottom) dimensionless voltage gain (g_m/g_d) with frequency in bulk and FDSOI devices at $V_g = V_d = 1.0$ V.*

Fig. 7 shows the gain as a function of L_g in bulk and FDSOI. For the longest devices (L_g = 150 nm), the gain at high frequency is ~15 dB higher in FDSOI devices than in bulk. In the shortest devices (L_g = 25 nm), this difference is ~5 dB. Fig. 8 compares FDSOI and bulk devices in terms of the analogue figure of merit g_m-gain at 100 kHz and 1 GHz. FDSOI outperforms bulk even at 1 GHz at all gate lengths from the analogue perspective.

As mentioned above, the temperature rise in FDSOI is higher than in bulk. However, its effect on device parameters might be attenuated. Firstly, the attenuation can be due to a smaller threshold voltage temperature dependence $\partial V_{th}/\partial T$. An estimated value of $\partial V_{th}/\partial T$ in the bulk devices is ~0.75 mV/K while in FDSOI it is ~0.6 mV/K [10]. Secondly, presumably higher R_{sd} in FDSOI compared with bulk (due to a smaller cross-section of the thin Si film) can weaken the impact of temperature on g_m and the drain current [10]. This effect can be compromised by higher doping in the bulk devices.

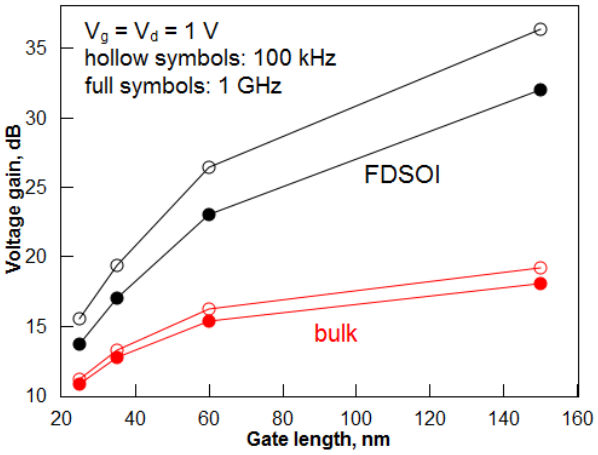


Fig. 7: *Voltage gain variation with L_g at 100 kHz and 1 GHz.*

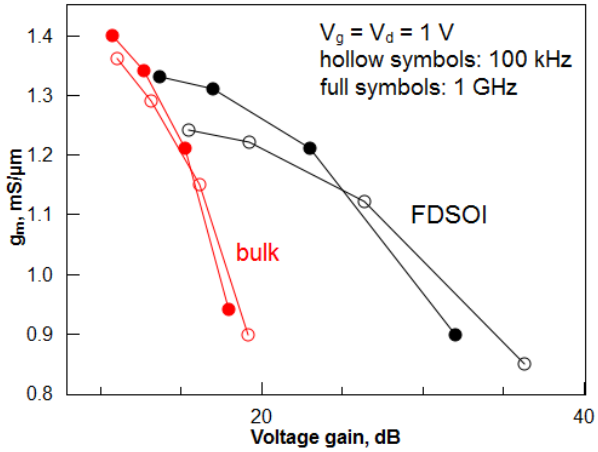


Fig. 8: *g_m variation with the voltage gain in bulk and FDSOI devices with 25 - 150 nm gate lengths at 100 kHz and 1 GHz.*

5. Summary

Self-heating and its impact on analogue performance were studied in 28 nm technology bulk and FDSOI devices. In spite of stronger self-heating, FDSOI outperforms bulk in a wide frequency range. While thermal effects are stronger in FDSOI, their influence on device parameters is limited.

Acknowledgement

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