Comparative Study of Parasitic Elements on RF FoM in 28 nm FD SOI and Bulk Technologies

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***Abstract*- This work presents a comparison of parasitic elements (capacitances and resistances) in a view of their effect on RF Figures of Merit (FoM) in 28 nm fully-depleted silicon-on-insulator (FD SOI) ultra-thin body and buried oxide (UTBB) MOSFETs and their Bulk counterparts. Complete set of small-signal equivalent circuit elements (both 'intrinsic", i.e. device related and "extrinsic", i.e. parasitic) are extracted from S-parameters measurements in a frequency range up to 40 GHz. It is shown that detrimental/harmful effect of parasitics, particularly capacitances, is stronger in 28 nm bulk technology compared to 28 FD SOI.**

Keywords: UTBB; Bulk; RF FoM; small-signal equivalent circuit; parasitic elements.

I. INTRODUCTION

Low cost, low power and low voltage Silicon MOSFET technology development has provided the possibility to produce highly integrated circuits for RF and wireless applications [1]-[2]. Application of proper and accurate small-signal model for a Silicon MOSFET allows for not only process development characterization but also to generate and verify large signal models [2]-[3]. Thanks to recent advanced developments in the complementary metal oxide semiconductor (CMOS) technology, RF CMOS FETs become an excellent choice for next-generation candidates for radio frequency (RF) applications [4]-[5]. Widely used bulk technology fails nowadays to continue developing highly efficient deeply downscaled devices due to many reasons, such as e.g. leakage current, parasitic capacitances and latch up, etc. Actually, the design rules used in SOI technology are extracted from Bulk technology and developed by including an oxide layer over the silicon substrate [6]. This, however, is more appropriate for partially depleted (PD) than fully depleted (FD) devices. One of the specific advantages of SOI CMOS technology comparing to Bulk is low crosstalk between devices such as RF and digital circuits in mixed-signal integrated circuits (ICs). Moreover, it is possible to integrate high quality passive elements thanks to effective reduction of substrate coupling in RF circuits [4], [6]-[8].

II. EXPERIMENTAL DETAILS

Devices studied in this work originate from 28LP and 28FDSOI processes by STMicroelectronics. More details on the process can be found in [9]. Bulk P-devices feature a thin SiGe layer for performance enhancement.

For RF characterization CPW (Coplanar Waveguide) feed line pads are embedded to the multi-finger devices. The effect of these interconnections on extrinsic capacitances is eliminated and de-embedded by means of dedicated open structures for each device. Studied devices feature gate length (L_g) from 25 nm up to 0.25 µm and a fixed nominal total gate width (W_g) of 120 µm. The on-wafer measurement is performed with a VNA, Anritsu 37369A calibrated by LRRM method and S-parameters are measured in a frequency range from 40 MHz up to 40 GHz.

III. RESULTS AND DISCUSSION

Fig. 1 shows the small-signal model of a MOSFET decomposed into "extrinsic" and "intrinsic" parts denoted by 'e' and 'i' indices, respectively. This model is applicable for both Bulk and SOI technologies.

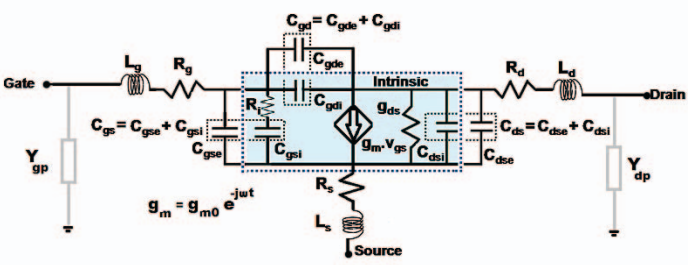

Fig. 1. Small-signal equivalent circuit used for modeling the RF behavior of UTBB and Bulk MOSFETs.

This equivalent circuit keeps valid for MOSFETs up to at least 55 GHz, allowing us to extract high-frequency parameters as reported in [10]. The different parameters of this model are obtained from the S-parameters measurements at different bias conditions, e.g. saturation (V_{ds} = 1 V) and cold (V_{ds} = 0 V) as well as different applied gate voltages (V_{gs}) [11-12]. According to the MOSFET small-signal equivalent circuit (Fig. 1) and Eq. 1-2 [10, 13], it can be seen that f_T and f_{max} are affected by intrinsic and extrinsic parasitic components.

$$f_T \approx \frac{g_m}{2\pi C_{gs}(1+C_{gd}/C_{gs})+(R_s+R_d)(C_{gd}/C_{gs}(g_m+g_{ds})+g_{ds})} \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} \approx \frac{g_m}{4.\pi.C_{gs}(1+C_{gd}/C_{gs}).\sqrt{g_{ds}(R_g+R_s)+0.5C_{gd}/C_{gs}.(R_s.g_m+C_{gd}/C_{gs})}} \quad (2)$$

where C_{gg}, g_m and g_{ds} are the total gate capacitance, gate transconductance and channel conductance, respectively.

In Fig. 2 the variation of g_{mi}, g_{me} and R_{sd} with L_g for SOI and Bulk technology is shown. As can be seen, L_g-dependence of both g_{me} (as measured) and g_{mi} (after R_{sd} withdrawal) is much weaker than $1/L_g$, revealing clearly the effect of velocity saturation in both technologies. Higher g_m in Bulk devices is due to employment of high-µ channel. Next to that, R_{sd} in FD SOI is lower than in Bulk regardless a thin film channel in FD

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SOI. This attests that employed source/drain engineering techniques tolerate/compensate R_{sd} related issues in thin-film devices. Thanks to lower R_{sd} in FD SOI the difference between g_{me_Bulk} and g_{me_SOI} (~8%) is smaller than difference between intrinsic parts g_{mi_Bulk} and g_{mi_SOI} (~17% due to high-μ channel in bulk devices) (Fig. 2).

Fig. 3 shows "extrinsic" and "intrinsic" parts of total gate capacitance C_{gg} in both technologies. Total and extrinsic C_{gg} in bulk devices are larger than in FD SOI. Thus, according to Eq. 1 and 2, higher cut-off frequencies can be achieved in FD SOI. Furthermore, the extrinsic gate capacitance, C_{gge} in FD SOI devices becomes dominant over intrinsic one for the devices with L_g < 45 nm whereas in bulk counterparts this happens already for L_g < 120 nm.

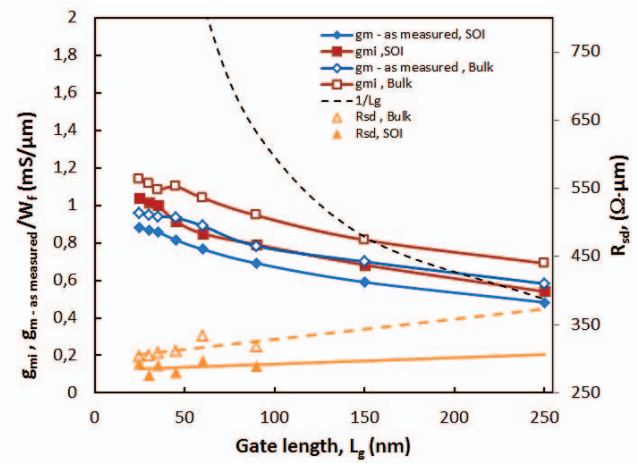

Fig. 2. Normalized g_{mi}, g_{me} and R_{sd} (R_s+R_d) versus gate lengths (L_g) for W_f = 2 μm, N_f (number of the fingers) = 60 in SOI and Bulk technologies.

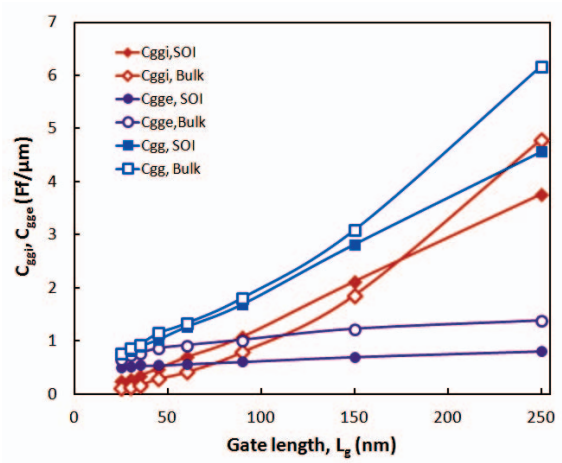

Fig. 3. Normalized C_{ggi}, C_{gge}, C_{gg} (C_{ggi}+C_{gge}) versus gate lengths (L_g) for W_f = 2μm, N_f (number of the fingers) = 60 in SOI and Bulk technologies.

Fig. 4a compares the output conductance (g_{ds}) in SOI and bulk technologies. As can be seen, g_{ds} in bulk technology is much higher than in SOI due to stronger short channel effects and implication of HALOs in bulk technology. Higher g_{ds} degrades both cutoff frequencies f_T and $f_{max,}$ according to Eq. 1 and 2.

Fig. 4b compares extrinsic source-drain capacitance C_{dse} in bulk and FD SOI technologies. One can see that C_{dse} is higher in bulk technology than in FD SOI attesting strong coupling between drain and source through the substrate in bulk technology. This will induce more losses and non-linearities in RF circuits based on the bulk technology.

Finally, as a result of better tolerated effect of parasitic elements on RF FoM in FD SOI technology, about the same value of cut-off frequencies $f_T \geq 270$ GHz was obtained in both FD SOI and bulk devices, despite the high-μ channel engineering employed in bulk.

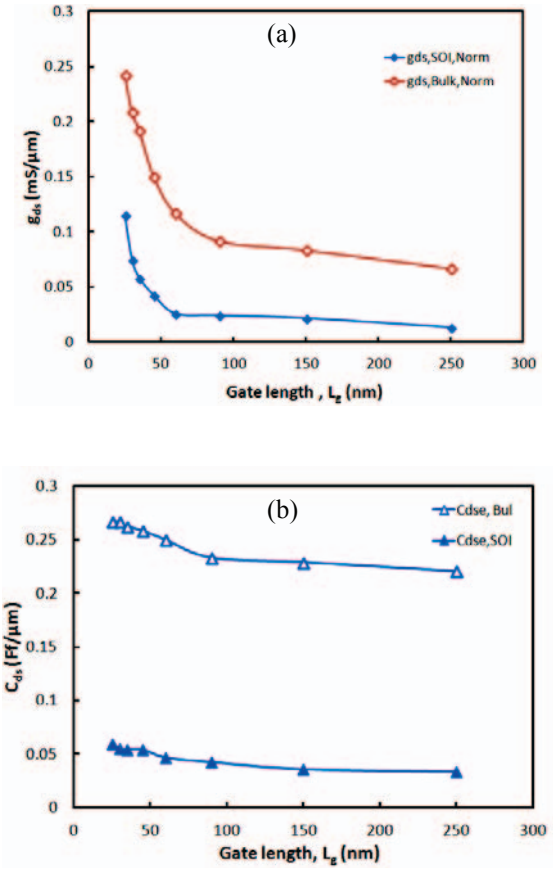

Fig. 4. (a) Channel conductance, (b) Extrinsic source-drain capacitance in SOI and Bulk technologies versus gate length (L_g) for W_f = 2 μm, N_f (number of the fingers) = 60.

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IV. CONCLUSION

In this paper, based on the small-signal equivalent circuit extraction, parasitic elements of 28 nm FD SOI and Bulk MOSFETs were comparatively analyzed. Lower values of output conductance, extrinsic gate and drain-to-source capacitance, as well as lower series resistance were revealed in FD SOI devices comparing to the bulk counterpart and explained in terms of improved short channel effect control, device architecture and well tolerated process. As a result regardless high-μ channel employed in bulk process, comparable f_T values of more than 270 GHz (close to the ITRS requirements for LSTP applications) have been obtained for both in bulk and FD SOI. By applying further device and process optimization in SOI technology, e.g. high-μ channel to obtain higher g_m, even better RF performance is expected.

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