Investigation of TSV noise coupling in 3D-ICs using an experimental validated 3D TSV circuit model including Si substrate effects and TSV capacitance inversion behavior after wafer thinning

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Abstract — This paper investigates the influence of TSV noise coupling on nearby devices based on an extended 3D TSV circuit model. This model not only takes into account the complex RF field distributions in bulk Si, but also incorporates the anomalous TSV capacitance inversion behavior, which has been found to occur due to the presence of fixed charges in the backside passivation layer after wafer thinning. The extended 3D TSV circuit model is validated by the excellent agreement between the simulation results and experimental data. It demonstrates that the inversion behavior of the TSV capacitance increases the noise coupling to adjacent devices mainly in the low frequency range. Furthermore, we show that noise mitigation techniques can be easily implemented in this 3D circuit model to predict the extent of noise coupling alleviation.

Index Terms — TSV, 3D circuit model, inversion layer, inversion behavior of TSV capacitance, noise coupling.

I. Introduction

TSVs are an important source of noise that can affect neighboring devices and degrade the circuit performance in 3D-ICs. Hence, it is crucial to evaluate the electromagnetic (EM) coupling to and from TSVs to enable reliable 3D-IC design. Most previous publications address the noise coupling through electromagnetic simulations. However, 3D EM solvers require an enormous amount of computing resources and are not appropriate for the simulation at the circuit and system level. Thus, a fast and accurate circuit-based TSV model, which can be easily integrated into standard circuit simulators is highly desired for 3D-IC design optimization.

The classic TSV circuit model [1] is not capable of capturing complex field distributions in lossy Si substrates. It is thus limited to modelling single TSV pairs without close substrate ground contacts, such as guard rings. The 3D-TLM model [2] overcomes these limitations by dividing the TSV and the substrate into a network of unit cells. Still, it cannot incorporate the anomalous TSV capacitance behavior [3], which can be expected to affect the RF behavior of TSVs in terms of noise coupling and signal integrity in neighboring devices.

To overcome these shortcomings, we have developed an extended 3D TSV circuit model that incorporates both the RF field distribution in bulk Si and the anomalous TSV capacitance behavior. This model shows excellent agreement with experimental data and can be used to study the noise coupling to adjacent devices by using standard circuit-based simulators (such as ADS) with or without the influence of the anomalous TSV capacitance behavior.

II. 3D TSV extended circuit model and validation

The TSV is a metal-oxide-semiconductor (MOS) structure, therefore the TSV capacitance is both frequency and bias dependent. The TSV inversion capacitance which can occur after wafer thinning is depicted in Fig. 4. Before wafer thinning, high capacitive behavior typical to inversion is observed only at very low frequency in the CV characteristic of TSVs, well below ~1 kHz, as expected. However, after wafer thinning and backside passivation deposition, inversion occurs up to frequencies as high as ~100 kHz. The origin of the TSV capacitance inversion in a *p*-type substrate is due to the presence of fixed positive charges in the backside (BS) passivation layer of the TSV after wafer thinning creating an inversion layer at the backside of the wafer as shown in Fig. 1. As a consequence, such a BS inversion layer can act as a conductive channel between neighboring TSVs and can increase the noise coupling to neighboring devices. More information of this behavior can be found in [3].

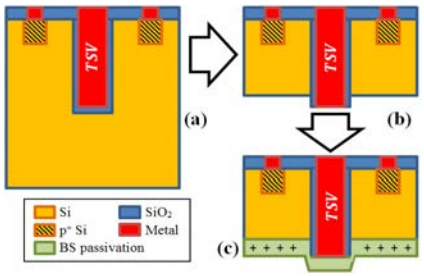

Fig. 1. Key steps in the TSV reveal and passivation process: a) TSV before wafer thinning. b) Wafer thinning and TSV reveal. c) Backside passivation.

A. 3D TSV extended circuit model including Si substrate effects and TSV capacitance inversion

In order to incorporate the anomalous inversion C-V behavior of TSVs and assess its influence on adjacent devices, it is necessary to insert additional circuit elements into the 3D-TLM TSV unit cell described in [2]. The original and adapted unit cell of the TSV 3D circuit model are depicted in Fig. 2 (a) and in Fig. 2 (b), respectively. In Fig. 2 (a), the parameters R_{TSV} and L_{TSV} represent the self-resistance and self-inductance terms of

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the TSV, whereas C_{ox} and C_{dep} model the oxide liner capacitance and the depletion region capacitance of the TSV, respectively.

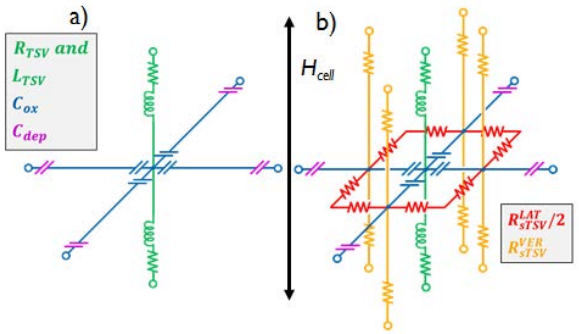

Fig. 2. Equivalent circuit model for the 3D TSV unit cell: (a) 3D view of the original TSV unit cell in [2]. (b) 3D view of the modified new TSV unit cell.

In Fig. 2 (b), new resistive elements were introduced in the vertical and horizontal directions that account for the inversion channel between the TSV oxide and the depletion capacitance elements. The added R_{sTSV} in red and yellow colors model the resistive paths around the TSV at the oxide/silicon interface for the vertical and horizontal directions and can be calculated by equations (1) and (2), respectively. This interface may be highly conductive due to the presence of an inversion layer or highly resistive if depleted. The sheet resistance of the inversion layer was calculated using the semiconductor simulation software Silvaco Atlas and was found to be 9 kΩ/Sq for a 20 Ωcm Si substrate and an interfacial charge density of $Q_{ox} = 10^{12}$ cm^{-2}. The sheet resistance was calibrated against DC measurements.

$$R^{VER}_{s_{TSV}} = R^{inv}_{sheet_{TSV}} \frac{H_{cell}}{\pi(r_{TSV}+t_{liner})} \quad (1)$$

$$R^{LAT}_{s_{TSV}} = R^{inv}_{sheet_{TSV}} \frac{\pi(r_{TSV}+t_{liner})}{2H_{cell}} \quad (2)$$

In addition to the TSV and substrate unit cells, a backside (BS) unit cell was also developed to model the BS interface that may be either in inversion or in depletion. An example of connecting a network of unit cells in a 3D volume is shown in Fig. 3. The element C_{dBS} in the backside unit cell represents the depletion capacitance in the BS unit cell, whereas R_{sBS} models the resistive path at the BS passivation layer/silicon interface. The following equations (3) and (4) can then be used to calculate the resistance in the x and z directions:

$$R^{X}_{s_{BS}} = R^{inv}_{sheet_{BS}} \frac{l_{unit}/2}{W_{unit}} \quad (3)$$

$$\mathrm{R}^{Z}_{s_{BS}} = R^{inv}_{sheet_{BS}} \frac{\mathrm{W_{unit}}/2}{l_{unit}} \quad (4)$$

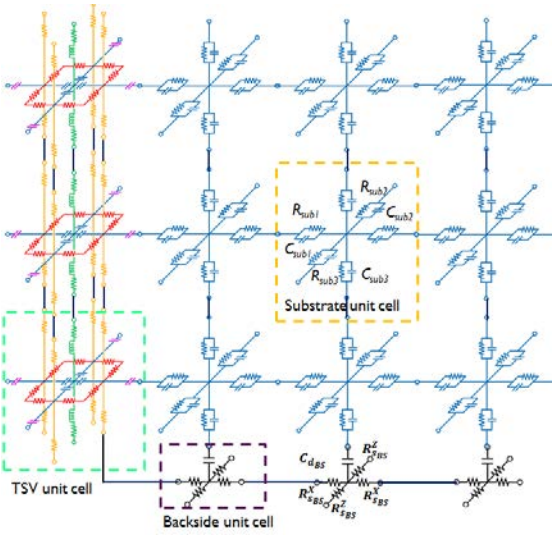

Fig. 3. Example of a 3D interconnect constructed using three types of unit cells: TSV unit cell, substrate unit cell and BS unit cell.

B. 3D extended circuit model validation again measurements

The red and blue curves in the C-V plot of TSVs in Fig. 4 (a) were measured at 10 kHz on a 64 TSV array before and after wafer thinning and BS passivation, respectively. While the red curve shows the expected depletion behavior for positive bias at this frequency, the blue curve (after thinning and passivation) shows inversion at the same frequency. Fig. 4 (b) shows the TSV capacitance *vs.* frequency at positive bias: the inversion capacitance persists up to much higher frequencies after thinning and backside passivation because of positive charges in the BS passivation layer that induce substrate inversion at the BS. This BS conductive channel is responsible for a large extension of the effective TSV depletion capacitance. This leads to the inversion-capacitance like behavior of the TSV all the way up to frequencies in the 400 kHz range, as observed by the after-wafer thinning measurements shown in Fig. 4 (b). The excellent agreement between the 3D circuit model (yellow dashed line) and the measurements validates our 3D circuit model. The black dashed lines in Fig. 4 (b) were obtained from the 2D models detailed in [3] and agree also well with experiments and the 3D circuit model.

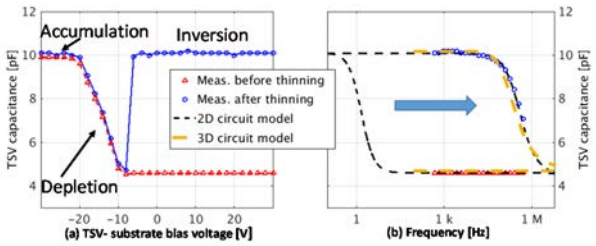

Fig. 4. Left: (a) C-V measurements at 10 kHz. Right: (b) C-f measurements (at positive TSV bias ensuring surface inversion) between p-substrate and a TSV array consisting of 64 parallel connected TSVs.

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III. Investigation of the TSV noise coupling in 3DICs using extended 3D circuit model implemented in ADS

The influence of the TSV capacitance on the adjacent device performance has been studied using the 3D circuit model in combination with the circuit-based simulator ADS. We focus on two cases: TSV-to-TSV as well as TSV-to-active coupling. Both occurrences were simulated for different combinations of $R^{inv}_{sheetTSV}$ and $R^{inv}_{sheetBS}$, that define respectively the sheet resistance values at the TSV oxide liner / bulk Si interface and at the BS interface between the passivation layer and the Si substrate. In strong inversion, the sheet resistance of inversion layer was set to 9 kΩ/Sq, as discussed above, whereas in depletion, it was set to a large value equivalent to infinity.

A. TSV to TSV coupling

The simulated TSV dimensions were 5/50 µm with a 200 nm thick oxide liner, with 10 µm pitch in between. In depletion, the sheet resistances are very large and the S_{21} coupling was not affected as shown in Fig. 5. The low-frequency capacitive coupling is then determined by $1/C_{tot} = 1/C_{ox}+1/C_{depTSV}$. However, when inversion is present at both the TSV and the BS interfaces, the TSV depletion capacitance is shunted by the BS inversion channel at low frequencies (see [3] for more details). The low-frequency capacitive region is then determined by $C_{tot} = C_{ox}$, which increases the noise coupling between the TSVs by about 10 dB at 1MHz. Excellent agreement between the model and simulation is also observed in Fig. 5

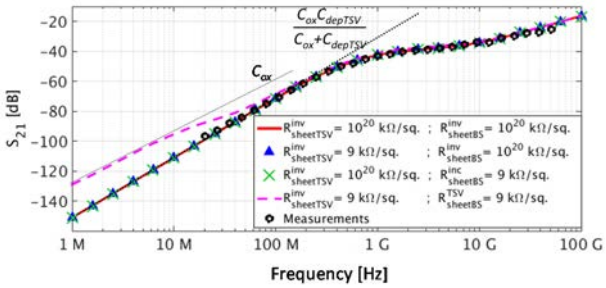

Fig. 5. TSV-to-TSV coupling, with and without BS inversion, as well as with and without TSV inversion.

B. TSV to active device noise coupling modeling and validation

Our 3D circuit model also allows to investigate the noise coupling of the test structure, consisting of a TSV and a 65 nm planar nMOSFET. A small signal model of this transistor was integrated into the 3D model: the two nodes of the transistor model labeled as NA and NB were connected to two corresponding nodes on the Si substrate labeled MA and MB, as shown in Fig. 6, reproducing the distance of 10µm from the TSV in the test structure (Fig. 7). The bulk node is defined as the region underneath the source, which is grounded in the design. A more detailed description of the test structure can be found in [4].

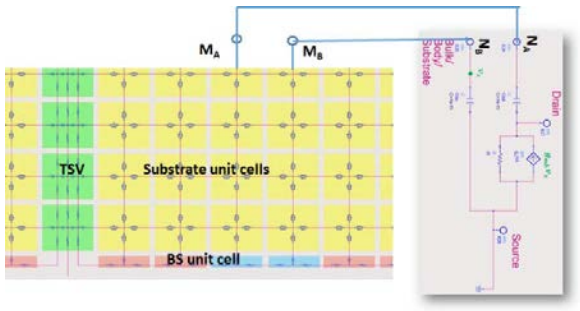

Fig. 6. Noise coupling between TSV and active device: simplified 2D cross sectional view of the 3D circuit implementation.

The simulated noise coupling between the TSV and the transistor in the ON/OFF state (Fig. 7) shows good agreement with RF measurements performed on real test structures. This agreement confirms the validity of the 3D circuit model, which enables the fast prediction of the EM coupling between TSVs and transistors of any dimension and technology node that can be represented by appropriate transistor models.

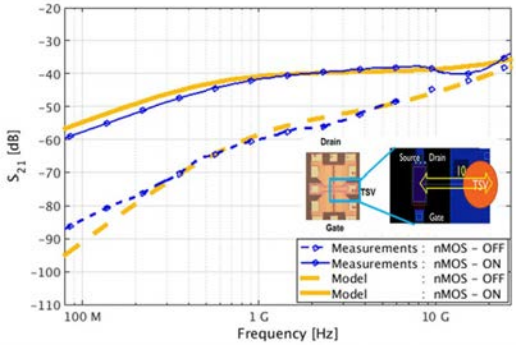

Fig. 7. Noise coupling between TSV and active device: RF measurement against 3D circuit model.

IV. Implementation of Noise mitigation techniques into the 3D extended circuit model

In addition, noise mitigation techniques such as guard rings, grounded substrate contacts, *etc.* can be easily implemented into the calibrated 3D circuit model by grounding the substrate unit cells at the specific locations. This enables the fast prediction of the noise coupling reduction due to the different noise mitigation techniques, which can be used as design guidelines.

A. Impact of substrate contact position

First, we investigate the impact of the substrate contact position on noise mitigation. To reduce the noise coupling between TSV and active device in Fig. 8 a), we place a grounded substrate contact at three different locations A, B, and C, respectively, as shown in Fig. 8 b).

Based on the simulation results in Fig. 9, a grounded substrate contact in position B or C suppresses about 6 dB noise

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coupling at 0.1 GHz, slightly better than a grounded substrate contact in position A (blue curve).

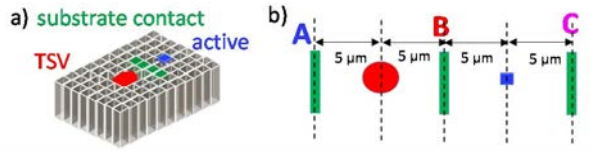

Fig. 8. Noise mitigation between TSV and active device: a) 3D view of TSV to active with substrate contact in the middle. b) Top view of a substrate contact in different locations A, B, or C.

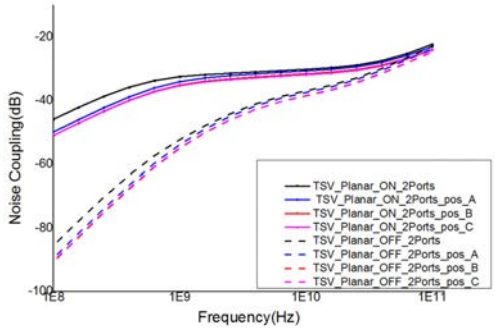

Fig. 9. Simulated noise coupling alleviation between TSV and active device at ON/OFF state with a substrate contact in positions A, B or C.

When the grounded substrate contact in position C moves gradually further away from the active device (Fig. 10), the noise coupling between the TSV and the active device increases. The noise increase is about 3-4 dB at 0.1GHz when the distance between active device and substrate contact increases from 5 µm to 100 µm.

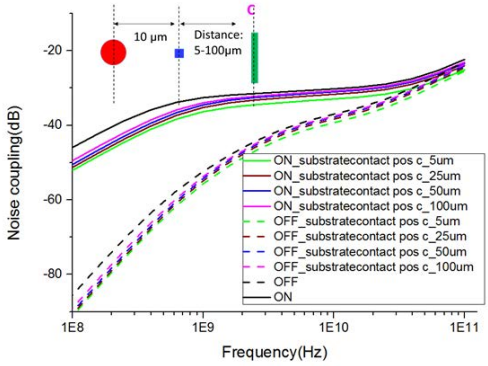

Fig. 10. Impact of the distance between the substrate contact and active device (at ON/OFF state) on noise coupling alleviation impact of the guard ring position

Besides the substrate contact, we have also investigated the impact of the guard ring position on noise coupling reduction. As shown in Fig. 11, we place a guard ring either around the TSV or around the active device. Simulations (Fig. 12) show noise coupling between TSV and transistor by about 6 dB (red curve) while the guard ring around the TSV leads to 12 dB coupling reduction (blue curve) at 0.1GHz. Moreover, the green curve shows that a guard ring around the active device reduces the noise coupling even further (by about 2 dB) than around the TSV.

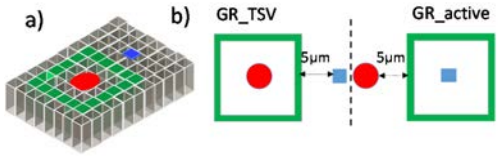

Fig. 11. Noise mitigation between TSV and active device: a) 3D view with guard ring. b) Top view: guard ring around TSV (left) and guard ring around active device (right)

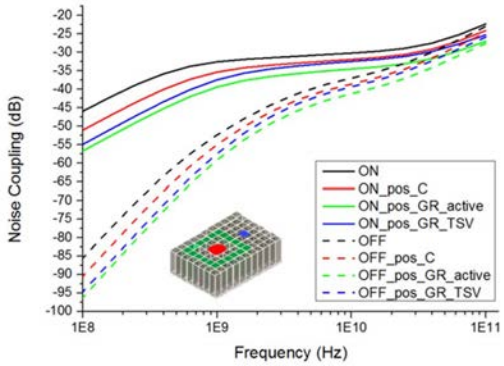

Fig. 12. Noise alleviation with different noise mitigation techniques.

V. Conclusions

An accurate 3D TSV circuit model including the TSV capacitance inversion has been proposed and calibrated against electric measurements. It has been integrated into standard circuit simulators to evaluate the noise coupling between TSVs and adjacent devices. In contrast to 3D full-wave EM solvers, this model is able to easily incorporate different device or transistor models. Noise mitigation techniques have also been easily implemented in the calibrated 3D circuit model, thus enabling a fast, simple, and efficient 3D-IC design optimization.

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