Nonlinear characteristics and RF losses of CPW and TFMS lines over a wide temperature range

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Outline

- Motivation
- Insertion losses and linearity performance of CPW and TFMS topologies in the case of SOI technology
  - at room temperature
  - up to 125°C
- Conclusions

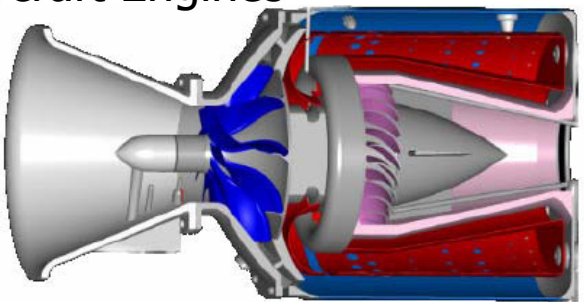
High Temperature applications

Automotive

Temperature range

- Standard/commercial: 0°C up to 70°C
- Industrial: 0°C up to 85°C
- Military: -40°C up to 125°C
- High temperature (HT): > 125°C
- Very high temperature: > 250°C

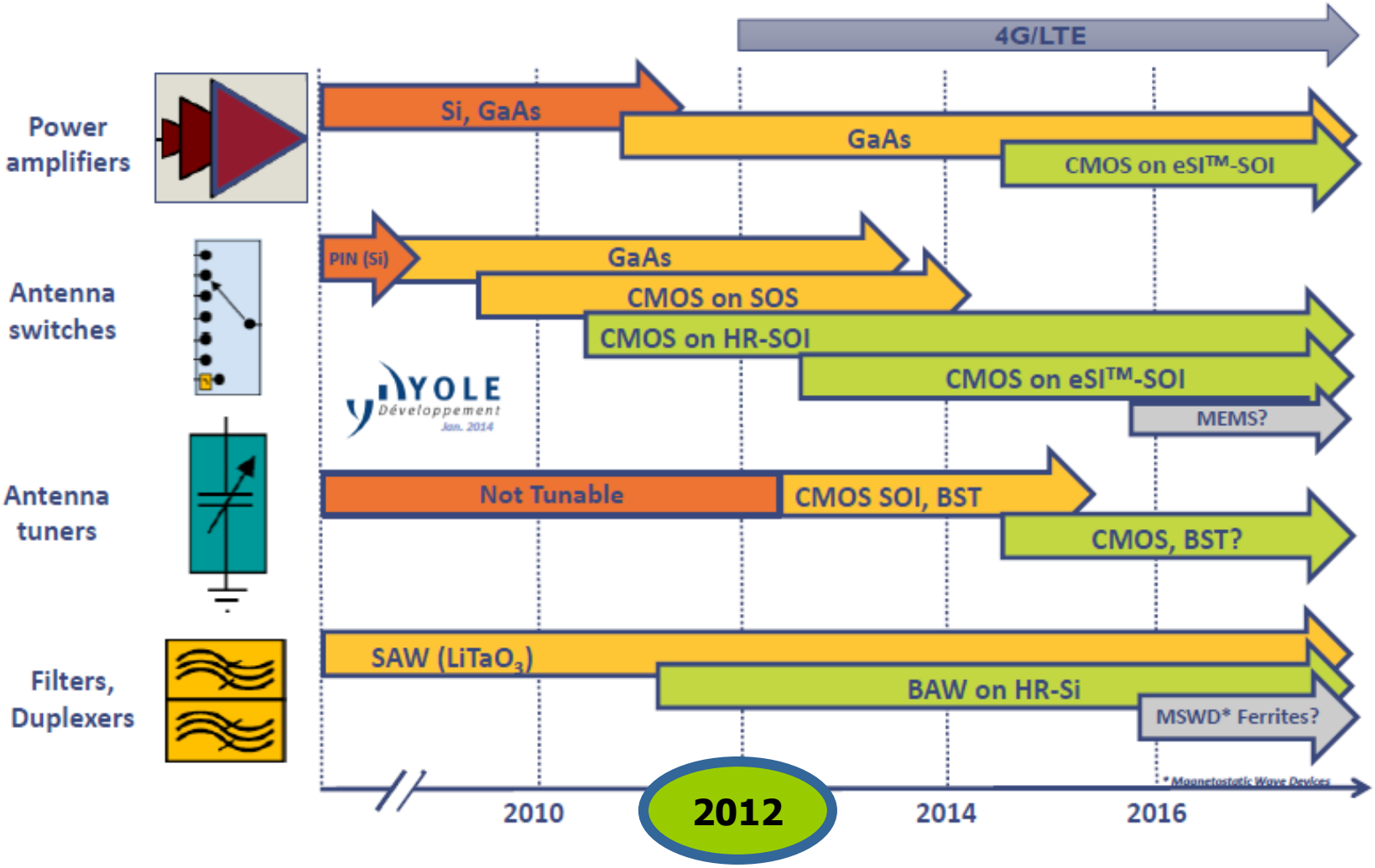
Aircraft Engines



Oil and Gas

Engineered RF SOI substrates - technology trend

RF Front-End Modules: key components



RF requirements for FEM

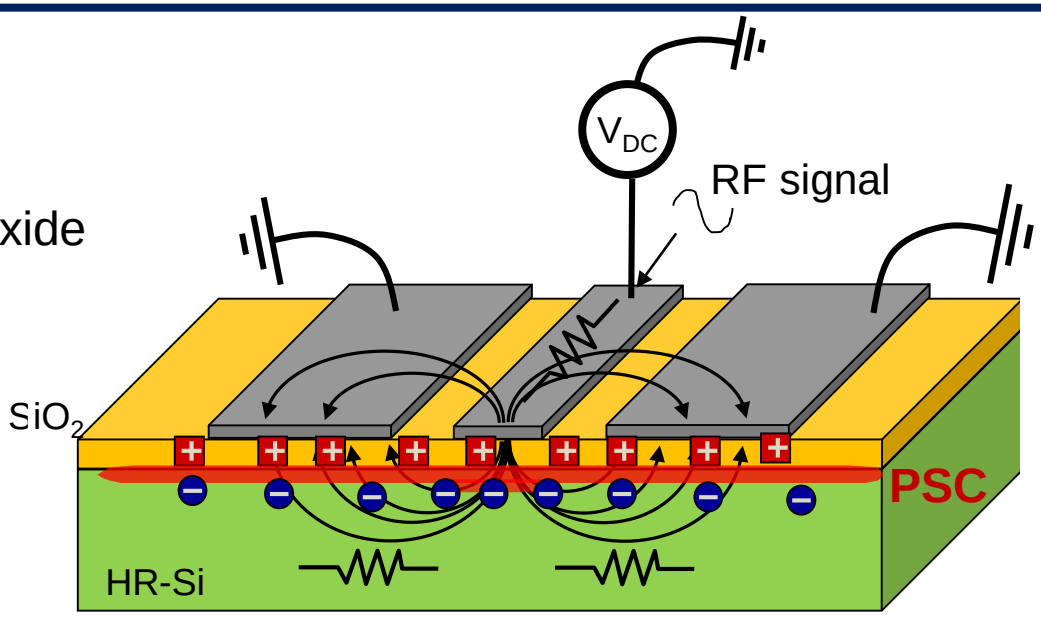
- Compatible with CMOS technology
- Low parasitic conductance/capacitance
- Low RF losses (ρ > 3 kΩ-cm)
- Low crosstalk
- High voltage capabilities (20 V or more)
- High temperature applications
- Linearity (< -70 dBc @ 35 dBm)
- Good thermal conductivity (> 100 W/m-K)
- High quality passive devices (ρ > 1 kΩ-cm)
- High capacitance densities (> 100 μF/cm^2)
- Availability (mainstream production, size)
- Low cost

CPW lines at room temperature

RF losses and harmonic distortion issues on HR-SOI

Parasitic Surface effect

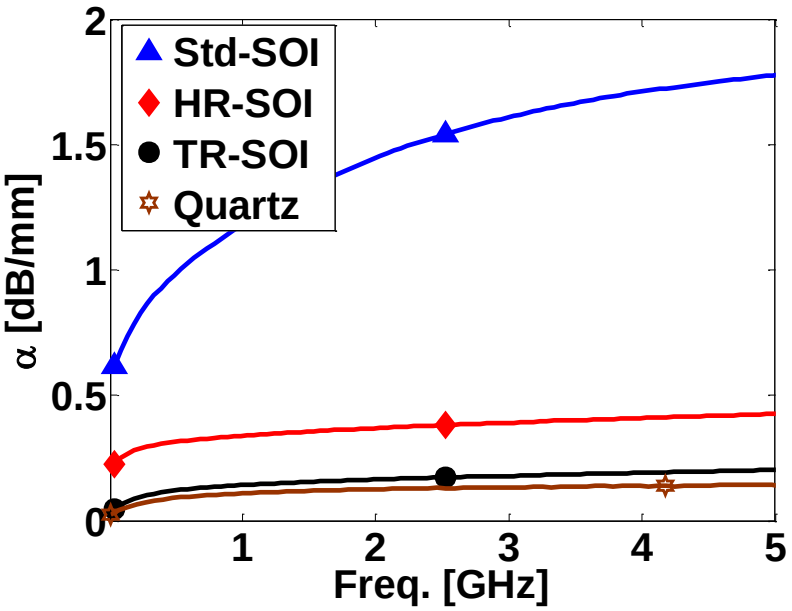
- Fixed charges (Q_f) in the oxide
- RF small or large signal
- Bias applied on the metallic conductors

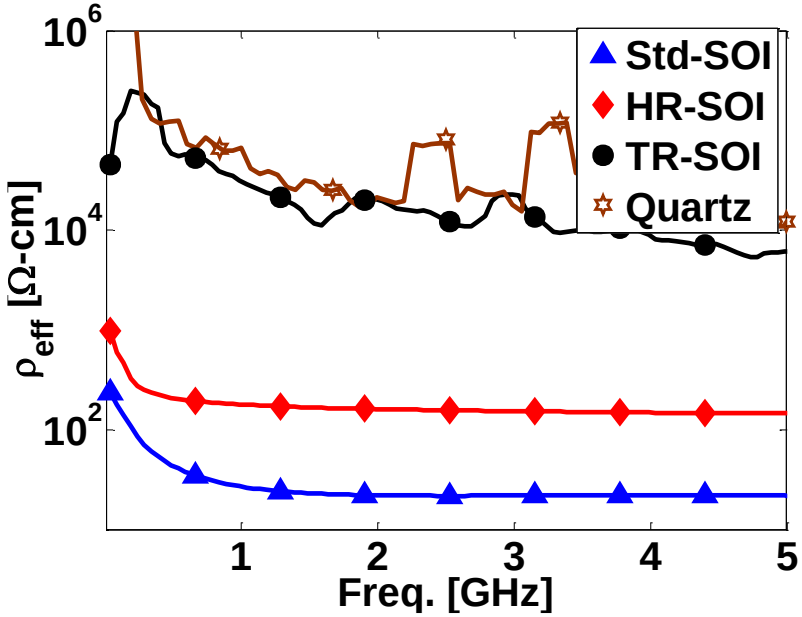


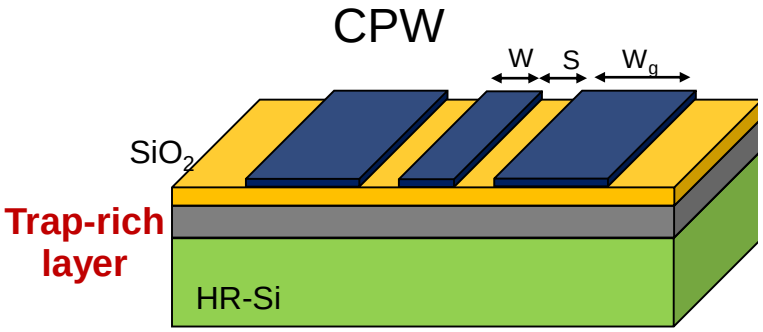
This Parasitic Surface effect needs to be mitigated using:

- **Engineered substrates: TR-SOI (commercial eSI from Soitec)**
- **Ideal dielectric substrate (glass/sapphire)**
- **RF Ground Shields (TFMS technology)**

TR-SOI addressing RF FEM requirements



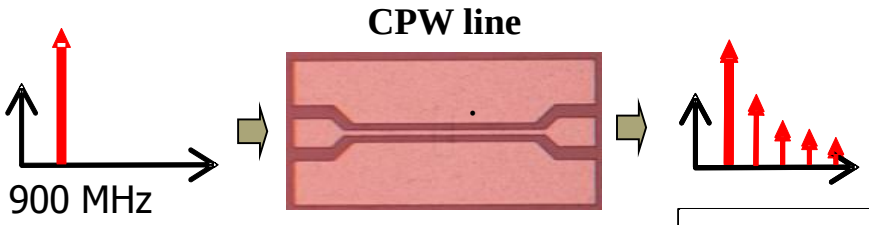


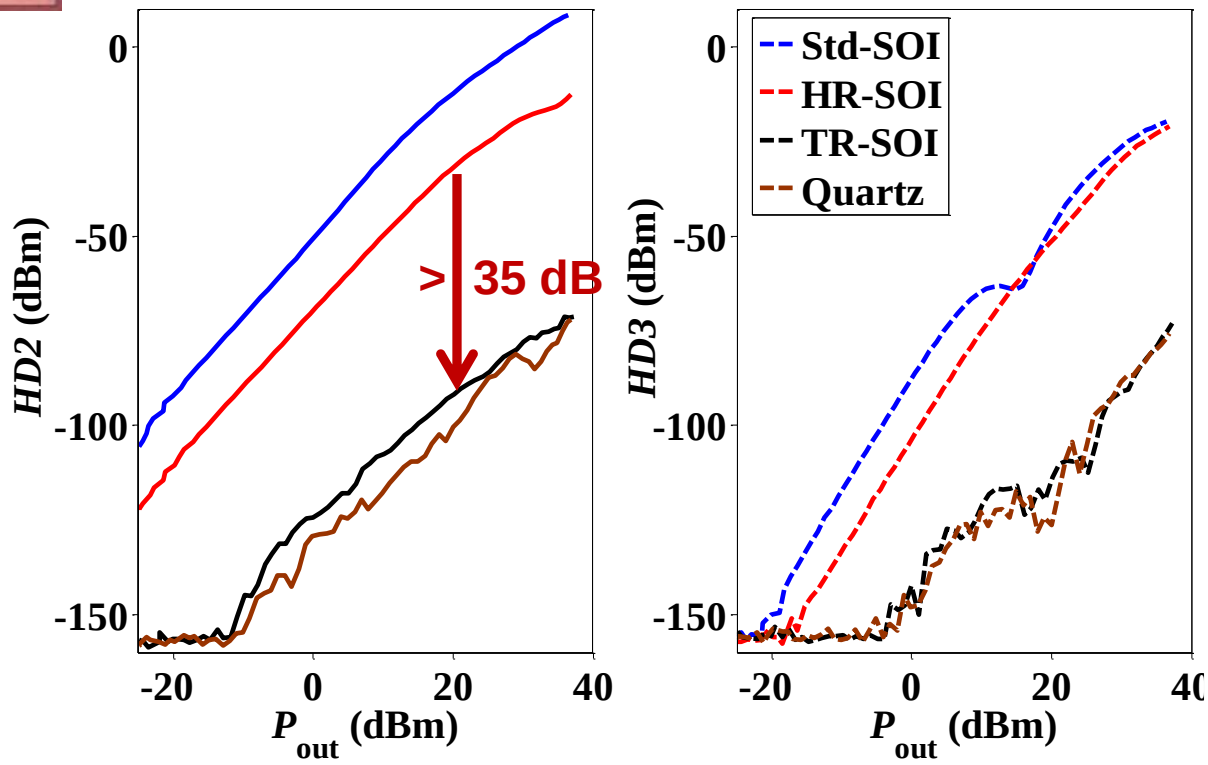


S = 12 µm
W = 26 µm
W_g = 208 µm

TR-SOI reduces RF losses

TR-SOI addressing RF FEM requirements

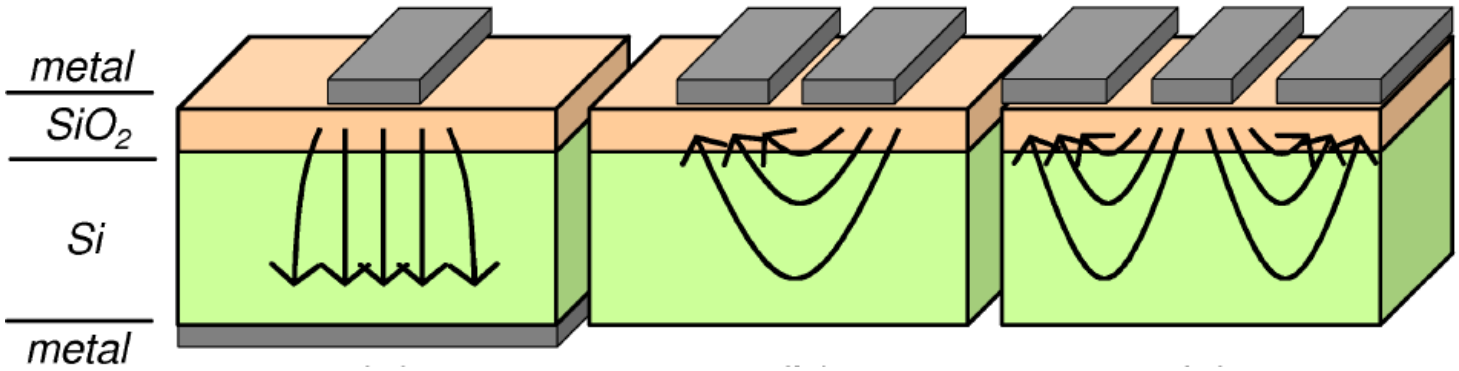


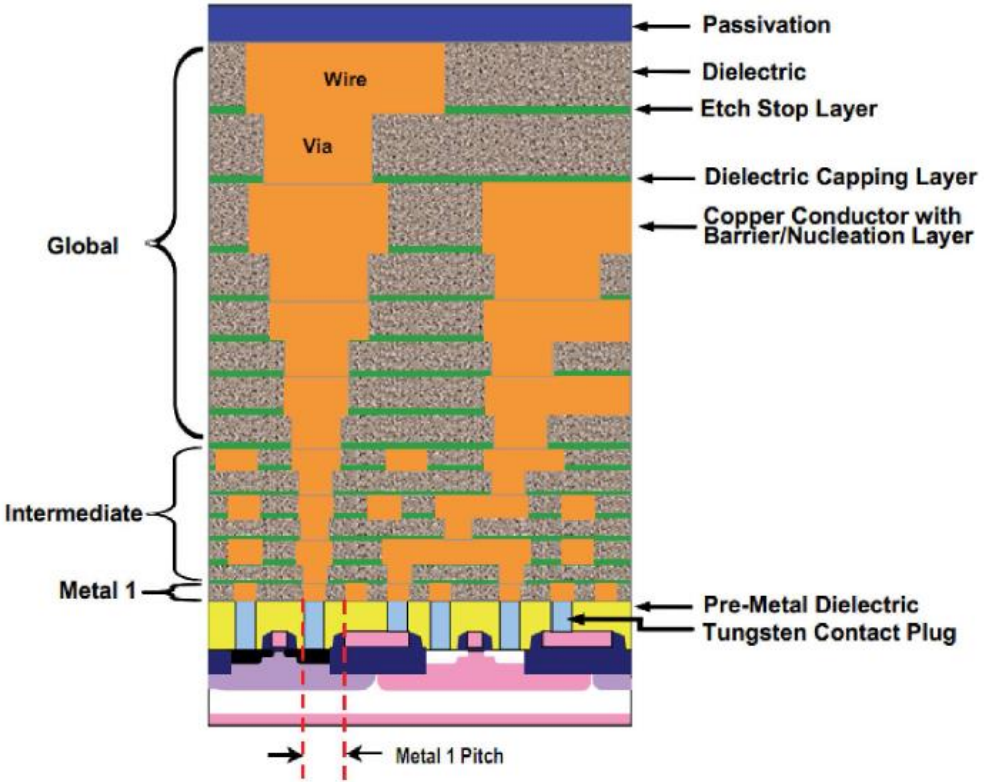


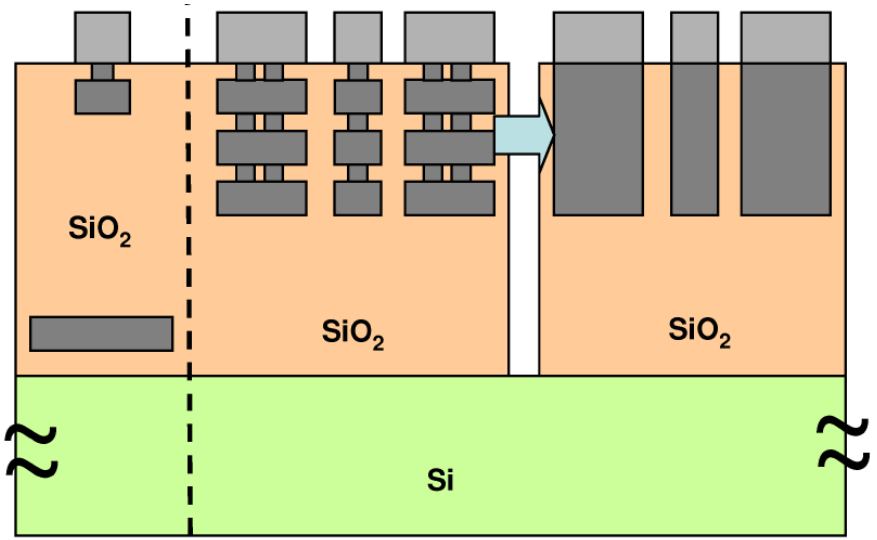
TR-SOI substrate meets LTE requirements

TFMS lines at room temperature

CPW versus TFMS

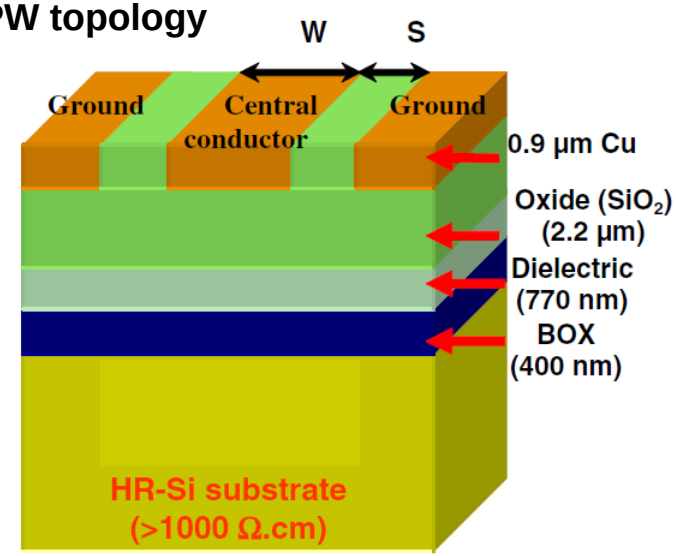




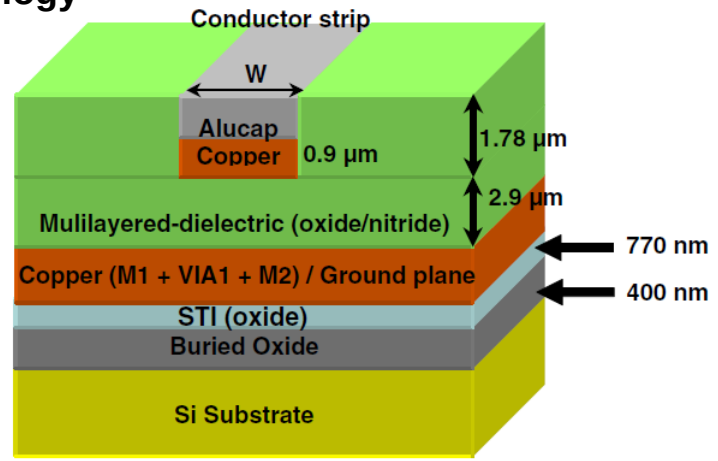


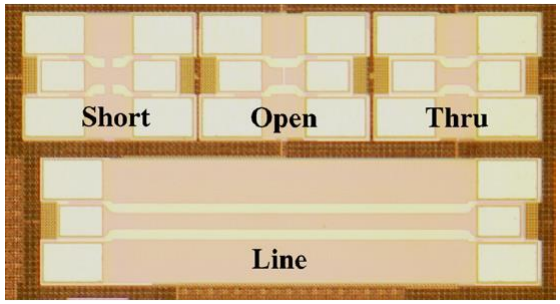
CPW and TFMS technologies

CPW topology



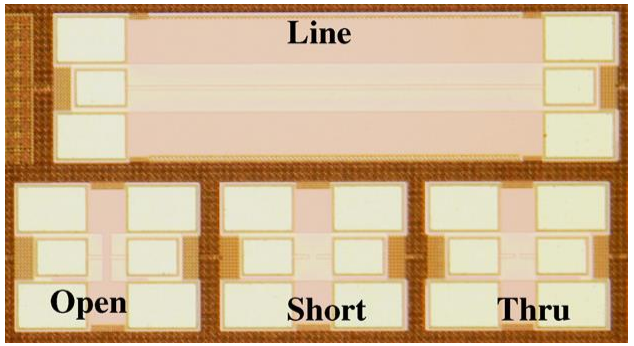
TFMS topology





CPW structures on M6

(800 µm-long)

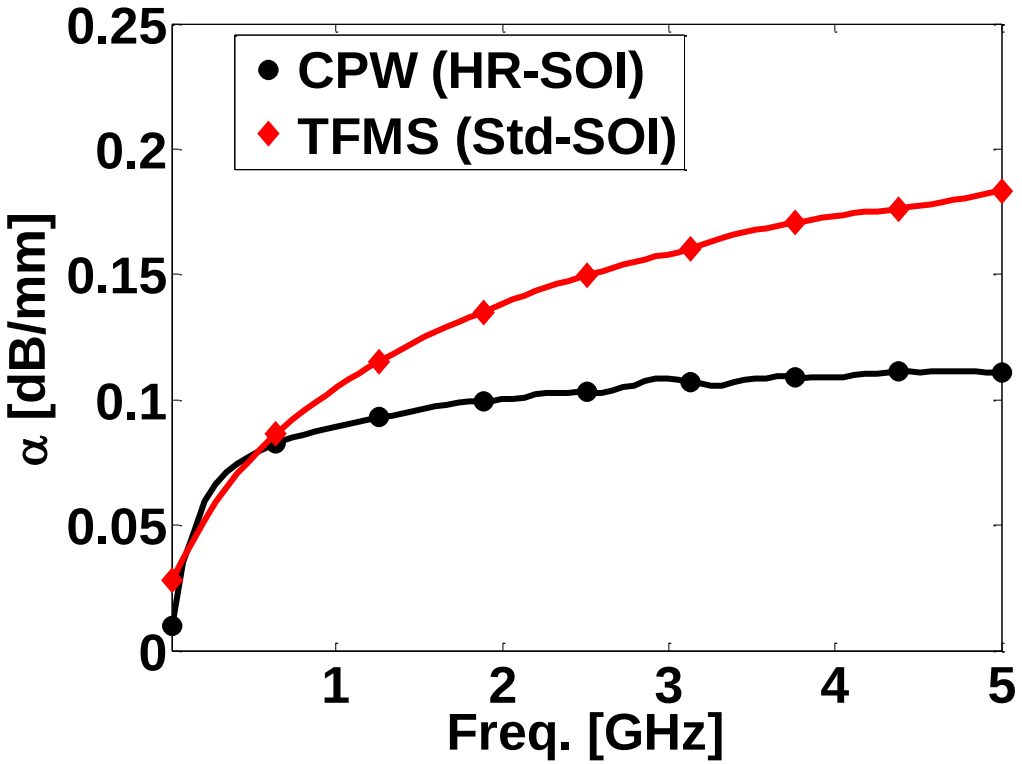


TFMS Conductor strip width, W (7 µm)
(800 µm-long)

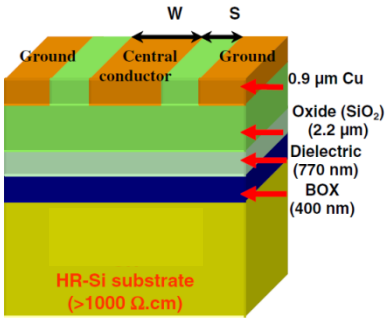
M6 + Alucap

ST-M technology

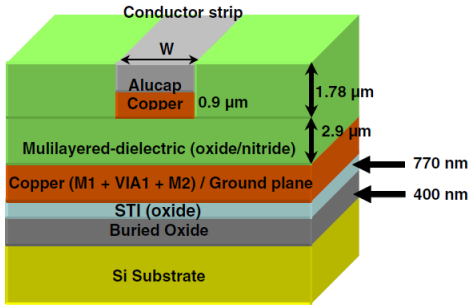
Insertion loss of CPW on HR-SOI and TFMS lines



CPW topology

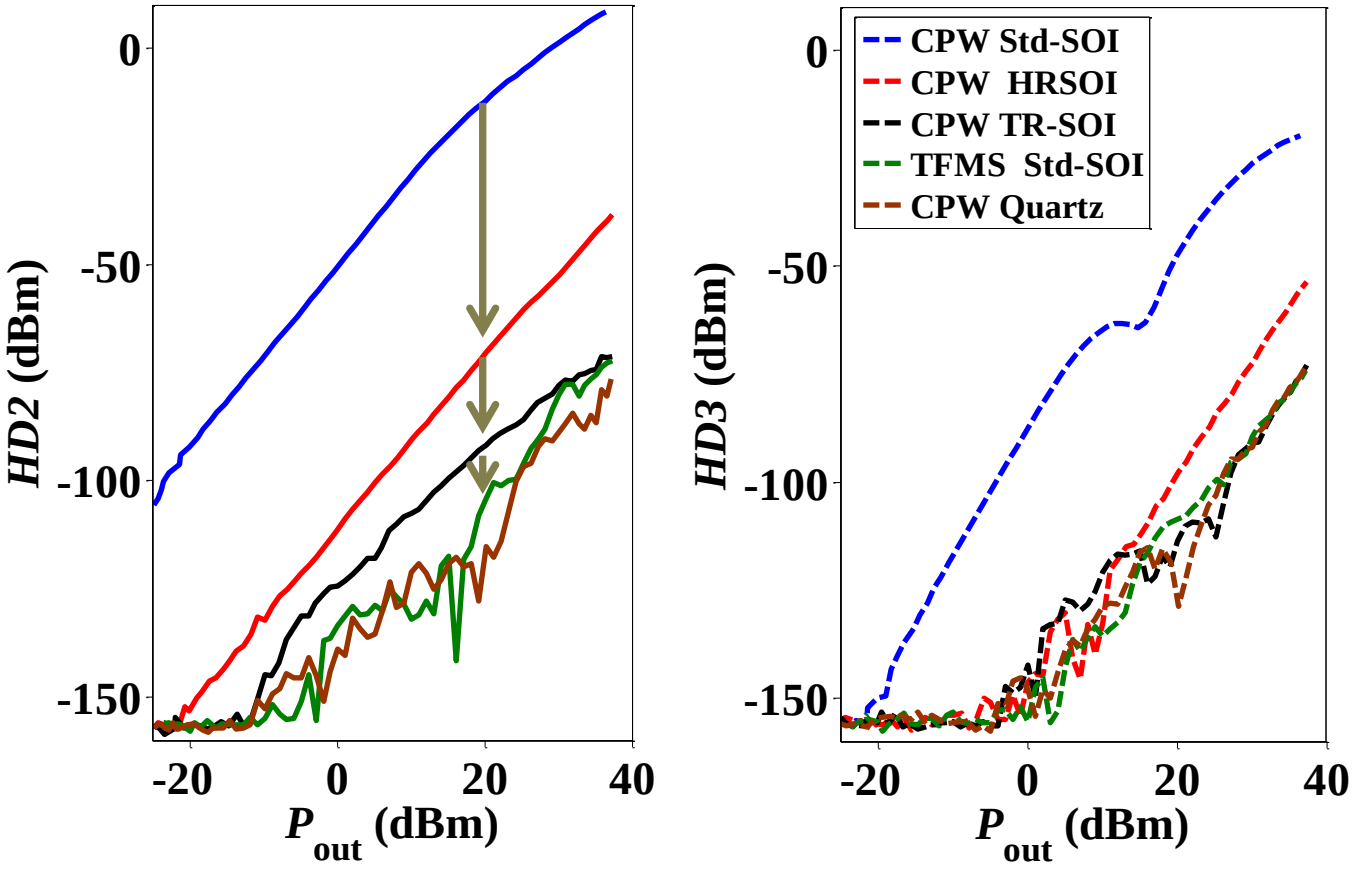


TFMS topology



TFMS exhibits higher RF losses than CPW technology

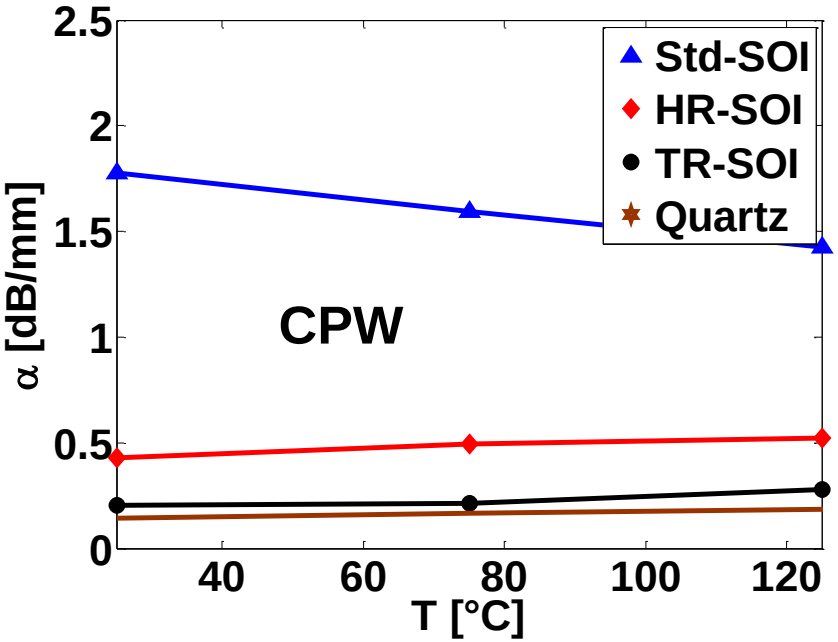
TFMS vs CPW non linear behavior on SOI substrates

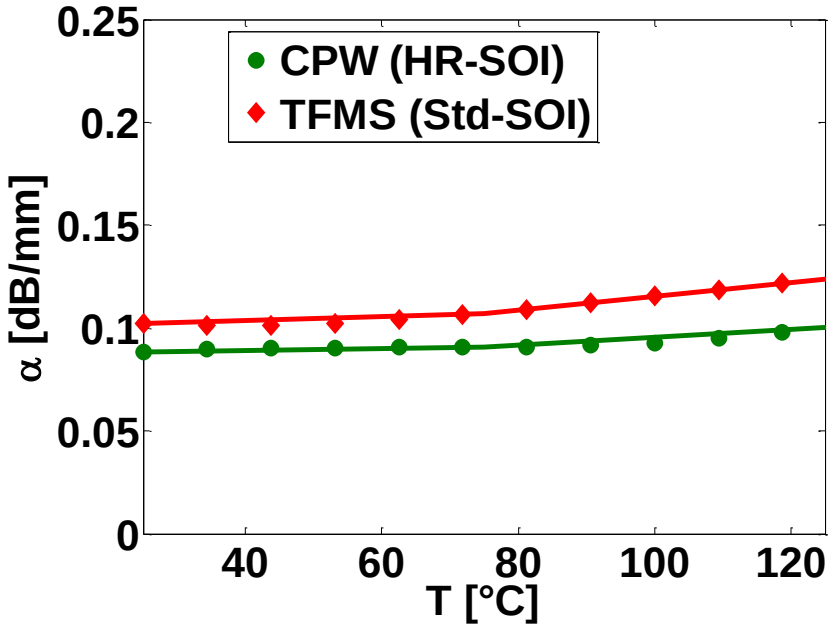


TFMS technology presents non-linearity characteristics similar than CPW on dielectric substrate

CPW vs. TFMS lines at high temperature

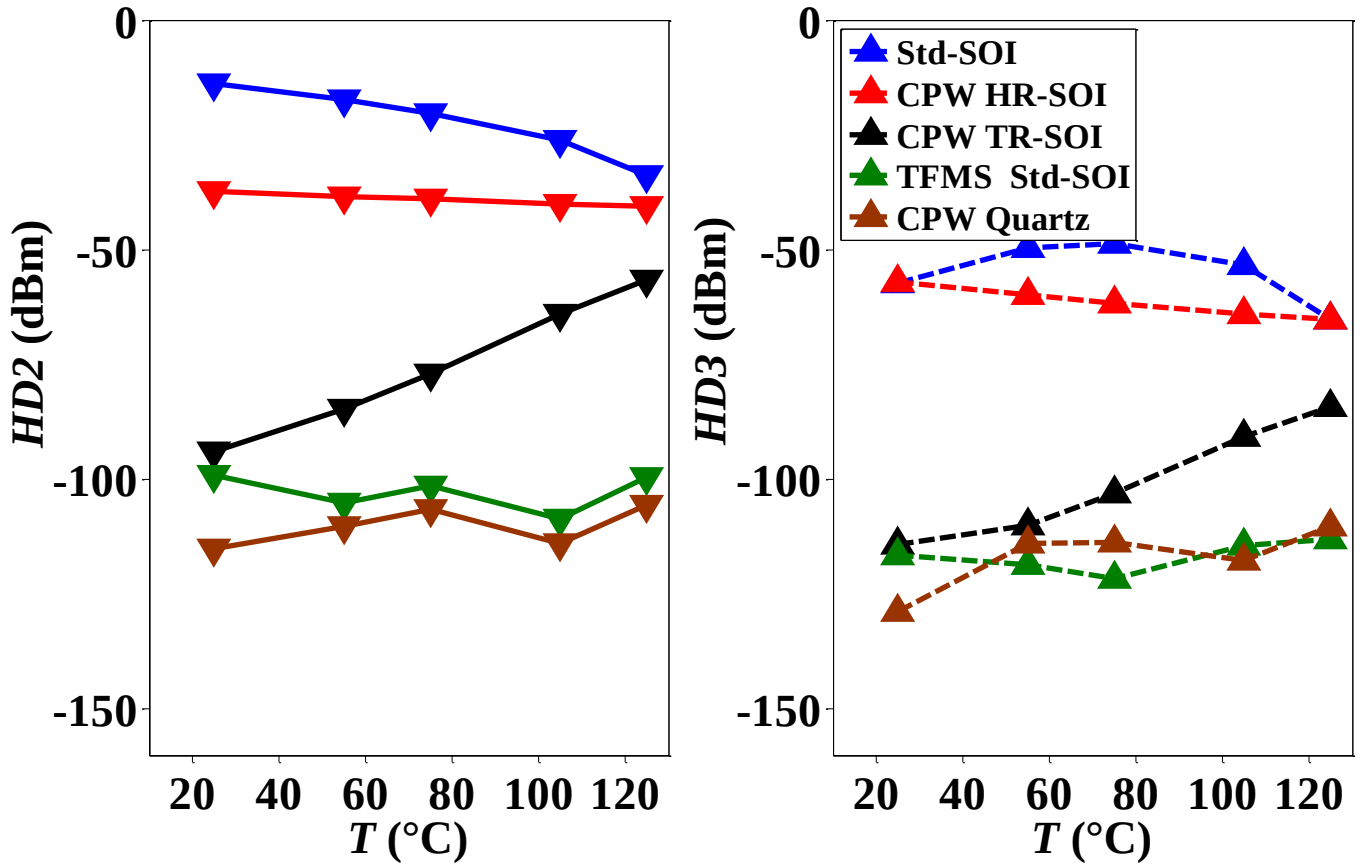
Insertion RF loss at high temperature





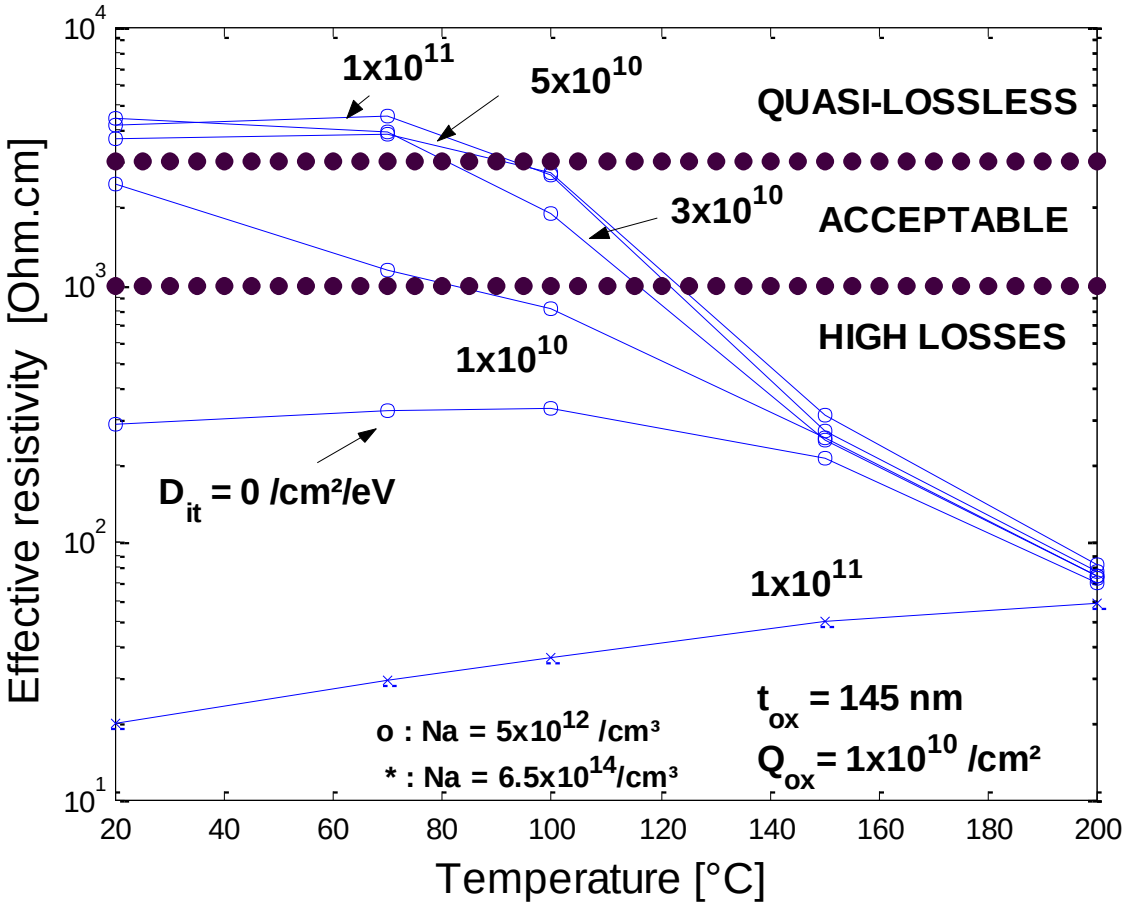
TFMS and CPW technologies show a slight increase of RF insertion losses with temperature (conductor and substrate free carriers)

High temperature effect on substrate linearity



- CPW on TR SOI approaches the non-linear characteristics of CPW on HR SOI above 125°C
- TFMS exhibits a stable non-linearity behavior over a high temperature range

Impact of temperature on the effective resistivity



Simulations

- HR (~3 kΩ.cm) become quasi-lossless up to 100°C when $D_{it} > 5 \times 10^{10}$ /eV/cm^2
- At 200°C, ρ_{eff} is independent on substrate doping (due to n_i increase)

Conclusions

- Due to the ground plane shield TFMS technology provides very low harmonic distortion levels

➡ **Allows use of low cost Std-SOI substrates**

TFMS: a cheap technology for highly-linear RF ICs

- Commercial TR-SOI (eSI HR-SOI from Soitec) demonstrates reduced RF insertion loss, low substrate coupling and better linearity

➡ **TR-SOI (eSI) substrates fulfill the isolation and linearity LTE specifications up to 125°C**