Performance of SOI devices transferred onto passivated HR SOI substrates using a layer transfer technique

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Introduction: High Resistivity (HR) silicon wafers are promising candidates for RF applications due, mainly, to their low cost, CMOS compatibility and substantial substrate loss reduction [1]. However, oxidized HR silicon (such as HR SOI material) is known to suffer from parasitic surface conduction (PSC) below the oxide [2], which can reduce the *effective* resistivity (ρ_{eff}) of the wafers by more than one order of magnitude [3]. This issue can be overcome by introducing a trap-rich passivation layer between the oxide and the Si substrate, such as polysilicon [2]. In this paper we demonstrate for the first time that: (1) polySi substrate passivation can be efficiently realized on an industrial SOI technology using a post-process circuit transfer technique and that: (2) this technique preserves the performance of active devices.

SOI devices transfer onto passivated HR substrates: The investigated SOI devices were initially processed on two distinct wafers at ST Microelectronics using a 0.13 µm Partially-Depleted (PD) HR SOI technology with a buried oxide (BOX) thickness of 400 nm. Only one of the wafers was submitted to a layer transfer process [4] based on direct bonding and mechanical/chemical thinning down (Fig. 1). The initial CMOS wafer was first transferred onto a temporary substrate by bonding and the back side Si substrate was removed. A 300 nm-thick polySi layer was deposited onto the final HR substrate as in [5], prior to an oxide deposition. Both the oxide on the HR substrate and the BOX on top of the temporary substrate were then conditioned and bonded. After removal of the temporary support, initial SOI devices were finally transferred onto a passivated HR substrate with a total buried oxide thickness ranging between 1 and 1.5 µm.

RF performance of passive structures: The efficiency of the passivation was assessed by measuring crosstalk structures (inset of Fig. 2) and CPW lines on both wafers. Fig. 2 displays the crosstalk level ($|S_{21}|$) measured for various DC bias (symmetrically applied on the two signal pads) values. The figure reports significantly higher (~13 dB at 0 V) crosstalk level below 1 GHz and a strong bias dependence for the standard HR SOI (un-passivated) wafer, due to conductive effects in the substrate and PSC [6]. The substrate-passivated wafer on the other hand displays no

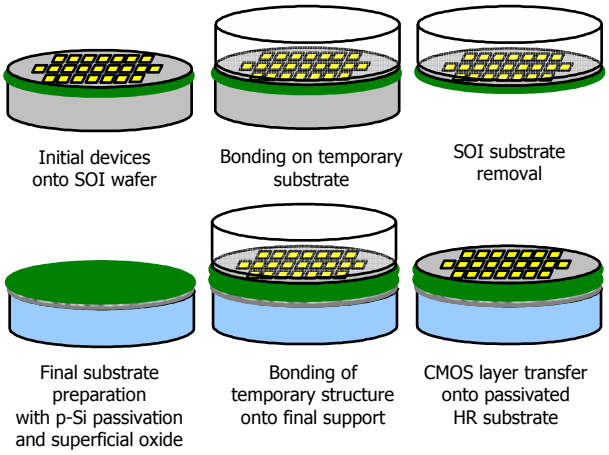

Fig. 1: CMOS layer transfer onto a passivated HR substrate.

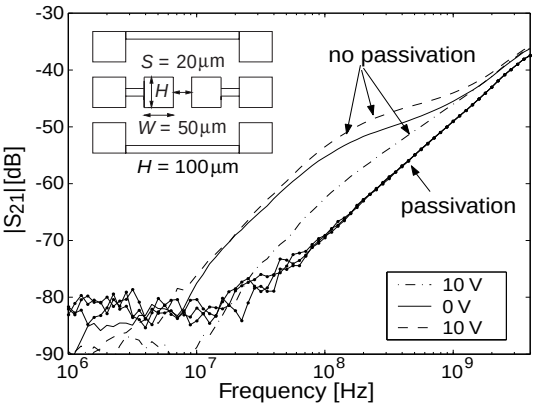

Fig. 2: Measured crosstalk on the passivated and un-passivated HR SOI wafers.

bias dependence and exhibits 20 dB/dec curves, suggesting a purely capacitive coupling in that frequency range and thus, a lossless substrate behaviour. The CPW lines were then measured and the line attenuation constant was extracted using a classical TLR calibration technique. The losses measured on the two wafers are shown in Fig. 3. The figure reports total losses that lie between 0.5 and 1.2 dB/cm higher for the un-passivated wafer. The corresponding values of the substrate effective resistivity (ρ_{eff}) were also extracted according to [3]. They were estimated to be, respectively, 0.6 kΩ.cm and higher than 10 kΩ.cm for the un-passivated and passivated wafers (data not shown). This further

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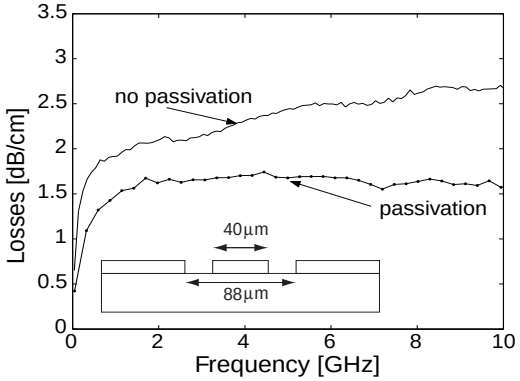

Fig. 3: Total losses measured on the passivated and un-passivated HR SOI wafers.

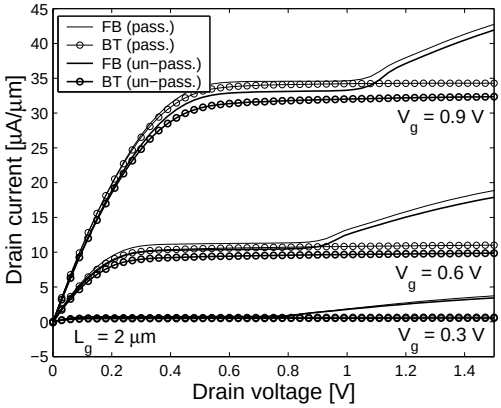

Fig. 4: I_d-V_d curves measured on the 2 µm FB and BT MOSFETs from the passivated and un-passivated HR SOI wafers.

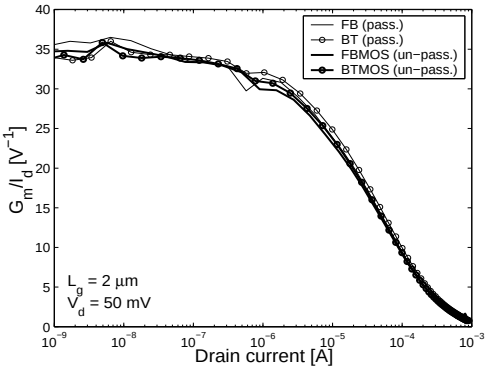

Fig. 5: g_m/I_d curves measured on the 2 µm FB and BT MOSFETs from the passivated and un-passivated HR SOI wafers.

demonstrates the lossless nature of the passivated substrate.

Performance of active devices: Floating body (FB) and body-tied (BT) N-type MOSFETs of 2 µm gate length were measured on the two wafers. The I_d-V_d curves are reported in Fig. 4, in which it can be seen that very similar results were obtained for the two wafers (both qualitatively and quantitatively). The g_m/I_d curves obtained in linear regime (Fig. 5) also outline a very good matching between the two wafers. In particular,

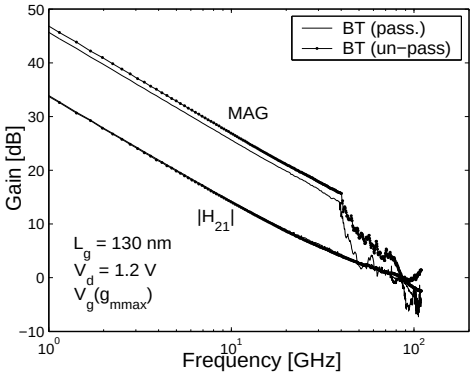

Fig. 6: Current ($|H_{21}|$) and maximum stable (MAG) gains measured on the 0.13 µm FB and BT MOSFETs from the passivated and un-passivated wafers.

identical g_m/I_d ratios were obtained in weak inversion regime, indicating identical body factors and subthreshold slopes. Additional RF measurements were also performed on 0.13 µm-long BT devices. The current and maximum stable gains obtained on the devices are reported in Fig. 6, where it can be seen that similar performance were recorded for both wafers.

Conclusion: We report here an investigation on the performance of RF passive and active devices from a substrate-passivated HR SOI wafer, which was obtained using polysilicon and a processed layer transfer. Crosstalk and CPW line measurements indicate that the passivated substrate behaves as lossless. First time measurements performed on the active devices also suggest that the polysilicon layer below the buried oxide does not affect the DC and RF device performance for the BOX thickness considered here. As substrate passivation of HR Si substrates is crucial to fully enjoy the benefits of HR wafers, these findings provide promising results on the feasibility of achieving truly-high resistivity silicon substrates using a passivation layer that does not affect the performance of active devices. The absence of substrate effects is also expected to be more advantageous in future SOI generations, which will make use of thinner BOX.

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