MicroElectroMechanical Systems in Silicon-on-Insulator Technology

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I. Introduction

MicroElectroMechanical Systems (MEMS) are miniature (micrometric and millimetric in size), multifunctional systems consisting of sensors, actuators, and electronics. They bring mechanical structures to microelectronics. It is the very promising way of building smart integrated tranducers. This technology comes from the integrated circuits microfabrication technologies and thus has access to a large pool of technical and scientific resources. The applications are only limited by our imagination. Right now, applications are found in transportation, domotic, biotechnologies, biomedical engineering, etc. The most popular devices are the pressure sensors and accelerometers used to control air bags in cars.

This last decade CMOS Silicon-on-Insulator (SOI) technology has been demonstrated as a very attractive and competitive technology for designing low-power, low-voltage circuits for harsh environment (high temperature, radiation, etc.) as well as Radio Frequency (RF) applications.

The main objective of our project is related to the development and the characterization of new CMOS-compatible microfabrication processes in order to build low cost, low power, low voltage MEMS for various applications in RF communications, biomedical engineering, domotic, etc.

II. Silicon-on-Insulator Technology

SOI stands for Silicon-on-Insulator. The basic difference with conventional bulk silicon indeed lies in the starting material :

- in bulk Si, the active devices are built atop the surface of a wafer of monocristalline silicon.
- in SOI, the top Si active layer is separated from the underlying mechanical substrate by a thick insulating layer, which leads to a number of advantageous device and circuit properties when compared to bulk Si. Eased CMOS processing, excellent device scalability, better device and circuit performance and potentially lower cost are among the reasons why SOI technology is considered as a serious contender for the fabrication of future integrated circuits [1].

After more than 20 years of steady evolution of the materials, devices and circuit applications, SOI has now reached maturity. SOI technology has indeed evolved from a mere laboratory curiosity in the early '80s to a technology in which large circuits such as 16 Mbit DRAMs or a 550 MHz 1.8 V Power PC microprocessors have been realized. Since August 1998, IBM and other major semiconductor IC

suppliers have announced the industrialisation of their SOI processes [2].
In our laboratories, we have extensively contributed to the demonstration that full-depletion (FD) operation of thin-film SOI MOSFETs may yield quasi-ideal device properties such as sharper subthreshold slope, lower body effect and smaller vertical field mobility degradation [3]. Improved subthreshold slopes in turn allow for the use of lower threshold voltages for identical subthreshold leakage current values. These characteristics all add up to significantly increase the drive capability, in particular for reduced supply voltages.

Over the years, our many circuit developments in FD SOI CMOS have confirmed the technology benefits [3], i.e:
- digital components with enhanced speed and static and dynamic power performance;
- analog components with enhanced speed, precision, power, swing and noise performance;
- and microwave components with enhanced gain, frequency, linearity and power performance over bulk counterparts.

Finally, considering the large range of analog and digital functions that will be required for future high-temperature system implementations, only SOI CMOS may fit the needs. The major limitation of large Si CMOS circuits for high-temperature operation has been linked to static power dissipation and we conclude from the investigation of the leakage current phenomenon in Si CMOS devices and circuits that, regarding the limits of integration,
- bulk Si CMOS may be limited to SSI/LSI components and temperatures of about 175-225°C and require complex design procedures;
- whereas fully-depleted SOI CMOS shows the potential for very large-scale integration of circuits operating above 300°C and designed using standard techniques [4].

The Microelectronics Laboratory runs a complete 0.75 - 2 µm FD-SOI CMOS process on its microfabrication pilot line, which is compatible with standard Bulk CMOS. The thicknesses of the layers are 400 nm for the buried oxide, 80 nm for the silicon and 31 nm for the gate oxide. We have demonstrated that only channel implantations need to be optimized to allow process compatibility both with applications at very low supply voltage (i.e. symmetrical threshold voltages (V_{th}) equal to 0.3-0.4 V at room temperature), and for operation up to 300°C (V_{th} = 0.7 V at 25°C, still above 0.3 V at 300°C). In the latter case, reliability can be improved replacing on-chip Al-metallization with Tungsten (W). For microwave applications, device access series resistances are minimized thanks to a proprietary NiSi self-aligned silicidation process of the source/drain Si and gate polysilicon regions.

III. Microfabrication Technologies

Micromachining techniques are essentially used to create the MEMS mechanical parts. Usually, micromachining process steps come after the fabrication of the analog and digital electronics and are therefore called postprocessing steps. Although microelectronics and micromachining structures are not processed at the same time, micromachining techniques must still be compatible with the integrated circuit manufacture in the sense that it shouldn't damage or affect the electronic devices.
The microfabrication techniques find their origins in microelectronics. They include photolithography, addition, evaporation, deposition, subtraction, dry and wet etching techniques as known in microelectronics which are sometimes slightly modified in order to obtain the right machining tools. Among these procedures we can define three categories: (1) thin film deposition techniques and selective

etching of these (i.e. ***surface (additive) micromachining***), (2) dry and wet etching of bulk silicon substrate (i.e. ***bulk (substractive) micromachining***) and (3) bonding of two or more wafers together for building complex multilayer electromechanical structures (***wafer bonding***). Each of these three micromachining techniques are analyzed, characterized and optimized in our laboratories.

A. Bulk micromachining

Bulk micromachining techniques allow to selectively remove portions of silicon substrate to create micromachined devices. Two etching techniques are currently used: the chemical etching in liquid phase (***wet etching***) and in gaseous phase (***dry etching***) [5].

Wet etching will be anisotropic to create high aspect ratio structures. Three solutions are currently used for wet etching: TMAH (*Tetramethylammonium Hydroxyde*, a strong organic base), KOH (*Alkali-OH*) and EDP (*Ethylene Diamine Pyrochatechol*). TMAH etches preferentially certain crystallographic planes of silicon material and its concentration and temperature control the depth of the etched cavity. Deep cavities or trenches with well-known shape as well as holes through the all silicon wafer thickness can be done with this etchant. TMAH can be also used to realize suspended thin structures such as bridges or membranes by etching the backside of the silicon substrate. An etch stop layer is used to accurately control the final thickness of the etched membrane.
For our applications, we selected this recent technique out of the many strong bases (KOH for example) because it is not as toxic, it does not deposit mobile ion in the silicon oxide (mobile ions such as sodium and potassium would be very damaging to the MOS transistor electrical characteristics) and it etches only slightly most of the materials currently used in microelectronics other than silicon such as polysilicon, silicon nitride, oxide, etc. However, TMAH attacks aluminum interconnections. Since aluminum is generally used to make contact with the external components to the device, it is exposed to the environment at the end of the process fabrication. It is then necessary to protect these metal contact areas from TMAH etching solution by the deposition of insulating (oxide) or driver (gold) layers or by modifying the TMAH solution (introduction of a certain % of Si in TMAH solution) or its conditions of etch in order to make it less aggressive to aluminum. Works in this direction are in progress at the Microelectronics Laboratory in order to find a simple (low cost) and CMOS-compatible wet bulk micromaching process.

The SOI technology is very attractive to manufacture integrated micromechanical structures such as thick suspended membranes. In fact, by only etching the buried oxide of the SOI wafer after patterning, we can release the silicon top acting then as a membrane.

The Microelectronics Laboratory uses a new dedicated maskaligner (K&W MA1006) to allow the double side aligment needed for back etching process.

Dry etching is a well-established pattern transfer technique for the IC technology, characterized by a very good ability to pattern fine and deep lines with a high fidelity of the pattern transfer. The etchant is a gas plasma which can attack the silicon substrate by two ways: either by chemical reactions between silicon and the generated reactive radicals, or physically, by material sputtering from substrate as a result of collisions with the accelerated plasma ions. The Reactive Ion Etching with Inductive Coupled Plasma

Source (ICP-RIE) is a combination between the two mechanisms but with a predominance of the physical erosion with accelerated ions, characterized by very high anisotropy and etch-rate without increasing the energy of the ions bombardment that could damage the selectivity. The aspect ratio will be very high by this method.

We are installing in our cleaning room a new plasma equipment (OXFORD Plasmalab System 100) which combines the PECVD of silicon oxide, nitride and oxi-nitride and the deep etching of silicon by the ICP-RIE technology.

B. Surface Micromachining

Surface Micromachining is a fabrication technique to deposit various films on top of the substrate (only acting as a support) and selectively remove parts of deposited films to create micromachined devices [6]. This approach is attractive because smaller structures can be produced with far better dimensional control (high precision controlled by thickness of the film) compared to bulk micromachining and promotes a capacitive detection. The process would typically use films of two different kinds, a structural material (LPCVD polysilicon, LPCVD or PECVD silicon nitride, thermal or PECVD silicon dioxide, PECVD silicon oxi-nitride, polyimide, tungsten, etc.) and a sacrificial material (commonly oxide but its composition depends on the choice of structural layer). These are deposited and dry etched in sequence. Finally the sacrificial material is wet etched away to release the structure. The more layers, the more complex the structure is, and the more difficult it becomes to fabricate. By this way, we can obtain free-standing micromechanical devices or hermetically sealed cavities.

The main difficulty with surface micromachining techniques is to assure reliable mechanical characterisitics for the structural layer. The mechanical properties of the released layer strongly depend on the residual stress existing in the thin film [7]. The value and the nature (tensile or compressive stress) of the residual stress depend on the nature of the deposited material itself, the deposition process used, the deposition temperature, the tempeature of annealing steps, etc. Consequently, the residual stress is one of the most common properties to be characterized since it affects the device performances. Unacceptable high residual strains may even cause buckling, warpage, or other damages of the structural layer. Test structures have to be designed and built to monitor and characterize residual stress in micromachined structures. Many measurement methods of residual stress in thin films have been developed these last years. A conventional approach involves microstructures for passive strain sensing. These are basically suspended microstructures that deform under residual stresses. These microstructures are fabricated in situ along with the active devices on the same chip. An example of these test structures is the strain sensor composed of a pair of cantilever beams with different lengths connected by a short tip for both tensile and compressive strain measurements. These structures may be analyzed by the ANSYS 5.6 simulator software.

The use of SOI substrate is likely the best way to overcome these remaining difficulties [8]. For piezoresistive detection, the silicon top layer may be used as an active material with the excellent properties of the single-crystalline silicon. Thanks to its very good electrical insulation from the substrate, high temperature sensors (up to 300°C) with low noise and high dynamic range can be obtained.

C. Wafer bonding

Wafer bonding is greatly used in microelectronics laboratories to create SOI structures and in MEMS to form vacuum or gas cavities and channels as well as to fabricate 3D sensors. The most common applications for wafer bonding in MEMS include bonding of the reference pressure chamber in pressure sensors and the holding and interconnection parts in accelerometers. In all those cases, the bonding must be strong and hermetic.
There are actually three different general bonding technologies: Si-Si direct thermal bonding, anodic bonding of silicon to Pyrex glass and bonding through the use of polymers or metals. Each technology has its drawbacks: ***thermal bonding*** has to be done at high temperature (1000°C), ***anodic bonding*** requires the presence of a strong electric field and relatively high temperature (500 kV/m and 400°C) and ***polymer bonding*** is complex and does not seal hermetically [9].

We have tested a strong low temperature Si-Si direct thermal bonding technique compatible with the electronic circuits [10]. The method is described as follows: cleaning the wafers with a RCA solution, alignment and contact of both wafers at atmospheric pressure with our new maskaligner K&W MA1006, vacuum storage at ambient temperature and annealing at 150°C. This bonding method relies on the fact that the bond energy improve when vacuum is made. The main advantages of this method are its simplicity and the fact that only low temperature annealing is needed. The main drawback is the long time of annealing. Indeed, in order to obtain a very strong bond, a 100 hours storage under vacuum is needed, followed by at least 48 hours annealing.

IV. MEMS applications

A. Biological and chemical sensors

Sensors are still the major application thrust of MEMS, particularly for commercial products. A sensor is a device that converts one physical or chemical quantity to electrical one. The chemical sensor is designed to discriminate and measure independently as possible important chemical species such as ions in solutions: protons (pH), Na+, K+ and combustible gases such as CO, H_2, alcohols, propane, and others hydrocarbons, and therefore is worth of interest.

A large proportion of chemical sensors are based on Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The ISFET (Ion Sensitive Field Effect Transistor) was introduced by Bergveld [11] in 1970, exploiting the sensitivity of MOS transistors to surface contaminants. Bergveld used a MOSFET without the metal gate and exposed the gate insulator to an aqueous solution. He found the device sensitive to pH. Both alumina Al_2O_3 and silicon nitride Si_3N_4 are suitable as a pH-sensitive dielectric, due to their lower drift and hysteresis in the long term compared to Si-dioxide gate. An example of commercial pH meters using this sensor is a silicone nitride gate ISFET probe, manufactured by Beckman Instruments, Inc, CA. By coating the gate region with an ion-selective membrane (polymer, borosilicate, LB films), one can make CHEMFETs (Chemical Field Effect Transistor) for detection of other ions (Na^+, K^+, $Ca^{2+,}$ Br^-, Ag^+).

FET-based sensors have also been used for gas detection, the most studied being a FET with a Palladium gate used for hydrogen detection [12], since the H_2 dissolves in the Pd and affects the gate voltage. Gases such as H_2S and NH_3, can be detected with Pd-gated MOSFET, since these molecules can dissociate to produce hydrogen. Dobos and Zimmer [13] developed a similar device with PdO-Pd gate that was lithographically perforated to allow CO gas to access the gate surface. On the other hand, we can find resistive metal-oxide sensors for gas detection. This class of sensors generally uses a semiconducting metal oxide as the tranducer, typically, SnO_2, TiO_2, ZnO, etc. The metal oxide is heated and the gas to be measured interacts with it, changing its resistance.

The biosensors are a special class of chemical sensors that take advantage of the high selectivity and sensitivity of a biological material. Typically, an enzyme (protein), antibody (protein), polysaccharide, or nucleic acid is chosen to interact with the sample to measure. The sensors can be: ISFETs [14] Enzyme in enzyme-sensitive Field Effect Transistors (EnFETs), antibodies or antigens in Immuno-FETs (ImmFETs), microelectrodes, microcalorimeters [15], acoustic wave devices [16], etc.

Recent developments in sensor technology allow to create different integrated and miniaturized biosensor arrays. It's easy to imagine arrays with different enzymes, antibodies, or DNA-probes immobilized precisely onto the tranducer surface for clinical diagnosis or for environmental monitoring. We are developing in collaboration with ARAMIS and the Laboratoire de Biochimie Cellulaire des FUNDP, a DNA-based prototype for clinical analysis. DNA-chip technology requires hybridisation of an unknown nucleotide sequence to an ordered array of known DNA immobilized electrically onto silicon chip which is made by standard microelectronic technology to produce array of Au-electrodes. The hybridisation results are detected by fluorescence and analyzed with fluorescent array scanner. The results are promising and we work on others detection methods to produce a new generation of DNA-chip.

B. Mechanical sensors

Silicon is used for the mechanical sensors, because it combines well-established electronic properties with excellent mechanical properties. There are two major categories of mechanical sensors: piezoresistive and capacitive sensors. The most common applications are pressure sensors, accelerometers and flow sensors. Our laboratory was focused on the piezoresistive pressure sensor which transform a pressure into an electrical differential voltage. It is based on a thin stretched membrane deflected under the difference between upper and lower applied pressures and on a Wheatstone bridge of four piezoresistors stripped on this membrane. The membrane deformation induce a resistance variation in the resistors and then a voltage difference, proportional to the differential pressure applied [10]. The manufacture of this kind of sensors include the silicon micromachining of the cavity contained the reference pressure, the silicon on glass bonding to close the cavity and the control of the silicon membrane's uniformity by the etch stop technique at the buried oxide layer (in SOI technology). All of these techniques are experimented in our laboratory and complete our work on modeling and characterization of piezoresistive sensors for investigating the fabrication of pressure sensors in the future.

C. Microwave and millimeter wave circuits

Vibrating mechanical tank components, such as crystal and surface-acoustic wave (SAW) resonators, are widely used for frequency selection in communication subsystems because of their high quality factor (Q's in the tens of thousands) and exceptional stability against thermal variations and aging. In particular,

the majority of heterodyning communication transceivers rely heavily upon the high Q of SAW and bulk-acoustic mechanical resonators to achieve adequate frequency selection in their radio-frequency (RF) and intermediate-frequency (IF) filtering stages and to realize the required low phase noise and stability in their local oscillators. Ceramic (dielectric) resonators or waveguide components are also required at RF or microwave/millimeter-wave frequencies to provide the needed high-Q functions. In addition, discrete inductors and variable capacitors are sued to properly tune and couple the front-end sense and power amplifiers. At present, the aforementioned resonantors and discrete elements are off-chip components and so must interface with integrated electronics at the board level, often consuming a sizable portion of the total subsystem area. In this respect, these devices pose an important bottleneck against the ultimate miniaturization and portability of wireless transceivers. For this reason, many research efforts have been focused upon strategies for either miniaturizing these components or eliminating the need for them altogether.

The rapid growth of integrated circuit (IC)-compatible micromachining technologies that yield microscale, high-Q tank components may now bring the first of the above strategies closer to reality. Specifically, the high-Q RF and IF filters, oscillators, and couplers, currently implemented via off-chip resonantors and discrete passives, may now potentially be realized on the microscale using micromachined equivalents based on a variety of novel devices, including high-Q on-chip mechanical resonators [17], voltage-tunable on-chip capacitors [18], isolated low-loss inductors [19], microwave/millimeter-wave high-Q filters [20], structures for high-frequency isolation packaging [21], and low-loss micromechanical switches [22]. Once these miniaturized filters and oscillators become available, the fundamental bases upon which communications systems are developed may also evolve, giving rise to new system architectures with possible power- and bandwidth-efficiency advantages. For systems operating past X-band, antennas can also be micromachined with potential cost savings and with additional capabilities attained via active antenna arrays (e.g., phased arrays, power combining, etc.).

Millimeter-wave integrated circuits require low-loss, low-dispersion, planar transmission line structures. Unfortunately, microstrip and coplanar waveguide (CPW) suffer from several problems at microwave and millileter-wave frequencies. These include dielectric loss, which increases with frequency, as well as dispersion, substrate mode problems, and radiation loss, all of which can be directly associated with the air/dielectric discontinuity inherent to substrate-supported transmission lines. Typically, substrate-supported structures rely mainly on substrate thinning to improve millimeter-wave performance of planar circuits. An alternative solution to the frequency limitations of planar circuits is to integrate the antennas, components, and/or transmission lines on a *thin dielectric membrane using bulk micromachining technique*. The development of high-efficiency planar antennas, receivers, power meters and microshield lines (which resemble to a CPW line in free space) using micromachining techniques have been reported in the literature [23], [24]. In addition, the removal of the silicon substrate eliminates any loss associated directly with the dielectric and any dispersion related to the dielectric/air interface, and allows a single mode TEM propagation over a very broad bandwidth. In fact, time-domain electro-optic sampling of a CPW line on a membrane has indicated that these lines are capable of propagating signals at frequencies as high as 2000 GHz (2 THz) with low loss and low dispersion.

Moreover, micromachined high-frequency circuits with integrated packaging offer light weight and controllable parasitics, which makes them appropriate for handheld communication systems and miniature intelligent millimeter-wave sensors where system requirements impose strict limits on electrical performance. Recent advances in semiconductor processing techniques allow for integration in

all of the directions of the three-dimensional space. The capability to incorporate one more dimension, and a few more parameters, in the circuit design, leads to revolutionary shapes and integration schemes. These circuit topologies have reduced ohmic loss and are of free parasitic radiation or parasitic cavity resonances without losing their monolithic character. Integration capabilities are thereby extended and performance is optimized. The evolution of micromachined circuits and antennas for operation in microwave and millimeter-wave frequencies is still in its infancy.

Prof. J.-P. Raskin spent two years at the Radiation Laboratory of The University of Michigan, Ann Arbor, MI, USA. He worked with Prof. Linda Katehi and Gabriel Rebeiz who are worldwide known for their studies about micromachining techniques for building efficient microwave and millimeter-wave circuits [25], [26]. Prof. J.-P. Raskin in collaboration with Prof. B. T. Khuri-Yakub of Stanford University, CA, USA, has analyzed the nonlinear behavior of vibrating membranes for building parametric amplifiers [27]. The gain of these amplifiers is based on the time-varying capacitance of a pumped surface micromachined metallic structure. The application areas are in amplifiers which operate at very high temperatures (200-600 °C), under high particle bombardment (nuclear applications), in non semiconductor-based amplification, and in low-noise systems since parametric amplifiers do not suffer from thermal, shot or *1/f* noise problems.

Prof. J-.P. Raskin came back to the Microwave Laboratory, UCL, in January 2000 and leads research subjects in collaboration with the Microelectronics Laboratory, UCL, concerning the development of micromaching techniques for building passive microwave and millimeter-wave circuits such as planar transmission lines, transitions between various planar technologies (CPW-to-microstrip, for example), high Q inductors, electromagnetic vertical interconnections, etc. The main objective of these research projects is to the development of low-cost, low-power, low-voltage one-chip IC for RF communication systems.

V. Conclusions

Microelectronics and Microwave Laboratories of UCL are working together to progress in the new and promising fields of MEMS. Our theorical and experimental experiences in SOI CMOS technology and our first investigations in the new world of micromachining techniques demonstrate the immense interests of these technologies and their co-integration to meet the specifications of the electronic circuits and transducers for the present and future applications in RF communications, biomedical engineering, domotic, etc…

VI. References

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