AN ASYMMETRIC CHANNEL SOI nMOSFET FOR IMPROVING DC AND MICROWAVE CHARACTERISTICS

M. Dehan, D. Vanhoenacker and J.-P. Raskin

Microwave Laboratory, Université catholique de Louvain
Place du Levant, 3, B-1348 Louvain-la-Neuve, BELGIUM
E-mail: raskin@emic.ucl.ac.be

I. Introduction

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of silicon-based technology and recent progresses of MOSFET's microwave performances [1]-[4], explain silicon success as compared to III-V technologies. Silicon-on-Insulator (SOI) based MOSFET's are very promising devices for multigigahertz applications. Thin-film SOI MOSFET's offer indeed interesting low-voltage performances, higher speed and increased integration density, all with simpler processing than bulk silicon MOSFET's of comparable size [5]. Many recent realizations of logic circuits, memories, and RF circuits [6] have confirmed both the advantages and the viability of thin-film SOI circuits, even in the case of very large systems. As shown in Fig. 1 and 2 the high frequency performances including thermal noise keep increasing by reducing the effective channel length of the MOS transistors. In fact, it can be shown that the cut-off frequencies (f_T and f_{max}) and the high frequency noise parameters (F_{min} and R_n) are at first order approximation inversely proportional to L^2 and L, respectively. The scaling down process of CMOS devices started years ago and it is still improving their DC and high frequency characteristics and, of course, their compactness and power consumption. However, in few years, we are going to reach the limits of the classical photolithographic systems for defining precise and reliable submicrometer structures. In order to overcome those limits or more exactly to push them farther, the asymmetric doped channel MOSFET's presented in [7] can be considered as an attractive solution. The microwave performances of asymmetric and conventional uniformly doped channel Fully Depleted (FD) SOI nMOSFET's are presented and compared in the present paper.

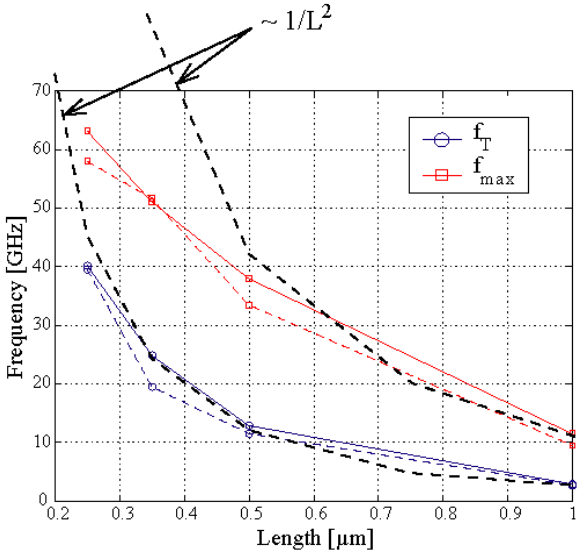

Fig. 1. Cut-off frequencies versus channel gate length for FD (solid line) and PD (dashed line) SOI nMOSFET's at V_{DS} = V_{GS} = 0.9 V. These transistors have been processed by LETI, Grenoble, France.

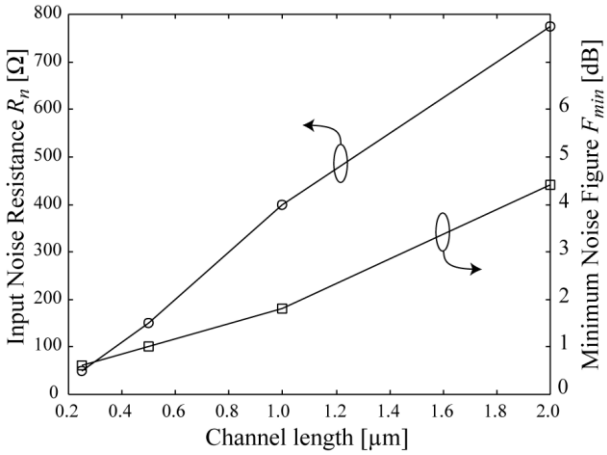

Fig. 2. Minimum noise figure and equivalent input noise resistance versus channel length of FD SOI nMOSFET's at 2 GHz and under V_{DS} = V_{GS} = 0.9 V. These transistors have been processed by LETI, Grenoble, France.

II. Graded Channel FD SOI MOSFET's

Asymmetric doped channel MOSFET's have recently been investigated by several authors in

bulk [8] and SOI technologies as a possible solution for the problems of premature drain break-down, hot carrier effects, and threshold voltage (V_{th}) roll-off issues in deep submicrometer devices. In these works, the doping of the channel region is performed by a tilted ion implantation in the source side after the gate formation. The high concentration at the source end improves the threshold voltage roll-off and drain induced barrier lowering, while the low doping near the drain ensures high mobility, reduced peak electric field, and impact ionization.

Recently, Pavanello *et al.* in [7] have presented a new asymmetrically doped body device, called the graded-channel SOI nMOSFET (GC) shown in Fig. 3. The asymmetric doping profile was obtained by varying the position of the V_{th} implant along the channel, preserving the body region near the drain at natural wafer doping. Contrary to previous reports, the GC SOI processing is fully compatible with the conventional FD SOI MOSFET process flow, with no additional steps needed. Similar to a DMOS [9], the device can be viewed as two sub-devices connected in series: an enhancement mode device at the source side, and a depletion mode device at the drain side, each has a different V_{th} and "channel" length. The effective channel length (L_{eff}), when the device is on, is mainly determined by the GC region, which is much shorter than the physical gate length. As the result, for the same physical gate length, the GC device can provide higher drive current, higher peak transconductance, higher output resistance than a conventional CMOS device with uniformly doped channel, resulting in a high performance device with high cut-off frequency and high gain as demonstrated in next sections.

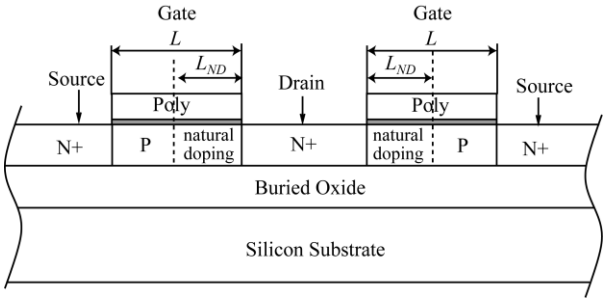

Fig. 3. Cross-section of interdigitized graded channel SOI nMOSFET's.

III. Fabrication process

Uniformly doped (UD) and GC SOI nMOSFET's were fabricated according to 0.5 micron nickel silicided, semirecessed local oxidation of silicon (LOCOS) isolated, SOI complementary metal oxide semiconductor (CMOS) processes in the same p-type Smartcut wafers, starting with a silicon film concentration of 10^{15} cm^{-3}. V_{th} ionic implantation was conventionally performed in the FD devices (boron at dose of 7.10^{11} cm^{-2} and energy of 20 keV), whereas a part of the channel (L_{ND} length) in the drain side was masked in the GC devices, preserving the natural wafer doping (Fig. 3). The same mask used to protect the p-type devices to the n-type V_{th} implant was used to mask the GC channel region and no additional photolithographic step need to be included in the full CMOS processing. The final thicknesses of the gate oxide, silicon film, and buried oxide were 30, 80, and 390 nm, respectively, and channel doping level (implanted region) was approximately equal to 10^{17} cm^{-3}, resulting in a threshold voltage of 0.3 V.

IV. Experimental results

The MOSFET's to be characterized at high frequencies are embedded in a coplanar waveguide (CPW) structure designed to minimize the ground inductance (Fig. 4). Using standards implemented on the SOI wafer, a through-reflect-line (TRL) calibration is performed. As a results, the reference planes are positioned close to the device, effectively reducing the input and output capacitances. More details about the calibration and de-embedding procedure can be found in [10], [11].

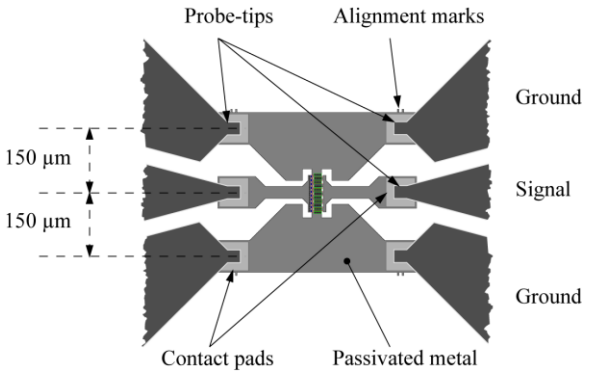

Fig. 4. Top view of on-wafer MOSFET test structure showing the CPW probes, the metallic CPW access lines and the transistor active zone.

The drain current (I_{DS}) is measured as a function of drain voltage (V_{DS}) and for various gate voltage (V_{GS}), for both UD and GC devices (Fig. 5). Comparing devices with almost identical effective channel length, i.e., UD with L = 1 µm

and GC with L = 2 µm and L_{ND}/L = 0.5, and UD with L = 0.6 µm and GC with L = 1 µm and L_{ND}/L = 0.5, it is clear that the GC configuration exhibits superior output characteristics, improving not only the saturation current but the parasitic floating-substrate effects as well. The premature breakdown voltage is increased, whereas the extremely flat saturation current exhibited by the SOI GC, presenting almost zero slope, indicates a tremendous improvement in the output conductance.

From Fig. 5 we extracted the Early Voltages (V_{EA}) of the GC's with similar effective channel than the UD devices (Table I), defining V_{EA} by the linear regression in the internal 1.5 < V_{DS} < 2.5 V. A great improvement in the Early Voltage of the GC devices is obtained due to the reduced channel length modulation provided by the presence of a strong depletion at the undoped region which is especially interesting in mixed analog-digital applications. Also shown in Fig. 5 is the ratio of the drain breakdown voltage for GC and UD transistors. For each effective channel lengths and V_{gs} the breakdown voltage of GC's is always larger than that for conventional UD's.

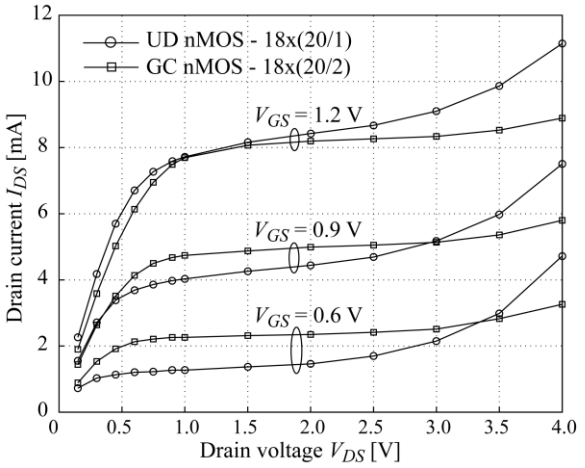

Fig. 5. Measured I_{ds} versus V_{ds} curves for GC and UD SOI nMOSFET's.

Fig. 6 presents the current (H_{21}) and maximum oscillation (MAG) gain for GC and UD SOI nMOSFET's with drawn channel length L = 1 µm and 0.6 µm, respectively. The maximum available gain can be achieved for a stable device when we have simultaneously a complex-conjugate matched load and complex-conjugate matched source.

f_{max} and f_T are defined respectively as the cut-off frequency of MAG and H_{21}, respectively, i.e. the frequency points when, respectively, the MAG and H_{21} equal to 1 (i.e. 0 dB).

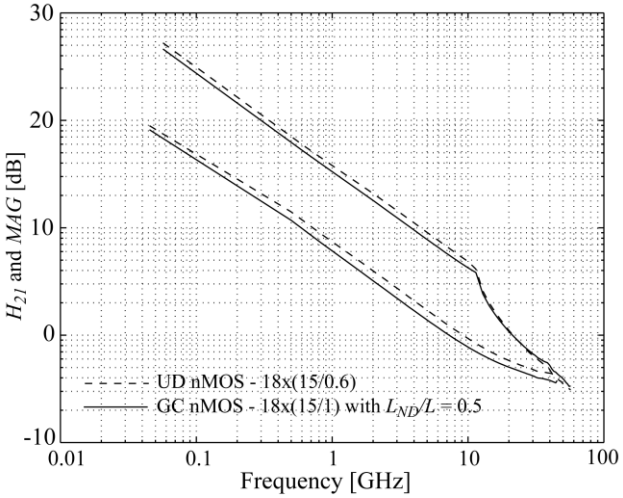

Fig. 6. Measured current gain and maximum oscillation gain for GC and UD SOI nMOSFET's.

	f_T [GHz]	f_{max} [GHz]	V_{EA} [V]
FD 1 µm	5.9	14	- 14
FD 0.6 µm	8.4	22	- 10
GC 2 µm	4.1	10.5	- 50
GC 1 µm	7.0	20.5	- 42

Table I. Extracted Early voltages (V), f_T and f_{max} for GC and UD SOI nMOSFET's. Cut-off frequencies are given at V_{GS} = 1.5 V and V_{DS} = 2.4 V.

Comparing the cut-off frequencies for UD and GC SOI nMOS with the same drawn gate length (L = 1 µm), the interest of asymmetric doped channel for high frequency applications appears clearly. The improvement provided by the GC device (with L = 1 µm and L_{ND}/L = 0.5) reaches 18 % and 46 % for, respectively, f_T and f_{max}, these cut-off frequency values are comparable to those obtained with a UD device with L = 0.6 µm, as shown in Table I. The increase of cut-off frequencies for GC devices is due to the artificial reduction of the effective gate length as explained in Section II. Actually, we can express f_T and f_{max} by the following approximate expressions:

$$f_T = \frac{G_{mi}}{2\pi\left(C_{gs} + C_{gd}\right)} \quad (1)$$

where G_{mi}, C_{gs} and C_{gd} are, respectively, the intrinsic gate transconductance, the gate-to-source and gate-to-drain capacitances.

Sze defines a very useful relationship between f_{max} and f_T in [12]:

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_{ge} C_{gd} + G_{dsi}\left(R_{ge} + R_{se} + R_{gsi}\right)}} \qquad (2)$$

where R_{ge}, R_{se}, R_{gsi} and G_{dsi} are the extrinsic gate and source resistances, the intrinsic non-quasi static gate-to-source resistance, and the output conductance of the transistor.

Approximate expressions (1)-(2) show that while f_T can simply be increased by scaling down the devices, f_{max} depends strongly on the parasitics, as well as on G_{mi} and G_{dsi} which are very sensitive to the drain current and thus V_{GS}.
Table II represents the comparison of the equivalent circuit lumped elements for UD and GC nMOSFET's with similar effective channel length (L_{eff}). It demonstrates that lower f_T for GC devices is due to the increase of the gate-to-drain capacitance (C_{gd}) and the decreases of R_{ge} and G_{dsi} lead to f_{max} values similar to UD devices with same L_{eff}.

UD nMOS	GC nMOS - L_{LD}/L = 0.5
L_{drawn} = 0.5 µm	L_{drawn} = 1 µm
L_{eff} = 0.4 µm	Similar
G_{mi}	Similar
G_{dsi}	Lower (G_{dsi}/10…50)
C_{gs}	Similar
C_{gd}	Higher (~1.5 x C_{gd})
R_{ge}	Lower (~R_{ge}/2)
R_{se}	Similar
f_T	Lower (~20 %)
f_{max}	Similar

Table II. Comparison of equivalent circuit lumped elements for UD and GC with similar effective channel length.

V. Conclusion

Static and high frequency characteristics of GC SOI nMOSFET's have been presented. GC MOS technology described here is fully compatible with mainstream CMOS technology and demonstrates improved performance without aggressively pushing the technology through device scaling to reduce cost.

VI. Acknowledgements

The authors would like to thank the technical staff of the Microelectronics Laboratory, Université catholique de Louvain, Belgium and the technical staff of LETI, Grenoble, France for processing the RF SOI transistors.

VII. References

[1] C. Raynaud *et al.*, "Fully-depleted 0.25 µm SOI devices for low power RF mixed analog-digital circuits", *Proceedings 1998 IEEE International SOI Conference*, October 1998, pp. 67-68.

[2] D. D. Rathman *et al.*, "High frequency performance of a fully depleted 0.25 µm SOI CMOS technology", *1999 IEEE MTT Symposium Digest*, June 1999, pp. 577-580.

[3] J. N. Burghartz *et al.*, "RF potential of a 0.18 µm CMOS logic technology", *1999 IEEE MTT Symposium Digest*, June 1999.

[4] C. Raynaud *et al.*, "Scability of fully-depleted SOI technology into 0.13 µm 1.2 V – 1 V CMOS generation", *Proceedings 1999 IEEE International SOI Conference*, October 1998, pp. 86-87.

[5] J.-P. Colinge, "Silicon-on-Insulator technology: material to VLSI", Boston – Dordrecht – London: Kluwer Academic Publishers, 1991.

[6] M. Goffioul *et al.*, "Microwave integrated CMOS oscillators on Silicon-on-Insulator substrate", *30th European Microwave Week proceedings EuMC'2000 and GAAS'2000*, Paris, France, October 2-6, 2000, pp. 407-410.

[7] M. A. Pavanello *et al.*, "An asymmetric channel SOI nMOSFET for reducing parasitic effects and improving output characteristics", *Electrochemical and Solid-State Letters*, 3 (1) 50-52, pp. 50-52, 2000.

[8] S. Odanaka and A. Hiroki, "Potential design and transport property of 0.1 µm MOSFET with asymmetric channel profile", *IEEE Trans. Electron Devices*, vol. 44, pp. 595-599, April 1997.

[9] M. Hong, "Simulation and fabrication of submicron channel length DMOS transistors for analog applications", *IEEE Transactions on Electron Devices*, vol. 40, pp. 2222-2230, Dec. 1993.

[10] R. Gillon *et al.*, "Determining the reference impedance of on-wafer TLR calibrations on lossy substrates", *26th European Microwave Conference proceedings EuMC '96*, Prague, Czech Republic, September 9-12, 1996, pp. 170-173.

[11] J.-P. Raskin *et al.*, "Accurate SOI MOSFET charateri sation at microwave frequencies for device performance optimisation and analogue modelling", *IEEE Transactions on Electron Devices*, vol. ED-45, no. 5, pp. 1017-1025, May 1998.

[12] S.M. Sze, "Physics of semiconductor devices", Wiley, New York, 1981, pp. 343-347.