Experimental Investigation of RF Noise Performance Improvement in Graded-Channel MOSFETs

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***Abstract*—In this paper, measured RF noise performance of graded-channel metal–oxide–semiconductor (MOS) transistors (GCMOS—also named laterally asymmetric channel transistors) shows impressive reduction in minimum noise figure $(NF_{\min})$ as compared to classical MOSFET transistors (with the same gate length $L_g = 0.5$ μm). The reason is proven to be because of the higher noise correlation coefficient (C). GCMOS also shows lower sensitivity to extrinsic thermal noise as compared to classical MOSFET. Moreover, it is demonstrated that the use of 0.5-μm-gate-length GCMOS gives a competitive RF noise performance as compared to 0.25-μm-gate-length classical nMOS transistors.**

***Index Terms*—Graded-channel metal–oxide–semiconductor (GCMOS), minimum noise figure, noise correlation coefficient, silicon-on-insulator (SOI), transition frequency (f_T).**

I. Introduction

THE IDEA of a graded-channel device was first introduced by DeMassa *et al.* [1], [2] in 1971 and 1973. In 1975, DeMassa and Iyer [3], [4] proposed a closed-form solution for a graded-channel junction field-effect transistor, and they introduced a study of thermal noise in the same device. Later, in 1978, Williams and Shaw [5] presented improved linearity and noise figure using a graded-channel FET. The RF-favored performance of graded-channel devices over classical uniform-doping devices was highlighted in 1980 by Malhi and Salama [6], where they reported a higher cutoff frequency for graded-channel FET.

The metal–oxide–semiconductor (MOS) version of the graded-channel devices was introduced for the first time in 2000 by Pavanello *et al.* [7], and since then, it has been receiving increasing attention. In these devices, the implantation used to adjust the threshold voltage V_T is masked near the drain over a distance $L_{\rm LD}$ [see Fig. 1(a)], yielding a high V_T region near the source in series with a low V_T part adjacent to the drain. The high concentration at the source end improves the threshold-voltage rolloff and drain-induced barrier lowering, while the low doping near the drain ensures high mobility and reduced peak electric field and impact ionization. As a result, a better analog performance is achieved with a better intrinsic gain, owing to a higher dc transconductance (G_m) and a lower output conductance (g_d). In addition, the analog and RF characteristics of the graded-channel MOS (GCMOS) are highly improved with a higher cutoff frequency (f_T) as compared to classical MOSFET transistors [see Fig. 1(b)] [8]–[13].

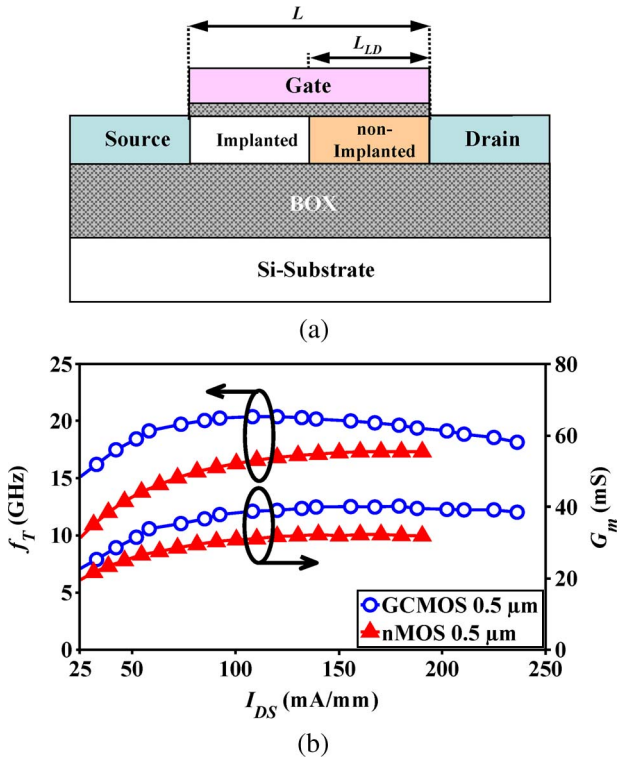

Fig. 1. (a) Cross section of a GCMOS structure. (b) Measured cutoff frequency f_T and dc transconductance G_m as a function of the drain current density for both GCMOS and classical nMOS devices with a channel length of 0.5 μm.

The low-frequency ($1/f$ noise) [14] performance of GCMOS have also been analyzed in order to investigate the ability of this device to integrate in the recent low-power low-noise applications. Using TCAD simulations, Lim *et al.* [15] showed that the minimum noise figure of the laterally asymmetric

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channel MOS should outperform the classical nMOS device due to a higher correlation factor C in the Pucel's model [20]. On the other hand, Roy *et al.* [16] described the noise sources distribution along the channel and showed a higher correlation factor in the case of GCMOS transistor as compared to classical nMOS. To our knowledge, an improvement of RF noise trend was never observed experimentally before this paper.

This paper investigates the RF noise performance of GCMOS in comparison to classical nMOS from an experimental, a modeling, and an analytical point of view. Section II starts by providing a description of the measurement setup and the devices analyzed in this paper. Section III presents the experimental results of the noise performance obtained for GCMOS as well as for the classical nMOS in the intrinsic case after removing the effect of extrinsic elements. This is followed by an analytical explanation of these results based on the extraction of noise-model parameters and analytical formulations. Section IV concerns the extrinsic noise performance of these two devices and their sensitivity to the thermal noise of extrinsic resistances. Finally, the impact of device downscaling on noise performance is presented, showing the advantages of GCMOS for low-noise applications.

II. Measurement Setup and Devices

A. Measurement Setup

Standard dc and RF characteristics are measured, at room temperature, using an HP4142B semiconductor parameter analyzer and an HP8510C vector network analyzer controlled by ICCAP 2006B software. Noise parameters are measured using a mechanical tuner system from Maury Microwaves in the 1–8-GHz frequency range.

B. Devices Under Test

The devices measured in this paper are all fabricated on a partially depleted silicon-on-insulator 0.25-μm technology. Results presented in this paper are for classical nMOS devices of 0.25 and 0.5 μm and for GCMOS devices of 0.5-μm channel lengths. All devices feature gates with 12 fingers each of which has a 13.2-μm width. The silicon-film, the buried-oxide, and the gate-polysilicon thicknesses are, respectively, 100, 400, and 200 nm. The ratio of the low-doped channel length to the total channel length $(L_{\rm LD}/L)$ is approximately 0.5 [13]. The threshold voltage is 0.4 V in case of $L = 0.5$ μm (for both GCMOS and classical nMOS) and 0.5 V in case of $L =$ 0.25 μm classical nMOS devices. All noise measurements are performed while keeping the transistor in saturation ($V_{\rm DS} =$ 1.2 V) and varying $V_{\rm GS}$ from 0.5 to 1.5 V.

III. Intrinsic Noise Performance

The intrinsic experimental noise performance is first presented in this section in order to provide a basic understanding of the advantage of using GCMOS devices over classical nMOS devices.

Tuner measurements give the four noise parameters ($NF_{\rm min}$, R_n, and $Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt}$) for each device and at each selected frequency point, where $NF_{\rm min}$ is the minimum noise figure, $Y_{\rm opt}$ is the optimum source admittance, and R_n is the equivalent noise resistance (a quantity which shows the effect of a nonoptimum source admittance on the noise figure of the device).

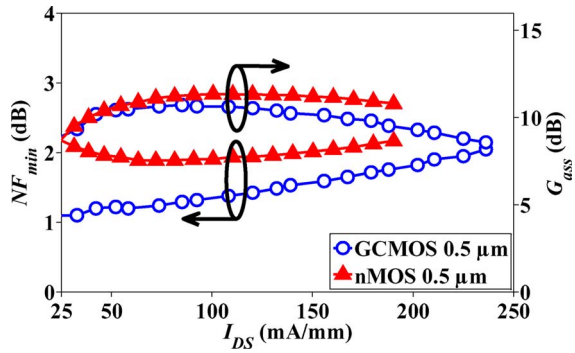

Fig. 2. Intrinsic minimum noise figure $NF_{\rm min}$ and intrinsic associated gain $G_{\rm ass}$ as a function of drain current density for both GCMOS and classical nMOS of 0.5-μm channel length (at 6 GHz).

First, a one-step (open) de-embedding procedure is applied to withdraw the pad parasitic network influence on noise parameters using a correlation matrix technique. Next, the procedure using [18] is used to remove the effect of the Nyquist noise in the extrinsic resistances (R_g, R_d, and R_s) and, thus, obtain what we refer to as intrinsic-noise parameters. Extrinsic resistances are extracted from measured S-parameters using Bracale's method [19] ($R_g = 3.8$ Ω and $R_s = 3.3$ Ω for both GCMOS and classical nMOS).

A. Intrinsic-Noise Parameters

Figs. 2 and 3 show the intrinsic-noise parameters as a function of drain current density $I_{\rm DS}$. The intrinsic minimum noise figure $NF_{\rm min}$ (Fig. 2) of GCMOS device shows an interesting reduction as compared to the intrinsic $NF_{\rm min}$ of classical nMOS device, both of which have the same geometry. This better noise performance is more pronounced in the low-current region, which is interesting for low-power low-voltage applications. However, the intrinsic associated gain $G_{\rm ass}$ (Fig. 2) of GCMOS shows relatively lower performance as compared to classical nMOS.

In the low-power low-voltage regime of operation, slightly lower $G_{\rm opt}$ and $|B_{\rm opt}|$ are observed in the case of GCMOS [Fig. 3(a)], which is indicative of a slightly greater difficulty in satisfying noise matching. However, R_n [Fig. 3(b)] is lower for GCMOS, yielding a lower sensitivity of noise-figure mismatch from optimum source impedance.

These intrinsic results are in complete accordance and provide experimental evidence of trends described in [15] where the authors used TCAD simulations.

B. PRC Noise Parameters

In addition to the four intrinsic noise parameters presented earlier for both devices, the extraction of Pucel's three-parameter (P, R, and C) noise model [20], [21] is of interest and should provide more insight in understanding this favored noise performance of GCMOS over classical nMOS device.

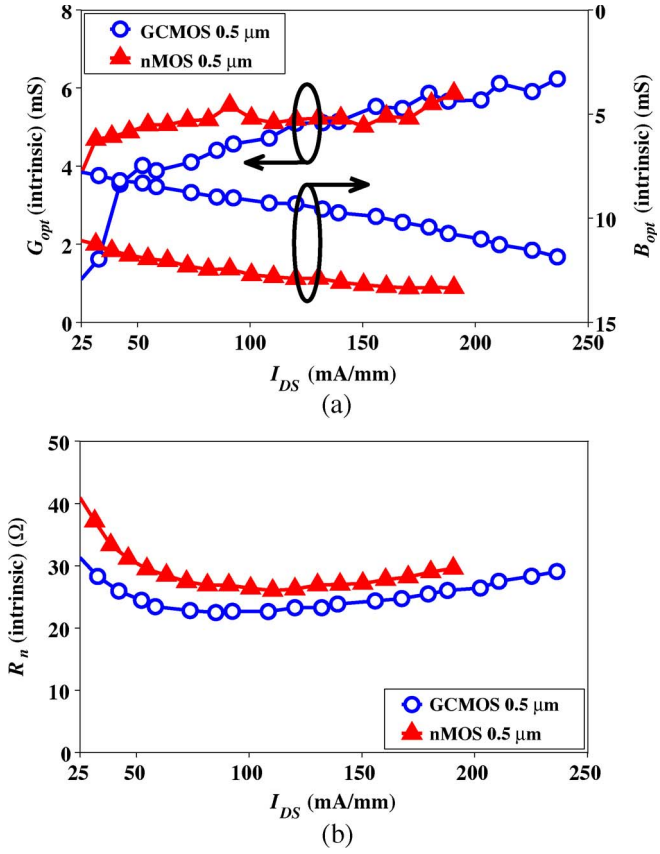

Fig. 3. (a) Intrinsic optimum noise conductance $G_{\rm opt}$ and susceptance $B_{\rm opt}$. (b) Intrinsic R_n variation as a function of drain current density for both GCMOS and classical nMOS of 0.5-μm channel length (at 6 GHz).

PRC noise parameters can simply be obtained from induced gate noise current ($\overline{i_g^2}$), drain noise current ($\overline{i_d^2}$) and their cross correlation ($\overline{i_g i_d^*}$) [22], and intrinsic admittance parameters (Y_{11} and Y_{21})

$$\overline{i_g^2} = 4kT_a \frac{|Y_{11}|^2}{|Y_{21}|} R\Delta f \tag{1}$$

$$\overline{i_d^2} = 4kT_a |Y_{21}| P\Delta f \tag{2}$$

$$\overline{i_g i_d^*} = jC\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \tag{3}$$

where T_a is the ambient temperature. Throughout, it is assumed that T_a is equivalent to the standard noise temperature T_0, thus $T_a = T_0 = 290$ K.

P, R, and C are dimensionless, and they depend on the physical properties of the device. They are bias-dependent and are frequency-independent. Fig. 4 shows the PRC noise parameters as a function of drain current density.

The value of P is somewhat similar for both devices while the value of R is higher for GCMOS, indicating a higher capacitive coupling between the diffusion channel noise and the gate. Higher values of C for GCMOS are clearly observed (nearly double the values of C for the classical nMOS), which is the main reason as why GCMOS $NF_{\rm min}$ outperforms the nMOS one. This fact is discussed in detail in the next section.

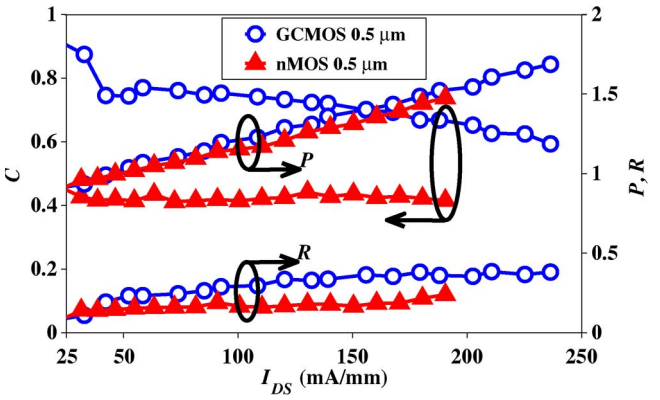

Fig. 4. Three-parameter noise model comparison between both GCMOS and classical nMOS of 0.5-μm channel length (extracted at 6 GHz) as a function of drain current density.

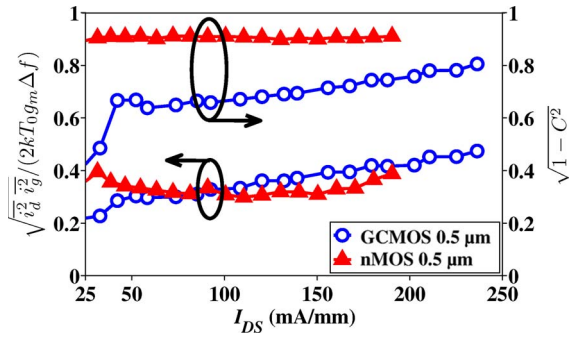

Fig. 5. Verification of the effect of the correlation factor C in both GCMOS and classical nMOS of 0.5-μm channel length (at 6 GHz).

C. Analytical Expressions

1) $NF_{\rm min}$: The analysis of the previously shown intrinsic results is based on the following analytical formula [23][1]:

$$NF_{\rm min} = 1 + \frac{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}{2kT_0 g_m \Delta f}\sqrt{1-C^2} \tag{4}$$

where g_m is the intrinsic transconductance calculated from the real part of the intrinsic admittance parameter Y_{21}.

The second term of (4) can be regarded as the product of two parts, i.e., $\sqrt{\overline{i_g^2}\,\overline{i_d^2}}/2kT_0g_m\Delta f$ by $\sqrt{1-C^2}$. By plotting both parts as a function of drain current density (Fig. 5), it is clear that $\sqrt{\overline{i_g^2}\,\overline{i_d^2}}/2kT_0g_m\Delta f$ (left axis) is quite similar for both devices while $\sqrt{1-C^2}$ (right axis) shows an obvious difference between GCMOS and classical nMOS. Therefore, the origin of better $NF_{\rm min}$ performance for GCMOS as compared to classical nMOS is clearly related to the higher correlation coefficient C in the case of GCMOS.

2) $G_{\rm ass}$: It is possible to express the intrinsic associated gain $G_{\rm ass}$ as follows (see the Appendix):

$$G_{\rm ass} = \frac{f_{\rm Ti}}{f}\frac{\sqrt{1-C^2}}{C}\frac{C_{\rm tot}}{C_{\rm gd}} \tag{5}$$

[1]It should be noted that the formula for $NF_{\rm min}$ in [15] is also derived from this formula.

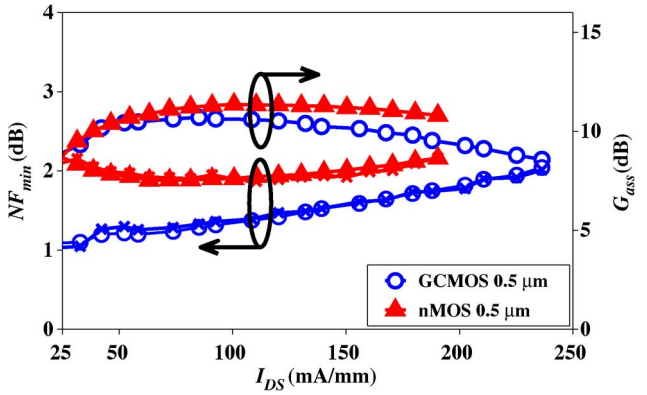

Fig. 6. Extrinsic minimum noise figure $NF_{\min}$ and extrinsic associated gain $G_{\rm ass}$ as a function of drain current density for both GCMOS and classical nMOS of 0.5-μm channel length at 6 GHz. $NF_{\min}$ calculated from (6) is shown in x shapes.

where $f_{\rm Ti}$ is the intrinsic cutoff frequency ($f_{\rm Ti} = g_m/2\pi C_{\rm tot}$), $C_{\rm tot}$ is the total input gate capacitance, and $C_{\rm gd}$ is the gate-to-drain capacitance. Equation (5) shows that higher values of C contribute to the decreasing values of $G_{\rm ass}$, as confirmed in Fig. 2. Yet, due to the higher $f_{\rm Ti}$ of GCMOS as compared to classical nMOS [Fig. 1(b)], only a relatively small decrease in $G_{\rm ass}$ is observed for GCMOS as compared to classical nMOS.

IV. Extrinsic Noise Performance

The previous investigation showed a favorable noise performance of GCMOS over classical nMOS in its intrinsic form. This trend should be confirmed by looking at the extrinsic noise parameters, based on raw measurements without removing the effect of extrinsic resistances. They are obtained directly from Tuner measurements (after open de-embedding). Minimum noise figure $NF_{\min}$, as well as associated gain $G_{\rm ass}$, is shown in Fig. 6. The difference between $NF_{\min}$ of GCMOS and nMOS shown in Fig. 6 is found to be bigger as compared to its intrinsic case (Fig. 2). It can also be seen that associated gain $G_{\rm ass}$ is reduced more in classical nMOS relative to GCMOS when comparing extrinsic to intrinsic cases.

The difference in the sensitivity of $NF_{\min}$ to the thermal noise of the extrinsic resistances between GCMOS and classical nMOS can be explained using the formula [21]

$$NF_{\min} = 1 + \frac{2f}{f_{\rm Ti}} \times\sqrt{PR(1-C^2) + (P+R-2C\sqrt{PR})(R_g+R_s)g_m}. \quad (6)$$

In order to check its accuracy, a comparison of (6) with experimental data is shown in Fig. 6. The impact of extrinsic resistances is quantified by the term $(P+R-2C\sqrt{PR})(R_g+R_s)g_m$. Given the higher correlation factor C in the case of GCMOS as compared to classical nMOS, the lower impact of thermal noise featured by extrinsic resistances (R_g and R_s) on GCMOS $NF_{\min}$ is obvious.

This important result shows that the benefit of higher C for $NF_{\min}$ is not limited to the intrinsic noise contribution [i.e., $PR(1-C^2)$ in (6)] but it also affects the sensitivity of $NF_{\min}$ to the thermal noise of the extrinsic resistances.

TABLE I
Sensitivity of Noise Parameters to Extrinsic Resistances in Both GCMOS and Classical NMOS of 0.5-μm Channel Length

		NF_{min} (Linear)	G_{ass}	G_{opt}	$\lvert B_{opt}\rvert$	R_n
GCMOS	Intrinsic	1.197	11.03	3.91	8.29	24.77
	Extrinsic	1.322	10.37	4.66	6.69	31.75
	Δ%	10.4	-5.98	19.2	-19.3	28.2
nMOS	Intrinsic	1.336	12.76	4.95	11.85	30.42
	Extrinsic	1.565	10.53	6.24	9.7	37.78
	Δ%	17.1	-17.5	26.1	-18.14	24.2

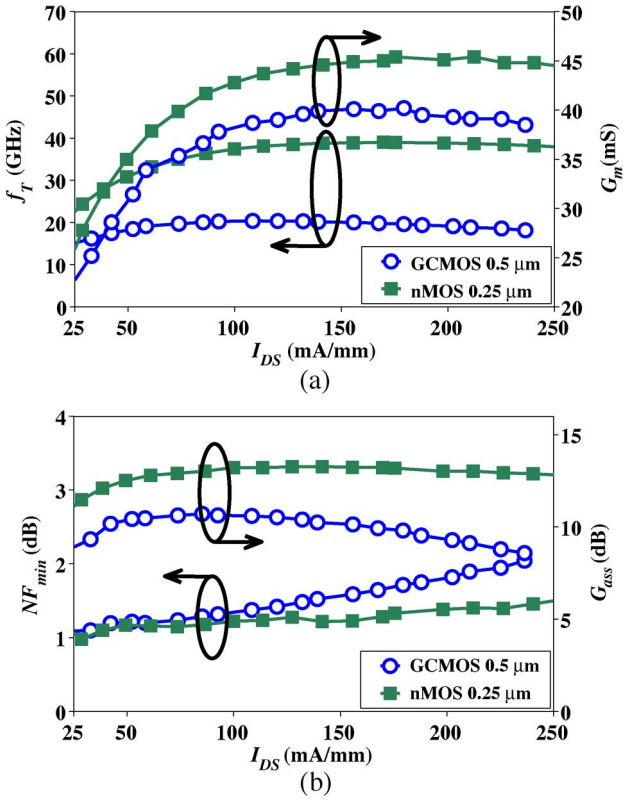

Fig. 7. (a) Cutoff frequency f_T and dc transconductance G_m variation with drain current density for 0.5-μm GCMOS and 0.25-μm classical nMOS. (b) Extrinsic minimum noise figure $NF_{\min}$ and extrinsic associated gain $G_{\rm ass}$ for the two devices of (a).

To have a complete picture, a comparison between all noise parameters in their extrinsic and intrinsic forms, as well as the percentage of change in each parameter (relative to the intrinsic case), is summarized in Table I, where values are given at a frequency of 6 GHz and $I_{\rm DS} = 50$ mA/mm.

V. RF Noise Trend: Perspective for Scaled GCMOS

As shown in Fig. 7(a), the 0.5-μm-gate-length GCMOS shows lower f_T and G_m than the 0.25-μm-gate-length nMOS devices. Nevertheless, the minimum noise figure of 0.5-μm GCMOS competes with the 0.25-μm nMOS, as shown in Fig. 7(b) (particularly for $I_{\rm DS}$ lower than 100 mA/mm). At $I_{\rm DS} = 50$ mA/mm, the 0.25-μm classical nMOS features f_T of 31 GHz, nearly double that of the GCMOS (~18 GHz),

whereas both values of $NF_{\min}$ are almost the same, i.e., 1.17 and 1.21 dB, respectively, at 6 GHz. This interesting scaling trend is explained by the lower sensitivity of GCMOS to extrinsic thermal noise effects described earlier.

One may argue that these similar values of $NF_{\min}$ are due to the fact that the value of R_g for the 0.25-μm classical nMOS is twice that of the 0.5-μm GCMOS, i.e., 7.6 and 3.8 Ω, respectively. However, it should also be noted that the value of f_T of the classical nMOS is almost twice that of the GCMOS. Therefore, it is expected that the downscaling would have a greater impact on the increase of f_T while keeping very low values of $NF_{\min}$ in the case of GCMOS by comparison with the classical nMOS device.

VI. Conclusion

Channel engineering, as presented in this paper using the GCMOS concept, proves to be very useful in enhancing RF noise performance. The experimental extraction of the PRC noise parameters has confirmed that this interesting behavior is related to the increased correlation coefficient C in GCMOS devices, which then leads to a reduction in minimum noise figure $NF_{\min}$. Although a slight reduction in associated gain $G_{\rm ass}$ was noticed for GCMOS devices, this will not affect low-power applications, as it starts to become critical only at higher currents. It has also been shown that this higher correlation coefficient C means that $NF_{\min}$ is less sensitive to the thermal noise in the case of GCMOS by comparison with the case of the classical nMOS device. Finally, the scaling advantage of GCMOS has been clearly highlighted, thus enabling the design of low-noise circuits at lower costs using currently well-understood and stable technologies.

Appendix

The general equation that describes associated gain in FETs was previously introduced as [24]

$$G_{\rm ass} = \frac{|Y_{21}|^2 \mathrm{Re}(Y_{\rm opt})}{|Y_{11}+Y_{\rm opt}|^2 \mathrm{Re}(Y_{\rm out})} \tag{A.1}$$

where $Y_{\rm out}$ is the output admittance and expressed as

$$Y_{\rm out} = \frac{Y_{11}Y_{22} - Y_{12}Y_{21} + Y_{22}Y_{\rm opt}}{Y_{11}+Y_{\rm opt}}. \tag{A.2}$$

The intrinsic admittance matrix of the transistor can be calculated from Fig. 1(b) as

$$Y = \begin{bmatrix} j\omega(C_{\rm gs}+C_{\rm gd}) & -j\omega C_{\rm gd} \\ g_m & g_d + j\omega(C_{\rm ds}+C_{\rm gd}) \end{bmatrix} \tag{A.3}$$

while $G_{\rm opt}$ and $B_{\rm opt}$ are expressed as [22]

$$G_{\rm opt} = \omega C_{\rm tot}\sqrt{\frac{R}{P}}\sqrt{1-C^2} \tag{A.4}$$

$$B_{\rm opt} = \omega C_{\rm tot}\left(C\sqrt{\frac{R}{P}} - 1\right). \tag{A.5}$$

It is easier to analyze (A.1) part by part, thus

$$\begin{aligned} |Y_{11}+Y_{\rm opt}|^2 &= |j\omega C_{\rm tot} + G_{\rm opt} + jB_{\rm opt}|^2 \\ &= \omega^2 C_{\rm tot}^2 \frac{R}{P} \end{aligned} \tag{A.6}$$

$$\begin{aligned} Y_{\rm out} = g_d &+ \frac{j\omega C_{\rm gd} g_m}{j\omega C_{\rm tot} + G_{\rm opt} + jB_{\rm opt}} \\ &\times \frac{G_{\rm opt} - j(\omega C_{\rm tot} + B_{\rm opt})}{G_{\rm opt} - j(\omega C_{\rm tot} + B_{\rm opt})}. \end{aligned} \tag{A.7}$$

Therefore

$$\begin{aligned} \mathrm{Re}(Y_{\rm out}) &= \frac{g_d \omega^2 C_{\rm tot}^2 \frac{R}{P} + \omega^2 C_{\rm gd} C_{\rm tot} g_m C\sqrt{\frac{R}{P}}}{\omega^2 C_{\rm tot}^2 \frac{R}{P}} \\ &\approx \frac{C_{\rm gd}}{C_{\rm tot}} . \frac{g_m \cdot C}{\sqrt{\frac{R}{P}}}. \end{aligned} \tag{A.8}$$

Then, applying (A.4)–(A.8) into (A.1), the intrinsic associated gain can be expressed as

$$G_{\rm ass} = \frac{f_T}{f}\frac{\sqrt{1-C^2}}{C}\frac{C_{\rm tot}}{C_{\rm gd}}. \tag{A.9}$$

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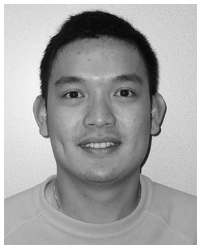

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