An investigation of High Temperature Effects on CPW and MSL on SOI Substrate for RF Applications

Mehdi Si Moussa[(1)], *Member, IEEE,* Christophe Pavageau[(2) (3)], *Member, IEEE,*
Dimitri Lederer[(1)], Laurence Picheta[(2)], François Danneville[(2)], *Member, IEEE,*
Jean-Pierre Raskin[(1)], *Member, IEEE,* Nicolas Fel[(3)], Jean Russat[(3)]
and Danielle Vanhoenacker-Janvier[(1)], Senior *Member, IEEE,*

(1) EMIC, Microwave Laboratory, Place du Levant 3, Louvain-La-Neuve, 1348, Belgium.
(2) IEMN-UMR CNRS 8520, Cité Scientifique, 59652 Villeneuve d'Ascq, France.
(3) CEA-DIF, BP 12, 91680 Bruyères-le-Châtel, France.
simoussa@emic.ucl.ac.be

Abstract — One of the main markets for Silicon-on-Insulator (SOI) devices is the high-temperature applications. In the last decade, the technology advances to deep submicron to improve device performances in term of cut-off frequency. Practical application of integrated circuits requires the consideration of a wide temperature range, and transmission lines are widely used in MMIC's as interconnects and matching networks. Therefore, there is a need to investigate the performances of the transmission line structures on SOI substrate in a wide temperature range, as a function of frequency.

The behaviour of 50 Ω microstrip (MSL) and coplanar waveguide (CPW) transmission line topologies versus temperature is presented.

Index Terms **— CMOS, MMIC, Silicon-on-Insulator, MSL, CPW, Standard and high resistivity, High temperature effect.**

I. Introduction

Large scale commercial applications, such as cellular communications require substrates that are low-cost, easy to manufacture and capable of being integrated with digital technology. Silicon substrate is a good candidate for these applications even if it suffers from dielectric losses.

One of the main challenges in silicon process is not anymore high performance transistors but ultra low loss passives, and especially transmission lines for achieving higher frequency and gain performances [1]. Some applications (well logging, avionics, automotive ...) require electronic circuits capable of operating at temperature up to 300°C. The capability of SOI circuits to expand the operating temperature range of integrated circuits up to 250°C has been demonstrated [1][2]. Thanks to its buried oxide (Box) as well as the fact that the transistor channel is defined in thin silicon layer. SOI devices and circuits present advantages in this field over bulk counterparts such as the absence of thermally-activated latch-up and reduced leakage current at the source-body and drain-body junctions.

Transmission lines can be implemented using thin film microstrip (MSL) or coplanar waveguide (CPW) lines in 6 metal layers technology. For the MSL, metal1 and 2 were used for the ground plane and metal6 for the signal line. The CPW is implemented on metal6 layer. Both configurations on 130 nm SOI process were modelled through full-wave EM simulations with HFSS Ansoft software environment. Correctness of line description in HFSS was ascertained by comparison with S-parameters measurements of MSL with an excellent agreement between simulation and measurements [3].

In the next paragraphs, the behaviour of both transmission line topologies, MSL and CPW, versus frequency and temperature is presented and compared. These transmission lines were built on standard and high resistivity silicon substrates.

On-wafer measurements were performed on the MSL and CPW, with a Anritsu 37369A™ vector network analyzer operating up to 40 GHz. Temperature control is provided by a Temptronics 8-in temperature chuck up to 250°C. 100 µm-pitch ground-signal-ground (GSG) high frequency coplanar Z Probes from Süss™ have been used for signal measurement. The measurements were done over the temperature range from 25°C to 250°C.

II. Microstrip lines

Microstrip lines (MSL) are made of a conductor, lying on a thin dielectric layrer above a ground plane. Fig. 1 shows the cross section of the line. MSL were realized on high resistivity (HR) and standard resistivity (STD) SOI wafers. Six metal layers+alucap layer were available on the 130 nm SOI process.

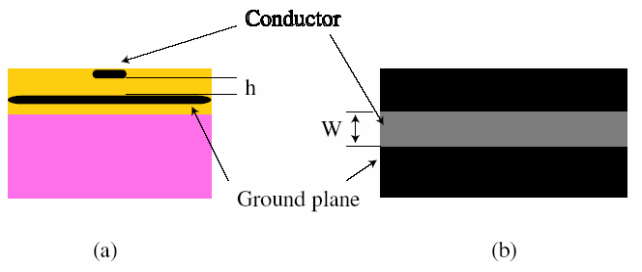

Fig. 1: MS lines: (a) cross-section and (b) top view.

In a MSL structure, the ground plane avoids coupling between the signal and the lossy silicon substrate. Thus, the properties of MSL are independent on the substrate resistivity, and the conductor losses are dominant.
For our study, we have drawn 4 MSL structures with different widths as summarized in Table I:

MSL structures	Metal width W (µm)
M6+Alucap	7
M6	7
M6	2
M6+Alucap	5
M6+Alucap	9

Table I: The drawn MSL structures.

Each structure contains 800 µm MS line, a thru line, a short and an open (Fig. 2). These structures allow the extraction of the losses using a TRL de-embedding method.

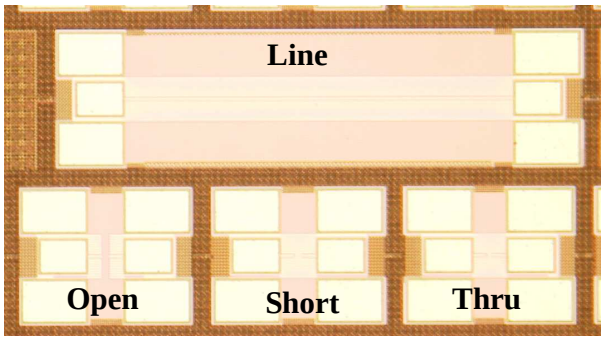

Fig. 2: Chip microphotograph of the designed MSL calibration kit.

The MS Lines were implemented using the upmost 0.9-µm-thick metal 6 layer as signal conductor, and using metal 1 and metal 2 layers stacked together to form the ground plane. The total dielectric layer thickness is 3 µm. It is composed of a multilayered structure of silicon dioxide and silicon nitride spacers, as shown in Fig. 3.

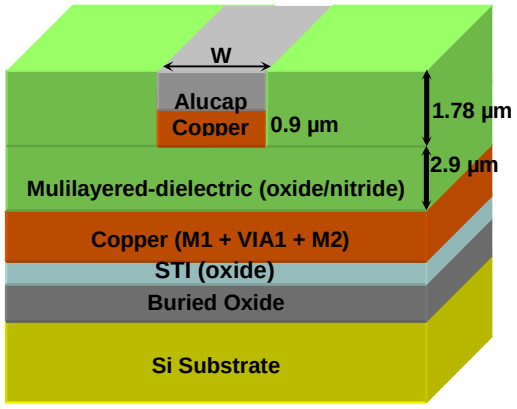

Fig. 3: Geometry of MSL.

Fig. 4 shows the losses versus frequency for various available MSL geometries. As expected, the line losses increase with the reduction of the conductor width.

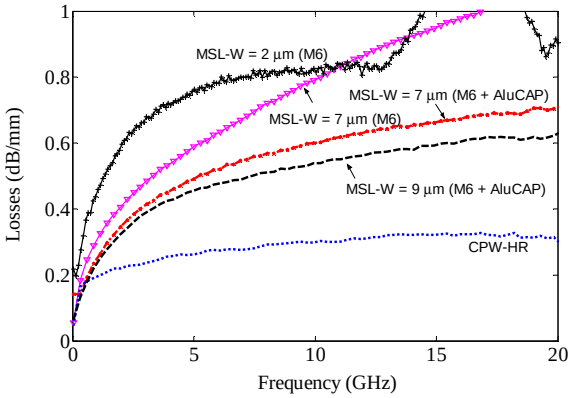

Fig. 4: Measured losses for various MSL line geometries.

2 versions of the 7 µm-wide MSL structures were designed, for one the signal conductor is made only in metal 6 and the other in stacking metal 6 and an extra Al layer (Alucap) of 0.88 µm.
The use of the Alucap layer enables a reduction of 33% of the losses at 20 GHz.

In MSL, the back ground plane shields the Si substrate and therefore avoids coupling between the signal and the lossy substrate. Thus the electrical characteristics of MSL are independent on the substrate resistivity, as shown in Fig. 5. Consequently, the MSL allows the use of standard resistivity (20 Ω.cm) SOI substrates.
Furthermore, compared to coplanar transmission lines, microstrip lines are preferred since they have a higher effective inductance per length. Thus, the lines can be kept compact.
In order to study the behaviour versus temperature, the measurements were performed over the temperature range from 25 to 250°C.

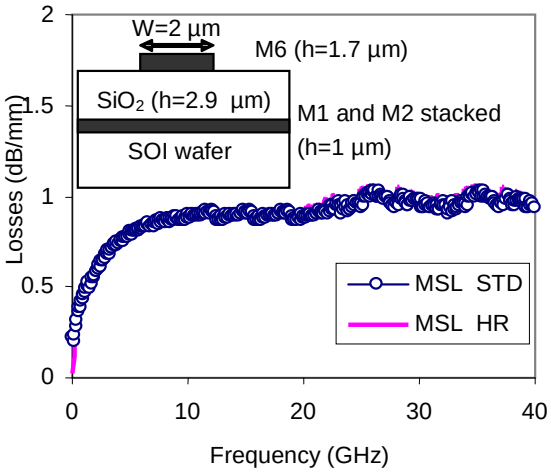

Fig. 5: Losses versus frequency for MSL lying on standard (STD, 20 Ω.cm) and high (HR, >1000 Ω.cm) SOI substrates.

Using a classical TRL de-embedding method, the lineic losses were extracted as shown in Fig. 6, the measurements done on the MSL show an increase of 80% of the lineic losses with respect to temperature which is due to the positive temperature coefficient of the metallic strip. The temperature dependence of resistivity is often represented by the empirical relationship:

$$\rho(T) = \rho_0 + k(T - T_0)$$

where ρ_0 is the resistivity at a reference temperature, usually room temperature, and k is the temperature coefficient.

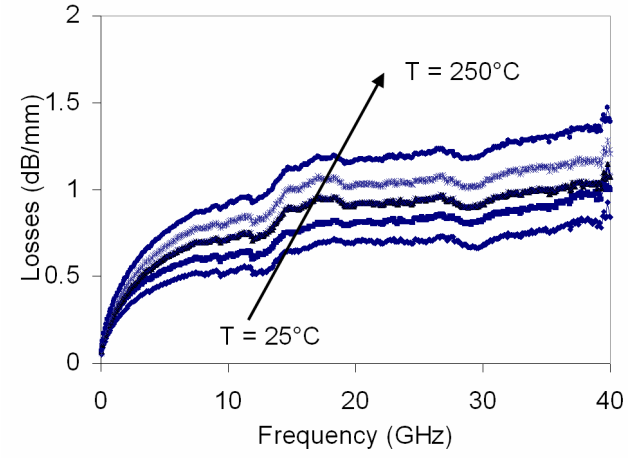

Fig.6: Measured lineic losses vs. frequency and temperature (W=7 µm).

III. Coplanar Waveguide (CPW)

Fig. 7 shows a cross section and a top view of the CPW structure built on SOI. The characteristic impedance of CPW can be fixed on a wide range by changing the width of the central conductor (W), or the spacing between the central conductor and the ground planes (S).

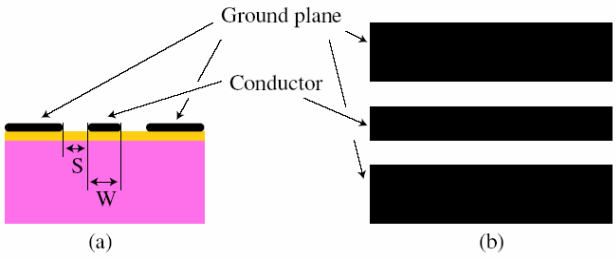

Fig. 7: CPW line: (a) cross-section and (b) Top view.

The losses in CPWs are of two kinds: conductor losses, due to the resistivity of the metal and substrate losses, due to the coupling between the central conductor and the planar grounds through the oxide and the silicon substrate.
In order to investigate the behaviour of a CPW in RF for high temperature application, a complete Calibration kit was drawn for 50 Ω characteristic impedance (W=40 µm, S=24 µm), containing 1 thru line, 1 short, 1 open and 1 long line (800 µm) in Metal 6 only, as shown in Fig. 8.

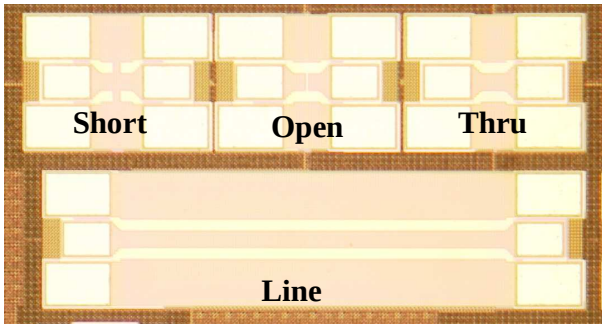

Fig. 8: Chip microphotograph of the designed CPW calibration kit.

The actual multilayered structure drawn on the 130 nm SOI process is detailed in Fig. 9.

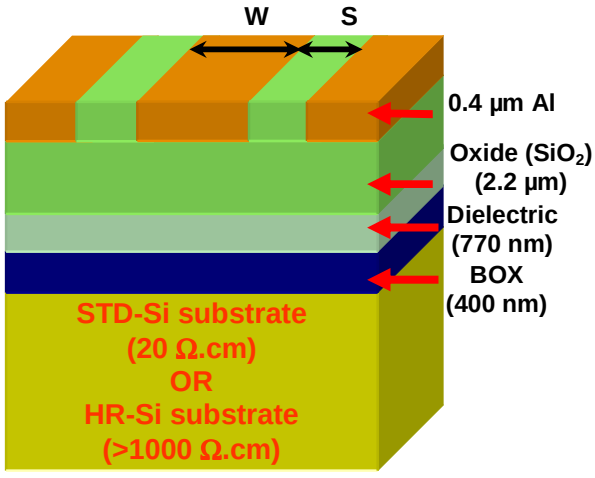

Fig. 9: Geometry of CPW.

The CPW structure was designed on STD (CPW_STD) as well as on HR (CPW_HR) Si substrates, and the measured losses are obtained after a TRL de-embedding method.

For CPW, the increase of the losses is more important on HR compared to STD, but its performance is still interesting at 250°C. The CPW_HR shows 50% less loss compared to a 50 Ω MSL at 250°C, because CPW structures enable using wider lines to achieve the same characteristic impedance which leads to reduced metallic losses (Fig. 10).
Lineic losses of CPW_HR, CPW_STD and MSL are plotted in Fig. 11 with respect to temperature. We note a decrease of the losses for the CPW_STD, till 200°C due to the mobility reduction of free carriers in the substrate at higher temperature [3]. Above 200°C, the losses start to increase for both CPW_STD and CPW_HR. This is due to the increase of the metallic losses on the one hand, and the degradation of the substrate resistivity on the other hand for the HR substrate. For the MSL, there is a linear increase of α as expected, because the conductor losses are dominant, as shown earlier.

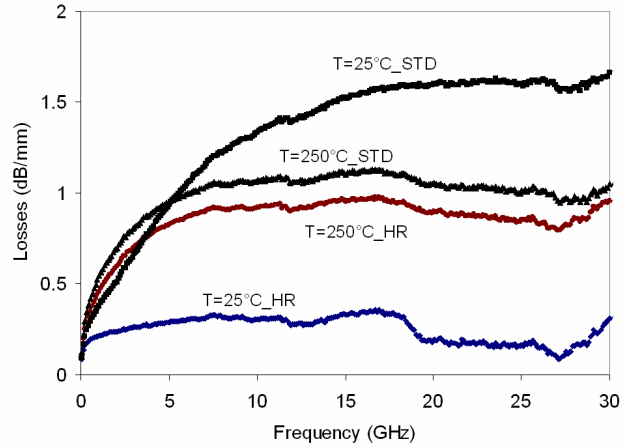

Fig.10: Measured lineic losses vs. frequency for CPW on STD and HR silicon substrates (W=40 µm, S=24 µm).

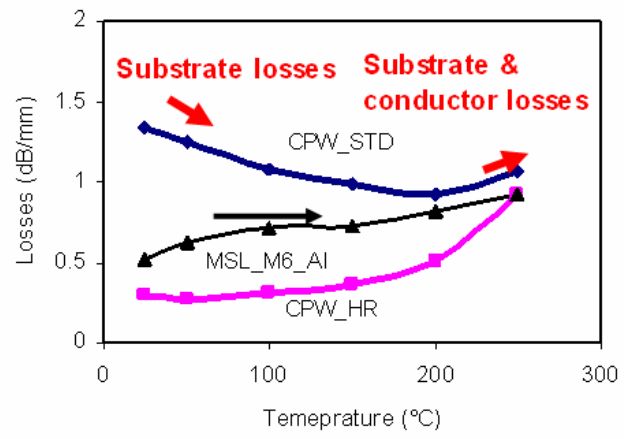

Fig.11: Comparison of measured lineic losses vs. temperature of CPW & MSL @ 10 GHz.

Fig. 12 shows the attenuation coefficient of CPW lines made on standard and high resistivity SOI wafers, as well as fused silica wafer. The CPWs were designed to obtain characteristic impedance close to 50 Ω.

By comparing, the attenuation coefficient (α) of the two lines made on SOI, the importance of the substrate losses is highlighted. The substrate losses dominate in the case of standard resistivity substrate.
The attenuations of the CPW structures were also compared to the 50 Ω MSL designed with and without the Alucap layer. MSL even without Alucap layer is still better than CPW on standard resistivity.
By comparing the results presented in Fig. 12, CPWs made on HR SOI or SOS exhibits better performance than MSL for impedances close to 50 Ω. In both structure, the losses are dominated by the conductor losses. But MS lines are independent of the substrate used.

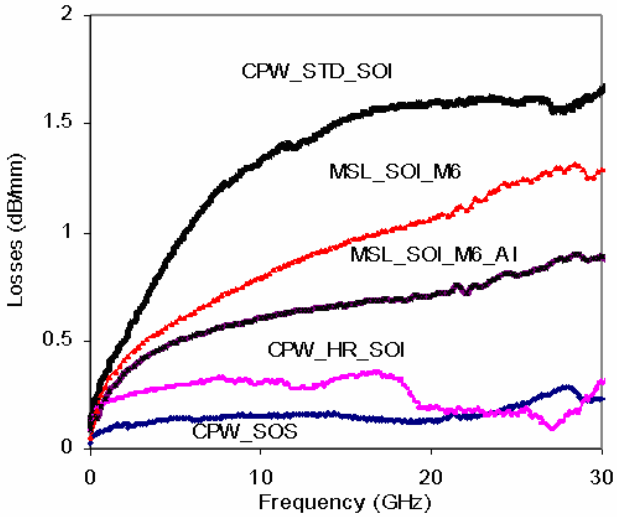

Fig. 12: Measured lineic losses of CPW on STD, HR and SOS @ room temperature.

IV. Discussion

- **MSL does not see the substrate, but suffers from higher losses than CPW lines on HR substrates due to small conductor width**: Indeed, the properties of MSL are independent on the substrate used, because the ground plane avoids coupling between the signal and the substrate. Thus, the conductor losses are dominant.

- **AluCap is efficient in reducing conductor losses for MSL:** We note a reduction in losses 0.35 dB/mm at 20 GHz when using Alucap. Adding Alucap exhibits much more impact comparing to the effect of increasing the width of the microstrip line W.

- **CPW losses are twice lower, despite the use of Metal 6 only:** more than 50% less loss for a 50 Ω CPW on HR compared to a 50 Ω MSL with Alucap. Because CPW structures enables using wider lines to achieve the same characteristic impedance which allows reducing the metallic losses.

- **Behaviour of passives versus temperature:** the loss characteristics of STD and HR CPW and MSL structures were investigated over a wide range of temperature. As expected, the losses increase with respect to the temperature except for the STD CPW: the substrate resistivity increases with the rise of temperature which compensate the metallic losses and thus make the CPW losses decreasing with respect to temperature till 200°C. These results demonstrate the feasibility and practical applicability of different passive structures in circuits design for both room and high temperature applications.

In CMOS processes, the steady increase in the number of metal layers and the increase of interlayer dielectric thickness enable using wider lines for a fixed characteristic impedance and yields conductor losses reduction with MSL. Moreover, signal conductor is shielded from the substrate avoiding coupling effects and thus MSL electrical characteristics are unrelated to substrate resistivity, allowing standard resistivity SOI substrates (20 Ω.cm).

With CPW configuration, characteristic impedance is inversely proportional to the aspect ratio *W/S*. This enables to use wide lines for reducing metal losses with the drawback of larger consumed area. Up to now, CPW lines on standard resistivity substrates (20 Ω.cm) exhibited very high losses. But recent availability of high resistivity SOI substrate (1 kΩ.cm) or the transfer onto fused silica of SOI standard resistivity substrates makes CPW configuration an interesting solution for implementing low loss lines [7].
High frequency characteristics of transferred layers on a fused silica are compared to the ones on standard SOI substrates by measuring coplanar transmission lines.
Fig. 13 shows the geometry of the measured coplanar line [7]. The coplanar waveguide (CPW) is fabricated with a 0.4-µm thick Al metallization. For the standard SOI Unibond substrate, the total SiO_2 thickness, including the passivation and the buried oxide layers is 2.6 µm. The underlying silicon substrate has a resistivity of 20 Ω.cm.
On the other hand, the "transferred layer substrate" is entirely composed of silicon dioxide, including the passivation, the buried oxide and the fused silica substrate.
Fig. 14 compares attenuation α in the CPW line on the standard Unibond substrate and on fused silica substrate.

The fused silica substrate clearly exhibits a significantly reduced loss, with a value lower than 0.25 dB/mm at 10 GHz. Even if the resistivity of aluminium lines and CPW geometry can slightly modify the attenuation, our low α values are comparable to results obtained on GaAs semi-insulating substrates and high resistivity Si-substrates [8, 9].

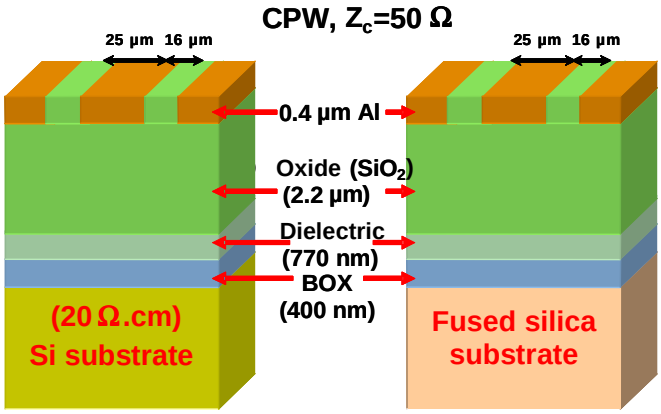

Fig. 13: 3D view of the measured transmission coplanar waveguide on standard Unibond substrate and transferred Unibond substrate on fused silica.

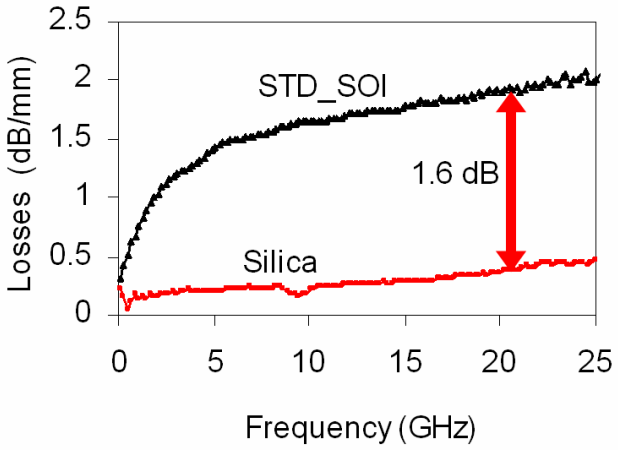

Fig. 14: Extracted attenuation on standard Unibond substrate, and transferred substrate on fused silica for the measured coplanar transmission line.

V. Conclusion

SOI CMOS technology is now emerging as a mature technology for the realization of high-temperature integrated circuits.
Losses of MSL and CPW made on HR and STD SOI wafers were analyzed with respect to temperature.
MSL allows the use of STD substrate because the back ground plane shields the Si substrate. MSL can then be an interesting topology if the losses can be lowered to the same level than CPW made on HR SOI or SOS.
For the CPW, the losses are of two kinds: conductor losses, due to the metal resistivity, and substrate losses, due to the coupling between lines through the substrate.
These results demonstrate the feasibility and practical applicability of different passive structures in circuits design for both room and high temperature applications.
To reduce the attenuation coefficient of MS lines, the width and the thickness of the conductor must be increased, but the capacitance between the conductor and the ground plane must be kept constant ensuring the same characteristic impedance. To achieve this goal, the thickness of the

dielectric layer must be increased, or low-*k* dielectric must be used instead of silicon dioxide.

These solutions are in agreement with the tendencies of semiconductor industries. Indeed, more and more metal levels are used, allowing a thicker isolator layer between the conductor, made with the top metal layer, and the ground plane. Furthermore, low-k dielectric will be used as insulator between the different metal layers to reduce the capacitive coupling between metal lines.

Due to the rapid increase in the number of metallic interconnects, the top level metals will be located further away from the SOI substrate as the technology scales, thus reducing the substrate losses for CPW and widen the metallic strip for MSL . In a near future, 12 metal levels will be available and will enable using 5 times wider strips for MSL and thus reduce the losses by a factor of 3 making MSL as a very promising structure for RF design for the next technological node.

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