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Behavior of gold-doped silicon substrate under small- and large-RF signal

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ABSTRACT

In this paper, small- and large-signal performances of passive devices integrated on high-resistivity, trap-rich and gold-doped silicon wafers are presented and compared through measurements and simulations. The gold-doped silicon substrate was produced starting from standard silicon having a nominal resistivity of 56 Ω·cm. We show that the gold-doped substrate presents high effective resistivity and low losses suitable for RF applications. This has been demonstrated by measuring coplanar waveguides, crosstalk, inductors and band pass filter where we observed similar performances for small-signal measurements compared with trap-rich substrate. Large-signal measurements of gold-doped substrates show 60 dBm lower harmonic distortion than high-resistivity substrates, and 10 dB lower than trap-rich substrate at 0 V DC bias. However, a large DC bias dependence on the harmonic distortion induced by the gold-doped substrate is observed. This unexpected behavior is explained using the Fermi level localization in the silicon bandgap for the different DC bias conditions.

1. Introduction

The microelectronic market is demanding more and more innovation and new capabilities in mobile devices, this is why the communications industry is looking for reliable fabrication processes and substrates that can meet all RF requirements [1]. Choosing the right substrate technology is an important step in order to cointegrate the digital devices, analog and RF front-end modules on the same substrate. Silicon technology has been considered as the promising solution for RF applications and communication systems due to its low cost, maturity and its continuous improvement [2]. The design and the fabrication of RF circuits (PA, LNA, switch…etc) are challenged by the substrate upon which the devices are built, because it is an important source for electromagnetic coupling, RF losses and non-linearities. Many silicon substrates have been developed in the past starting with standard silicon substrate (nominal resistivity around 20 Ω·cm), however the digital noise coming from digital devices propagates through the bulk and affect the performance of analog and RF devices built on this substrate, thereby reducing the ability of co-integration of the RF devices on the same substrate (SiPs and SoCs). New integration levels were reached thanks to the optimization of the silicon substrate [3]. Silicon substrates with high effective resistivity [4] (higher than 3 kΩ·cm [5]) are the most appropriate for RF applications due to the high quality passives, less RF loss, decreased crosstalk and reduced signal distortion.

High-resistivity Silicon-on-Insulator (HR-SOI) substrates were introduced to be a good candidate for RF applications thanks to its high isolation, low substrate loss and low cost [6–8]. Although the HR substrate is significantly low doped (nominal resistivity as high as 3 kΩ·cm) compared to standard substrate, its RF performances are barely improved [9,10]. The main problem of HR substrate is the Parasitic Surface Conduction (PSC) originating from the fixed charges in the insulating layer which attract free carriers from the substrate to the Si-SiO_2 interface and create a highly conductive layer leading to inhomogeneity in the substrate thereby reducing its effective resistivity [4]. The trap-rich substrate resolves the problem of PSC by introducing a thin layer of polysilicon (between 300 nm and 2 μm) between the Si and the insulating layer. Polysilicon introduces a large amount of defects that trap the free carriers at the interface. These traps pin the Fermi level near the silicon midgap, and the substrate recover its high effective resistivity.

A new concept called deep level doping compensation was introduced in order to increase the resistivity of SOI substrate, consequently reducing the PSC effects by introducing a high density of traps in the entire silicon substrate thickness [11]. The effects of background free carriers are compensated by implanted dopant atoms, thus reducing the carrier concentration, consequently increasing the resistivity of

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the silicon substrate [12]. The material chosen for doping is gold, because it can be used for both n-type and p-type silicon in contrast to other dopants that only introduce either donor or acceptor traps centers. Gold also introduces equal concentrations of donor and acceptor traps at energy levels near the midgap [13]. Doping with gold does not require exact control of the quantity of dopants to achieve the resistivity needed, and also the gold is among most studied materials in the litterature [14–16]. Deep level compensation technique has showed its capabilities to improve the RF performance of the substrate by reducing attenuation from 0.8 dB/mm to 0.3 dB/mm [17], for CPW fabricated on gold-doped silicon and standard silicon, respectively. Resistivities around 100 kΩ·cm have been achieved for gold-doped silicon substrate [18]. It was also shown that this technique can suppress the PSC effects and eliminate the bias dependence [11], however the non-linearities of the gold-doped silicon substrate and its performances under large RF signal have not been reported in the literature yet.

In this paper, we present the behavior of the Au-Si substrate under small- and large-RF signal. In Section II we describe the experimental results under small RF signal and the characteristics of the CPW line including the behavior of the effective resistivity, crosstalk measurements, inductor quality factor, band pass filter, then we show the harmonic distortion measurements. In Section III, we will explain the unexpected behavior of the non-linearities in gold-doped silicon substrate using Fermi level extraction and the impedance variations, the location and the effect of trap densities will be shown as well.

2. Experiment

2.1. Substrates description

Coplanar waveguides (CPW) were fabricated for RF characterization on three types of high-resistivity silicon substrates (Fig. 1) with 700 µm thickness: (i) n-type Si substrate with 5 kΩ·cm nominal resistivity (HR), (ii) high resistivity Si with a 1 µm thin layer of trap rich polysilicon (TR), and (iii) Au-doped Si substrate (Au-Si). For this last substrate we started with a standard n-type silicon wafer with a nominal resistivity of 56 Ω·cm. Gold atoms were then implanted at the backside of the wafer with a dose of 4×10^{13} cm^{-2} at an energy of 100 keV. After implantation, the gold atoms are not yet activated and do not contribute to the resistivity increase. This is why the wafer was subsequently annealed at

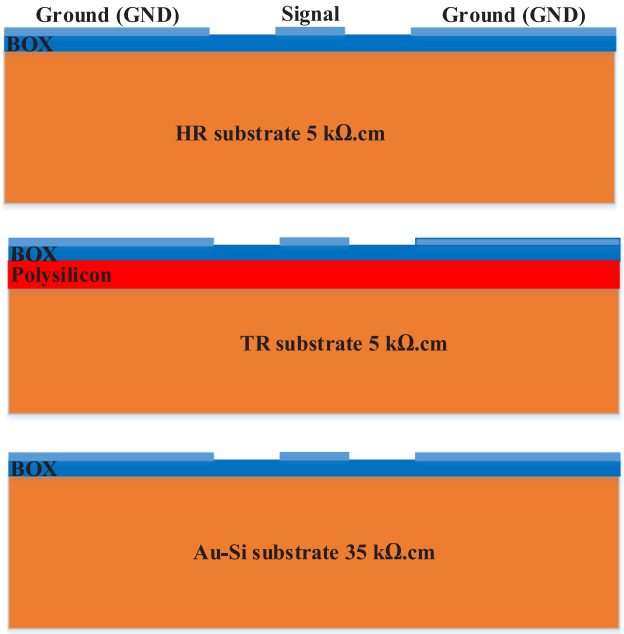


Fig. 1. The three Si-based substrates fabricated.

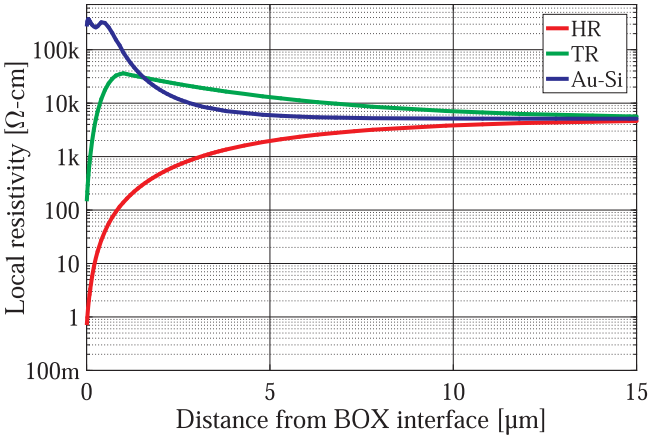


Fig. 2. Simulated resistivity profiles in the silicon volume below the insulating layer for the three Si-based substrates.

950 °C. After that we obtained a substrate with a nominal resistivity of around 35 kΩ·cm. All substrates have an insulating layer with thickness of t_{ox} = 200 nm that was deposited using low-pressure chemical vapor deposition (LPCVD). The 50 Ω CPW line was defined as: W_c = 26 µm (central signal conductor width), S = 12µm (signal-to-ground line spacing) and W_g = 208 µm (ground conductor width). Finite element simulations were carried out using Atlas software which simulates accurately the physical parameters such as fixed oxide charges, interface and volume traps by resolving Poisson's and semiconductor equations in the Si-based substrates. The density of positive fixed oxide charges Q_{ox} was set at 10^{11} cm^{-2} for all substrates. The spatial Au distribution was defined based on experimental SIMS data presented in [17]. The trap-rich substrate was simulated using tail distribution for donor and acceptor traps to model the polysilicon layer according to the model given in [19], and using characteristic decay energy of 33 meV and edge band state density of 10^{22} cm^{-3} eV^{-1}.

2.2. Simulated local resistivity profile

In Fig. 2 are depicted the local resistivity profiles below the insulating layer simulated for the three different substrates (HR, TR and Au-Si) using the finite element semiconductor simulation tool Atlas [20] from Silvaco. It appears clearly that HR substrate suffers from the PSC effect due to the low resistivity layer near the Si-SiO_2 interface and shows a local value around 700 mΩ·cm. The trap-rich which is a solution to the PSC problem shows better performances with a local resistivity near the Si-SiO_2 interface higher than the later, this is due to the traps generated by the polysilicon layer. The Au-Si substrate does not suffer from the PSC effects and shows values higher than 200 kΩ·cm near the Si-SiO_2 interface. This is due to the gold atoms that create acceptor and donor levels in the silicon band-gap and close to the midgap, this latter compensates the free carriers that are in the substrate.

2.3. Effective resistivity as a function of frequency

The small-signal measurements of the CPW lines were performed using an Agilent 2-port performance network analyzer (PNA)-X vector network analyzer and a pair of ground-signal ground (GSG) |Z| probes from Cascade Microtech with 150 µm pitch. The effective resistivity was extracted from S-parameters measurements. We used short-open-thru-load (SOLT) calibration method in order to calibrate the system at the probe tips. The deembeding proposed by Gillon [21] was used in order to remove the pad parasitics by measuring the open and the thru on-wafer after measuring the CPW line.

The small-signal measurements and simulations of the CPW line are

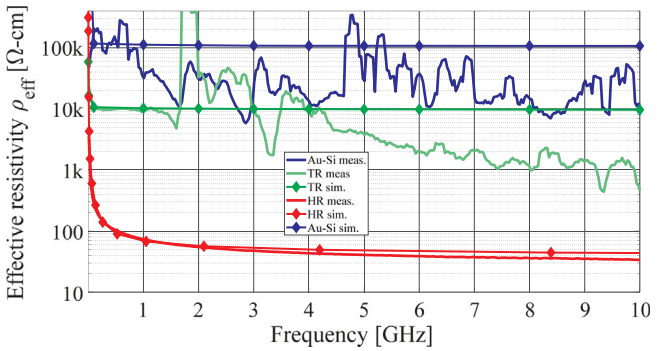


Fig. 3. Measurement and simulation results of the effective resistivity extracted from CPW lines designed on the three different substrates at 0 V DC bias.

depicted in Fig. 3. We can see that the simulations agree well with the measurements.

The HR substrate suffers from PSC: the effective resistivity is therefore low as expected, and shows a value of around 40 Ω·cm at 4 GHz. This low value translates to an increase in the CPW line's RF losses. The TR substrate effectively mittigates the PSC effect and its effective resistivity is reletively high around 10 kΩ·cm at 4 GHz. The Au-Si substrate shows better performances than TR, with an effective resistivity reaching a value of more than 15 kΩ·cm at 4 GHz. The gold atoms in substitutional sites create traps in the bandgap of the silicon, deep donors and deep acceptors at $E_C - 0.78$ eV (0.78 eV below conduction band) and $E_V + 0.58$ eV (0.58 eV above valence band), respectively [22]. The traps created by gold atoms capture free charges in the silicon bulk, the Fermi level at the Si-SiO_2 interface is located near the mid-gap, thereby increasing the overall resistivity.

2.4. Effective resistivity bias dependance

To better understand of the behavior of the substrates, we extracted the effective resistivity as a function of the DC bias points of the CPW line which is depicted in Fig. 4. The effective resistivity of the HR substrate is bias dependent, as we can see it is around 40 Ω·cm for positive bias points and around 130 Ω·cm for negative bias points. When applying a positive DC bias we create more electrons below the signal electrode, so that enhance the PSC effect, therefore we register low effective resistivity. When we apply a negative DC bias, we are creating holes below the signal electrode, this leads to the creation of a depletion region between the signal and ground electrodes. The electric field will face a high resistive region between the signal and ground electrodes, so the effective resistivity is relatively high compared to when we apply a positive DC bias.

For the TR substrate, the effective resistivity is bias independent and

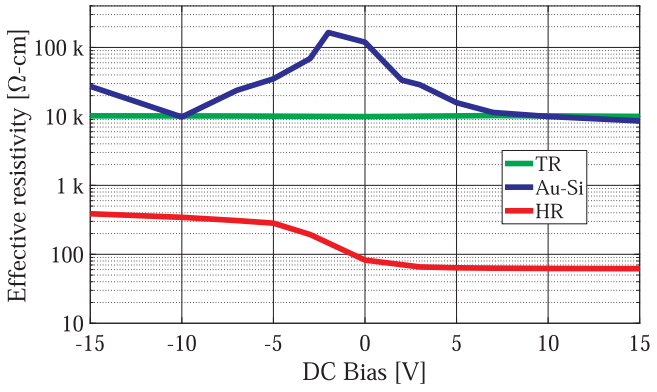


Fig. 4. Extraction of the effective resistivity as a function of DC bias for the Si-based substrates at 800 MHz.

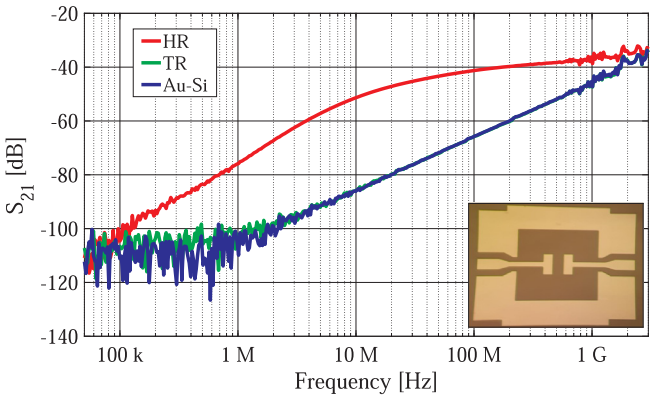


Fig. 5. Comparison of the measured crosstalk levels on the various Si-based substrates under consideration.

is around 10 kΩ·cm. The bias independency is due to the traps created by the polysilicon, so when electrons (or holes) are generated in the substrate by applying a positive (or negative) DC bias, they are captured by the traps and do not participate to conduction, or alter the effective resistivity. In the Au-Si substrate, the effective resistivity is high but also shows some bias dependency. This is because the traps created by gold are sufficient to counter the oxide charges, but not to counter the high number of carriers induced by the application of several Volts of DC bias.

2.5. Substrate crosstalk levels

Since the integration of RF and millimeter-wave devices on the same substrate became crucial, it is of first importance to reduce the coupling through the substrate. The RF coupling is caused by the neighboring devices especially RF switches and digital components. The assessment of the crosstalk level was performed by the passive structure shown in the inset of Fig. 5 that was carried out and measured on the three silicon-based substrates described above. The crosstalk pads have the specifications: length L of 150 μm, the spacing between the two pads is 50 μm and the width W of 50 μm.

The HR substrate shows strong coupling curve compared to TR and Au-Si and it shows a flattening tendency between 100 MHz and 2 GHz that represents the resistive behavior of the substrate. This value around −40 dB is relatively high due to the low effective resistivity of the substrate created by the PSC effect that facilitates the coupling in the first 100 nm below the insulating layer. The slope of 20 dB/dec below 100 MHz is due to the insulating layer capacitance. However, the slope above 20 GHz is due to the substrate capacitance, and since all the studied substrates are silicon-based (they are showing an effective permittivity of 9), we notice that the three curves join each other.

The TR and Au-Si show similar coupling because they are highly resistive due the traps contained in the two substrates. We can notice that theses curves do not show a flattening behavior, this is because it is so small that it does not appear (below a few MHz). The curves of these two substrates shows only the capacitive behavior of the substrate.

2.6. Quality factor measurements

In order to investigate the behavior of the substrate on the performances of inductors, we designed an inductor having the following characteristics: the spacing between the lines S = 10 μm, the width of the lines W = 40 μm, the inner radius Ri = 100 μm and the number of turns N = 3.5.

After the measurement of the S parameters we extracted the values of R and L then the quality factor was computed as::

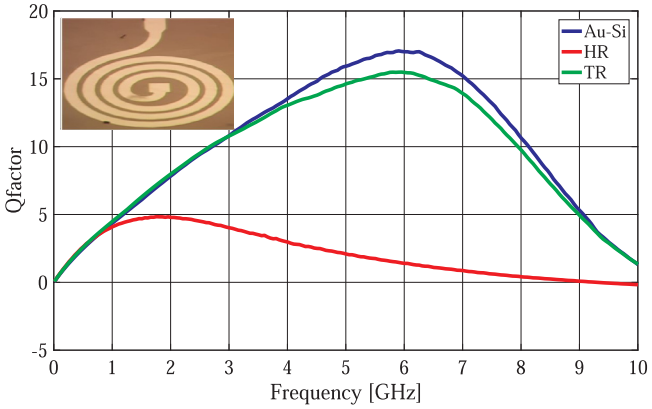


Fig. 6. The value of the quality factor as a function of frequency for inductor integrated on the HR, TR and Au-Si substrates.

$$Q = \frac{2\pi * f * L}{R} \quad (1)$$

where R and L are the internal resistance and the reactance of the inductor, respectively. The value of the inductor L is found 3.6 nH (The value at low frequencies between 0.4 and 4 GHz) and was plotted in Fig. 6. The HR substrate show a maximum Qf around 5 at 2 GHz, that is relatively low due to the PSC effect. In contrast, the TR substrate shows a value around 15 at 6 GHz and is close to that of Au-Si (around 17 at 6 GHz), this is because of the high resistivity offered by the two substrates.

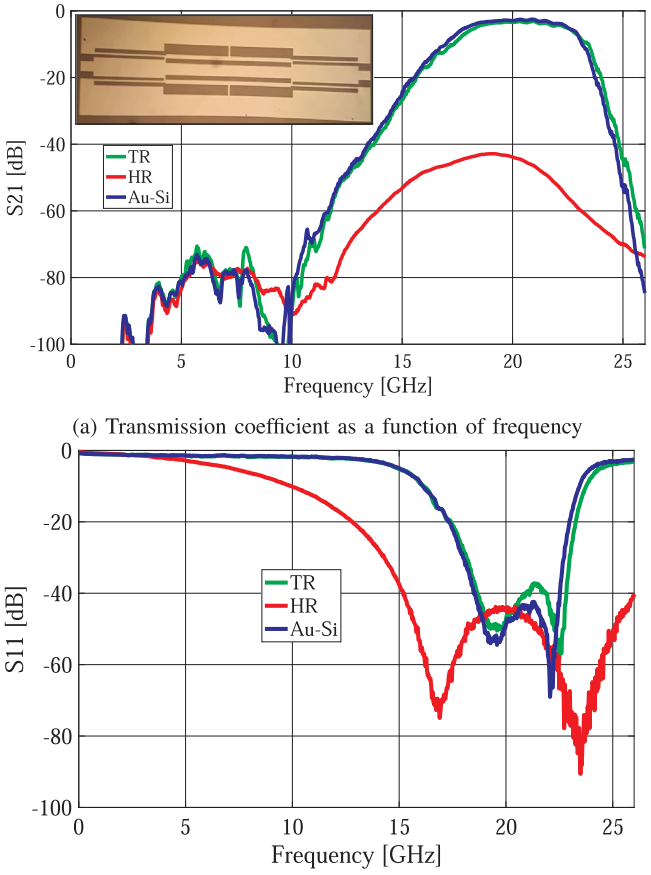
2.7. Coupled line bandpass filter measurements

The substrates were characterized by designing a 18–22 GHz coupled line band pass filter as in [23]. This later was implemented on the three silicon-based substrates. Fig. 7 shows the behavior of the designed filter during reception (a) and transmission (b), the picture of the filter is in the inset of Fig. 7a. It is shown in Fig. 7a that the filter implemented in HR substrate is bad in term of insertion loss (S21) and presents a maximum value of −40 dB, this is due to the substrate loss caused by the PSC effect. However, TR and Au-Si substrates offer a bandwidth of 5 GHz (17 to 22 GHz) and are so close to the design and presents more than 40 dB gain better than HR substrates because of the traps created by both poly-silicon layer and gold atoms. Fig. 7b shows the reflection coefficient of the studied substrates, where we confirm the good performances of TR and Au-Si substrates over the HR.

2.8. Large-signal measurements

In the case of passive devices fabricated on Si-based substrates it was shown that the harmonic distortion comes from the substrate itself and not from the metallic lines [24], connectors or contact surfaces. The distribution of free carriers in the substrate is modulated by the electric field applied to the CPW line.

For the large-signal measurements, a single tone with a fundamental frequency of 900 MHz is injected into one port of the CPW line by varying the power from −25 to 25 dBm. The harmonics H2 and H3 measured at the output of the CPW line are plotted versus fundamental output power H1 in Fig. 8 for the Si-based substrates described above at 0 V DC bias. It is shown that the HR substrate presents high harmonic distortion and shows a value of the second harmonic of −53.37 dBm at an input power of 15 dBm due to its low effective resistivity (around 40 Ω·cm). The TR substrate shows better linearity compared to HR (H2 = −95.6 dBm at an input power of 15 dBm) due to its higher resistivity (around 10 kΩ·cm). The Au-Si shows a second harmonic of −111 dBm at an input power of 15 dBm because of the high effective resistivity compared to TR because of the effective resistivity value



(a) Transmission coefficient as a function of frequency

(b) Reflection coefficient as a function of frequency

Fig. 7. Evolution of the S_{11} (a) and S_{21} (b) values of the bandpass filter with the frequency for the three studied substrates.

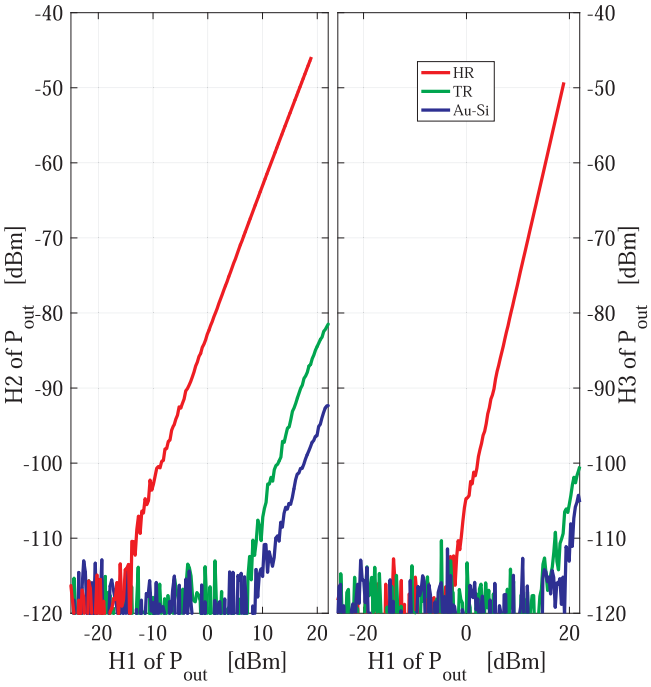


Fig. 8. Measured H2 (left) and H3 (right) for CPW line built on Au-Si, HR and substrates versus fundamental H1 output power at 900 MHz and at 0 V DC bias.

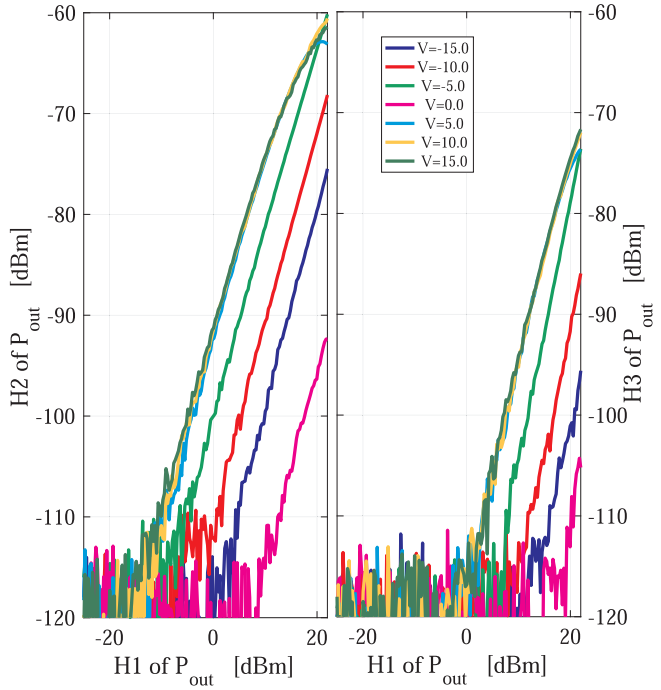


Fig. 9. Measured H2 (left) and H3 (right) for CPW line built on Au-Si substrate versus fundamental H1 output power at 900 MHz.

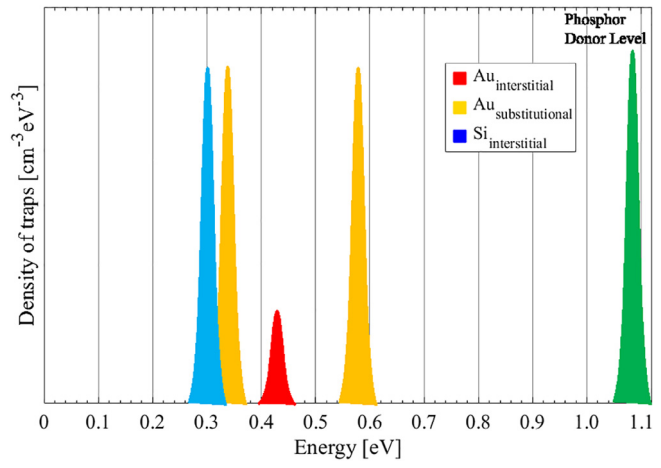


Fig. 10. Impurity energies in the Au-Si sample bandgap.

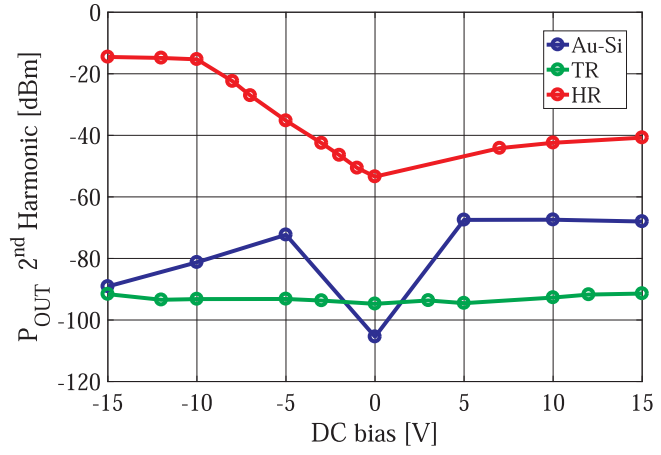


Fig. 11. Measured variation of the second harmonic at H1 = 15 dBm with the applied DC bias for the three different substrates.

above 20 kΩ·cm.

However, it is worth to know that Au-Si substrate has a different behavior at other DC bias points. The harmonics H2 and H3 measured at the output of the CPW line are plotted versus fundamental output power H1 in Fig. 9 for the Au-Si substrate at different DC bias levels. The harmonic distortion is quite low at 0 V and comparable to TR (Fig. 11), however, for other DC bias points we register second harmonic distortion that are relatively high but still better than HR substrate.

3. Non linear behavior of Au-Si substrate

3.1. Traps distribution in the silicon band-gap

As mentioned above, the Au-Si substrate has many traps introduced in the silicon bandgap. After the introduction of the gold atoms in the silicon crystal, they occupy both substitutional and interstitial sites, the substitutional ones will take the Si atoms position thanks to the kick out mechanism [25], the interstitial ones will occupy a position within the crystal network. It was mentioned in different works that the gold atoms in substitutional (Au_s) sites creates two energy levels of traps in the silicon bandgap, donor level at $E_c - 0.78$ eV (0.78 eV below the Conduction band) and acceptor level at $E_v + 0.58$ eV (0.58 eV above the valence band), however it was also mentioned in [26] that gold atoms in interstitial (Au_I) sites creates donor traps at $E_v + 0.43$ eV. It was explained also that silicon atoms in inerstitial (Si_I) sites creates acceptor traps at energy level $E_v + 0.30$ eV. Fig. 10 shows the distribution of the different traps in the silicon bandgap where we can see that the traps introduced are near the silicon midgap. However, the Au_I and Si_I will not participate to the increase of the resistivity of the substrate [27].

3.2. Fermi level localization

The variation of the second harmonic (H2) at an output fundamental power H1 = 15 dBm with the applied DC bias for the described substrates is depicted in Fig. 11. While TR is almost bias independent (variation in a small range between −87 and −90 dBm), the HR shows high H2 values and is strongly bias dependent varying from −14 to −54 dBm over the measured DC bias range. For the Au-Si substrate the harmonic distortion (HD) is quite low at 0 V (−105 dBm), however large degradations in H2 are observed at the other DC bias points (variation between −65 and −90 dBm).

In order to explain the behavior of Au-Si under large signal, we simulated the Fermi level below the signal electrode of the CPW line just at the Si-SiO_2 interface and was represented in Fig. 12 as a function

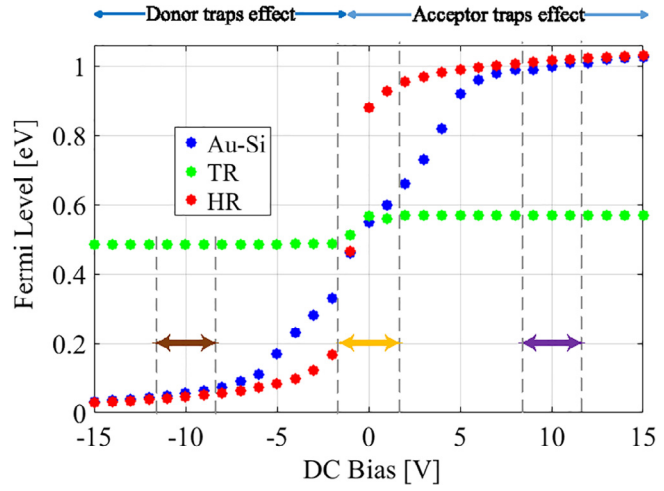


Fig. 12. Variation of the Fermi level as a function of the DC bias points for Si-based substrates.

of the applied DC bias. Eq. (2) that shown the space charge density extracted from Poisson's equation:

$$\rho = q(p - n + N_D - N_A + \rho_p - \rho_n) \quad (2)$$

where q is the elementary charge, p and n the hole and electron concentrations, respectively. N_D, N_A, ρ_p and ρ_n are donor impurities, acceptor impurities, trapped holes and electrons, respectively.

It is well known that the HR substrate does not contain traps in the silicon bandgap ($\rho_p = \rho_n = 0$), so the applied DC bias is compensated by a large variation of in free carriers consequently a large variation in the Fermi level as shown in Fig. 12. For the TR substrate the Fermi level is pinned near the midgap thanks to the polysilicon layer that introduces high trap density, so the applied DC bias is compensated by activating and deactivating the acceptor(ρ_n) and donor(ρ_p) traps, the value of ρ in the Eq. (2) will remain almost constant whatever the value of the applied DC value. The Au-Si substrate shows a different Fermi level behavior comparing to HR and TR. Around 0 V DC bias, when a large signal (15 dBm) is applied (a sine wave of 2 × 1.7 V peak to peak), the Fermi level will oscillate between E_v + 0.62 eV and E_v + 0.4 eV (yellow arrow), the traps are able to compensate this DC bias variation by donor and acceptor traps. In contrast, at 10 V DC bias, when the same large signal is applied, a high density of electrons is generated in the substrate the Fermi level will oscillate near the conduction band between E_v + 0.98 eV and E_v + 1.01 eV (purple arrow), this is because the traps density is not large enough to compensate the applied DC bias. the same for −10 V DC bias, where we will have a high density of holes and the traps can not compensate this amount, consequently the Fermi level oscillate between E_v + 0.01 eV and E_v + 0.06 eV (brown arrow).

The position of the Fermi level near the mid-gap allow us to say that the linearity of the substrate is high enough, however when its position is close to one of the bands there will be an excess of free carriers that will be modulated by the applied signal thus lower linearity, leading to a low harmonic distortion for 0 V and higher harmonic for other DC bias points.

It is worth to note that the acceptor traps are activated only when a positive bias is applied because the electrons are generated by a positive DC bias, however the donor ones will be activated only for the negative DC bias due to the holes generated by this latter in the substrate.

3.3. Impedance seen by the CPW line

The non-linearities of the studied substrates are described using impedances network at the Si-SiO_2 interface. As shown in Fig. 13, Z_{signal} represents the impedance below the signal electrode and $Z_{sig-gnd}$ is the impedance at the Si-SiO_2 interface between signal and ground electrodes. The HR substrate presents a highly non linear impedance Z_{signal} (very low impedance) that is in series with very low impedance $Z_{sig-gnd}$ due to the large quantity of electrons (PSC effect), thus the overall impedance is low, so the substrate is non-linear. In contrast to HR, the TR substrate shows a high $Z_{sig-gnd}$ impedance as it overcomes the PSC effect, and relatively low variation below the signal electrode (Z_{signal}) as shown in Fig. 12, so the overall impedance seen by the CPW line is high and can not be influenced by the large signal applied to it. This explains

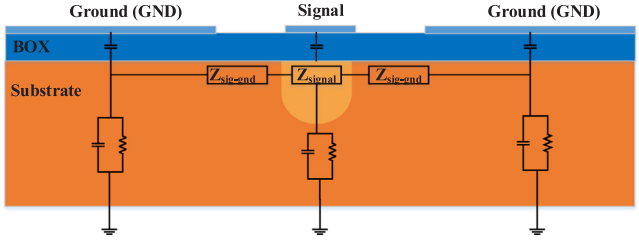


Fig. 13. Substrate modeling using the impedance seen by the coplanar waveguide line (CPW).

Table 1
Linearity comparison between the studied substrates.

	Z_{signal}	$Z_{signal-ground}$	Linearity
HR	Strong variation	Low	Poor
Au-Si	Strong variation	High	Medium
TR	Little variation	High	High

the high linearity of the TR substrate and its bias independence.

The non-linear behavior of the substrate beneath the central CPW line on the Au-Si substrate is similar to that on HR, as Fig. 12 shows. The interface Fermi level is not pinned by the traps as in the TR case, so we have a highly non-linear impedance Z_{signal}. However, in the Au-Si substrate this non-linear impedance (Z_{signal}) comes in series with a highly resistive impedance $Z_{sig-gnd}$, and so its contribution to the overall CPW shunt impedance is attenuated, and as a result the harmonic distortion is significantly lower than for HR. Table 1 summerizes the linearity (variations) of Z_{signal} and the value of the series impedance $Z_{sig-gnd}$ (the overall impedance linearity is the sum of the two latters) of the CPW line lying on the Si-based substrates.

3.4. Effect of traps concentration

Fig. 14 shows the simulated Fermi level for Au-Si substrate as a function of the applied DC bias with different gold atoms densities, and this starting from standard substrate (56 Ω·cm) until reaching a concentration of 1×10^{17} cm^{-3} (maximum gold solubility in silicon [28]). These densities are introduced uniformly in the entier thickness (700 μm) of the substrate. It is clear that the standard resistivity substrate (Std) presents a Fermi level that oscillates between the two bands such that the DC bias voltage is compensated by induced free carriers.

However by increasing the density of traps, the Fermi level becomes less dependent on the applied bias, and more tightly constrained in the mid-gap region. The pinning is not as tight as in the case of the TR substrate (see Fig. 12), but the presence of a sufficiently high quantity of Au atoms has the effect of rendering the Fermi level less voltage sensitive, particularly in the −2 to +2 V range, and to place the Fermi level near mid-gap at 0 Volts. This analysis explains the high value of $Z_{sig-gnd}$, and the strong variations of Z_{signal} in Au-Si.

4. Conclusion

In this paper, we demonstrate that we cannot rely on the unique extraction of the effective resistivity of a substrate to predict its harmonic distortion. It was shown that the Au-Si presents similar small signal performances compared to the benchmark trap-rich solution in terms of crosstalk, RF losses, and quality of integrated passives, demonstrated in this work by the implementation of CPW lines, spiral

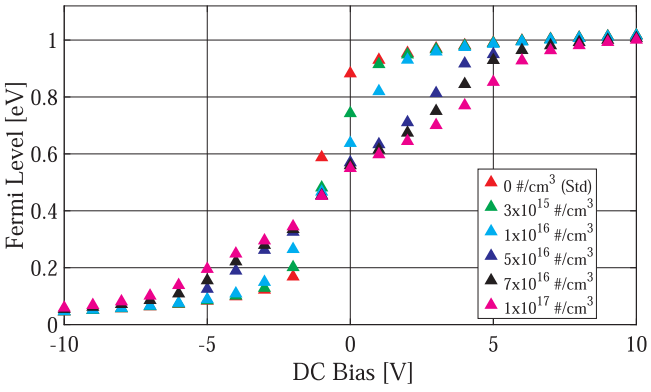


Fig. 14. Simulated Fermi level for Au-Si substrate with different densities of gold atoms.

inductors and edge-coupled band pass filters. The harmonic distortion in Au-Si is lower than in HR because though the Fermi level and local resistivity beneath the signal line of the CPW varies strongly in both substrates in response to the large signal, the Si-SiO_2 interface is in a highly conductive state (PSC) for the HR, but is highly resistive for the Au-Si. Indeed, the gold traps are in sufficient quantity to effectively counter the oxide charges, and add a high substrate impedance in series with the voltage sensitive region below the signal line that enables lower HD and higher effective resistivity than HR. The traps are however not sufficient to fully pin the Fermi-level such as is the case in the TR sample, which therefore presents much lower harmonic distortion. Gold is usually unwelcomed in CMOS fabs due to its high diffusivity and mobility degradation. Though the integration of the Au-compensated RF substrate into industrial fabs is difficult to foresee at the moment, such a low-loss and highly-linear substrate may still find potential applications immediately for RF MEMS or acoustic filters.

References

[1] Laurent S, Eric D. RF Substrate Technologies for mobile communications, white paper; 2011.
[2] Rack M, Belaroussi Y, Ali KB, Scheen G, Esfeh BK, Raskin J-P. Small-and large-signal performance up to 175-C of low-cost porous silicon substrate for RF applications. IEEE Trans Electron Dev 2018;65(5):1887–95.
[3] Ali KB, Neve CR, Gharsallah A, Raskin J-P. RF performance of SOI CMOS technology on commercial 200-mm enhanced signal integrity high resistivity SOI substrate. IEEE Trans Electron Dev 2014;61(3):722–8.
[4] Lederer D, Raskin J-P. Effective resistivity of fully-processed SOI substrates. Solid-State Electron 2005;49(3):491–6.
[5] Ali KB, Neve CR, Shim Y, Rais-Zadeh M, Raskin J-P. Non-linear characteristics of passive elements on trap-rich high-resistivity Si substrates. Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2014 IEEE 14th Topical Meeting on. IEEE; 2014. p. 4–6.
[6] Celler G, Cristoloveanu S. Frontiers of silicon-on-insulator. J Appl Phys 2003;93(9):4955–78.
[7] Tombak A, Carroll MS, Kerr DC, Pierres J-B, Spears E. Design of high-order switches for multimode applications on a silicon-on-insulator technology. IEEE Trans Microwave Theory Tech 2013;61(10):3639–49.
[8] Adan AO, Yoshimasu T, Shitara S, Tanba N, Fukurni M. Linearity and low-noise performance of SOI MOSFETs for RF applications. IEEE Trans Electron Dev 2002;49(5):881–8.
[9] Lederer D, Raskin J-P. RF performance of a commercial SOI technology transferred onto a passivated HR silicon substrate. IEEE Trans Electron Dev 2008;55(7):1664–71.
[10] Gianesello F, Gloria D, Raynaud C, Montusclat S, Boret S, Touret P. Integrated inductors in HR SOI CMOS technologies: on the economic advantage of SOI technologies for the integration of RF applications. SOI Conference, 2007 IEEE International. IEEE; 2007. p. 119–20.
[11] Hashim NZ, Abuelgasim A, de Groot CH. Suppression of parasitic surface conduction in Au-compensated high resistivity silicon for 40-GHz RF-MMIC application. Microwave Conference (APMC), 2014 Asia-Pacific. IEEE; 2014. p. 55–7.
[12] Abuelgasim A. High resistivity Czochralski-silicon using deep level dopant compensation for RF passive devices [Ph.D. dissertation]. University of Southampton; 2012.
[13] Collins C, Carlson R, Gallagher C. Properties of gold-doped silicon. Phys Rev 1957;105(4):1168.
[14] Bullis W. Properties of gold in silicon. Solid-State Electron 1966;9(2):143–68.
[15] Morooka M, Tomokage H, Kitagawa H, Yoshida M. Three states of substitutional gold in silicon. Japanese J Appl Phys 1985;24(2R):133.
[16] Bemski G. Recombination properties of gold in silicon. Phys Rev 1958;111(6):1515.
[17] Abuelgasim A, Mallik K, Ashburn P, Jordan D, Wilshaw P, Falster R, de Groot C. Reduced microwave attenuation in coplanar waveguides using deep level impurity compensated Czochralski-silicon substrates. Semicond Sci Technol 2011;26(7):072001.
[18] Abuelgasim A, Hashim N, Chong H, Ashburn P, De Groot C. Low loss 67-GHz coplanar waveguides and spiral inductors on 100 kΩcm gold-doped high resistivity Cz-Silicon. Silicon monolithic integrated circuits in Rf systems (SiRF), 2014 IEEE 14th topical meeting on. IEEE; 2014. p. 10–2.
[19] Kemp M, Meunier M, Tannous C. Simulation of the amorphous silicon static induction transistor. Solid-State Electron 1989;32(2):149–57.
[20] Atlas DS. Atlas user's manual. Santa Clara, CA, USA: Silvaco International Software; 2005.
[21] Gillon R, Raskin J-P, Vanhoenacker D, Colinge J-P. Determining the reference impedance of on-wafer TLR calibrations on tossy substrates. 1996 26th European microwave conference, vol. 1. IEEE; 1996. p. 170–3.
[22] Hull R. Properties of crystalline silicon. IET 1999;no:20.
[23] Weller TM. Edge-coupled coplanar waveguide bandpass filter design. IEEE Trans Microwave Theory Tech 2000;48(12):2453–8.
[24] Neve CR, Raskin J-P. RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates. IEEE Trans Electron Dev 2012;59(4):924–32.
[25] Gösele U, Morehead F, Frank W, Seeger A. Diffusion of gold in silicon: a new model. Appl Phys Lett 1981;38(3):157–9.
[26] Bracht H, Rodriguez Schachtrup A. Diffusion of gold into heavily boron-doped silicon. MRS Proc 1997;469:25.
[27] Hashim NZI. Au-compensated high resistivity silicon for low loss microwave devices-suppression of parasitic surface conduction effect [Ph.D. dissertation]. University of Southampton; 2015.
[28] Jordan DM, Haslam H, Mallik K, Wilshaw PR. The development of semi-insulating silicon substrates for microwave devices. ECS Trans 2008;16(6):41–56.

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