Broadband Smart mmWave Front-End-Modules in Advanced FD-SOI with Adaptive-Biasing and Tuning of Distributed Antenna-Arrays

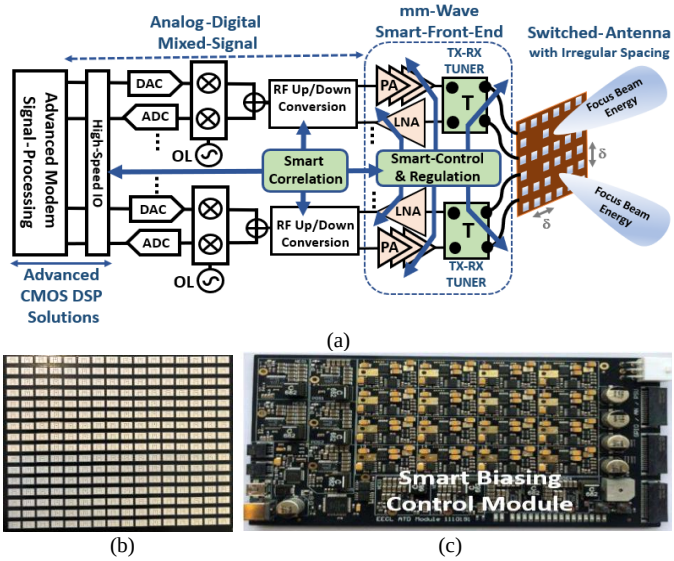
S. Wane[$], V. Huard[*], M. Rack[#1], L. Nyssens[#], B. Kieniewicz[$], D. Bajon[$], J.-P. Raskin[#]
[$]eV-Technologies, France, [*]Dolphin Design, France, [#]ICTEAM, UCL, Belgium

***Abstract*—In this paper, we propose new *correlation-aware* real-time adaptive tuning of distributed antenna-arrays using innovative broadband physics-based RLC circuit synthesis. The resulting *correlation-tuning* solution combines software-based *circuit-synthesis* with hardware-based *Smart-Control*. The software circuit synthesis runs on advanced signal-processing resources. The hardware implementation of the adaptive antenna tuning exploits the Body-Biasing control and regulation available in FD-SOI technologies. Broadband (DC-40 GHz) SPDT switches, fabricated in 22 nm FD-SOI process from GLOBALFOUNDRIES, are proposed for integration with *agile-tuners* for real-time noise and load matching of distributed antenna-arrays in a varying stochastic electromagnetic environment. The SPDT switches are characterized, using on-wafer measurements in small and large-signal conditions, as a function of transistor back-gate bias, demonstrating performance improvements of 0.2dB in insertion-loss, 2 dB in isolation, 1dB in P1dB and 4dB in IIP3. A Smart-Biasing-Module (SBM) is proposed demonstrating a wide range of bias control from 1*00pA* to *300mA* over ±8V with 24 bit resolution for adaptive-biasing control and regulation of RF and mmWave front-end-module building blocks.**

***Keywords*—Smart Front-End-Modules, FD-SOI, Adaptive Body Biasing, 4-Terminal, Noise and Load-Matching, SPDT Switches.**

I. INTRODUCTION

RF front-end-modules (FEMs) play a critical role in mobile devices since they are generally the block that consumes most of the power and therefore determines the energy-efficiency of the system [1]. As a consequence, the RF FEM tends to be the most non-linear part of the transmitter and also the most dominant stage in determining noise level, both of which may impact the quality of the communications. In transmit-mode, several techniques, including envelope tracking, Doherty, polar loop, and load-line-modulation provide efficiency improvements over classical class-AB amplifiers [2]. However, most of these efficiency improvement techniques require adaptive regulation loops to meet challenging linearity and power consumption requirements. In the receive path, multiple signal paths are typically used, combined with filter banks, to overcome the challenges associated with a single broadband RF signal path that would meet receiver sensitivity and noise-level requirements. Implementation of re-configurable and adaptive RF FEMs is expected to drive cost and size reduction with the benefit of a limited number of parallel RF signal paths. Broadband switches on high resistive silicon (HRS) substrate with low-loss, high isolation performance and extremely low harmonic distortion will enable next generation re-configurable FEMs. Such re-configurability requires environment awareness in order to properly compensate for stochastic changes affecting the efficiency and quality of the wireless link in real-time.



(a)

(b) (c)

Fig. 1. (a) mm-Wave Front-End-Module with (b) Smart Biasing regulation integrated with advanced Signal-Processing and Distributed Antenna-Array, (c) Smart-Biasing Control Module.

These stochastic changes, resulting from fluctuations in the environmental electromagnetic (EM) properties, strongly affect the reflection coefficient of antenna elements while the FEMs are generally optimized for a specific load-impedance.

In this paper, a new correlation-aware real-time adaptive tuning of distributed antenna-arrays (see Fig. 1) is proposed using innovative physics-based RLC circuit synthesis combined with *Smart-Biasing* control and regulation [3-4]. The efficiency of the RLC synthesis solution is demonstrated in a broad frequency range from DC to 40 GHz, showing excellent agreement between modeling and measurement results. The extracted RLC circuit elements can be cast in the form of canonical eigen-state representations for linking EM-based parameters (*impedance, noise, correlation, radiation*) to signal-processing brought close to the FEM RF channels.

II. MAIN RESULTS, ANALYSIS AND DISCUSSION

A. *Broadband Correlation-aware RLC Synthesis Solution*

We introduce a *correlation-aware* RLC synthesis solution for linking electromagnetic theory-based fundamental analysis of wireless communication systems to classical circuit-theory based on Kirchhoff laws, properly accounting for impedance matching, interference and coupling between noisy radiating elements. Organically bridging the gap between the EM-description of electric and magnetic fields and SPICE-netlist representation of induced currents and voltages will open new possibilities in communication system design for properly

978-1-7281-6192-1/20/$31.00 ©2020 IEEE

combining Information-Signal Theory (IT) and Physical-Information Theory (PT) into a unified approach. The Shannon–McMillan–Breiman theorem [5] provides a formal basis for such unified approach where Shannon's entropy can be directly related to Boltzmann's entropy for accurate extraction of key parameters characterizing the quality of RF wireless systems such as SNR, channel capacity, data rate and correlation between antennas in MIMO applications. Such approach will be facilitated by the emergence of advanced FDSOI technologies, bringing new operational attributes with transistors represented by *four effective terminals*: source, drain, gate, and body – the volume underneath the conduction channel. By regulating a voltage bias on this fourth terminal, the transistor's threshold voltage can be accurately controlled. The resulting adaptive-body-biasing (ABB) creates new paradigms for the convergence of analog and digital design solutions with improved RF performance and reduced energy consumption and process spread (see Fig. 2(a),(b)).

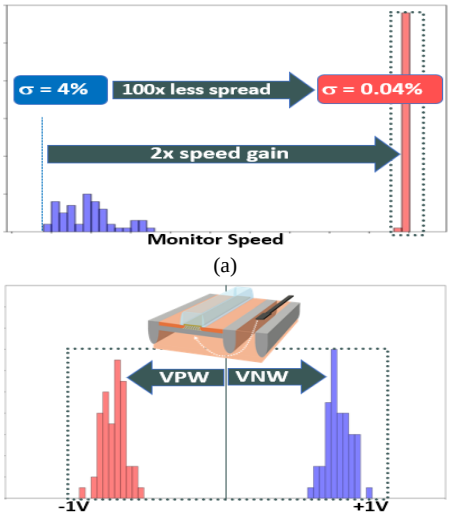


Fig. 2. Design performances in terms of speed and spread control resulting from Adaptive-Body-Biasing (*VPW and VNW referring to p/n wells*) in advanced FDSOI Technologies.

The proposed *correlation-aware* RLC synthesis solution is built using eigen-states EM-based modal representation accounting for distributed floating local ground references, in accordance with the f*our-terminal* representation of transistors in FDSOI technologies. The ability of the proposed solution to map physical design parameters into a broadband physics-based RLC equivalent circuit model is demonstrated using parameterizable CPW matching transmission lines accounting for harmonic distortions. The resulting RLC synthesis enables Q-controllable components with compact broadband equivalent circuit representation fully scalable with respect to the device geometry and architecture with the following attributes:

- Meaningful interpretation of synthesized RLC elements.
- Broadband accuracy with minimal complexity.
- Preservation of passivity and causality.

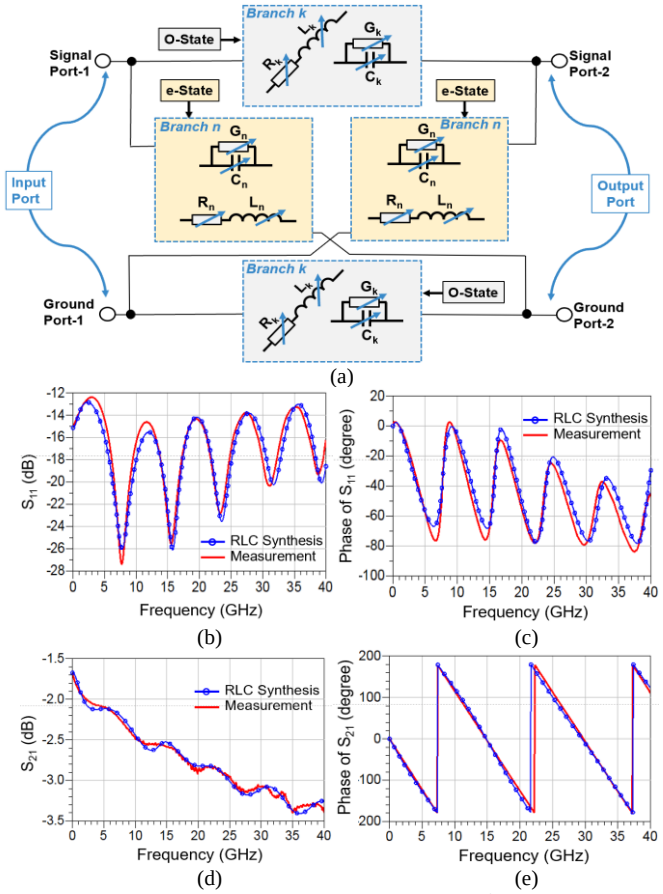


Fig. 3. Broadband power-dependent RLC-synthesis (a) of matching-networks for smart-antenna tuning in SOI technologies. RLC-synthesis versus measurement for (b) S11-magnitude, (c) S11-phase, (d) S21-magnitude, and (e) S21-phase.

Table I. Eigen-State Operators and Associated RLC-Synthesis.

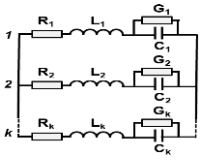
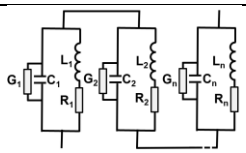
Eigen-State Operator & Modal Expression	Equivalent-Circuit SPICE-Representation [k=n=6]
Reflection-Operator $\Gamma^{O-State} = \frac{1 - z_{ref} Y^{O-State}}{1 + z_{ref} Y^{O-State}}$	 *R_1=0.006mΩ, L_1=0.133nH, G_1=0.193mS, C_1=52.769fF* *R_2=8.115Ω, L_2=1.151nH, G_2=0.020mS, C_2=97.907fF* *R_3=9.991Ω, L_3=0.928nH, G_3=0.024mS, C_3=30.328fF* *R_4=0.008mΩ, L_4=7.742nH, G_4=0.061mS, C_4=1.617fF* *R_5=115.874Ω, L_5=7.455nH* *R_6=11.720Ω, L_6=3.159nH*
Reflection-Operator $\Gamma^{e-State} = \frac{1 - z_{ref} Y^{e-State}}{1 + z_{ref} Y^{e-State}}$	 *G_1=8.891S, C_1=100.143pF* *G_2=0.001S, C_2=643.544fF* *R_3=2.373Ω, L_3=0.334nH, G_3=0.117mS, C_3=353.354fF* *R_4=1.124Ω, L_4=0.112nH, G_4=0.112mS, C_4=269.744fF* *R_5=0.015Ω, L_5=0.084nH, G_5=2.416mS, C_5=139.550fF* *R_6=0.878Ω, L_6=0.042nH, G_6=0.241mS, C_6=2946.150fF*

Table II. State-of-the-art mm-wave SPDT modules in SOI technologies.

		[11] 2011	[12] 2014		[13] 2017	[14] 2017	[15] 2018	[16] 2019	This Work 2020	
Technology		45-RFSOI	180nm SOI		130nm SOI	40nm SOI	45-RFSOI	22FDX	**22FDX**	
$R_{on}C_{off}$	[fs]	/	/		/	/	90	98	**98**	
Substrate		13.5 Ωcm	> 1 kΩcm		> 1 kΩcm	/	> 1 kΩcm	10 Ωcm	**10 Ωcm**	
Switch Type		SPDT	SPDT		SPDT	SPDT	SPDT	SPDT	**SPDT**	
Topology		Series-Shunt with matching	Series-Shunt with matching		Series-Shunt with matching	Series-Shunt	Series-Shunt	Transform-based	**Series-Shunt with matching**	**Series-Shunt**
Band	[GHz]	DC-60	DC-40		DC-50	DC-50	DC-50	26.5-29.5	**DC-40**	
IL (@ 28 GHz)	[dB]	1.4	1.1	2.1	1.0	1.4	0.7	1.6	**1.66**	**2.29**
ISO (@ 28 GHz)	[dB]	30	16.5	17.5	32	33	24	22	**33.4**	
P1dB	[dBm]	7.1	11	15	14	21	29.5	/	**20.5**	
IIP3	[dBm]	18.2	25.8	/	27	/	46	/	**38.5**	
Switching time	[ns]	0.35	/	/	10	/	/	/	**0.25**	
Size	[10^{-3} mm²]	39	25	/	40	/	4	150	**34**	**1.8**

The RLC synthesis derived in Table-I, based on eigen-states represented in Fig. 3(a), incorporates combined thermal and power-dependent effects. Thermal noise in strongly coupled arrays can be correlated. In [6], a method is proposed for the analysis of this thermal noise correlation and for the estimation of its effect on the system noise temperature, which becomes dependent on scan angle. It is observed that the correlated part of the noise can play a significant role in the *mutual-information* of lossy antenna array systems.

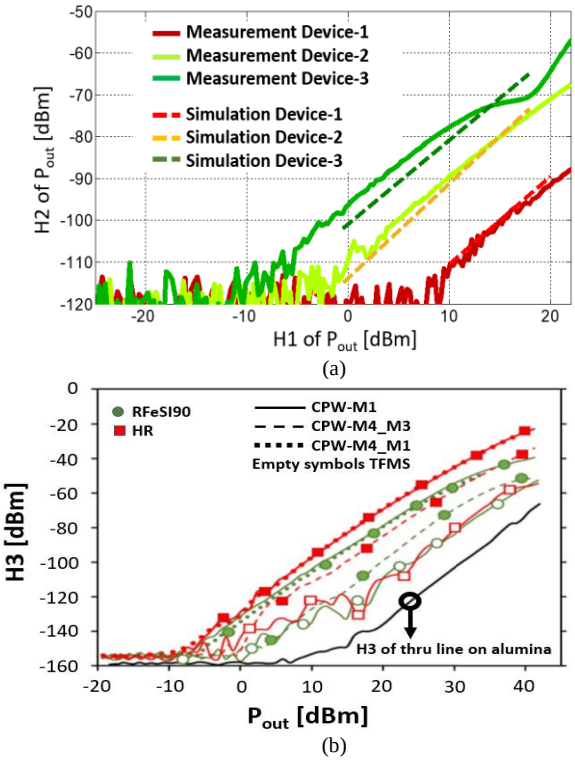


Fig.4 Harmonic distortion of SOI substrates for RF and mmWave applications (a) Measured H2 compared to simulation results, (b) H3 [8].

In Fig. 4(a) and 4(b) power-dependent effects of harmonic distortions are shown for passive interconnects as building blocks of feeding and matching networks. In Fig.4(a), the measured second harmonics (H2) are properly captured by the proposed nonlinear model developed based on physical considerations. In Fig. 4(b), the measured third harmonic (H3) components at the output port of CPW and TFMS lines at 0-V DC bias are plotted versus the output power at the fundamental (H1). The harmonic components obtained from the measurement of a thru-line on a standard calibration alumina substrate are reported in Fig. 4(b), highlighting the nonlinearity floor levels of the measurement setup [7-9]. TFMS lines with shielding from the silicon substrate show the lowest level of harmonic distortion.

B. *Adaptive-Body-Biasing for Smart-Front-End-Modules*

22FDX/12FDX FD-SOI is seen as a driving technology for low power RF SOCs and ASICs suitable for unifying *Smart-IoT* and *Cognitive mmWave* applications with the following benefits:

- Very low FD-SOI FET capacitance for ultra-broadband mmWave circuits.
- Stacked SOI FETs for high output power (P_{out}) and power-added efficiency (PAE) power amplifier (PA), switch [9-10], low-noise amplifier (LNA) integration with TRX; low PA self-heating (20 nm-thick BOX).
- Back-gate knob for performance tuning over temperature, process and aging.
- Allows wide threshold voltage (V_{th}) adjustment to accommodate process, voltage and temperature (PVT) variations.
- Can be used to tune RF performance for the targeted use conditions.
- Ultra-low power and area for analog-to-digital (ADC) or digital-to-analog (DAC) converters (<10 fJ/conv).
- High density (>5M gates/mm²), high performance, ultra-low power digital signal processing (DSP) for digital filtering and high speed serializer/deserializer. Such capability opens new avenues for bringing intelligence and cognition to RF and FEMs using advanced signal-processing.

Fully-Depleted (FD) SOI with ultra-thin-body and BOX (UTBB) is the most advanced flavor of SOI today. This versatile technology offers high-performance LNAs and PAs, along with low loss switches [9-10], towards full monolithic integration of mm-wave FEMs. The unique architecture of FD-SOI devices incorporates a back-gate beneath the BOX, which can be biased to further boost performance. Ultra-wideband SPDT switches (targeting Ka-band) have been fabricated using 22 nm FD-SOI technology (22FDX ®) from GLOBALFOUNDRIES, featuring three different types of back-gate configurations offered in the foundry library. The impact of the three types of FD-SOI back-gate on the SPDT figures of merit (FoMs) is analyzed, having in mind the use of the Smart-Biasing-Module (SBM) in future designs.

The SPDT switches were designed based on a series-shunt topology, as shown in Fig. 4, for wideband functionality. The designs were made to achieve the lowest possible insertion-loss (IL) while maintaining an isolation (ISO) of 30 dB at 28 GHz. A stack of three transistors was used in each branch targeting 20 dBm of input power 1-dB compression point. NFET devices with 20 nm nominal gate length were used to implement the SPDTs.

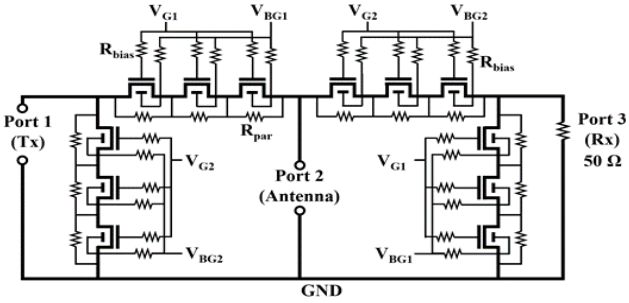


Fig. 5. Schematic of the SPDT switches with back-gate biasing control.

Three SPDTs were fabricated based on the three types of transistors: regular-V_{th} (RVT), super-low-V_{th} (SLVT) and no back-gate implant (BFMOAT), as shown in Fig. 5. The sizes chosen to achieve these specs are W_{series} of 72 µm and W_{shunt} of 29.4 µm. The bias resistors at the gate and back-gate terminals are 9.20 kΩ, and the resistors in parallel with the FETs are 2.45 kΩ. SPDTs with and without matching circuits are considered in this work. To reduce return loss, inductors of 150 pH can be added as series elements at all three ports. Table-II benchmarks our results against state-of-the-art mm-wave SPDT modules in SOI from [11-16] and shows our designs to be competitive. It also highlights that by forgoing the inductor matching circuits, a drastic reduction in SPDT area is achievable at the price of a degraded IL (2.29 dB at 28 GHz). We show that conventional-well devices (Fig. 6) with regular-V_{th} (RVT) and flipped-well devices with super-low-V_{th} (SLVT) make for the best switches below 20 GHz, thanks to the back-gate bias improving device channel resistance and reducing insertion-loss. We also show how the back-gate bias can be used to boost large-signal FoMs, such as P1dB and IIP3.

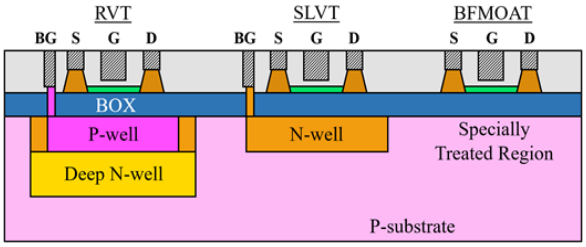


Fig. 6. Simple representation of the three different flavors (RVT, SLVT, BFMOAT) of UTBB-FD-SOI devices considered for the implementation of the mm-wave SPDT switches. The source (S), drain (D), gate (G) and back-gate (BG) terminals are depicted.

The third device, named BFMOAT, lacks the back-gate contact, as the substrate region directly beneath the BOX is specially treated in order to reduce substrate parasitics. Thanks to this, we were able to confirm that these devices are the best choice for switch applications above 40 GHz.

Further improvements of SPDT switches in terms of their DC and RF performance [17-30], accounting for radiation effects, will benefit the following enablers [31-34]:

- Unifying modeling & measurement through converging complementarities in time and frequency-domains [31].
- Qualifying industrial over-the-air (OTA) test solutions handling energy-based metrics [33].
- Enabling smart chip-package-PCB-antenna co-design solutions using advanced FD-SOI RFIC technologies [34].

III. CONCLUSION

In this paper, new *correlation-aware* real-time adaptive tuning of front-end-modules (FEMs) integrated with distributed antennas, using innovative broadband *power-level dependent* physics-based RLC circuit synthesis compliant with f*our-terminal devices*, was proposed. The resulting *Smart-Tuning* solution, in operating the convergence of *Smart-IoT* and *Cognitive-mmWave* applications, exploits the a*daptive-biasing* control available in FD-SOI technologies. Studies of its effects on the RF performance of integrated SPDT switches fabricated in 22 nm FD-SOI technology have demonstrated improvement in key RF parameters. Beyond standard figures of merit used for qualifying SPDT switches, new requirements related with time and frequency domain correlation will lead to new metrics accounting for radiation effects (e.g., *non-reflective smart-loading*) and power-dependent harmonic signatures (e.g., *TDD operation*). A smart-biasing-module (SBM) has been developed and experimentally evaluated demonstrating a wide range of bias control from 1*00pA* to *300mA* over ±8V with 24 bit resolution. Smart-control and regulation in FEMs will open new possibilities for merging Information-Signal Theory (IT) and Physical-Information Theory (PT) into a unified approach. This will foster a wide range of applications in mobile communications with smart devices and systems including m*achine-learning* and a*rtificial-intelligence* brought to FEMs operating at RF, mmWave and optical frequencies [35-36].

ACKNOWLEGMENT

Helpful review and discussions with Dr. Oren Eliezer are gratefully acknowledged.

REFERENCES

[1] S. Wane, D. Bajon et al., “Cognitive Beamformer Chips with Smart-Antennas for 5G and Beyond: Holistic RFSOI Technology Solutions including ASIC Correlators”, in proceedings of European Microwave Week Paris 2019.

[2] T. Cappello, P. Pednekar, C. Florian, S. Cripps, Z. Popović and T. W. Barton, "Supply- and Load-Modulated Balanced Amplifier for Efficient Broadband 5G Base Stations," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3122-3133, July 2019.

[3] Bich-Yen Nguyen, Philippe Flatresse, et al., “A Path to Energy Efficiency and Reliability for ICs: Fully Depleted Silicon-on-Insulator (FD-SOI) Devices Offer Many Advantages”, IEEE Solid-State Circuits Magazine (Volume: 10 , Issue: 4 , Fall 2018).

[4] Sidina Wane, Vincent Huard and Frederic Renoux, “Smart IoT & Cognitive 5G: Importance of FD-SOI Adaptive-Body-Biasing”, 2019 IEEE SOI-3DSubthreshold Microelectronics, San-Jose California.

[5] A. Lesne, “Shannon entropy: a rigorous notion at the crossroads between probability, information theory, dynamical systems and statistical physics”. Mathematical Structures in Computer Science 24(3) (2014).

[6] C. Craeye, “Including Spatial Correlation of Thermal Noise in the Noise Model of High-Sensitivity Arrays,” IEEE Trans. Antennas & Propagation, Vol. 53, No. 11, pp. 3845–48, Nov 2005.

[7] M. Rack and J.-P. Raskin, “SOI Technologies for RF and Millimeter Wave Applications,” *ECS Transactions 2019*, vol. 92, n° 4, pp. 79-94.

[8] B. K. Esfeh, M. Rack et al., “RF small- and large-signal characteristics of CPW and TFMS lines on trap-rich HR substrates”. IEEE Trans. Electron Devices, 2018, 65, 3120.

[9] M. Rack, L. Nyssens, S. Wane, D. Bajon, J.-P. Raskin, “DC-40 GHz SPDTs in 22 nm FD-SOI and back-gate impact study*”, The 2020 IEEE Radio Frequency Integrated Circuits Symposium – RFIC 2020*, Los Angeles, CA, USA, June 21-23, 2020.

[10] S. Yadav *et al*., "Demonstration and Modelling of Excellent RF Switch Performance of 22nm FD-SOI Technology for Millimeter-Wave Applications," *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Cracow, Poland, 2019.

[11] M. Parlak and J. F. Buckwalter, 2011 IEEE Compound Semiconduct. Integrat. Circuit Sympos. (CSICS), Waikoloa, HI, 2011, pp. 1-4.

[12] A. S. Cardoso et al., 2014 IEEE Radio and Wireless Symposium (RWS), Newport Beach, CA, 2014, pp. 199-201.

[13] B. Yu et al., IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 10, pp. 3937-3949, Oct. 2017.

[14] C. Chen, X. Xu and T. Yoshimasu, 2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpar, 2017, pp. 5-8.

[15] C. Li et al., 2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Anaheim, CA, 2018.

[16] C. Elgaard et al., 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019, pp. 303-306.

[17] M. Rack and J.-P. Raskin, *ECS Trans*. 2019, vol. 92, 4, pp. 79-94.

[18] Y. Liu *et al*., *2018 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conference (S3S)*, Burlingame, CA, USA, 2018.

[19] J.-P. Raskin and E. Desbonnets, “High resistivity SOI wafer for mainstream RF system-on-chip,” in *Proc. IEEE 15th Top. Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, San Diego, CA, USA, Oct. 2015, pp. 33–36.

[20] C. R. Neve and J.-P. Raskin, “RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates,” *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 924–932, Apr. 2012.

[21] D. Lederer and J.-P. Raskin, “New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity,” *IEEE Electron Device Lett*., vol. 26, no. 11, pp. 805–807, Nov. 2005.

[22] M. Rack, Y. Belaroussi, K. Ben Ali, G. Scheen, B. Kazemi Esfeh, and J.-P. Raskin, “Small- and large-signal performance up to 175 °C of low-cost porous silicon substrate for RF applications,” *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1887–1895, May 2018.

[23] L. Nyssens, M. Rack and J.-P. Raskin, "New Method for Accurate Transmission Line Characterization on Low-Loss Silicon Substrate at Millimeter-Wave Frequencies," *2019 Microwave Technology and Techniques Workshop ESA-ESTEC*, April 2019.

[24] L. Nyssens, M. Rack and J. Raskin, "Effective Resistivity Extraction of Low-Loss Silicon Substrate at Millimeter-Wave Frequencies," *2019 14th European Microwave Integrated Circuits Conference (EuMIC)*, Paris, France, 2019, pp. 1-4.

[25] N. André, M. Rack, L. Nyssens, *et al*., "Ultra Low-Loss Si Substrate for On-Chip UWB GHz Antennas," in *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 393-397, 2019.

[26] G. Scheen, R. Tuyaerts, M. Rack, L. Nyssens, J. Rasson and J. Raskin, "Post-process local porous silicon integration method for RF application," *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 1291-1294.

[27] M. Rack, L. Nyssens and J.-.P. Raskin, "Low-Loss Si-Substrates Enhanced Using Buried PN Junctions for RF Applications," in *IEEE Electron Device Letters*, vol. 40, no. 5, May 2019.

[28] L. Nyssens, A. Halder, B. K. Esfeh, N. Planes, D. Flandre, V. Kilchytska and J.-P. Raskin, "28 FDSOI RF Figures of Merit down to 4.2 K," *2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Jose, 2019.

[29] L. Nyssens *et al*., "Self-Heating in 28 FDSOI UTBB MOSFETs at Cryogenic Temperatures," *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Cracow, Poland, 2019, pp. 162-165.

[30] L. Nyssens, A. Halder, B. Kazemi Esfeh, N. Planes, D. Flandre, V. Kilchytska and J.-P. Raskin, "28-nm FD-SOI CMOS RF Figures of Merit down to 4.2 K," *in IEEE Journal of the Electron Devices Society*, in press, 2020.

[31] S. Wane, R. Patton, and N. Gross, “Unification of instrumentation and EDA tooling platforms for enabling smart chip-package-PCB-probe arrays co-design solutions using advanced RFIC technologies,” in *IEEE Conf. on Antenna Measurements Applications*, Sept. 2018, pp. 1–4.

[32] S. Wane and N. Aflakian, “Photonics Chip-to-Chip Communication for Emerging Technologies: Requirements for Unified RF, mm-Waves and Optical Sensing”, IEEE Texas Symposium on Wireless and Microwave Circuits and Systems, 2019.

[33] S. Wane, et al., “Energy-Geometry-Entropy Bounds aware Analysis of Stochastic Field-Field Correlations for Emerging Wireless Communication Technologies”, URSI General Assembly Commission, New Concepts in Wireless Communications, Montreal 2017.

[34] Q.H. Tran, S. Wane, et al., “Toward Co-Design of Spin-Wave Sensors with RFIC Building Blocks for Emerging Technologies”, 2018 2nd URSI Atlantic Radio Science Meeting (AT-RASC).

[35] Patent application no. FR1915810, “*Régulation Intelligente des Performances de Composants, Circuits et Systèmes Intégrés incluant des Dispositifs Auto-Tests et une Gestion de l'Efficacité Énergétique*” –"*Adaptive Body Biasing for Smart Thermal-Electrical Harvesting and Built-in-Self-Test (BIST) Control and Regulation of RF performances including Stochastic Antenna Tuning*", 2019.

[36] Patent application no. EP20305671, “*Smart Emitting-Receiving Surfaces and Volumes for 3D Conformal Objects*”, 2020.