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Variable temperature characterization of low-dimensional effects in tri-gate SOI MOSFETs

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ABSTRACT

We report on variable temperature charge transport measurements of tri-gate silicon-on-insulator MOSFETs with fin widths of 11 nm, fin heights of 58 nm and gate lengths ranging from 80 nm to 250 nm. Reproducible inflection points were observed in drain current vs. gate voltage data acquired at low temperature (4–8 K) and low drain bias (0.1 mV), yielding oscillations in the extracted transconductance data which are consistent with formation of a one-dimensional electron gas in the channel. Simulations of the variation in fin potential with gate voltage indicate transport through ~3 sub-bands per fin at gate overdrive of 100 mV above threshold. Observed multi-peak envelopes in measured transconductance vs. gate voltage data for multiple-fin devices suggest sub-band separations ~20 mV, in reasonable agreement with simulation results (27–55 mV). The measured conductance per fin at low temperatures (4–6 K) was on the order of the quantum conductance, consistent with diffusive transport through multiple sub-bands. Measured transconductance features were largely reproducible for repeated measurements on a given device, although slight variations could be observed, possibly due to quantum interference or interface charges.

1. Introduction

As current planar CMOS approaches its scaling limits, three-dimensional transistor designs are being considered as potential alternatives, since enhanced gate coupling from multiple gates result in good control over short-channel effects and leads to higher drive currents [1]. As the width and/or height decrease the influence of quantum effects becomes more prominent and variable temperature electrical characterization can provide valuable insight into carrier transport and scattering in these nanoscale devices. A multiple-gate device with a sufficiently small height and/or width should operate in volume inversion causing the confined carriers to behave as a one-dimensional electron gas (1-DEG), with higher carrier mobility arising from reduced interface scattering [2]. Energy sub-bands within the conduction band have previously been modelled by a number of groups [1–4]. Experimentally, current vs. gate voltage (I_d–V_g) measurements of three-dimensional devices have shown reproducible oscillations [2–6], both for tri-gate (multi-fin) devices with fin widths and heights of 45 nm and 82 nm, respectively [2], as well as for gate-all-around nanowire devices with channel diameters (d) in the range $3 < d < 11$ nm [4,6,7]. At these length scales and at sufficiently low temperatures, such narrow-channel devices would also be expected to show universal conductance fluctuations [8,9], which can arise due to quantum interference effects from scattering of carriers at the channel edges [10]. Here we report on variable temperature charge transport characteristics of tri-gate SOI MOSFETs with fin widths and heights of 11 nm and 58 nm, respectively.

2. Device fabrication and electrical measurements

Standard Unibond SOI wafers were used as the starting substrates. The silicon top layer was 60 nm thick and the buried oxide thickness was 150 nm. The silicon film was doped using boron with a doping concentration of 2×10^{15} cm^{-3}. Silicon fins were patterned with 193 nm lithography and reactive ion etching (RIE). The devices underwent a hydrogen annealing step to smooth the silicon surfaces, round fin corners, and to thin the fins. A 1.7 nm gate oxide was grown by wet oxidation in an Advanced Materials

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in situ steam generation (ISSG) reactor [2,11]. A 6 nm thick TiSiN gate layer was then deposited by low-pressure chemical vapor deposition on the gate oxide, and capped with a 100 nm polysilicon layer. The work function of the TiSiN gate is 4.65 eV, which makes it a "midgap" gate material. Gate electrodes were patterned using lithography and RIE. Source and drain regions were formed by arsenic implantation followed by a 1000 °C, 10 s anneal step. Classical aluminium/silicon metallization was used to complete the process. The devices used in this study had gate lengths of 80 nm, 90 nm, 100 nm, 250 nm and 1000 nm, respectively, where each device consisted of 20 fins operating in parallel. Capacitance–voltage measurements (not shown) on long gate length devices (L_g = 10 μm) yielded a value of C_{ox} = 1.57 μF cm^{-2} and indicated a low density of oxide charge (Q_{ox} < 10^{11} cm^{-2}) [12].

The devices were measured under vacuum (~10^{-6} mbar) in a cryogenic variable-temperature probe station (operating temperatures 4.2–400 K) interfaced to a semiconductor parameter analyser (HP4156A). All devices were measured with constant drain bias (V_{ds} = 100 μV) and the source-, drain- and gate-currents were measured as a function of the gate voltage (V_g). A low drain bias was selected because the oscillations are not observable at drain voltages greater than 1 mV [5]. Both single ($V_{g,min} \rightarrow V_{g,max}$) and double ($V_{g,min} \rightarrow V_{g,max} \rightarrow V_{g,min}$) sweeps were acquired with gate voltage increments (ΔV_g) of either 2.5 mV or 0.5 mV. The maximum measured gate leakage current, I_g < 20 pA for all devices reported here. Of the 72 devices measured at room temperature, eight devices were measured at temperatures down to 4.2 K, these data are presented here.

3. Results and discussion

Fig. 1 shows a cross-sectional transmission electron micrograph of a single fin from a multi-fin device. The fin width, W_{Si} = 11 nm, and the fin height t_{Si} = 58 nm. The density of states (DoS) for a single fin with these dimensions was simulated as described previously [2,11] using a single effective mass m^* = 0.98m_0, where m_0 is the free electron mass. These simulations (not shown) yield a series of sharp peaks (1-D character) on a staircase/parabolic background (2-D/3-D character) [5], where the energy separation between the lowest energy sub-bands (ΔE_{sb}) is in the range 7–15 meV. Fig. 2 shows the simulated variation in the energy of the lowest sub-bands with gate voltage (V_g) for a single fin at low temperature (T = 30 K). Just above threshold, where the influence of the inversion charge is no longer negligible, the variation in energy of the lowest sub-band with gate voltage is ~0.26 eV/V. This variation corresponds to sub-band separations ~27–55 mV in I_d–V_g or transconductance data.

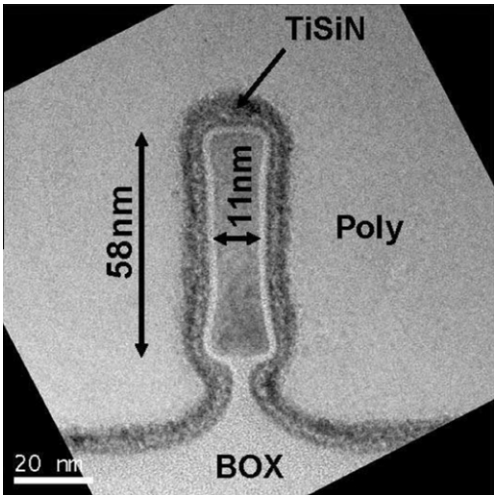

Fig. 1. Cross-sectional transmission electron micrograph of a single fin from a tri-gate device with a width of 11 nm and height of 58 nm.

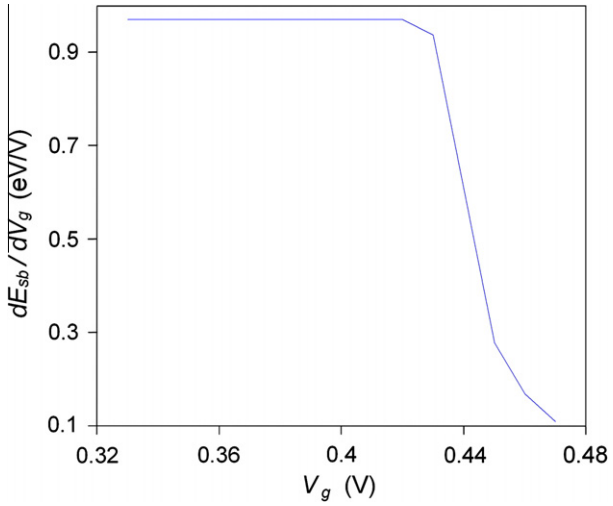

Fig. 2. Modeled variation in the energy of the lowest sub-bands with gate voltage plotted as a function of gate voltage at low temperature (T = 30 K) for a single fin of width 11 nm and height 58 nm.

Fig. 3a (inset) shows the drain current vs. gate voltage (I_d–V_g) measurements for a 20-fin device with gate length (L_g) of 100 nm, acquired under constant drain bias (V_{ds} = 100 μV) at room temperature (T = 300 K). The threshold voltage is V_{th} = 0.35 V with sub-threshold swing, SS = 69 mV/decade. Fig. 3a (main panel) shows consecutive I_d–V_g measurements for the same device at low temperature (T = 4.2 K), where each sweep reveals a sharp increase in conductance as the gate voltage is increased above threshold. Each curve also shows an inflection point at higher gate voltage (V_g ~ 0.62 V), followed by small but reproducible oscillations in the drain current, likely due to increased interface scattering as the carrier density at the fin edges is enhanced relative to the center of the channel. The drain current at constant overdrive voltage ($V_g = V_{th}$ + 0.15 V) is a factor of two lower at room temperature vs. low temperature, indicating significant phonon scattering.

For extraction of the transconductance (g_m) from measured drain current data, the current noise was first minimized by locally averaging the current at each gate voltage measurement value over a 5-point window, e.g., for the ith data point $I_d^{av}(V_g[i]) = I_d(V_g[i-2]) + I_d(V_g[i-1]) + \cdots + I_d(V_g[i+2])$. Eight iterations of this procedure were employed and the transconductance, $g_m = \partial I_d^{av}/\partial V_g$, was then obtained from local linear regression of the averaged drain current **vs. gate voltage data using a 5-point window for each value of V_g. Fig. 3b shows the transconductance (g_m) for the I_d–V_g data shown in Fig. 3a, with peak values in the range 4–6 μS. For the first two sweeps (i and ii), obtained using a relatively large gate voltage increment, ΔV_g = 2.5 mV, three reproducible oscillations can be observed: A broad envelope centred at $V_g \approx 0.59$ V and weaker peaks at $V_g \approx 0.665$ V and 0.705 V, respectively.

Fig. 3b(iii) shows the transconductance for data measured with a smaller gate voltage increment (ΔV_g = 0.5 mV), which enables resolution of the peaks within the broad envelopes observed in Fig. 3b(i and ii). Fitting Gaussian lineshapes to the five peaks observed in the transconductance data shown in Fig. 3b(iii) for gate voltages in the interval 0.54–0.65 V yielded full-width-half-maximum (FWHM) values in the range 8–15 mV and measured center–center peak separations ~14–24 mV. These separations are in reasonable agreement with the estimates calculated from the simulation data presented in Fig. 2 (25–50 mV). Thus, the transcon-

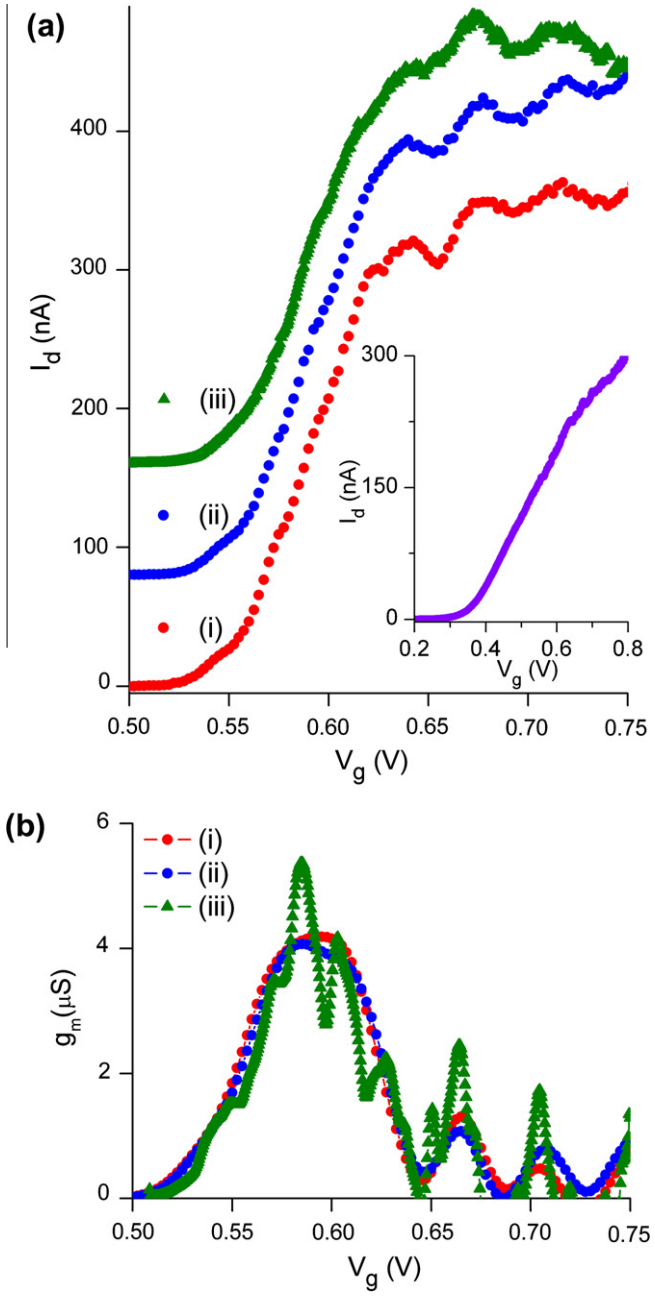

Fig. 3. (a) Sequence of three successive I_d–V_g sweeps measured at $T = 4.2$ K for a $L_g = 100$ nm device with $V_{ds} = 100$ μV (raw data): (i) V_g: 0.4 V → 0.8 V, gate voltage increment $\Delta V_g = 2.5$ mV; (ii) V_g: 0.8 V → 0.4 V, $\Delta V_g = 2.5$ mV; (iii) V_g: 0.75 V → 0.5 V, $\Delta V_g = 0.5$ mV. The curves are offset by 80 nA for clarity. Inset: I_d–V_g for this device at $T = 300$ K with $V_{ds} = 100$ μV and V_g: 0.1 V → 0.8 V. (b) Transconductance (g_m) as a function of gate voltage extracted from the I_d–V_g data shown in (a).

ductance data suggest filling of 3–5 sub-bands at a gate voltage of $V_g = 0.62$ V. Extraction of the precise number of sub-bands is challenging since at these ultra-narrow fin widths (11 nm), additional peaks could appear in measured data arising from minor variations in fin geometry across the 20 fins in the device or from universal conductance fluctuations [8,9], e.g., due to carrier scattering at the fin edges [10]. Measurements on devices with a smaller number of fins (ideally single-fin devices) are needed to investigate the relative magnitudes of the various scattering mechanisms.

Considering the width of the features in the extracted transconductance data, peak broadening resulting from the iterative averaging procedure used to minimize noise in the measured drain current must also be considered. Simulated drain current curves were employed to estimate this broadening, using either a step-function or a step-function superimposed on a parabolic background as the simulated I_d–V_g data with gate voltage increments, $\Delta V_g = 0.5$ mV. Using the same averaging and linear regression procedure described above to extract the transconductance, these step-function changes in the simulated "raw" I_d–V_g data resulted in peaks in simulated transconductance data with FWHM values $\leqslant 7$ mV, comparable to or smaller than the FWHM values extracted from measured data (8–15 mV).

Considering a nanowire fin as a ballistic conductor with n_{SB} modes (sub-bands), the conductance per fin can be written as $G_{FIN} = T_{tr} n_{SB} G_0$, where T_{tr} is the transmission and G_0 is the quantum of conductance, $G_0 = 2e^2/h$, e is the electronic charge, and h is Planck's constant [13]. The conductance of the 20-fin device with data shown in Fig. 3a is $G = 39G_0$ at $T = 4.2$ K and $V_g \approx 0.62$ V, corresponding to a conductance per fin of $G_{FIN,11nm} = 2.0G_0$. For the eight devices measured at low temperatures, with gate lengths ranging from 80 nm to 1000 nm, the conductance per fin at comparable overdrive voltages ($V_g \approx V_{th} + 0.1$ V) ranged from $0.7G_0 \leqslant G_{FIN,11nm} \leqslant 2.0G_0$ with an average value of $1.1 \pm 0.2G_0$. These data compare well with the low-temperature conductance data acquired at similar overdrive voltages for devices with fin widths of 45 nm, $G_{FIN,45nm} = 1.6G_0$ [2], and with reported low-temperature conductance data for gate-all-around nanowire devices with core diameters of 6 nm. $G_{NW-6nm} \leqslant 0.1G_0$ [4,6]. For the 11 nm devices presented here, the simulation results (Fig. 2), together with the transconductance data (Fig. 3b) suggests a small number of sub-bands per fin ($n_{SB} \approx 3$–5). For ballistic conduction in these devices, the maximum conductance per fin at ~100 mV above threshold would then be several times the quantum conductance. While the corresponding conductance data presented here, $0.7G_0 \leqslant G_{FIN,11nm} \leqslant 2.0G_0$, indicate non-negligible scattering, i.e. diffusive transport, it is worth noting that the measured device conductance represents a lower bound for the actual channel conductance due to the access resistance of the source and drain contacts [14–16]. Furthermore, the conductance contribution per sub-band is expected to decrease as the sub-band energy increases, due to increased carrier density close to the gate dielectric interfaces [1].

Fig. 4a shows three consecutive measurements of the drain current (I_d) as a function of gate voltage (V_g) acquired at low temperature ($T = 4.2$ K) for a second device with 100 nm gate length. The same gate voltage increment, $\Delta V_g = 0.5$ mV, was chosen for all three sweeps. The conductance (per fin) of the device at $V_g \approx 0.64$ V is $1.0G_0$, indicating significant scattering. Again, the measured drain current shows reproducible characteristics, with inflection points at $V_g \approx 0.56$ V, 0.58 V and 0.61 V, respectively. Fig. 4b shows the corresponding transconductance (g_m). Reproducible broad envelopes in the transconductance are observed, with maxima at $V_g \approx 0.54$ V, 0.57 V and 0.62 V, respectively and peak g_m values ~3 μS. These data are reproducible although subtle differences are revealed in repeat measurements, possibly due to incomplete surface passivation [6]. Measurements on longer gate length devices ($L_g = 250$ nm, not shown) also reveal reproducible envelopes in the extracted transconductance data, again with slight variations between data obtained for successive gate voltage sweeps.

Thus, oscillations in the transconductance can be observed at low temperature, corresponding to filling of one-dimensional sub-bands. While the position of the peaks corresponding to the sub-band energies varies between devices, possibly as a result of minor differences in device geometry or incomplete surface passivation, the oscillations are largely reproducible for a given device. Concerning the variations in measured conductance (even for devices with the same gate length), a number of factors could contribute: Resistance of the source and drain contacts, crystallographic orientation, surface scattering and Coulomb scat-

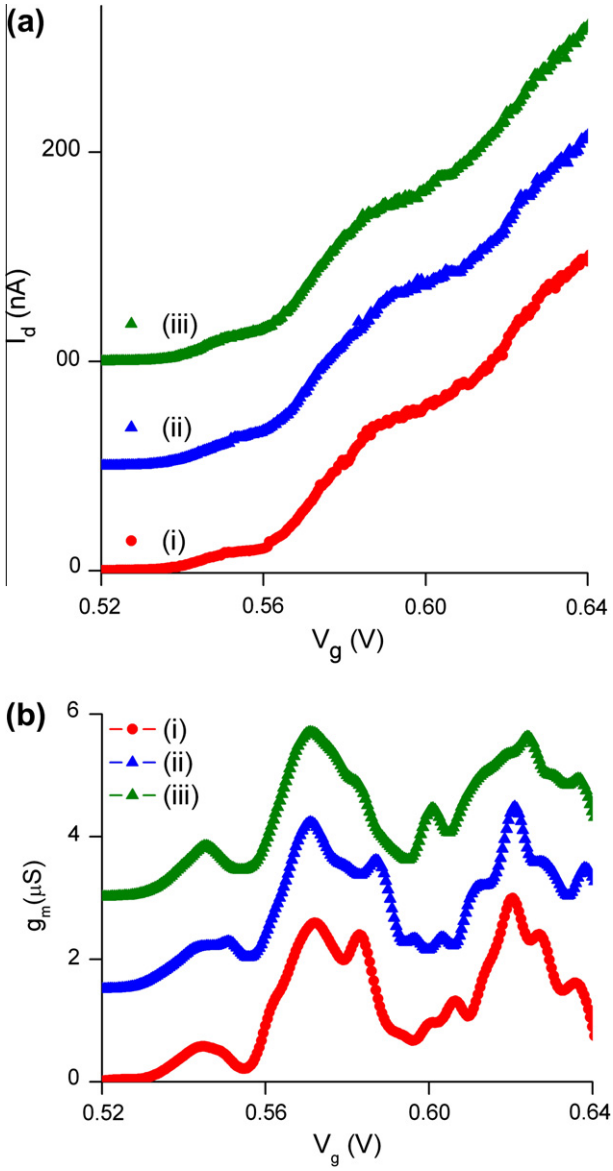

Fig. 4. (a) Sequence of three successive I_d–V_g sweeps (raw data) measured at 4.2 K for a second L_g = 100 nm device with V_{ds} = 100 μV. The gate voltage increment, ΔV_g = 0.5 mV for all sweeps and the curves are offset by 50 nA. (i) V_g: 0.5 V → 0.75 V; (ii) V_g: 0.5 V → 0.8 V; (iii) V_g: 0.8 V → 0.5 V. (b) Corresponding transconductance (g_m) data. The curves are offset by 1.5 μS.

tering [1]. High source(drain) resistance have been reported for tri-gate devices with fin widths of 25 nm or less [16]. For narrow-fin tri-gate devices, the resistance due to the small source(drain) contact area dominates the overall resistance [15,17,18]. The crystallographic orientations of the respective channel–dielectric interfaces are also significant. For the device shown in Fig. 1, the sidewalls are (1 1 0)-oriented while the top fin is (1 0 0)-oriented. The (1 1 0) orientation has a lower mobility [19], relative to the (1 0 0) orientation. For these devices, the fraction of the total effective channel width with (1 0 0) orientation to the total effective width, is given by W_{Si}/W_{eff} = 11 nm/127 nm ≈ 9%. This ratio is considerably smaller than the corresponding fraction for the larger fin devices measured previously (W_{Si}/W_{eff} = 45 nm/209 nm ≈ 22%) [2,11]. Finally, at low temperatures, phonon scattering no longer dominates. Thus, the influence of scattering at the gate dielectric interface(s) becomes more significant [20].

Fig. 5 shows the measured sub-threshold swing as a function of temperature for devices with L_g = 90 nm, 100 nm and 250 nm,

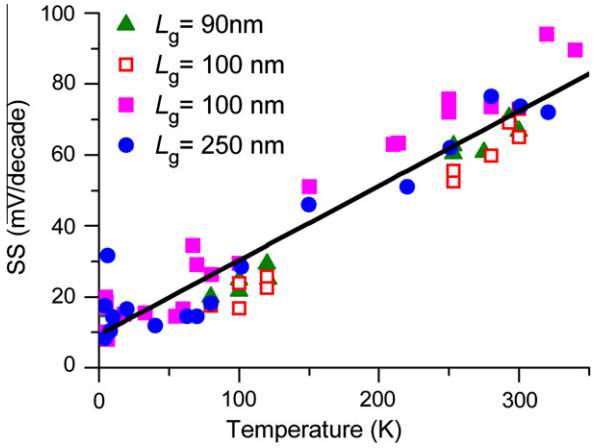

Fig. 5. Sub-threshold swing (*SS*) measured as a function of temperature for tri-gate devices with different gate lengths: L_g = 90 nm device (open triangles), L_g = 100 nm devices (open squares, solid squares), L_g = 250 nm device (solid circles). The solid line represents a linear fit to the entire data set, with slope $(1.06 \pm 0.04)[k_B/e]\ln(10)$.

respectively. A linear fit across all data gives a slope of $(1.06 \pm 0.04)[k_B/e]\ln(10)$, where k_B is Boltzmann's constant and e is the electronic charge. The small offset to the fit (finite swing at zero temperature) is similar to previous reports [4,6,21], and suggests the presence of interface charges, possibly due to incomplete surface passivation [6]. Fits to the temperature dependence of the threshold voltage (V_{th}) yielded slopes from −0.56 mV/K to −0.79 mV/K, in good agreement with previous reports [2,6,11,14,19,22–27].

Of the 72 devices measured at room temperature, 22 showed step-like discontinuities in the I_d–V_g characteristics. The majority of these 22 devices (16) showed small but abrupt changes in conductance ($\Delta G \sim 0.5G_0$) at the same gate voltage in both the forward and reverse sweeps. Similar step-changes in conductance have been reported for nanoscale planar silicon MOSFETs and attributed to fluctuations in occupancy of single electron traps [28,29]. Further work is needed to assess the influence of such traps on device performance and stability.

4. Conclusion

The charge transport characteristics of ultra-narrow multiple-gate SOI MOSFETs with varying gate lengths were investigated at temperatures between 300 K and 4.2 K. Reproducible inflection points were observed in the I_d–V_g measurements at low temperature, yielding oscillations in the extracted transconductance data, arising from filling of one-dimensional sub-bands. Measured conductance data indicate non-negligible scattering in these nanowire devices, consistent with diffusive transport through a small number of sub-bands. Considering the low V_{ds} bias used, these devices show good transconductance with peak g_m values of 1.5–6 μS. The observed envelopes in transconductance data also raise the possibility of convolution of sub-bands with near-identical energies, possibly arising from minor fluctuations in geometry across the fins in each device. While measured transconductance features are largely reproducible for repeated measurements on a given device, slight variations can be observed, possibly due to incomplete interface passivation or universal conductance fluctuations. Measured sub-threshold swing vs. temperature data also suggest the presence of interface charges. The data indicate that variable temperature electrical characterization provides valuable insight into the mechanisms governing carrier transport in these ultra-narrow devices.

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