Performances Evaluation of On-Chip Large-Size-Tapped Transformer for MEMS Applications

Farès Tounsi, Denis Flandre, Libor Rufer, *Senior Member, IEEE*, and Laurent A. Francis, *Member, IEEE*

***Abstract*— This article aims at providing a better behavior understanding and performance evaluation of a large-size passive on-chip tapped transformer when used as a transducer in low-frequency integrated microsystems [30–300 kHz]. Thus, a CMOS-based 1:1 transformer, consisting of 70 turns of 1.6-μm-wide top-level metal spaced by 0.6 μm and with a total length of 1.7 mm, has been investigated and tested. The spatial separation between the two transformer windings was set to 70 μm. An electrical equivalent lumped model has been extracted through an exhaustive specific measurement procedure. The model is useful to simulate and evaluate the voltage transformation ratio (TR) between the two transformer windings. The effects of parasitics and imperfect coupling between transformer windings and through the silicon substrate are outlined from the circuit point of view. We report a magnetic coupling coefficient that does not exceed $k = 0.15$, with a voltage TR of about 0.39 around the resonance frequency of ∼5.3 MHz, when the secondary is unloaded. It has been proven that the interwindings capacitance introduced by close conductors of each winding, evaluated to 13 pF, assures the most important role in the power transfer. This article has shown that by optimizing properly the transformer realization and limiting some parasitics elements, the inductive and capacitive links could both play a key role in MEMS transducers through tapped transformers operation around 100-kHz frequencies.**

***Index Terms*— Capacitive transduction, electrodynamic transduction, lumped elements model, planar microinductors, tapped transformer, voltage transformation ratio (TR).**

I. Introduction

In RECENT technologies, embedding a high number of electronic functions on the same silicon chip notably requires an improvement of passive components integration. Inductive components, such as inductors or transformers, are already key elements in RF and power systems [1], [2]. Integrated planar spirals have been extensively studied and optimized throughout the last two decades, and as a result, their performance has been noticeably improved for inductance values varying from a few tens of nanohenry up to 4 μH, with a quality factor exceeding $Q = 20$ [3]. Transformers, made of two coils placed close together, are useful for various electronic applications, as for energy transfer between two circuits, such as implantable medical devices [4], RF identification tags [5], and wireless power transmission [6], [7]. Monolithic planar transformers fabricated on silicon substrates have been successfully implemented in RF-integrated circuits (RFICs) enabling the implementation of high-frequency circuits in low-noise amplifiers (LNAs) [8], voltage-controlled oscillators (VCOs) [9], mixers [10], and power amplifiers [11]. The advantage of using an integrated microtransformer comes from its full integrability with other electronic circuits, such as dc/dc converters, mobile power delivery applications, wireless applications, or portable devices [12], [13]. During the last two decades, various designs of integrated transformers have been studied with the aim to improve their performance, including high inductance values and quality factor, reduction of losses, and increase of the magnetic link between both inductors. The implementation of these ideas allows enlarging their applications field as documented by various works. For instance, Ahmed *et al.* [14] designed a MEMS-based 3-D-integrated transformer using a magnetic core with a high permeability so as to concentrate the magnetic flux inside the inductor and to increase the quality factor in a small area. This device can improve performances especially for frequencies between 10 and 600 kHz where the output voltage can reach values around 120 mV for an input voltage of 90 mV [14]. The magnetic core presence increases the inductance comparing to similar structures without a magnetic core by a factor of 4–5 [15]. Other authors designed a planar integrated transformer based on a surface micromachining technology, producing a gap between the transformer and the silicon substrate [16], [17]. This technique can suppress the substrate parasitic parameters and can increase the transformer coupling coefficient [18]. On-chip transformers have been studied thoroughly in the literature [19]–[21], and however, their use as a transduction means has not beenaddressed. Thus, this article aims at providing a better behavior understanding and performance evaluation of a large-size passive on-chip transformer when used as a transducer in low-frequency integrated microsystems [20 Hz–200 kHz].

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Passive on-chip transformers can be classified mainly following three different topologies depending on their implementation, namely: stacked, interleaved, and tapped [22]. In stacked transformer, first described by Finlay [23], primary and secondary coils layout are implemented in two different superimposed metal layers. Thus, both vertical and lateral magnetic couplings are utilized to maximize the self- and mutual inductances, and the coupling coefficient can reach the value of 0.9 if the metal windings layers are perfectly aligned [22]. Since one of the windings is closer to the substrate, the stacked transformer is considered to be asymmetric and usually has the lowest self-resonant frequency. For the interleaved transformer first described by Frlan *et al.* [24], both windings are sketched symmetrically on the same plane, so mutual inductance is lower than that of the stacked transformer. Since the dielectric thickness is often much smaller than the minimal space between the two neighboring top metal traces, the interwinding capacitances caused by the lateral electric field between windings of the interleaved transformer are smaller than those of the stacked transformer. The interleaved transformer is considered to be symmetric and can reach high efficiency and high isolation [25]. Concentric transformer, or tapped transformer, wherein both wound planar spirals are implemented concentrically in the same top metal layer, is the less examined topology. Since the two coils are completely separated, the self-inductance is maximized and the intercoil capacitance is minimized. However, because only a single turn in the two coils share the common periphery, the coupling coefficient is lower than 0.5, depending on the separation distance. Since the two inductors are located on different areas, tapped on-chip transformer could be used, beside conventional RF applications, as a transduction element converting a mechanical motion into proportional electrical signal. Such a system could benefit from the variation of the inductive and/or the capacitive link between the two inductances. Subsequently, the electrodynamic transduction of the tapped on-chip transformer can be investigated on a structure consisting of a fixed outer planar inductor on top of the substrate, and an inner one implemented on a micromembrane suspended over a micromachined cavity [26]. Regarding such potential application, the determination of magnetic and electrical fields and corresponding forces between these coils and induced currents is essential.

In this article, we first aim at evaluating and validating an accurate lumped-element equivalent circuit, including all possible links between the two windings of a large-size on-chip tapped transformer realized on a silicon substrate. Due to the substrate parasitics, the large number of turns, the high windings resistivity, and especially the intensity of the capacitive coupling, the classical procedure based on scattering parameters extraction is not applicable [27]. Thus, we determined the lumped parameters in each branch through successive two-port direct measurements in Section III. Next, we examine the voltage transformer ratio in the absence of any fluctuation of the inner inductor when actuating the outer inductor by an ac voltage. The evaluation is made both experimentally and using transformer lumped model. When using this model in a parametric sensitivity analysis, some guidelines toward an optimized configuration will be proposed for designing MEMS applications in Section V [28].

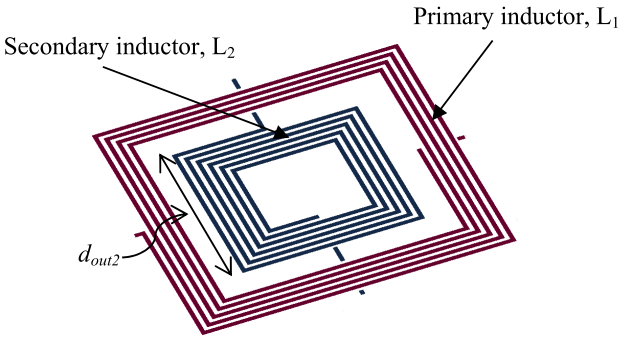

Fig. 1. Basic concept of the tapped on-chip planar transformer composed of two concentric square spirals (the number of turns is randomly set in this figure).

II. Fundamentalsin Tapped Transformers

The operation of a passive transformer basically lies in the mutual inductance M between two or more conductors, or windings. In an ideal transformer, there are no losses, so it can be defined as an element that entirely transmits the input ac power to the load, while blocking the dc component. The voltage transformation ratio (TR) in ideal transformers, once all the flows are coupled, can be expressed by current and voltage TR between windings according to

$$\mathrm{TR} = \frac{v_2}{v_1} = \frac{i_1}{i_2} = \sqrt{\frac{L_2}{L_1}} \tag{1}$$

where v_1, i_1, and L_1 are, respectively, the voltage, current, and inductance of the primary winding (subscript 2 refers to the secondary winding). However, in nonideal transformers, the main electrical parameter is the coefficient of magnetic coupling k. Indeed, since the materials used in the fabrication of an IC chip have magnetic properties similar to air, there is a poor confinement of the magnetic flux in integrated transformers and then $M < \sqrt{(L_1 \cdot L_2)}$ [29]. The strength of the magnetic coupling between both windings, always substantially smaller than one, can be evaluated by the k-factor, as $k = M/\sqrt{(L_1 \cdot L_2)}$.

The tapped monolithic transformer is assembled using conductors interwound in the same plane forming two concentric inductances. In practice, silicon planar transformer includes numerous parasitic components, and a complete lumped-elements equivalent circuit must be derived from the physical layout and the process technology. This is achieved by representing both the primary and the secondary inductors by their equivalent π-models, completed by the mutual capacitive and inductive couplings [30]. Lumped-elements approximation is valid since the physical length of each conducting segment is typically much less than the guided wavelength λ_g in the target operation frequency band.

The fabrication of a 1:1 tapped on-chip transformer was done in a CMOS-compatible process using a CSMC 0.6-μm 2P2M technology, provided by Integrated Circuit design Center (ICC, Shanghai), with main dimensions of the fabrication

TABLE I
TAPPED TRANSFORMER DIMENSIONS

Name*	Description	Value
d_{out2}	outer side of the inner inductor	*1.4 mm*
n_1, n_2	number of turns	*70*
w_1, w_2	width of the metal spiral	*1.6 μm*
s_1, s_2	spacing between metal turns	*0.4 μm*
ε	separation between the two inductors	*70 μm*

*Parameters with i as subindex belongs to the inductor L_i (with i=1 or 2).

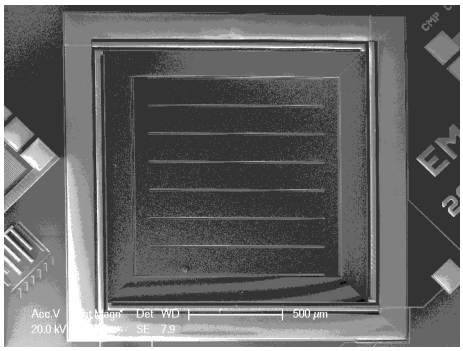

Fig. 2. Scanning electron microscope (SEM) image of the on-chip tapped transformer die.

process listed in Table I. The device was designed for measuring the fluctuations of a diaphragm, triggered by an acoustic and/or ultrasonic wave in the range of 20 Hz–200 kHz. Because of the transducer low operating frequencies, the membrane generally needs to have a large size, around millimeters, which increases the side of both inductors and consequently their series resistances. The secondary inductance would be embedded on the diaphragm to exploit the electromagnetic induction in the device. Its outer side, d_{out2} (see Fig. 1), to be almost equal to the diaphragm side, was determined according to the working resonant frequency. The other dimensions (w_i, s_i, ε) represent the lower limit distances allowed by the technology design rules. Fig. 2 shows the inductors arrangement of the fabricated tapped on-chip transformer. The turns number was taken high in order to quantify their individual contribution on the one hand, and to identify their effects on the device performances on the other. In this article, however, for characterization and modelling purpose before full MEMS optimization and processing, the membrane was not released and the two inductors remain on the silicon substrate. In the final section, removing the substrate parasitics below the inner coil will enable to assess the achievable couplings in an optimally designed MEMS transducer.

III. LUMPED ELEMENTS IDENTIFICATION AND MEASUREMENTS

A. Self-Inductances and Parasitic Elements

The characterization of the on-chip transformer was performed on a die mounted on a DIL-24 package, interconnected with an ultrasonic wire bonding. Transformer lumped parameters are measured by using a precision Agilent LCR Meter 4284A (from 100 Hz to 1 MHz) combined to an integrated parameter analyzer Keithley 4200-SCS (from 10 kHz to 10 MHz). The test equipments were calibrated in the concerned operating frequency band, i.e., from 100 Hz to 10 MHz, and their noise uncertainty verified to be insignificant. Generally, the higher the operating frequency, the more significant the impact of the parasitic elements on the design and performance of the transformer [31]. Initially, primary and secondary inductors are measured separately as a two-port device [32] while keeping the opposite winding open-circuited. P+/− (resp. S+/−) denotes the primary (resp. secondary) transformer accesses. Lumped parameters are extracted and compared via both instruments using four-terminal pair configuration (4TP). Fig. 3(a) shows the measured and fitted log curves of the inner on-chip inductor's reactance and resistance. It is worth noting that the series resistance value is very high due to the large inductor side and number of turns, as well as the material used in the fabrication process, which was a Ti–Al alloy (measured resistivity $\rho = 7.37 \times 10^{-8}\ \Omega \cdot \text{m}$). Consequently, both impedance meters were unable to provide directly the accurate inductance value of both inductors. Nevertheless, it can be extracted by following some additional steps. First, the dc-resistance was determined directly from the real part of the circuit equivalent impedance at low frequencies [see Fig. 3(a)]. In the experienced frequency band, skin effect and other magnetic field effects do not affect the series resistance for more than 2% of the initial value. Subsequently, the intrinsic inductor value was extracted using a "best fitting" procedure, applied separately to L_1 and L_2. The inductor equivalent circuit is usually described as a series inductance $L_{s,i}$ in series with a series resistance $R_{s,i}$, representing the conductive planar spiral, all in parallel with a stray capacitance $C_{s,i}$ (with $i = 1$: primary, or 2 : secondary). The latter models both the interstrip capacitance and the overlap between the spiral and the underpass, resulting in a direct capacitive coupling between the two inductor terminals [13]. This interstrip capacitance between adjacent traces causes the inductor to self-resonate at a specific frequency ($\sim 1/\sqrt{(L_s \cdot C_s)}$). Beyond this resonance frequency, the inductance becomes equivalent to a pure capacitance, and then, the C_s value could be extracted from the slope of the total impedance modulus. Last, the series inductance $L_{s,i}$ can be extracted from the frequency band before resonance, i.e., 10 kHz–1 MHz in this case, wherein the reactance slope is ~20 dB/decade, as

$$\left(L_{s,i} - C_{s,i}\ R_{s,i}^2\right) \quad \omega = X_{e,0} \tag{2}$$

where ω is the angular frequency and $X_{e,0}$ is the reactance value measured at any frequency in the mentioned range (preferably at the center, 100 kHz). From this identification method, a first-order model, which corresponds to the inductor classical model, has been proposed in Fig. 3(b). However, the latter does not fully fit the measured curve, especially around the resonant frequency. An improved model, which corresponds closely to the measurements, is proposed in Fig. 3(c). In this model, it is assumed that turns, belonging to one winding, placed far away from the secondary winding will contribute neither to the main series inductance nor to the interstrip capacitance, due to the impact of large separation distances. This implies that turns located near the outer

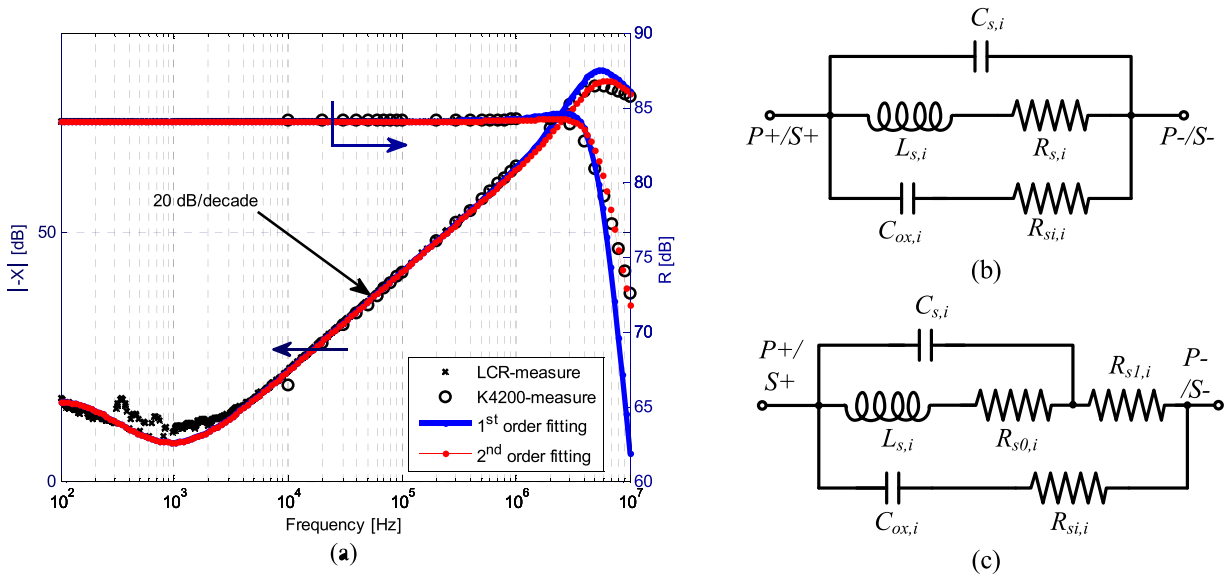

Fig. 3. (a) Inner on-chip inductor equivalent reactance (left axis) and resistance (right axis), measured and fitted curves. (b) On-chip inductor first-order lumped model. (c) On-chip inductor second-order lumped model.

TABLE II
INDUCTORS PARAMETERS FROM THE SECOND-ORDER LUMPED MODEL [SEE FIG. 3(c)]

Parameters	Primary	Secondary
Total series resistance $R_{s,i}$	17.71 kΩ	16.06 kΩ
Partial series resistance, $R_{s1,i}$	2420 Ω	2194 Ω
Interstrips capacitance, $C_{s,i}$	1.91 pF	2.53 pF
Series inductance, $L_{s,i}$	346.7 µH	282.9 µH
Oxide capacitance, $C_{ox,i}$	128.06 pF	77.54 pF
Silicon substrate resistance, $R_{si,i}$	22.79 MΩ	20.92 MΩ

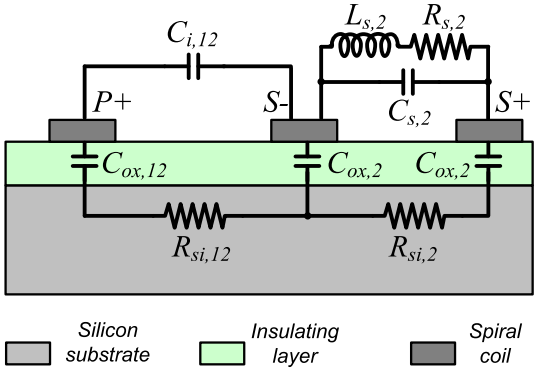

Fig. 4. Origin of parasitic elements of the on-chip transformer in silicon cross section (lumped elements of outer inductor are not represented).

boundary of the primary winding will have weak interactions with those located in the inner boundary of the secondary, and inversely. Accordingly, the series resistance is divided into two parts: the first component $R_{s0,i}$ still acts in parallel with the stray capacitor, while the second $R_{s1,i}$ is in series with the inductor equivalent model [see Fig. 3(c)]. Extracted values of all lumped elements of the circuit shown in Fig. 3(c) are specified in Table II, for the frequency range of interest at which measurements were performed, i.e., [100 Hz–10 MHz]. Finally, from Fig. 3(a), we noted that the equivalent reactance of the on-chip inductor ascends, in absolute value, toward low frequencies. This could be explained by leaks between inductor traces through the silicon substrate, which can be modeled by a capacitor in series with a resistor. This leaky branch, when assembled in parallel with the model of the inductor, creates a first resonance, toward low frequencies ∼kHz, in the inductor reactance curve. The capacitance $C_{ox,i}$ models the vertical field oxide between the spiral trace and the silicon substrate, while $R_{si,i}$ is modeling the lateral silicon substrate resistivity, for frequencies lower than 1 kHz, in this case. Their values are extracted from the reactance curve fitting before the first resonance frequency [see Fig. 3(a)]. The physical origin of the parasitic elements on the transformer is depicted on a silicon cross section shown in Fig. 4 [33]. During the measurement, to neutralize the impact of any possible coupling between transformer windings when measuring the self-inductance of the primary, the secondary accesses were tied together and court-circuited to ground (and similarly for secondary measuring). In this way, zero potential and current conditions are imposed on the nonmeasured winding, which prevents any interactions.

B. Inductive and Capacitive Couplings

In absence of relative motion between the two coils, inductive and capacitive couplings depend on purely geometrical parameters, which are constant and proportional to the conductors length and inversely proportional to the average separation ε_a between the two windings [34]. Mutual inductance, or inductive coupling, value could be derived from the measured inductance in series-aiding and series-opposing configurations, as shown in Fig. 5(a). Since the combined inductance (L_a) in the series aiding connection is $L_a = L_{s,1} + L_{s,2} + 2M$, while L_o in the series opposing connection is $L_o = L_{s,1} + L_{s,2} - 2M$, the mutual inductance is calculated as $M = (L_a - L_o)/4$ [7].

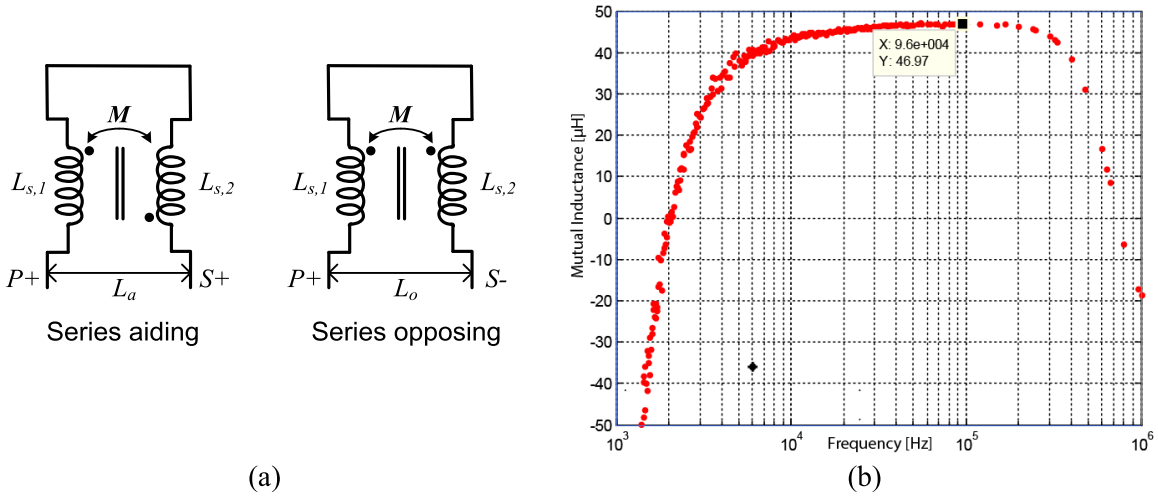

Fig. 5. (a) Inductances series-aiding and series-opposing configurations. (b) Measured mutual inductance curve.

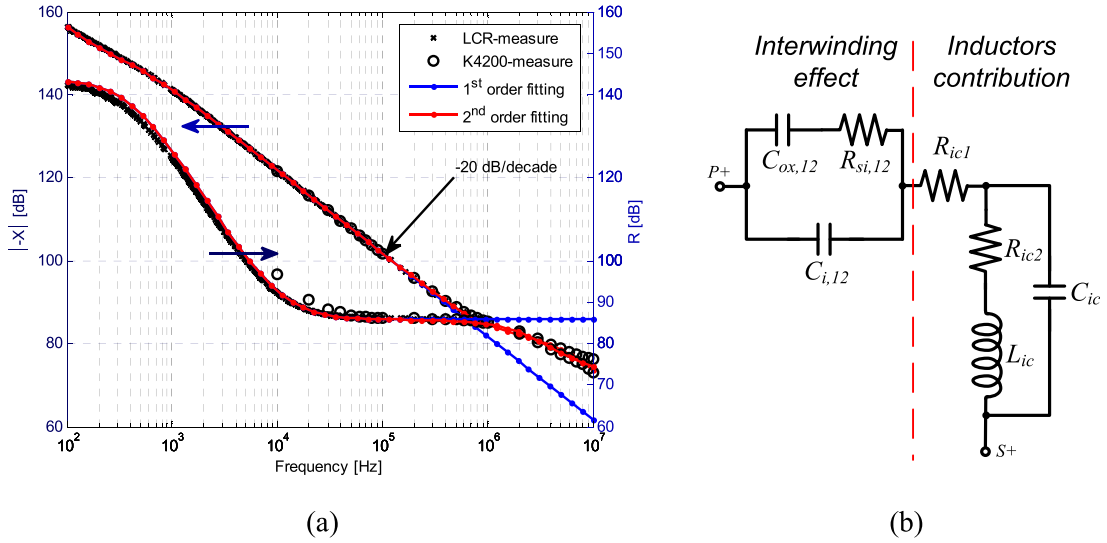

Fig. 6. Interwinding (a) reactance absolute value and resistance measured and fitted curves. (b) Equivalent electrical model.

Practically, Fig. 5(b) shows the circuit reactance over frequency measured in series aiding connection, then inversely, and the difference is divided by 4. Here, it is obvious that the mutual inductance, evaluated to 46.94 μH, is measurable only within the frequency band where the inductive behavior is existing, i.e., ∼10 kHz–400 kHz [see Fig. 3(a)]. Despite inductor high resistivity, the magnetic coupling coefficient in the on-chip transformer is assessed to be $k = 0.15$. Thus, as reported in bibliography, tapped transformer provides moderate magnetic coupling ($k < 0.5$) due to the poor confinement of the magnetic flux, and consumes a large amount of the chip area. However, the self-inductance is maximized, and port-to-port capacitance is minimized.

In addition to the mutual inductance link between turns belonging to each inductor, a capacitive coupling coexists. This interwinding capacitance between primary and secondary was measured by connecting the instrument between the secondary winding accesses tied together, referenced back to the tied primary accesses. Measured interwinding reactance and resistance are shown in Fig. 6(a), by merging data collected from LCR meter and impedance analyzer. As shown, in the frequency band [1 kHz–1 MHz], the coupling reactance is purely capacitive, represented by $C_{i,12}$ shown in Fig. 4, and equal to ∼13 pF. As in the inductance measurement, a leakage branch between the two windings exists through a substrate, modeled by $C_{\mathrm{ox},12}$ and $R_{\mathrm{si},12}$ [see Figs. 4 and 6(b)], it is influential only toward low frequencies and is connected in parallel with the coupling capacitor $C_{i,12}$. Furthermore, since the current flows through a portion of the primary inductor tracks before being coupled with the secondary, the resistance of this portion must be considered. It is modeled by a resistor, $R_{\mathrm{ic1}} + R_{\mathrm{ic2}}$, connected in series with both coupling branches (capacitive and through substrate). A first-order estimate of the interwinding capacitance by considering only the measured series resistance of the traces ($R_{\mathrm{ic1}} + R_{\mathrm{ic2}}$) works well up to 1 MHz [see Fig. 6(a)]. The obtained resistive value is of the same order of magnitude as the series resistances obtained in Table II. Beyond 1 MHz, the first-order interwinding model diverges from measurement, whereas considering a part of the inductors lumped elements allows for adjusting

TABLE III
SECOND-ORDER FITTED MODEL PARAMETERS OF THE INTERWINDING EQUIVALENT ELECTRIC MODEL BETWEEN THE TWO ON-CHIP TRANSFORMER INDUCTORS

Physical parameter	$C_{i,12}$ [pF]	$C_{ox,12}$ [pF]	$R_{si,12}$ [MΩ]	R_{ic1} [kΩ]	R_{ic2} [kΩ]	C_{ic} [pF]	L_{ic} [μH]
Value	13.03	12.88	62.89	3.4	15.06	3.55	120

the fitting [see Fig. 6(a)]. The second-order fitting considers the influence of a part of the lumped elements from both inductors, C_{ic} and L_{ic}, which introduce a supplementary pole close to the megahertz, and shifts the reactance higher than the −20 dB/decade first-order behavior [see Fig. 6(b)]. The obtained reactance has no straightforward physical meaning since it only represents the contribution of a portion of the two inductances which appears around the self-resonating frequency. Hence, this is only useful here for fitting the fully interwinding response beyond 1 MHz and will have no effect on the transformer behavior. Table III gathers the fitted parameters of the interwinding model, as shown in Fig. 6(b), which are in agreement with the curve shown in Fig. 6(a).

IV. VOLTAGE TR DETERMINATION

Transformers are designed to couple alternating currents from one winding to the other without a significant loss of power. Based on the lumped parameters identified in Section VI, the output voltage will be generated because of two effects: inductive and capacitive couplings between the two spiral inductors. Consequently, the transduction between the primary and secondary windings is ensured by a superposition of an electromotive force and a filtered voltage through the capacitive coupling branch. The capacitive coupling between both windings is disadvantageous in pulse transformers working around radio frequencies because it limits their bandwidth; however, it will be valuable in the case of transformers operating at low and medium frequencies for maximizing the electromechanical transduction in MEMS. The electromotive force component, as given by Faraday's law of induction, is a voltage that arises in a closed conducting path from the time rate of the flux change ($\text{emf} = -d\Phi/dt$). A nonzero value of the emf may result from a relative motion between a steady flux and a closed path (motional emf), and/or a time-changing flux linked over a stationary closed path (transformer emf) [35]. In the absence of motion between tapped transformer windings, we can generate a time-varying magnetic field by applying an ac-current to the primary which will induce an emf in the secondary. The experimental setup to measure the device voltage TR is using a three-port configuration, as shown in Fig. 7. In this assembly, a function generator (50 Ω) is connected to the primary winding, and an oscilloscope to the secondary through an active probe (4.9 pF and 10 MΩ). The oscilloscope should have a high input impedance to avoid output signal degradation. The output voltage magnitude and phase change over frequency are measured for a range from 10 kHz to 40 MHz. This experiment allows as well the quantification of inductive and capacitive links.

Fig. 8 shows the measured TR module and phase shift, which are strongly frequency dependent. The measured

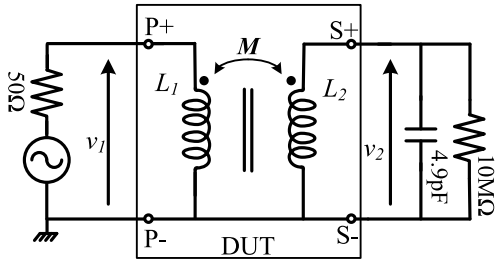

Fig. 7. Direct measurement of the transformation voltage ratio in a 3-port configuration.

induced voltage reached a magnitude of about 2 V around a resonance frequency of ∼2 MHz, when applying a 10-V_{pp} ac voltage. Alongside, the phase shift varies from $\pi/2$ to $-\pi/2$, vanishing around the same resonance frequency [see Fig. 8(b)]. The voltage TR increases with a slope of 20 dB/decade in the frequency band before resonance. The parasitic elements determine many characteristics in the frequency response, such as the presence of the interstrip capacitance, causing the cicuit self-resonance, which limits the applicable frequency range of the tapped transformer. For validation, the extracted on-chip transformer lumped equivalent model was simulated with Advanced Design System (ADS), and Fig. 8 shows the simulated voltage TR and phase shift versus the frequency, which match well with measured curves. One point to emphasize is that in the simulated circuit, as shown in Fig. 9, the series resistance $R_{s,i}$ was divided before and after the capacitive/inductive couplings. Indeed, the resistance between transformer windings terminals (e.g., P+ and S+) should be equal to the one measured when evaluating the interwinding capacitance given in Table III (i.e., $R_{ic1} + R_{ic2}$). As a result, the resistance considered in the same branch in series with the capacitance $C_{i,12}$ is represented by the sum of ($R_{s2} + R_s/2$), whereas the series resistance with the inductance is represented with $R_s/2$. This division is justified since the current flows through a portion of the primary winding before being coupled with the secondary. The simulated model considers as well the generator internal resistance and the oscilloscope probe input impedance. Fig. 9 shows the equivalent total circuit of the tapped planar transformer at low frequencies; it could be more simplified since the parasitic elements represented in gray do not significantly affect the voltage response. The latter is evaluated when using 3-port configuration (grounding two transformer extremities) and symmetrical consideration of the substrate. This simplified compact model will be useful thereafter to determine the most impactful circuit elements on the voltage gain. It is clear that the inductor in the primary affects the low end of the frequency response by shunting energy to ground, while the series element blocks transmission of the

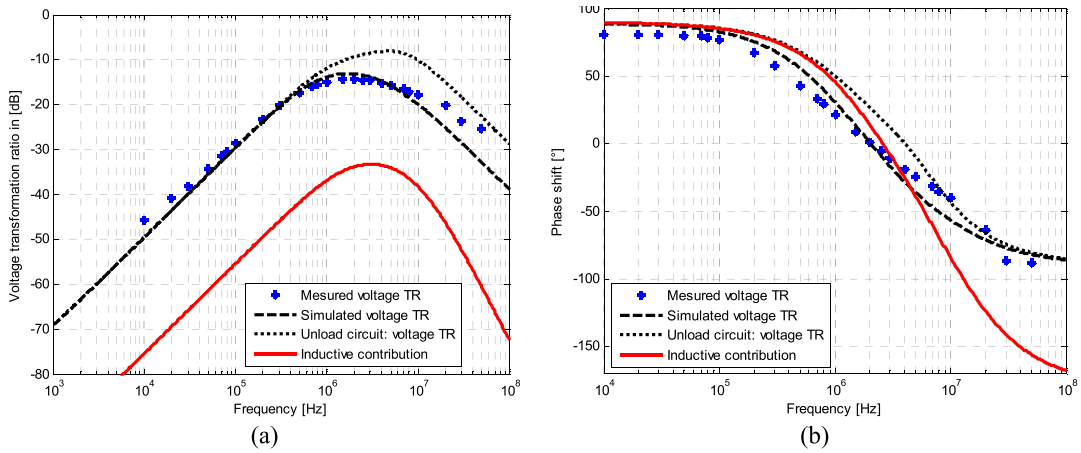

Fig. 8. Voltage TR function of the tapped on-chip transformer (a) module and (b) phase shift versus frequency.

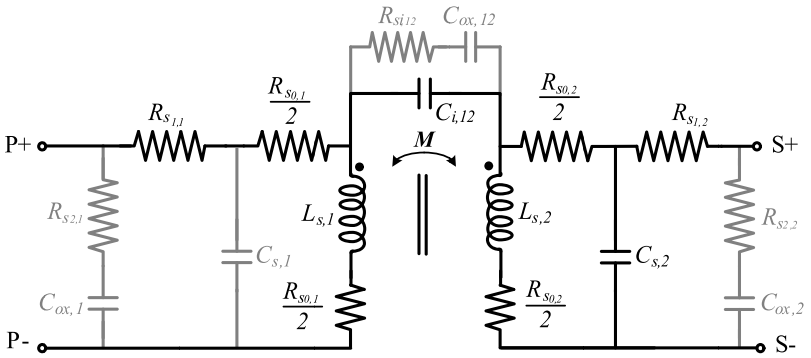

Fig. 9. Simplified lumped physical model of the tapped on-chip planar transformer (elements in gray are uninfluential).

signal from primary to secondary as the operating frequency increases. The output voltage is the superposition of inductive and capacitive contributions; the inductive contribution in voltage TR module and phase is shown in Fig. 8. As can be estimated from Fig. 8(a), the inductive contribution represents only 10% of the total measured gain, so the rest comes as the capacitive coupling contribution. Finally, the unloaded lumped circuit is simulated, and the voltage ratio and phase shift are also plotted in Fig. 8. Two essential features are noted: the resonant frequency increases to ∼5.3 MHz, and the maximum gain module increases to ∼0.39 (corresponds to −8.17 dB shown in Fig. 8).

It is worth to note that in tapped configuration, the inductive contribution remains low compared with the capacitive one. Indeed, using a high number of inductor turns, the inductance increases and the k-factor weakens since M does not raise proportionally to the inductance. In fact, the mutual inductance (and capacitance) of the transformer is proportional to the peripheral length of each winding. Hence, the more distant the inductor turns are from the secondary winding, the more their contribution will be only on the series resistance, capacitance, and self-inductance. Thus, when increasing turns number, the capacitive link becomes dominant over the mutual inductance, and vice versa. Unlike tapped transformers, interleaved and stacked (i.e., overlaying) planar metal traces or conductors maximize the periphery between windings and promote mutual inductance at the expense of increased interwinding capacitance.

V. Applicability and Discussion

The tapped transformer, formed by two concentric coplanar inductors separated by a spatial distance, permits a transfer of energy between its two windings via an inductive coupling superimposed to a capacitive one. The simplest way to exploit this type of transformer as a transducer is to place the internal inductor on a silicon micromachined cavity, and the external inductance on the substrate. Under the effect of, e.g., a pressure, both inductive and capacitive couplings between the two windings will vary, and subsequently, the amplitude of the induced voltage at the secondary. It is worth noting that substrate losses in the doped substrate, which cause usually a large degradation in the overall quality factor and reduce performances, are excluded since the inner inductor will be suspended over a membrane and the substrate back side is not grounded. In addition, the absence of substrate underneath the diaphragm, as shown in Fig. 10, cancels any leaks through the substrate already identified in the model of the inductance (i.e., $C_{\mathrm{ox},2}$ and $R_{\mathrm{si},2}$). The developed model based on a lumped-element equivalent circuit, as shown in Fig. 9, constitutes an efficient and accurate approach to predict the voltage transformer ratio variation. Because of nonidealities, transformer ratio is low even around resonance frequency mainly due to the leakage in the magnetic flux confinement, strip metal losses, parasitic capacitance, and substrate losses, which result in $v_2/v_1 < n_2/n_1$. One disadvantage of tapped design is that the total length of unwounded primary and secondary windings,

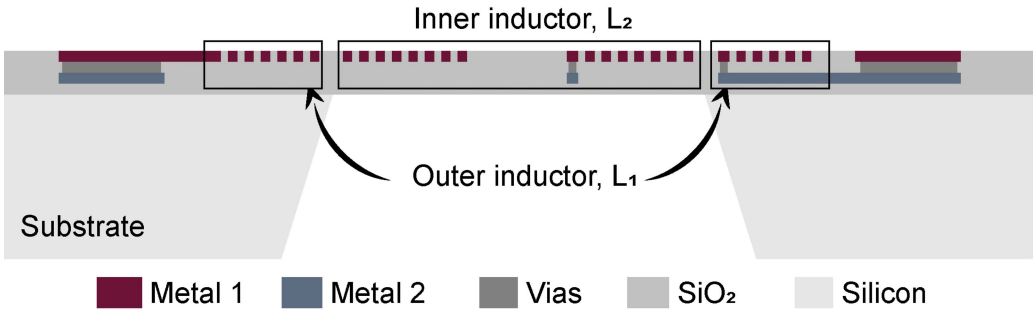

Fig. 10. Proposed structure exploiting large-size tapped transformer as MEMS-based transducer with silicon removed underneath the membrane.

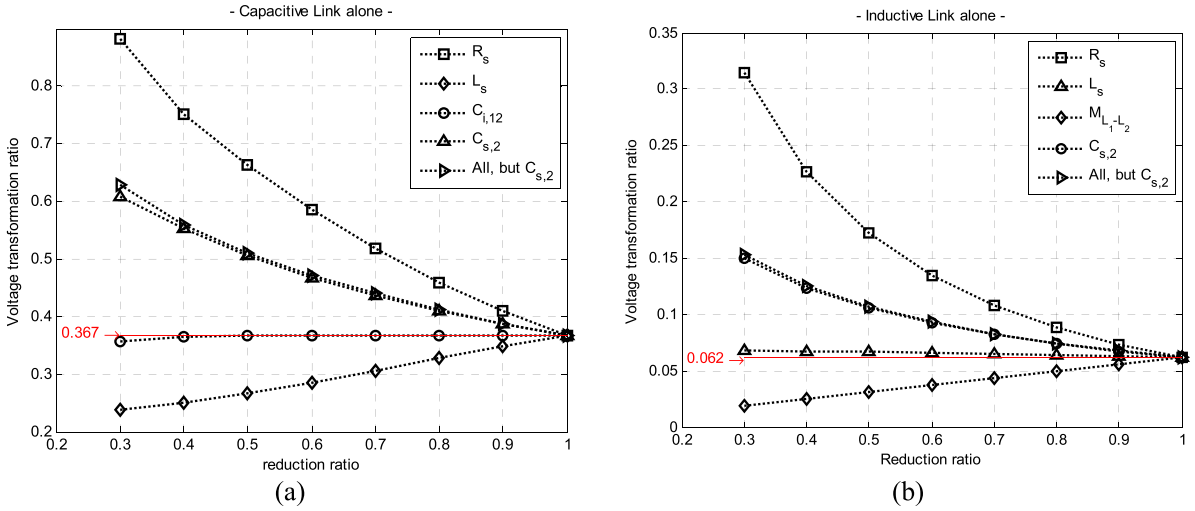

Fig. 11. On-chip lumped parameters influence on the voltage TR when considering only (a) capacitive link and (b) inductive link. (the straight line in both figures represents the initial voltage TR).

when setting the same turns number, is not equal because windings size are asymmetric, which affect the inductance, series capacitance, and resistance values. The interwinding parasitic capacitances and substrate equivalent circuit resonate with the inductance of each winding, and above self-resonance frequencies, the transformer reactance appears capacitive. As in the modeling of any distributed system, the accuracy of the lumped circuit approximation breaks down at higher frequencies since other phenomena begin to act such as skin effect, proximity effect, and Eddy current in the substrate. Hence, the self-resonant frequency is often used as a figure of merit to define and compare the operating frequency limit of transformers. Therefore, the lumped model exhibits a sufficient accuracy up to the self-resonant frequency of the transformer, which delimits the frequency range of interest as it represents the region where both spirals act as an inductor.

Compared with stacked and interleaved on-chip transformers, less research has been done on the modeling and design of integrated tapped transformers, which make difficult to obtain a generic analytical model. Its advantage lies in the fact that its two windings occupy two distinct zones, and therefore, the device can be useful as a transducer in MEMS applications. The lower interest in this structure could be explained by the lower transformer performance compared with other transduction types, which is due to the weaker coupling between its windings and the effect of the larger spatial separation distance. Consequently, there are no straightforward and accurate equations that can be used to evaluate coupling parameters, i.e., mutual inductance and interwinding capacitance, as a function of the transformer geometrical characteristics. In this article, to evaluate energy transfer between both transformer windings, we assessed the influence degree of each parameter from the lumped circuit on the voltage TR in order to propose some guidelines to improve the design performances. First, the influence of each parameter has been examined separately as follows. The capacitive coupling voltage TR of the unloaded circuit, as shown in Fig. 9, has been quantified through ADS simulations, using the extracted lumped-circuit parameter values and resulting in a capacitive partial gain of ∼0.367. When using a parametric analysis, Fig. 11 shows the effect of a reduction ratio of each lumped element on the voltage TR. It can be clearly seen that the total series resistance R_s is the most influential parameter followed by the parasitic capacitance $C_{s,2}$ of the secondary. Thus, a thicker metal could practically reduce the series resistivity and, then, the ohmic losses in the primary and secondary windings. In addition, reducing the number of inductor turns allows for minimizing the parasitic capacitance and the series resistance; however, the inductance L_s could also be reduced. Moving away transformer windings will also reduce the interstrip capacitance, but it will also decrease inductive and capacitive couplings. Therefore, a compromise between these three critical parameters will need to be studied carefully on a large variety of tapped transformers. On the other hand, when considering inductive

coupling simulated in ADS, similar trend can be obtained when reducing the values of R_s and $C_{s,2}$. In all swept configurations, the influence of the capacitive link is higher than the inductive one. Methods of increasing k include: increasing the number of turns in order to increase the couplings and reducing the spacing between windings. However, a high number of winding traces increase the mutual coupling between adjacent turns, and hence, contribute to the self-inductance of each individual winding and as a result, less mutual inductance. Nonetheless, as 13% of the winding lengths do not contribute to the interwinding couplings (obtained from the $R_{s1,i}/R_{s,i}$ ratio shown in Table II), scaling down all the lumped elements by this same ratio except for $C_{i,12}$ and M could be a first obvious optimization leading to increase the voltage TR up to 0.52 according to ADS simulations. Another conceivable improvement is to design a step-up transformer configuration setting $n_2 > n_1$ ($n = n_1{:}n_2$), in addition to designing a better balanced transformer by bringing $L_{s,2}$ value equal to $L_{s,1}$. A major drawback of the tapped transformer is the spatial separation between its two inductors, which leads to lessen the mutual coupling ($k \ll 0.5$) compared with interleaved and stacked counterparts. This spatial separation could significantly improve both couplings, once optimized. A point to emphasize is that in presence of motion between the two windings, the total fem will be generated by the motional fem superimposed to the transformer one. Next step in this work is to analytically investigate the inductive and capacitive couplings to maximize transduction between primary and secondary windings through a microfabrication followed by an investigation of wide range on-chip transformers dimensions.

VI. Conclusion

In this article, we presented an exhaustive experimental measurement procedure, which aims to determine a lumped scalable model of an on-chip large-size planar tapped transformer fabricated with a CMOS-standard technology. All useful and parasitic elements of the model have been identified and linked to the physical implementation in the frequency range [100 Hz–10 MHz]. The outer and inner inductance values are on the order of $\sim$300 μH and the mutual inductance is $\sim$47 μH, for a spatial separation of 70 μm. It was verified that the measured and simulated transformation voltage ratios between primary and secondary windings agree well and feature an increase over frequency up to a ratio of 0.39, around a resonance frequency of 5.3 MHz when the transformer is unloaded. The large-size on-chip extracted model allowed to discriminate the dominant capacitive coupling versus the magnetic one, as well as the main parasitic sources of losses which could play an important role as a transduction. A first-order parametric analysis based on the extracted lumped model indicates that by scaling down adequately the outer and inner winding dimensions, the inductive and capacitive couplings could be enhanced, while reducing the parasitics, to achieve a higher overall TR. Potential designs optimization guidelines are discussed. Capacitive coupling, estimated to be around 13 pF, appears to be highly beneficial in transducers operating in low frequencies and having a potential use in several microsensors and actuators. Indeed, it could detect mechanical motions, when suspending the transformer inner winding, by means of a combination of inductive and capacitive transductions.

References

[1] V. C. Valchev and A. V. Bossche, *Inductors and Transformers for Power Electronics*. 1st ed. Boca Raton, FL, USA: CRC Press, Mar. 2005.

[2] E. Ragonese, A. Scuderi, T. Biondi, and G. Palmisano, *Integrated Inductors and Transformers: Characterization, Design and Modeling for RF and MM-Wave Applications*, 1st ed. Boca Raton, FL, USA: CRC Press, Nov. 2010.

[3] R. Wu, S. Raju, M. Chan, J. K. O. Sin, and C. P. Yue, "Silicon-embedded receiving coil for high-efficiency wireless power transfer to implantable biomedical ICs," *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 9–11, Jan. 2013.

[4] M. Sawan, S. Hashemi, M. Sehil, F. Awwad, M. Hajj-Hassan, and A. Khouas, "Multicoils-based inductive links dedicated to power up implantable medical devices: Modeling, design and experimental results," *Biomed. Microdevices*, vol. 11, no. 5, pp. 1059–1070, Oct. 2009.

[5] C. Sauer, M. Stanacevic, G. Cauwenberghs, and N. Thakor, "Power harvesting and telemetry in CMOS for implanted devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2605–2613, Dec. 2005.

[6] Y. P. Su, X. Liu, and S. Y. R. Hui, "Mutual inductance calculation of movable planar coils on parallel surfaces," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 1115–1123, Apr. 2009.

[7] Z. K. Yue, Z. Z. Liu, Y. J. Hou, H. Zeng, L. H. Liang, and S. Cui, "A new type of coil structure called pan-shaped coil of wireless charging system based on magnetic resonance," *IOP Conf. Ser., Earth Environ. Sci.*, vol. 93, Nov. 2017, Art. no. 012061.

[8] D. J. Cassan and J. R. Long, "A 1-V AC low-noise amplifier for 5-GHz wireless lan in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.

[9] J. W. M. Rogers and C. Plett, "A 5-GHz radio front-end with automatically Q-tuned notch filter and VCO," *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1547–1554, Sep. 2003.

[10] J. P. Maligeorgos and J. R. Long, "A low-voltage 5.1-5.8-GHz image-reject receiver with wide dynamic range," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1917–1926, Dec. 2000.

[11] W. Simburger, H.-D. Wohlmuth, and P. Weger, "A monolithic 3.7 W silicon power amplifier with 59% PAE at 0.9 GHz," in 1st ed *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers. (ISSCC)*, Jan. 2003, pp. 230–231.

[12] C.-H. Huang *et al.*, "Design and modeling of planar transformer-based silicon integrated passive devices for wireless applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Boston, MA, USA, Jun. 2009, pp. 7–9.

[13] E. Ragonese *et al.*, "A fully integrated galvanically isolated DC converter with data communication," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1432–1441, Apr. 2018.

[14] M. Z. Ahmed, M. S. Bhuyan, A. K. M. T. Islam, and B. Y. Majlis, "Design and fabrication of a MEMS 3D micro-transformer for low frequency applications," *Asian J. Sci. Res.*, vol. 8, no. 2, pp. 237–244, Feb. 2015.

[15] C. H. Ahn and M. G. Allen, "A planar micromachined spiral inductor for integrated magnetic microactuator applications," *J. Micromech. Microeng.*, vol. 3, no. 2, pp. 37–44, Jun. 1993.

[16] Y.-S. Choi, J.-B. Yoon, B.-I. Kim, and E. Yoon, "A high-performance MEMS transformer for silicon RF ICS," in *IEEE Tech., Dig. (MEMS)*, Jun. 2003, pp. 653–656.

[17] C. D. Meyer, S. S. Bedair, B. C. Morgan, and D. P. Arnold, "high-inductance-Density, air-core, power Inductors, and transformers designed for operation at 100–500 MHz," *IEEE Trans. Magn.*, vol. 46, no. 6, pp. 2236–2239, Jun. 2010.

[18] J. Yunas, A. A. Hamzah, and B. Y. Majlis, "Surface micromachined on-chip transformer fabricated on glass substrate," *Microsyst. technol.*, vol. 15, no. 4, pp. 547–552, Apr. 2009.

[19] S. S. Mohan, C. P. Yue, M. del Mar Hershenson, S. S. Wong, and T. H. Lee, "Modeling and characterization of on-chip transformers," in *Int. Electron Devices Meeting Tech. Dig.*, San Francisco, CA, USA, Nov. 2002, pp. 531–534.

[20] J. Chen and J. J. Liou, "On-chip spiral inductors for RF applications: An overview," *Semicond. Technol. Sci.*, vol. 4, no. 3, pp. 149–167, 2004.

[21] R. Bajwa and M. K. Yapici, "Integrated on-chip transformers: Recent progress in the Design, Layout, modeling and fabrication," *Sensors*, vol. 19, no. 16, p. 3535, Aug. 2019.
[22] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
[23] J. Laskar, B. Matinpour, and S. Chakraborty, *Modern Receiver Front-Ends: Systems, Circuits, and Integration*. Hoboken, NJ, USA: Wiley, 2004.
[24] E. Frlan, S. Meszaros, M. Cuhaci, and J. S. Wight, "Computer aided design of square spiral transformers and inductors (MIC application)," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jan. 2003, pp. 661–664.
[25] R. Wu, N. Liao, X. Fang, and J. K. O. Sin, "A silicon-embedded transformer for high-efficiency, high-isolation, and low-frequency on-chip power transfer," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 220–223, Jan. 2015.
[26] F. Tounsi, B. Mezghani, L. Rufer, and M. Masmoudi, "Electroacoustic analysis of a controlled damping planar CMOS-MEMS electrodynamic microphone," *Arch. Acoust.*, vol. 40, no. 4, pp. 527–537, Dec. 2015.
[27] P. Arcioni, R. Castello, G. De Astis, E. Sacchi, and F. Svelto, "Measurement and modeling of Si integrated inductors," *IEEE Trans. Instrum. Meas.*, vol. 47, no. 5, pp. 1372–1378, Oct. 1998.
[28] F. Tounsi, M. H. Said, A. B. Kouki, and B. Mezghani, "AC actuation contribution to the induced electromotive force in the miniaturized inductive planar microphone," *Anal. Integr. Circuits Signal Process.*, vol. 90, no. 3, pp. 551–562, Mar. 2017.
[29] H. C. Luong and J. Yin, "Transformer design and characterization in CMOS process," in *Transformer-Based Design Techniques for Oscillators and Frequency Dividers*. Cham, Switzerland: Springer, 2016.
[30] S. S. Mohan, "The design, modeling and optimization of on-chip inductor and transformer circuits," Ph.D. dissertation, Stanford University, Stanford, CA, USA, 1999.
[31] W. Zou, J. Hu, D. Chen, and Y. Zeng, "An equivalent lumped circuit model for on-chip helical transformers," *IEICE Electron. Exp.*, vol. 15, no. 3, 2018, Art. no. 20170818.
[32] J. Aguilera, G. Matias, J. de No, A. Garcia-Alonso, and R. Berenguer, "A comparison among different setups for measuring on-wafer integrated inductors in RF applications," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 3, pp. 487–491, Jun. 2002.
[33] A. Viviani, J. P. Raskin, D. Flandre, J. P. Colinge, and D. Vanhoenacker, "Extended study of crosstalk in SOI-SIMOX substrates," in *Proc. Int. Electron Devices Meeting*, Nov. 2002, pp. 713–716.
[34] F. Tounsi, M. Hadj Said, L. Rufer, B. Mezghani, and M. Masmoudi, "Optimization of induced voltage from CMOS-compatible MEMS electrodynamic microphone with coaxial planar inductances," *IEEE Sensors J.*, vol. 16, no. 18, pp. 6879–6889, Sep. 2016.
[35] T. L. Chow, *Introduction to Electromagnetic Theory: A Modern Perspective*, vol. 4, 1st ed. Boston, MA, USA: Jones & Bartlett, Dec. 2005, pp. 126–170.

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