This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2945040, IEEE Transactions on Nuclear Science

Ultra Low Power Ionizing Dose Sensor Based on Complementary Fully Depleted MOS Transistors for Radiotherapy Application

Fabricio Alcalde Bessia, Denis Flandre, Nicolas André, Julieta Irazoqui, Martín Pérez, Mariano Gómez Berisso, and Jose Lipovetzky

***Abstract*—We evaluate the use of the thick buried oxide (BOX) of Fully Depleted Silicon-on-Insulator (FD-SOI) transistors for Total Ionizing Dose (TID) measurements in a radiotherapy application. The devices were fabricated with a custom process in *Université Catholique de Louvain* (UCL) which allows to make accumulation mode PMOS transistors and inversion mode NMOS transistors. We characterized the temperature behavior of these devices and the response under X-ray radiation produced by an Elekta radiotherapy linear accelerator, and compared the obtained dose sensitivity to other published works. Taking advantage of these devices, an ultra low power MOS ionizing dose sensor, or MOS dosimeter, with inherent temperature compensation is presented. This dosimeter achieved a sensitivity of 154 mV/Gy with a temperature error factor of 13 mGy/°C and a current consumption below 1 nA.**

***Index Terms*—Silicon radiation detectors, Ionizing radiation sensors, Silicon-on-insulator**

I. Introduction

THE radiation-induced Threshold Voltage (V_T) shift of MOS transistors has been used for many years for the measurement of Total Ionizing Dose (TID) [1]. To obtain devices with sensitivities useful for space and radiotherapy applications, the gate oxide thicknesses must be greater than several hundreds of nanometers, which is usually obtained in ad-hoc processes [2], [3]. In the past years, there have been excellent publications about radiation effects in MOS oxides and devices [4], [5], even for Silicon On Insulator (SOI) devices [6]. Several works proposed the use in dosimetry of transistors built using the Buried Oxide (BOX) available in SOI processes, either using the V_T shift in the back-gate transistor [7], [8] or the shift in front gate transistors through body effect [9]. The present work is an extension of [10] and is mainly focused on presenting and evaluating a new circuit that uses FD-SOI devices in an especial arrangement to produce an output voltage proportional to the absorbed dose. The first part of the work deals with the characterization of single transistors against TID and temperature. This part serves as presentation of devices and methods used in this work, and gives an idea of the performance that can be achieved using single devices. In the second part, an ultra low power (ULP) circuit that can be used as an ionizing dose sensor, or dosimeter, is presented along with an initial evaluation of its performance. We finalize the paper with a discussion of the advantages of the ULP dosimeter when compared to single devices and the conclusions of the work.

Manuscript received May 21, 2019. This work has been supported in part by MINCYT, Argentina, and F.N.R.S., Belgium, under collaboration agreement BE1403. It has also been supported in part by ANPCyT under Project PICT 2014-1966 and Project PICT 2015-1644, in part by UNCuyo under Grant C018, and in part by the Micro+ project, co-funded by the European Regional Development Fund (ERDF) and Wallonia, Belgium.

Fabricio Alcalde Bessia, José Lipovetzky, and Mariano Gómez Berisso are with Balseiro Institute, Bariloche R8402AG, Argentina, and also with Consejo Nacional de Investigaciones Científicas y Técnicas, Buenos Aires C1425FQB, Argentina (e-mail: falcalde@ib.edu.ar).

Denis Flandre and Nicolas André are with Université Catholique de Louvain, ICTEAM, Electrical Engineering, Louvain-la-Neuve B-1348, Belgium (e-mail: denis.flandre@uclouvain.be).

Julieta Irazoqui is with Fundación Instituto de Tecnologías Nucleares para la Salud, Bariloche R8402AG, Argentina.

Martín Pérez is with Balseiro Institute, Bariloche R8402AG, Argentina, and also with Comision Nacional de Energia Atomica, Buenos Aires C1429BNP, Argentina.

José Lipovetzky is also with Comision Nacional de Energia Atomica, Buenos Aires C1429BNP, Argentina, and also with International Centre for Theoretical Physics: I, 34151 Trieste, Italy (e-mail: jose.lipovetzky@ieee.org).

II. Devices and Experimental Details

The FD-SOI MOS transistors used in this work, which are depicted in Fig. 1, were fabricated in the *Université Catholique de Louvain* (UCL) clean-room using a heterogeneous fabrication process that was developed in-house [11], [12]. These transistors have a gate oxide thickness of 31 nm, a 80 nm thick layer of silicon and a 400 nm thick buried oxide (BOX) and are built on high-quality industrial-grade SmartCut UNIBOND wafers. The gate is n^+-poly and the channel is doped with Boron only, which leads to accumulation operating mode p-MOSFETs [13], [14] and inversion operating mode n-MOSFETs. The Boron doping is divided in two lithography and implantation steps in a way that it is possible to obtain four different channel dopings at low cost by only masking the desired areas. Blocking or masking both implant steps yields a channel with an intrinsic Boron concentration of approximately $3 \times 10^{14}\,\mathrm{cm}^{-3}$ (I). Blocking either the first step or the second gives approximated channel concentrations of $2 \times 10^{16}\,\mathrm{cm}^{-3}$ and $3 \times 10^{16}\,\mathrm{cm}^{-3}$ (P1 and P2, respectively). And finally allowing both implant steps on the same device gives a higher concentration of $5 \times 10^{16}\,\mathrm{cm}^{-3}$ (P12) which is the combination of both implants P1 and P2. Each implant gives a pair of threshold voltages for n- and p-MOS transistors that leads to quite symmetrical I-V curves.

A test chip was fabricated containing all types of transistors with channel lengths of $20\,\mu\mathrm{m}$ and widths of $20\,\mu\mathrm{m}$. The die was encapsulated in a DIL24 ceramic package with open lid and each transistor was wire-bonded to separated pins.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2945040, IEEE Transactions on Nuclear Science

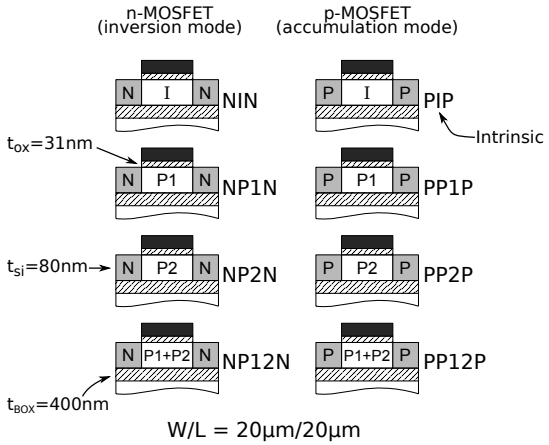

Fig. 1. FD-SOI MOS devices. The fabrication process allows different film dopings using 2 doping masks P1 and P2. Adapted from [11].

These devices were irradiated using an Elekta Synergy Linear Accelerator (LinAc) in a radiotherapy facility. This LinAc uses high energy electrons to produce X-rays with an energy spectrum ranging from 1MeV to 6MeV, and most probable energy is 2MeV. More information about the irradiation field and energy spectrum of this equipment can be found in [15]. The chip was placed inside a water equivalent phantom, in order to simulate a radiotherapy charged particle equilibrium condition, on the central axis of the radiation beam and at the depth of maximum dose. The LinAc field size was set to $10 \times 10\,\mathrm{cm}^2$ and the source-to-surface distance (SSD) was 100 cm. All dose values throughout this work will be given as absorbed dose in water. A conversion to absorbed dose in Silicon is straightforward.

During irradiations, the transistor back-gate, i.e. the backside of the SOI wafer, was biased with different voltages in order to analyze the dependence of hole trapping with bias. It has been reported that the hole trapping in the BOX can be improved this way and so the sensitivity to ionizing dose is improved [4]. The other three terminals (drain, source and gate) of the front transistors were grounded. The irradiation was performed in incremental steps at a dose rate of 4 Gy/min. After each step, the chip was removed from the phantom and the drain currents versus front-gate and back-gate voltages ($\mathrm{I_D(V_G)}$ and $\mathrm{I_D(V_B)}$ curves) were measured. All measurements were taken at room temperature within 10 minutes of the end of the irradiation. I-V curves were measured sweeping the front-gate voltage while $\mathrm{V_B} = 0\,\mathrm{V}$ and sweeping the back-gate voltage while $\mathrm{V_G} = 0\,\mathrm{V}$. In all cases the drain voltage was $+50\,\mathrm{mV}$ and the source was grounded. Figure 2 shows schematically the irradiation and measurement setups. The drain currents were measured with a *Keithley 2450 SourceMeter* unit which, in its lowest current range (10 nA), has an accuracy of $\pm 60\,\mathrm{pA}$ in the worst case.

The temperature dependence of the drain current versus back-gate voltage was analyzed prior to do the experiments. Figure 3 shows the I-V curves of four devices in the same chip measured at 2°C, 10°C, 19°C and 27°C. It can be seen that in the sub-threshold region the drain current increases with temperature following the inverse sub-threshold slope

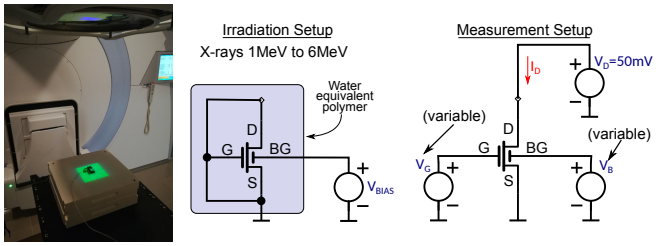

Fig. 2. *Left:* Test chip placed in the radiotherapy facility. It was later covered with 13cm of water-equivalent polymer. *Right:* Irradiation and measurement setups. For every measurement the drain voltage was always 50 mV, whereas $\mathrm{V_G}$ was swept with $\mathrm{V_B}$ fixed at 0 V in order to measure the front-gate characteristic curve, and $\mathrm{V_B}$ was swept with $\mathrm{V_G}$ fixed at 0 V to obtain the back-gate transistor characteristic curve.

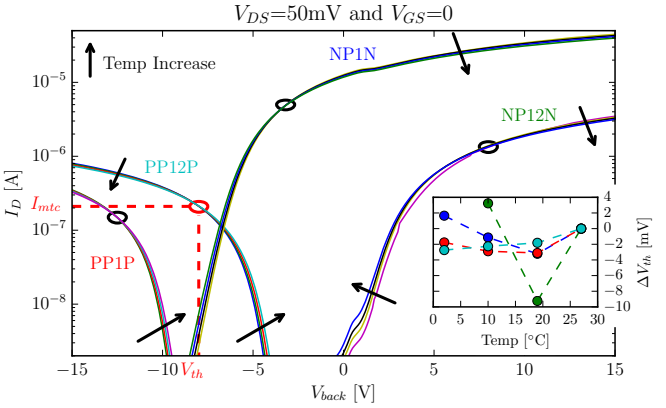

Fig. 3. Drain current versus back-gate voltage of four devices on the same die for 2, 10, 19 and 27°C. The $\mathrm{I_{mtc}}$-$\mathrm{V_{th}}$ points were marked with circles. The inset shows ΔV_{th} with respect to 27°C. Using this method, the error introduced by temperature in the extraction of V_{th} is less than $\pm 10\,\mathrm{mV}$ (for the given temperature range).

usual dependence [16], whereas in inversion/accumulation it decreases with temperature following the usual mobility dependence. In between those regions there is an $\mathrm{I_{mtc}}$ current that is almost independent of temperature (*mtc* stands for "minimum temperature coefficient"). Usually, MOS dosimeters are biased with this current and the voltage variation is taken as a measure of absorbed dose, independently of temperature. This method was used successfully before in [17] and [18].

In this work the effective threshold voltage $\mathrm{V_{th}}$ of the devices was defined as the voltage for which the current is $\mathrm{I_{mtc}}$, and this current was obtained prior irradiation. The inset of figure 3 shows the change in the threshold voltage due to temperature when the devices are biased with the $\mathrm{I_{mtc}}$ current and it can be seen that the voltage variation is less than $\pm 10\,\mathrm{mV}$ in the measured temperature range. It is worth noticing that the $\mathrm{I_{mtc}}$ point must be found for each device independently.

III. Evaluation of Single Transistors as Dosimeters

Single devices were tested with the aim of using them as radiation dosimeters for radiotherapy applications. Hence, the dependence of the threshold voltage with absorbed dose was evaluated using the radiotherapy LinAc mentioned above.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2945040, IEEE Transactions on Nuclear Science

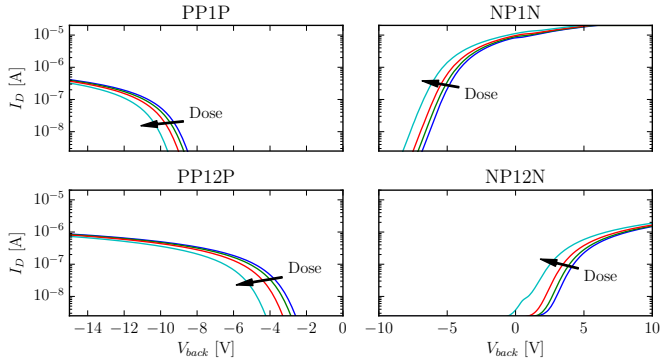

Fig. 4. Drain current versus back-gate voltage with source and front-gate grounded, and 50 mV applied to the drain. Accumulated doses are 0, 10, 30 and 80 Gy.

Before the beginning of the experiment the initial I-V curves were measured. Then, a single chip containing the devices was introduced in the water equivalent polymer where it received a dose step of 5 Gy in approximately 1 minute. Next, the chip was taken to the measurement setup where the actual measurement of the devices began three minutes after the end of the irradiation and took place in around ten minutes. This process was repeated for the next 5, 10, 10, 25 and 25 Gy steps, which accounted for a total accumulated dose of 80 Gy. These irradiation steps were performed with all terminals grounded.

Figure 4 shows the I-V curves of the devices, where some dose steps were skipped for clarity. The curves show a monotonic change in the threshold voltage with accumulated dose due to buildup of charge in the BOX. Also, there is no significant change in the sub-threshold slope during the irradiation, which is an indication that the interface traps do not play a significant role on the V_{th} shift of these transistors.

A. Threshold voltage shift under 0V bias

Fig. 5 shows the V_{th} shift as a function of accumulated dose and its recovery after the experiment due to annealing. This figure corresponds to the same chip of figure 4 that was irradiated under 0 V bias, i.e. with all terminals grounded. The effective threshold voltages of interest for this work were extracted from the I_{mtc} point of the I-V curves.

The sensitivity of the back-gate transistors (BGT)—transistors formed by the back-substrate, the BOX and the Si film—is higher than that of the front-gate transistors (FGT). This is expected and can be explained by the Lim-Fossum model of inversion-mode FD-SOI transistors [19] and by the Flandre-Terao model for accumulation-mode transistors [14], by introducing a fixed charge in the BOX, although some front-gate oxide charge is also needed to account for the total shift. Therefore FGT are less sensitive to radiation resulting in a variation of the threshold voltage of front-gate transistors ΔV_{tf} being around 10% of that of back-gate transistors ΔV_{tb} and this is related to the ratio of gate oxide and buried oxide thicknesses.

Also, devices with a higher channel doping seem to be more sensitive to radiation, as seen in Fig. 5 where ΔV_{th} for P12 doping profile is higher than for P1. This could be explained

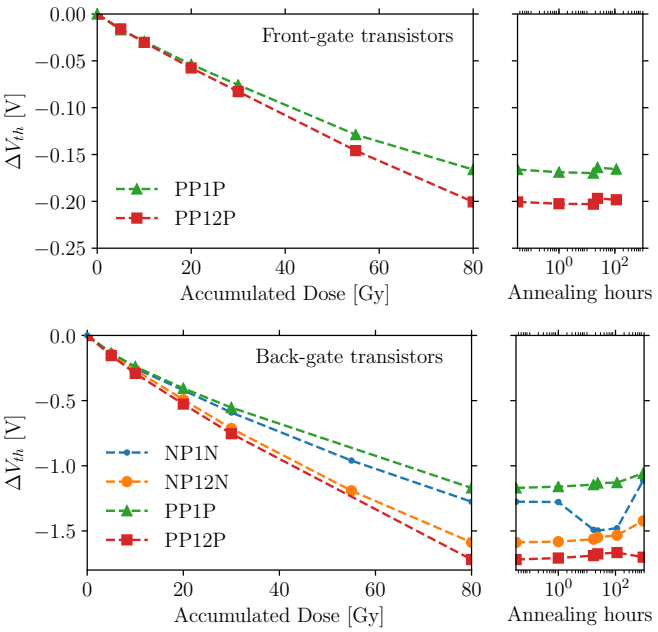

Fig. 5. Variation of the threshold voltage versus accumulated dose for successive irradiations with 0 V back-gate bias, followed by an annealing period. The dose steps were: 5, 5, 10, 10, 25 and 25 Gy.

as a stronger electric field in the BOX, which increases the trapping yield [4]. Also devices with higher doping have a more linear response with dose.

The annealing was performed at room temperature, between 18°C and 24°C, and with all terminals grounded. The devices presented a 10 to 12% reduction in ΔV_{tb} after one month.

B. Threshold voltage shift for different bias conditions

Another chip was irradiated in the radiotherapy facility and the procedure was analogous to what was described previously. The only difference was that this time the back-gate was biased to increasing voltages, from 0 to 20 V, during each irradiation step, while the rest of the terminals were grounded. In all steps the dose was 5 Gy. The first irradiation step was performed with a back-gate bias of 0 V. The second step with 3 V. The third with 6 V and so on with 12 V and 20 V applied to the back-gate. In between steps the I-V curves of the devices were measured as was described before.

Fig. 6 shows V_{th} shift of the front and back-gate transistors and their annealing. The first thing to notice in is that the sensitivity is lower for 3 V bias. This effect could be due to a lower electric field (lower trapping yield) in the BOX, and this in turn due to depletion of the third interface as in Martino's potential drop model [20].

For bias voltages higher than 3 V the sensitivity is higher but it remains almost constant with bias. Although a higher electric field imply a higher charge yield—i.e. the fraction of holes that escape initial recombination—it also implies a reduction in the hole trapping cross section near interface, as was reported in [21]. Therefore, there is a saturation for electric fields in the range 0.2 MV.cm^{-1} to 1 MV.cm^{-1}.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2945040, IEEE Transactions on Nuclear Science

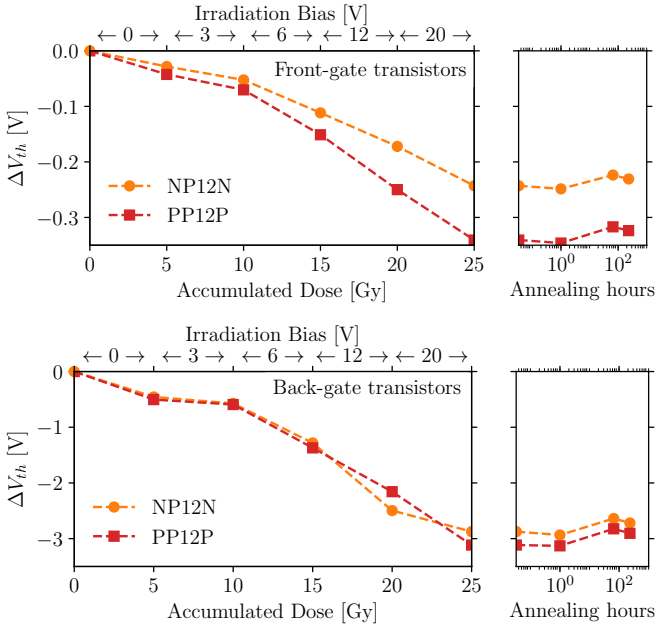

Fig. 6. Variation of the threshold voltage versus accumulated dose for successive 5 Gy irradiations, each one with an applied back-gate bias voltage shown by the top arrows, followed by an annealing period. The maximum obtained sensitivity is 191mV Gy^{-1} for BGT PP12P with 20 V bias.

Finally, the annealing was performed in the same conditions as before, obtaining a recovery of the threshold voltage below 15% after 120 hours.

IV. Ultra Low Power MOS Dosimeter

In this section we present a Ultra Low Power (ULP) dosimeter using FD-SOI devices which is based on the ULP voltage reference published in [22]. This dosimeter uses two transistors connected as seen in figure 7. The drains of the N and P MOSFETs are connected to V_{DD} and V_{SS} respectively, while their sources are short-circuited with their gates and connected together to form the output node V_O. Using V_{SS} as reference voltage, V_{DD} must be biased positive at a voltage greater than the equilibrium voltage of V_O, which depends on the back-gate voltage V_B. As both transistors are fabricated on the same handling wafer, the back-gate is the same for both devices. Figure 7 also shows in a single plot the I_D-V_{SB} curves of NP1N and PP1P devices before and after 10 Gy. It is worth noticing that in the case of V_S equal to 0 V the x-axis is the same as in figure 4 but reversed.

Since the devices are in series in the ULP dosimeter, the same amount of current must flow through both channels. Also both devices have their front-gates connected to their sources, making $V_{gs}^N = V_{gs}^P = 0$ V. To satisfy these 2 conditions, the voltage V_O must settle at the intercept point of the I_D-V_{SB} curves of the N and P transistors, shown with red circles in the plot of figure 7, i.e. around 5 V with $V_B = 0$ before irradiation. The drain current at this point is below 0.1 nA, and hence the power dissipation is less than 1 nW.

When the devices are exposed to ionizing radiation, the I-V curves that were shifted to the left on the plots of figure 4 now are shifted to the right in figure 7 (due to the change of reference from source to back-gate), increasing the output voltage of the ULP dosimeter. According to Levacq's equations [23] and since the subthreshold slope shift with dose is negligible, V_O will be increased by the same magnitude as the V_{th} shift, making the output voltage proportional to the absorbed radiation dose. Also, since both devices can be placed next to each other, with the exact same size and an almost equal doping profile, the threshold voltage shift with dose will match very well. This means that, in principle, the curves of N and P transistors of figure 7 will shift by the same amount and the current at the crossing point of N and P will not change. However, the plot shows a slight increase in the current that can be attributed to the small difference in the threshold voltage shift of N and P MOSFETs, as was seen in figure 5.

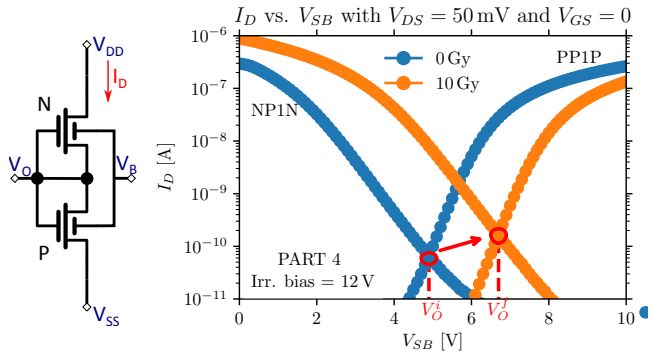

Fig. 7. Left: Proposed ultra low power dosimeter. Right: Drain current vs. source-backgate voltage of NP1N and PP1P transistors. For $V_B = 0$ V, the voltage at crossing point of the NMOS and PMOS curves is the output voltage of the ULP dosimeter.

The circuit is also stabilized against temperature. As shown in [22], an increase in temperature will increase the current consumption exponentially due to the increase in thermally generated carriers in the sub-threshold region. But again, since both devices are equally doped, the increase will be almost equal for both and ideally there won't be any voltage shift of the equilibrium point, mitigating temperature-induced output voltage variations.

A. Experimental verification of the ULP MOS dosimeter

The sensor built with a pair of N and P transistors on the same die was irradiated using the same irradiation setup as in figure 2. After irradiation the devices were connected as in the ULP dosimeter circuit of figure 7 and the output voltage and current consumption were measured. For this experiment, devices with the highest doping profiles were used (NP12N and PP12P), as they have shown the best sensitivity in section III.

The experiment was carried out in two different campaigns: On the first one, the chip was irradiated under 0 V bias and the ULP dosimeter measurements were done with $V_B = 0$ V. The ionizing dose was delivered in 5 Gy steps up to 25 Gy. The procedure was the same as explained in section III: after each irradiation step, the chip was taken to the measurement setup and the output voltage was read approximately 2 minutes after exposition.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2945040, IEEE Transactions on Nuclear Science

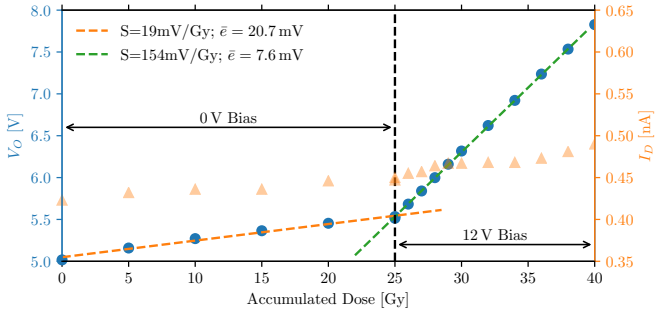

Fig. 8. Experimental results of the ULP dosimeter: equilibrium voltage V_O and bias current I_D measured at $V_{DD} = 8\,V$, $V_B = 0\,V$ and $V_{SS} = 0\,V$. The devices were irradiated in two different campaigns under back-gate bias equal to 0 V and 12 V, using the same irradiation setup as in figure 2. In between campaigns there was an annealing period of 20 days in which a recovery of 0.5% was measured.

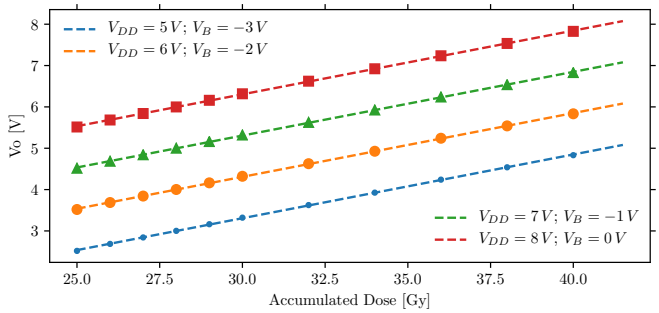

Fig. 9. Measurements during the second campaign for different back-gate voltages and maintaining a voltage difference of 8 V between V_{DD} and V_B. The sensitivity is equal to 154 mV/Gy in all cases.

On the second campaign the same chip was used and the procedure was similar, but this time the irradiation was performed with 12 V applied to the back-gate and the output voltage was measured for different back-gate voltages V_B. In between campaigns the devices were kept at room temperature with all terminals grounded. A slight recovery was observed, but it was below 0.5% of V_O nominal value.

Figure 8 shows the results of both campaigns, where data points were fitted with a linear regression using the least squares method. The deviation of the data points with respect to the linear fit is given by the $\bar{e}$ parameter, which was calculated as the mean absolute error. The plot shows that the circuit behave as expected, i.e. increases the output voltage with absorbed dose, and also that applying a bias voltage during irradiation increases the sensitivity in the same way as in the previous section. Linearity was much better for the irradiation under 12 V bias than for 0 V bias, as shown by the mean errors $\bar{e}$. Finally, there is a slight increase in the current consumption that can be attributed to the difference in threshold voltage shifts of N and P devices.

Figure 9 shows measurements of the second campaign for different back-gate voltages. The only effect of changing V_B is shifting the output voltage by the same amount, but V_{DD} must be changed accordingly to keep the 2 MOSFETs in saturation.

The temperature dependence of the output voltage was measured prior to irradiation and is shown in figure 10. It

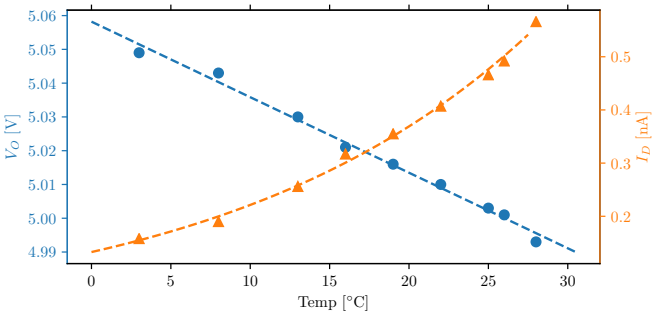

Fig. 10. Temperature characterization of the ULP dosimeter. V_O varies linearly with slope equal to -2 mV/°C, while I_D increases exponentially with temperature.

can be seen that the output voltage decreases 2 mV per degree Celsius, while the current consumption increases exponentially as expected.

The *temperature error factor* (TEF) is defined as the ratio between the sensitivity to dose and the sensitivity to temperature, and it gives the error in dose measurement per unit of temperature change [24]. For a sensitivity of 154 mV/Gy (figure 9), the TEF of the ULP dosimeter is 13 mGy/°C.

V. Discussion

In sections III-B and IV-A a bias voltage was applied to the back-gate, so it is worth mentioning that no back-gate bias instabilities were observed before or after irradiation for the electric fields (up to 0.5 MV.cm^{-1}) and stressing times (up to 300 seconds) used in this work. Such effect has been reported to happen at high temperatures [25] or for substrates that received a special treatment, like annealing in a forming gas atmosphere [26], or Silicon implantation [27], while we use here the highest-quality recent SOI wafers.

Although the primary application here is external beam radiotherapy, it is worth mentioning what to expect when irradiating single devices or the ULP dosimeter with other dose rates and other energies. With respect to dose rate, it has been shown that generally the response of MOS oxides to radiation can show "apparent" dose rate effects, but is commonly accepted that there are no true effects [4], [5], even for dose rates orders of magnitude different. This mean that for lower or higher dose rates than the one used in this work, the measured ΔV_{th} immediately after irradiation will be different, but if the time elapsed between the beginning of the irradiation and the ΔV_{th} measurement is the same, then the final ΔV_{th} will be equal no matter the dose rate used, at least to the first order. Therefore, in the specific case of radiotherapy with Megavoltage LinAcs, in which the average dose rate does not change significantly—it is fixed around 1 Gy.min^{-1} for radiobiological reasons [28]—, the response of the devices will be quite the same for different dose rates.

Also, it has been shown [29], [30] that by using the linear systems theory and carefully modeling the impulse response of devices to a short radiation pulse, it is generally possible to predict the response of devices to different dose rates—except when the response is non-linear with dose. Since a

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2945040, IEEE Transactions on Nuclear Science

Megavoltage LinAc delivers the dose as a train of high dose rate and short width radiation pulses ($\approx 2\,\mu$s), which are milliseconds apart, the application of this theory is viable, in principle.

For photon energies different than the ones used in this work, the studies of MOS oxides ([4], [5]) have shown that the only difference is the fractional yield, i.e. the fraction of initial charge that escapes recombination. For higher energy photons the fractional yield will be higher and for lower energy photons the fractional yield will be lower. The initial recombination might have other behavior when using other particles than photons. For example, highly ionizing particles tend to produce lower fractional yields. Therefore, the response of single devices and the response of the ULP dosimeter will change accordingly. The limit to this behavior is generally for photon energies below 100 keV, when the interaction of radiation with the package material starts to modify the dosimeter response [31]. But this limit energy is much lower than range generally used with Megavoltage Linacs.

In the following sub-sections a comparison between single devices and other MOS dosimeters and single devices vs. the ULP dosimeter is presented. The sensitivity to ionizing radiation dose is compared and also the temperature error factor.

A. Single devices vs. other MOS dosimeters

The 400 nm thick BOX used in this work exhibits a sensitivity of 165 mV/Gy under 12.4 V bias. This sensitivity is higher than other similar devices used in dosimetry. For instance, the sensitivity of the 400 nm thick Field Oxide transistors presented in [32], was 40 mV/Gy under the same 12 V gate bias. In [3] it was reported that 400 nm thick Tyndall dosimeters had approximately 100 mV/Gy under 5V gate bias. RFT 300 REM Oxford dosimeters [2] with 300 nm thick gate oxide had a sensitivity of 125 mV/Gy under 9 V gate bias—the same gate oxide field. Compared to other FD-SOI works which use BOX for dosimetry, [7] reported a sensitivity of 15 mV/Gy with 5 V gate bias on a 150 nm thick BOX; [9] 12.5 mV/Gy on a 200 nm thick BOX manufactured by SOITEC, under zero volts bias; and Ref. [8] 1 mV/Gy with 145 nm BOX layer.

The higher sensitivity observed in the devices of this work is not only caused by the thicker oxides, but also because a high hole capture probability. Assuming an electric field of $\simeq 0.3$ MV/cm with a generation yield $\simeq 30\%$ [4], and that the charge is captured very close to the Si-SiO_2 interface, the fraction of charge which remains trapped in the oxide is roughly a 95% of the available holes. This high trapping probability is consistent with the fact that BOX have a high oxygen vacancy defect concentration due to high temperature anneals during fabrication [9].

Another important parameter for a dosimeter is the fading due to neutralization of trapped charges. For the FD-SOI devices in [9] the authors observed a recuperation of less than 10% in the threshold voltage shift for their BOX RadFETs during a period of 700 hours; on the other hand, in [8] the retention of the charge lasted up to 90 days without considerable fading. The devices of the present work showed a fading of charge, or recovery of the threshold voltage, of around 10% in a period of 100 hours after irradiation. Since radiation response is related to the processing and history of the oxide in particular [5], there is no significant difference between the three works, at least for the periods of time analyzed.

B. Single devices vs. the ULP dosimeter circuit

The sensitivity obtained with single devices and the ULP dosimeter is roughly the same ($\approx 160\,\mathrm{mV/Gy}$ at 12 V bias) and this is expected because the ULP dosimeter is an arrangement of two single devices with the same dimensions, doping profiles and oxide thicknesses. In principle, charge trapping in the BOX produces a shift in the threshold voltages that has the same magnitude and sign in both devices. This $\mathrm{V_{th}}$ shift is also affected by the interface charge density which adds to the oxide charge induced shift, but with different sign for N and P MOSFETs. During the characterization of single devices it has not been seen that the interface charge played a significant role in the back-gate transistors, especially when irradiated with a high back-gate bias voltage. If there was such an effect, then the difference introduced in the shift of the I-V curves of N and P devices would be reflected in a strong increase of the current consumption of the ULP dosimeter with accumulated dose.

Regarding temperature, the ULP dosimeter has an intrinsic temperature shift rejection, which depends on the device mismatch mostly. On the other hand, it has been proven that the $\mathrm{V_{th}}$ extraction using the $\mathrm{I_{mtc}}$ current is dose dependent [33] and so the main source of inaccuracy when using single MOS devices as dosimeters. The temperature error factor obtained with the ULP dosimeter in this work ($13\,\mathrm{mGy/^\circ C}$) is lower than the one reported in [33] ($20\,\mathrm{mGy/^\circ C}$) by using only the $\mathrm{I_{mtc}}$ method, but is higher than the one reported in the same work using a reduced temperature range ($6\,\mathrm{mGy/^\circ C}$), and also higher than the TEF obtained with differential circuits in [24] ($0.7\,\mathrm{mGy/^\circ C}$), and [34] ($5.9\,\mathrm{mGy/^\circ C}$).

The mismatch between devices plays an important role in the sensitivity and power consumption of the ULP dosimeter. So, it is important to note that in this work the N and P devices were laid out on the same substrate, but separated from each other. Therefore the mismatch could be reduced by using layout matching techniques such as common centroid and the addition of dummy devices. It is also possible to adapt the W/L ratio of transistors in order to reduce the temperature sensitivity of the output voltage as demonstrated in [35].

Finally, the ULP dosimeter circuit requires no power during irradiation and its power consumption is below 0.1 nW during readout. For example, a typical RadFET [2] or FoxFET [32] is read out with currents in the order of hundreds of micro-amperes and voltages from 1 to tens of volts, consuming power in the μW range on the best case. Another CMOS-based ultra low power dosimeter described in [36] has a power consumption of 1 μW, at least three orders of magnitude more than the ULP circuit presented here.

VI. Conclusions

A characterization of the FD-SOI MOS transistors fabricated with the process developed at UCL has been presented. It has been shown that these devices are suitable for MOS dosimetry due to their 400 nm thick buried oxide and their high sensitivity to dose, up to 191 mV/Gy under a back-gate bias of 20 V. It has also been shown that the sensitivity to ionizing radiation can be improved by applying a bias voltage to the back-gate of the devices during irradiation and by using the devices with the highest doping profiles.

Moreover, the high sensitivity to dose of the BOX and low threshold voltage shift of the front-gate transistors can be used for the development of a dosimeter with integrated read-out electronics on the top side of the chip.

In this last direction we presented an ULP dosimeter made of only one n-MOSFET and one p-MOSFET working in subthreshold regime and with intrinsic temperature compensation. This is a small circuit that can be connected to amplifiers or signal conditioning circuits directly fabricated on the same thin silicon film. The ULP dosimeter has the same sensitivity as single devices but it has the advantage of a reduced temperature error factor ($13\,\mathrm{mGy}/^{\circ}\mathrm{C}$ @ 12 V bias), which could be reduced even more with a careful design of the sensor, i.e. using layout matching techniques and adjusting the W/L ratio of N and P devices.

References

[1] A. B. Rosenfeld, "Electronic dosimetry in radiation therapy," *Radiation Measurements*, vol. 41, pp. S134 – S153, 2006, the 2nd Summer School on Solid State Dosimetry: Concepts and Trends in Medical Dosimetry. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1350448707000091

[2] L. Fröhlich, S. Grulja, and F. Löhl, "DOSFET-L02, an advanced online dosimetry system for RADFET sensors," *Proc. IBIC*, vol. 13, pp. 481–484, 2013.

[3] M. M. Pejović, M. M. Pejović, A. B. Jaksić, K. Stanković, and S. A. Marković, "Successive gamma-ray irradiation and corresponding post-irradiation annealing of pMOS dosimeters," *Nuclear Technology and Radiation Protection*, vol. 27, no. 4, pp. 341–345, 2012.

[4] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 483–499, June 2003.

[5] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in MOS oxides," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, Aug 2008.

[6] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation effects in SOI technologies," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 522–538, June 2003.

[7] Y. Li, W. M. Porter, C. Kshirsagar, I. Roth, Y. Su, M. A. Reynolds, B. J. Gerbi, and S. J. Koester, "Fully-depleted silicon-on-insulator devices for radiation dosimetry in cancer therapy," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3443–3450, 2014.

[8] J.-B. Yau, M. S. Gordon, K. P. Rodbell, S. J. Koester, P. W. DeHaven, D.-G. Park, and W. E. Haensch, "FDSOI radiation dosimeters," in *VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on*. IEEE, 2011, pp. 1–2.

[9] M. R. Shaneyfelt, T. A. Hill, T. M. Gurrieri, J. R. Schwank, R. S. Flores, P. E. Dodd, S. M. Dalton, and A. Robinson, "An embeddable SOI radiation sensor," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3372–3380, 2009.

[10] F. Alcalde Bessia, D. Flandre, N. André, J. Irazoqui, M. Pérez, M. Gómez Berisso, and J. Lipovetzky, "Fully-Depleted SOI MOSFET sensors in accumulation mode for total dose measurement," in *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. In Press, 2018.

[11] D. Flandre, S. Adriaensen, A. Afzalian, J. Laconte, D. Levacq, C. Renaux, L. Vancaillie, J. P. Raskin, L. Demeus, P. Delatte, V. Dessard, and G. Picun, "Intelligent SOI CMOS integrated circuits and sensors for heterogeneous environments and applications," in *Proceedings of IEEE Sensors*, vol. 2, 2002, pp. 1407–1412 vol.2.

[12] D. Flandre, S. Adriaensen, A. Akheyar, A. Crahay, L. Demeûs, P. Delatte, V. Dessard, B. Iniguez, A. Nève, B. Katschmarskyj, P. Loumaye, J. Laconte, I. Martinez, G. Picun, E. Rauly, C. Renaux, D. Spôte, M. Zitout, M. Dehan, B. Parvais, P. Simon, D. Vanhoenacker, and J.-P. Raskin, "Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems," *Solid-State Electronics*, vol. 45, no. 4, pp. 541 – 549, 2001. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110101000843

[13] D. Flandre, "Problems in designing thin-film accumulation-mode p-channel SOI MOSFETs for CMOS digital circuit environment," *Electronics Letters*, vol. 27, no. 14, pp. 1280–1282, July 1991.

[14] D. Flandre and A. Terao, "Extended theoretical analysis of the steady-state linear behaviour of accumulation-mode, long-channel p-MOSFETs on SOI substrates," *Solid-State Electronics*, vol. 35, no. 8, pp. 1085 – 1092, 1992. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110192900092

[15] M. Fippel, F. Haryanto, O. Dohm, F. Nüsslin, and S. Kriesen, "A virtual photon energy fluence model for monte carlo dose calculation," *Medical Physics*, vol. 30, no. 3, pp. 301–311, 2003.

[16] J.-P. Colinge, D. Flandre, and F. Van de Wiele, "Subthreshold slope of long-channel, accumulation-mode p-channel SOI MOSFETs," *Solid-State Electronics*, vol. 37, no. 2, pp. 289 – 294, 1994. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110194900809

[17] S. H. Carbonetto, M. A. Garcia Inza, J. Lipovetzky, E. G. Redin, L. Sambuco Salomone, and A. Faigon, "Zero temperature coefficient bias in MOS devices. dependence on interface traps density, application to MOS dosimetry," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 3348–3353, Dec 2011.

[18] G. Sarrabayrouse and S. Siskos, "Temperature effects and accuracy of MOS radiation dosimeters," in *WSEAS International Conference. Proceedings. Mathematics and Computers in Science and Engineering*, no. 7. World Scientific and Engineering Academy and Society, 2008.

[19] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Transactions on Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct 1983.

[20] J. A. Martino, L. Lauwers, J. P. Colinge, and K. D. Meyer, "Model for the potential drop in the silicon substrate for thin-film SOI MOSFETs," *Electronics Letters*, vol. 26, no. 18, pp. 1462–1464, Aug 1990.

[21] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge yield for cobalt-60 and 10-keV X-ray irradiations of MOS devices," *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1187–1194, Dec 1991.

[22] S. Adriaensen, V. Dessard, and D. Flandre, "25 to 300°C ultra-low-power voltage reference compatible with standard SOI CMOS process," *Electronics Letters*, vol. 38, no. 19, pp. 1103–1104, Sep. 2002.

[23] D. Levacq, C. Liber, V. Dessard, and D. Flandre, "Composite ULP diode fabrication, modelling and applications in multi-Vth FD SOI CMOS technology," *Solid-State Electronics*, vol. 48, no. 6, pp. 1017 – 1025, 2004, silicon On Insulator Technology and Devices. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110103004404

[24] M. Garcia-Inza, S. H. Carbonetto, J. Lipovetzky, and A. Faigon, "Radiation sensor based on MOSFETs mismatch amplification for radiotherapy applications," *IEEE Transactions on Nuclear Science*, vol. 63, no. 3, pp. 1784–1789, June 2016.

[25] A. Nazarov, "Hydrogen and high-temperature charge instability of SOI structures and MOSFETs," in *Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment*, D. Flandre, A. N. Nazarov, and P. L. Hemment, Eds. Dordrecht: Springer Netherlands, 2005, pp. 121–132.

[26] K. Vanheusden, J. Schwank, W. Warren, D. Fleetwood, and R. Devine, "Radiation-induced H+ trapping in buried SiO_2," *Microelectronic Engineering*, vol. 36, no. 1, pp. 241 – 244, 1997, proceedings of the biennial conference on Insulating Films on Semiconductors. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931797000567

[27] H. D. Xiong, B. Jun, D. M. Fleetwood, R. D. Schrimpf, and J. R. Schwank, "Charge trapping and low frequency noise in SOI buried oxides," *IEEE Transactions on Nuclear Science*, vol. 51, no. 6, pp. 3238–3242, Dec 2004.

[28] N. Suntharalingam, E. B. Podgorsak, and J. H. Hendry, "Ch.14 - Basic radiobiology," in *Radiation Oncology Physics*. Vienna: International Atomic Energy Agency, 2005, pp. 485–504. [Online]. Available: https://www.iaea.org/publications/7086/radiation-oncology-physics

[29] F. B. McLean, "Generic impulse response function for MOS systems and its application to linear response analysis," *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, pp. 1178–1185, Dec 1988.

[30] T. R. Oldham, "Analysis of damage in MOS devices for several radiation environments," *IEEE Transactions on Nuclear Science*, vol. 31, no. 6, pp. 1236–1241, Dec 1984.

[31] G. J. Brucker, S. Kronenberg, and F. Gentner, "Effects of package geometry, materials, and die design on energy dependence of pMOS dosimeters," *IEEE Transactions on Nuclear Science*, vol. 42, no. 1, pp. 33–40, Feb 1995.

[32] J. Lipovetzky, M. A. Garcia-Inza, S. Carbonetto, M. J. Carra, E. Redin, L. S. Salomone, and A. Faigon, "Field oxide n-channel MOS dosimeters fabricated in CMOS processes," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4683–4691, 2013.

[33] G. Sarrabayrouse and S. Siskos, "Behaviour of high sensitivity MOS radiation dosimeters biased in the MTC current region," *Proceedings of the 9th WSEAS International Conference on Instrumentation, Measurement, Circuits and Systems, IMCAS '10*, pp. 38–41, 01 2010.

[34] M. Garcia-Inza, S. Carbonetto, J. Lipovetzky, M. J. Carra, L. S. Salomone, E. G. Redin, and A. Faigon, "Switched bias differential MOSFET dosimeter," *IEEE Transactions on Nuclear Science*, vol. 61, no. 3, pp. 1407–1413, June 2014.

[35] S. Adriaensen, V. Dessard, and D. Flandre, "A voltage reference compatible with standard SOI CMOS processes and consuming 1 pA to 50 nA from room temperature up to 300°C," in *2002 IEEE International SOI Conference*, Oct 2002, pp. 130–131.

[36] M. Arsalan, A. Shamim, M. Shams, N. G. Tarr, and L. Roy, "Ultra low power CMOS-based sensor for on-body radiation dose measurements," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1, pp. 34–41, March 2012.