Silicon-substrate enhancement technique enabling high quality integrated RF passives

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***Abstract*—A novel method for increasing effective resistivity in low doped silicon substrates is presented. By creating a chain series of PN depletion junctions beneath the insulator, the parasitic surface conduction channel is interrupted, significantly lowering substrate losses, increasing substrate isolation and improving linearity. We demonstrate the integration of high quality CPW transmission lines and spiral inductors on depletion-enhanced silicon achieving performances close to the widely used trap-rich substrate at RF frequencies.**

***Keywords*—RF CMOS, substrate losses, crosstalk, effective resistivity, oxide charges, substrate linearity, inductor quality factor.**

I. Introduction

Nowadays advanced silicon CMOS are offering competitive radio-frequency (RF) characteristics towards applications for wireless communication circuits in 2G, 3G, 4G and the upcoming 5G generations of cellular networks [1]. In this RF Integrated circuits (ICs) electrical signals propagate in a conductive metal layer atop an insulator-semiconductor stack. A coplanar waveguide (CPW) is depicted in Fig. 1a atop such a stack of materials. To avoid losses in such lines, and also to mitigate coupling between them, it is important for the underlying substrate to have a high effective resistivity. Furthermore, it is required that the substrate be as linear as possible to minimize distortion of the line signals. For these reasons the standard-doped (~10 Ωcm) silicon substrate (widespread among digital applications) is unsuited to wireless systems, RF devices and power circuits due to its high conductivity, high RF losses and low linearity. Low-doped silicon is then favoured with high nominal resistivity (ρ_{nom}) above 1 kΩcm. However, the effective resistivity (ρ_{eff}), which is sensed by the overlying planar circuits, can differ strongly from the nominal resistivity ρ_{nom} due to band bending effects at the semiconductor/insulator interface that severely reduce the local resistivity, impacting greatly on the overall sensed ρ_{eff}. The resistivity of semiconductors is by nature dependent on the local electric field (field-effect). Low-doped high-resistivity (HR) substrates are particularly field-sensitive, and it is typical for the semiconductor volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer. The most common parasitic fields originate from fixed charges (usually positive in Si/SiO_2 heterostructures) present at the insulator/semiconductor interface. Then, a highly conductive channel-like layer is induced beneath the insulator, as depicted in Fig. 1a. These charges (represented "+" symbols in Fig. 1), are inevitable in the IC fabrication process, and induce free electrons at the interface in very high concentrations, locally lowering the resistivity beneath the circuits by a factor of 10^3 to 10^6. This in turn lowers the sensed effective resistivity by a factor of 10 to 10^4, to values as low as 1 Ωcm. This is referred to as the parasitic surface conduction (PSC) effect that renders the use of a HR substrate ineffective for improving the performance of overlying ICs as compared to standard-doped silicon (ρ_{nom} ~10 Ωcm) [2]. A breakthrough on this matter was made in 2002 with the introduction of a thin polysilicon layer rich in defects (traps) beneath the buried oxide (BOX) in silicon-on-insulator (SOI) technology [3]. This layer effectively mitigates the PSC effect by pinning the Fermi-level near mid-gap at the interface in a highly resistive state, enabling ρ_{eff} of over 1 kΩcm. Integrating multiple functionalities (RF alongside digital) on a single chip is a main driving force behind the progress of ICs, and today the trap-rich (TR) SOI substrates are used in front-end modules of virtually all modern-day smartphones for the implementation of the RF switch banks. However, integration issues exist between advanced FDSOI nodes and TR substrates due to the difficulty of defining back-gate contacts below the BOX within the poly-Si trapping layer. In this paper we present a novel method for combatting the PSC effect that relies on locally interrupting the PSC channel by inducing a chain series of buried depletion junctions at the Si/SiO2 interface. In particular, we demonstrate significantly reduced RF substrate losses and highly improved quality factor of CPW lines and integrated RF inductors. Enabling RF performances close to those of TR wafers, this method is compatible with bulk, SOI and FDSOI technology.

II. Characterization and Modelling of Depletion-Enhanced Silicon

A. Concept: Buried PN Depletion Junctions

Depletion junctions induced between adjacent P and N implant zones serve to impede the electric field in unwanted directions. This technique enables the interruption of the conductive PSC path is interrupted in the direction perpendicular to the buried junctions, resulting in an increase of the effective substrate resistivity ρ_{eff} sensed by the planar circuits. Furthermore, these implanted P and N regions are much less field-sensitive thanks to the strong dopant concentrations, which leads to an increase in the substrate's linearity. The resistivity profile in such depletion-enhanced (DP) high-resistivity substrates is shown in Fig. 1b. Such profiles were simulated using the process flow TCAD software Athena from Silvaco. Although the resistivity in the P and N regions themselves is low, they come in series with the depleted junctions characterized by very low free carrier density and are therefore highly resistive. This is highlighted in Fig. 3 which

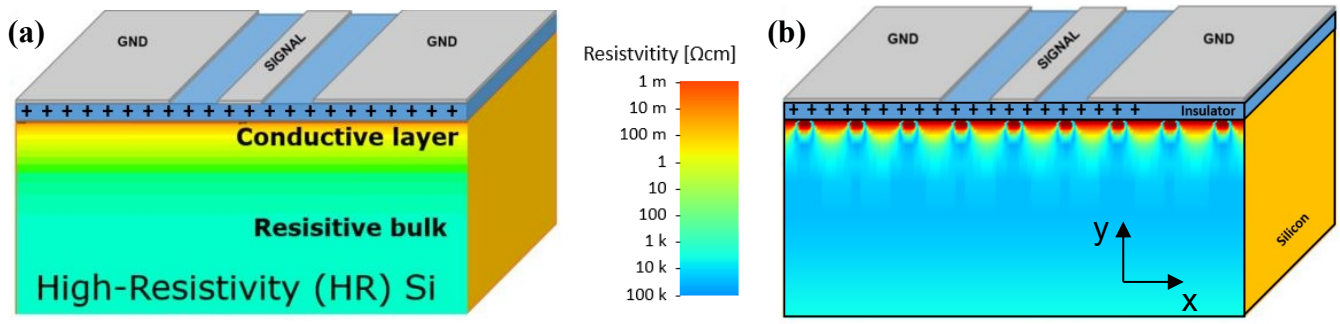

Fig. 1. Representation of the 2D resistivity profile in a HR substrate suffering from PSC (a) and in a DP substrate enhanced with buried PN depletion junctions (b), viewed normal to the PN junctions.

presents the carrier concentrations and local resistivity as a function of the horizontal direction directly beneath the BOX.

B. Small-Signal RF Substrate Performance

RF measurements of CPW lines were performed on-wafer using a PNA-X vector network analyzer and a pair of GSG Infinity Probes. From the measured S-parameters we extract the effective resistivity ρ_{eff}, effective relative permittivity $\varepsilon_{r,eff}$ and RF line losses α over a wide frequency range using the method described in [4]. The dimensions of the CPW lines are a signal line width of 26 µm, a spacing of 12 µm and ground line widths of 155 µm. The metallic passives are isolated from the semiconductor regions in all substrates by a 200 nm layer of SiO_2. Fig. 2 presents the extraction results pertaining to both the measured (i) and simulated lines (ii) and (iii) using two separate simulation methods. A TCAD solver (ii), Atlas from Silvaco, is used to compute the substrate C and G components of the CPW

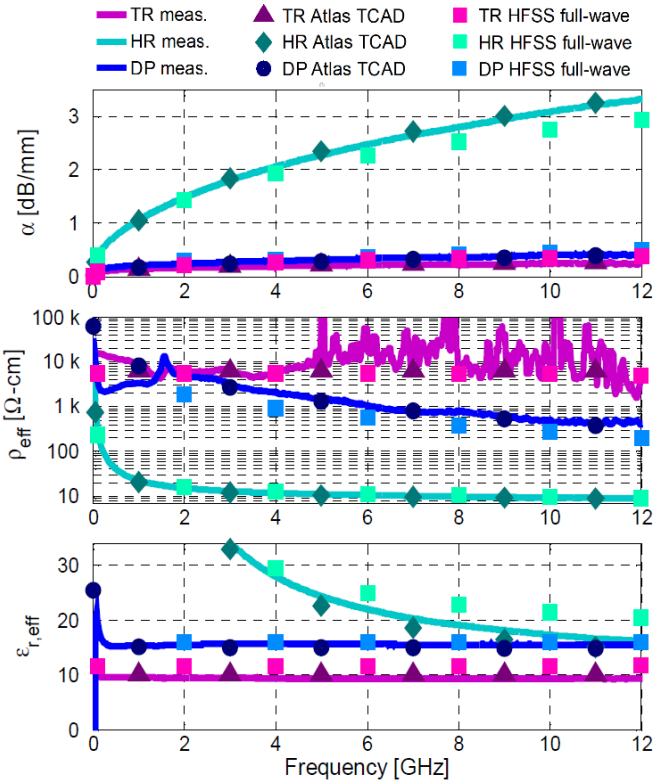

Fig. 2. Effective electrical substrate parameters extracted from CPW-lines S-parameters obtained by (i) on-wafer measurements, (ii) Atlas TCAD simulations and (iii) HFSS full-wave simulations.

lines, taking into account material parameters such as oxide charge density and traps. The TCAD software solves for semiconductor transport equations, calculating the induced band-bending potential at each finite element substrate node. Combined with closed form expressions for the R and L parameters of the CPW [5], the line's S-parameters are constructed. A second simulation method (iii) is used based on HFSS software from Ansys. HFSS is a full-wave electromagnetic solver of Maxwell's equations in 3D. The substrate parameters used in these simulations are based on the resistivity profiles obtained from the TCAD results. Silicon layers and blocks with various resistivity values are placed in the HFSS simulated structure to account for the HR bulk, the PSC region, and for the depletion junctions. The exact values used are detailed in section III. A.

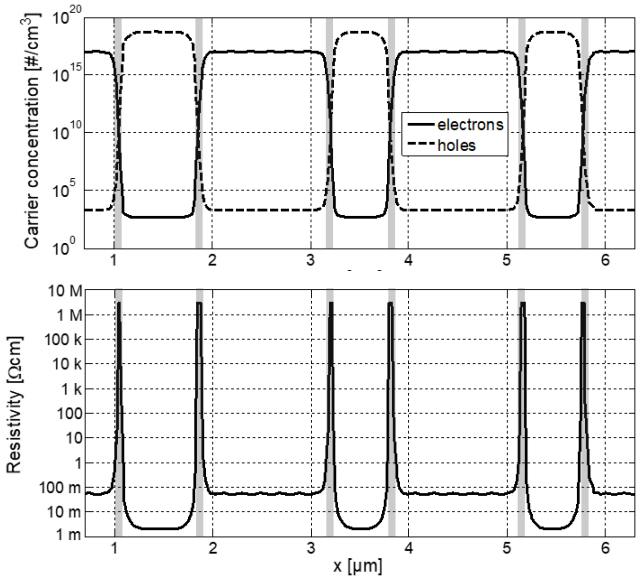

Fig. 3. Electron and hole concentration (top) and local resistivity (bottom) in a depletion enhanced-substrate as a function of position directly beneath the BOX, in the direction of increased impedance.

Suffering from the PSC effect, the HR substrate presents low ρ_{eff}, high α (mainly shunt substrate losses), and $\varepsilon_{r,eff}$ that converges towards 11.7 at high frequency, as the propagation mode shifts from the slow-wave to the quasi-TEM mode. The TR sample shows high performance with ρ_{eff} above 5 kΩcm and low α (mainly series metallic losses). In this highly resistive wafer the propagation mode in the CPW is quasi-TEM starting

from a few tens of MHz and therefore $\varepsilon_{r,eff}$ is at a constant value close to 11 over almost the entire measured frequency range.

The DP substrate shows increased performance compared to the HR wafer thanks to its high density of PN junctions between signal and ground lines in the CPW. The PN junction density is one per 2 µm (in the x-direction in Figs 1a and 3), yielding at least 6 junctions between the signal and ground lines of our CPW that drastically increase the substrate impedance between these two lines of the RF device. Furthermore, the implant doses were tailored to low values in order to obtain maximal depletion junction widths, while remaining sufficiently high to effectively counter the PSC effect induced by the fixed oxide charges. Athena process simulations estimate the depletion width of each junction of our fabricated sample to be around 160 nm at a depth of 200 nm below the BOX using N and P doses of 1e13/cm² (Phosphorous) and 1e14/cm² (Boron), respectively, and N and P implant energies of 50 keV and 30 keV, respectively (through 20 nm of SiO_2 to prevent channelling effects). Fig. 2 shows that the DP substrate achieves high ρ_{eff} in the range of 2 kΩcm at 5 GHz and low RF losses. Since the conductivity in the P and N regions is very high, the E-fields flatten there and they are seen as local equipotential regions. This has the effect of concentrating the E-field in the small depletion volumes in between them, which translates to a higher $\varepsilon_{r,eff}$ sensed by the overlying coplanar technology. Though undesired, the increase in $\varepsilon_{r,eff}$ is acceptable, as the DP substrate presents a value of 15.6. Although this value is larger than the relative permittivity of silicon (11.7), it is a worthwhile trade-off enabling a 200-fold increase of the ρ_{eff} as compared to HR.

The proportion of depleted volume in the interfacial silicon layer (P- and N-doped regions) of our samples, using the given lithography (limited to 1-µm resolutions) and implant parameters, is then 8% density (160 nm / 2 µm). The use of a more advanced fabrication process is expected to produce even better RF results than those presented here, as it would enable a higher density of depletion junctions to be defined in a given space, thereby increasing the substrate impedance even further.

III. High Quality RF Inductors on Depletion-Enhanced Silicon

The substrate improvement concept of buried depletion junctions interrupting the PSC layer in a HR substrate is applied via simulations to the design of high-quality RF inductors. Full-wave simulations are employed using HFSS software to compute the S-parameters of an integrated spiral inductor, illustrated in Fig. 4 (top), on all considered Si-based substrates.

A. HFSS Substrate Definition and Calibration

The TR substrate is defined as having a homogenous resistivity of 5 kΩcm below a 200 nm BOX.

In the HR substrate a 1.5 µm-deep layer with a resistivity of 1 Ωcm is introduced between the BOX and the high-resistivity bulk to model the PSC layer. This approach of modelling the PSC region as a single layer of silicon with a homogeneous resistivity is chosen in order to avoid ultra-fine meshing and unreasonable computation times in the full-wave solver.

For the enhanced DP substrate, additional 1.5 µm-deep shapes with 10 kΩcm resistivity are patterned inside a 1.5 µm-deep conductive 100 mΩcm layer for the modelling of the depletion junctions induced between adjacent P and N regions.

All of these discussed layers are depicted in Fig. 4 (bottom). The given depths and resistivities associated to the PSC and depletion regions are based on the extracted resistivity profiles from the TCAD simulations, and are calibrated such that simulated CPW lines in HFSS fit to the measured data. These results are shown in Fig. 2, where a good fitting between the HFSS data and the measurements is observed, demonstrating an efficient calibration of the substrates defined in HFSS.

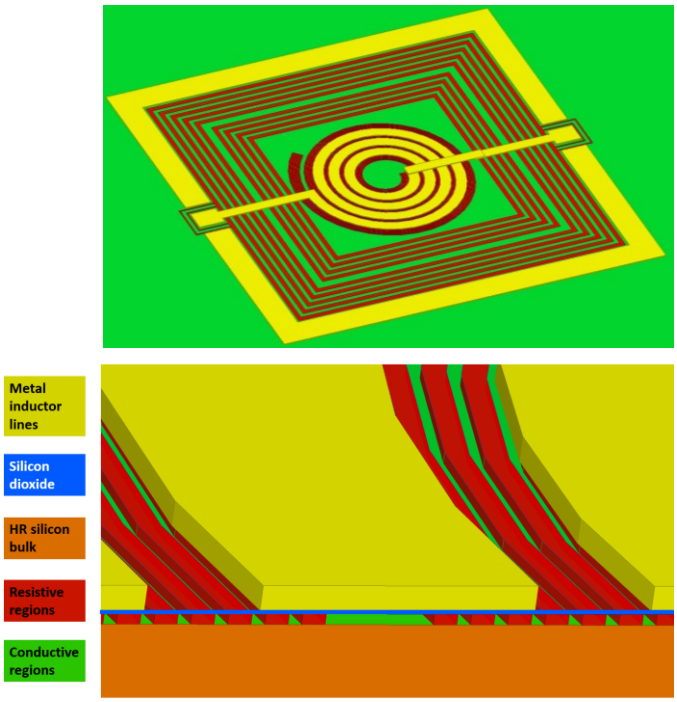

Fig. 4. Schematical representation of (top) Spiral inductor (yellow) on depletion-enhanced substrate simulated using Ansoft HFSS software. (bottom) Zoomed view of the highly resistive depletion regions (red) interrupting the conductive PSC layer (green) beneath the SiO_2 BOX layer (blue).

B. RF Inductor Results

These calibrated substrates are then used to simulate other passive RF devices, such as an integrated spiral inductor. The designed inductor's layout is shown in Fig. 4. It is a 3.5 turn spiral coil track that is 40 µm wide with a distance of 17 µm between each spiral and with an inner radius of 100 µm. The metal is 3 µm thick with a conductivity of 2.9×10^7 S/m.

Fig. 5 plots the inductance L and quality factor Q, calculated from the simulated two-port Y-parameters according to [6].

The inductance on TR substrate boasts a peak Q-factor of 22 at 5 GHz for an inductance value of 35 nH, with a self-resonant frequency of 10.4 GHz.

When the device is transposed on the modelled HR substrate its quality at 5 GHz is poor, presenting a Q-factor of 1.4. The peak Q-factor drops to a value of 7.7 and its frequency point drops to 1 GHz. This degradation in quality factor is associated to the presence of the PSC layer that degrades the device's performance by facilitating strong coupling between

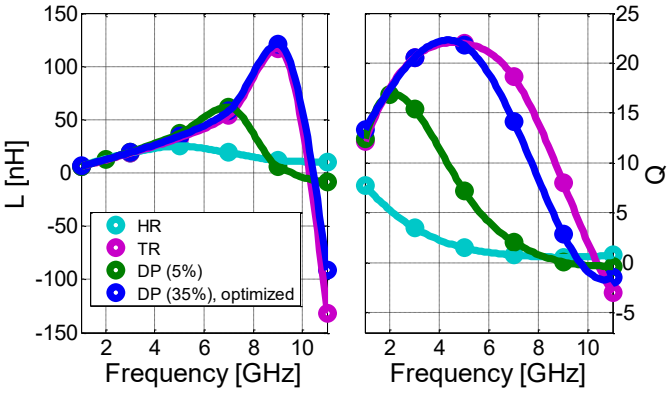

Fig. 5. Simulated inductance and quality factor of integrated spiral inductors on HR, TR and depletion-enhanced Si-based substrates.

the parallel spirals of the inductance. A simple lumped equivalent circuit model of an integrated inductor on TR and HR substrates is presented in [7], where insight is given on the PSC layer's influence on inductor Q-factor.

Therefore, by adding depletion junctions in a spiral pattern between the metallic spirals of the device, a drastic increase in substrate impedance between neighbouring spirals is achieved, which impacts positively on the overall Q-factor. This careful layout design is presented in Fig. 4, in which the top image shows the entire device. The added depletion regions (shown in red) are placed in parallel spiral patterns between the metal spirals of the inductor (yellow). The bottom image of Fig. 4 highlights these depletion patterns (red) implemented beneath the BOX (blue) that interrupt the highly conductive P- and N-doped regions (green). By adding a 5% density of depletion regions interrupting the conductive layer, the inductor's Q-factor is improved to a peak value of 17 at 2.2 GHz, and to a value of 7.2 at 5 GHz, as illustrated by the green data in Fig. 5. By increasing the depletion density to 35% the inductor quality is further improved, as shown by the blue data of Fig. 5. For this device, depletion junctions were also added to isolate the signal line of the spiral inductor from the RF-ground ring around it, using a series of concentric square patterns. Such patterns are also introduced around the signal port pads to isolate them from the ground lines as well, as can be seen from Fig. 4 (top). For this optimized design, the Q-factor reaches a peak value of 22 at 4.3 GHz, and present a Q-factor of 21 at 5 GHz, closely rivalling the performance on the TR substrate, and demonstrating the potential for this substrate-enhancement method for RF integrated passive inductors. We note a slight lowering of the inductor's self-resonant frequency on this DP substrate that is attributed to a slightly higher effective substrate permittivity sensed by the device, as discussed in section II B.

IV. Large-Signal Non-Linear Performance of Depletion-Enhanced Silicon

Large-signal measurements of the CPWs were performed on-wafer using a dedicated setup. A single tone with fundamental frequency of 900 MHz is injected into one port of the CPWs on each substrate. The power of this input tone H'1, is swept from -30 dBm to +25 dBm, and the output signal's components H1 (fundamental), H2 and H3 (second and third harmonics) are retrieved by a spectrum analyzer. The HD components are

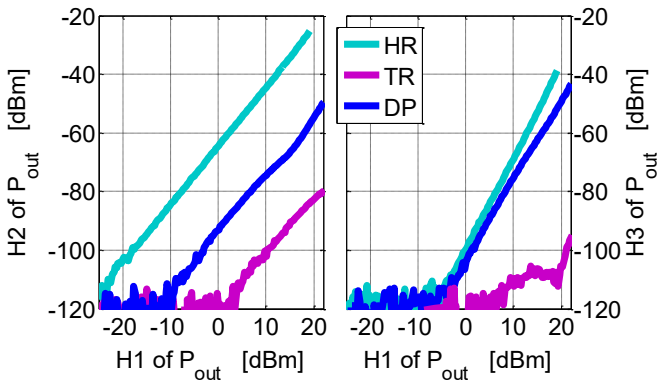

Fig. 6 Harmonic distortion components H2 and H3 at the output of a 2 mm CPW line on HR, TR and depletion-enhanced Si-based substrates.

plotted in Fig. 6. It is shown that the voltage sensitive HR sample is highly non-linear, whereas the CPW on the TR wafer shows low distortion. The DP substrate presents intermediate results, achieving 30 dB total linearity increase over HR.

V. Conclusion

In this work a novel substrate enhancement technique is presented enabling high quality RF performance to be achieved. Using initial prototypes alongside simulations it is shown that integrated CPW lines and inductors implemented on these substrates highly outperform those on a high-resistivity wafer by effectively combatting the parasitic surface conduction effect, presenting low-loss along with high quality factor and linearity. By careful design of the PN depletion junctions it is shown that the RF performances are close to those of the widely used benchmark trap-rich solution and are promising candidates for integrated RF applications. Indeed, full-wave simulations of an integrated spiral inductor on calibrated substrates demonstrated the technique's potential for achieving high quality factor devices on a depletion-enhanced substrate. The technique is equally suited to SOI and bulk technology, with a unique compatibility with FDSOI, first due to below-BOX implants being readily available at the foundry level, and second because of being able to offer high-quality RF substrates without compromising the quality of the back-gate contacts. Furthermore, industrial level lithography (in the tens of nm) will enable the fabrication of substrates with even higher RF performances to those given in this work (with µm- lithography) by packing a higher density of depleted junctions beneath devices.

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