Post-process local porous silicon integration method for RF application

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Abstract— The interest of porous silicon (PSi) for RF applications has been widely demonstrated in many previous works. In most of them, PSi is integrated into the substrate during its fabrication (PRE-PSi) prior to a standard process (e.g. CMOS). Such PRE-PSi technology has major incompatibilities with foundry-level processes (mechanical instability during annealing, warp, bow, etc.). This paper presents an innovative technique of post device fabrication integration of porous silicon (POST-PSi) with the substrate to overcome these incompatibilities. Furthermore, the frontside is not involved in porous layer growth and therefore the integrity of the RF circuitry is not impacted by the POST-PSi process. Additionally, the novel technique allows for local porosification, enabling local pockets of high-quality RF PSi-substrate, beneath the RF devices of interest, to be embedded within a structurally stable silicon crystalline bulk. Similar to PRE-PSi, the POST-PSi substrates are produced by anodization starting from the most widespread highly doped milliohm-centimeter Si wafers. A comparison of the RF performances with various advanced trap-rich (TR) silicon-on-insulator (SOI) and PRE-PSi substrates are presented. In addition to its compatibility with standard microfabrication processes and stable final structure, POST-PSi provides characteristics of low losses, high isolation and very high linearity, unmatched by any other silicon-based substrate.

***Keywords*—Effective dielectric permittivity, effective resistivity, harmonic distortion (HD), microwave losses, porous silicon (PSi), CMOS compatibility, RF characterization, RF substrate, silicon-on-insulator (SOI) technology, trap-rich (TR) high-resistivity (HR) silicon.**

I. Introduction

Despite the emergence of new materials in substrate composition, silicon-based technologies remain a strategic choice for RF applications. The co-integration of high-speed digital circuits alongside analog and RF front-end modules on the same chip, the excellent control of the silicon process and the low production cost of the substrates are some advantages of silicon technologies. However, due to its electrical conductivity and high permittivity, standard doped silicon suffers from high losses and poor isolation for co-integrated circuits. Over the past three decades, a series of silicon-based substrate technologies have successfully reduced this parasitic coupling, mainly by reaching higher resistivity. First, high-resistivity (HR) low-doped silicon was used as a handle substrate in silicon-on-insulator (SOI) substrates providing only a slight improvement in the RF properties of the substrates. It is well known that they suffer from parasitic surface conduction (PSC) effects beneath the buried oxide (BOX) layer, which degrade the effective resistivity of the substrate [1].

Over the past decade, research efforts have been made to develop technological solutions to reduce these PSC effects [2]–[4] and improve the effective electrical properties of HR silicon substrates. The introduction of a thin trap-rich (TR) layer beneath the BOX has been proven as a very effective technique while being compatible with industrial SOI wafer fabrication and with the important thermal budget of a standard CMOS process [4].

As an alternative to HR-SOI or TR-SOI, porous silicon (PSi) has been proposed for several decades [5]. This material is formed by electrochemical dissolution (anodization) of bulk silicon [6]. PSi achieves high resistivity, low permittivity, low losses, low crosstalk levels, and strong linearity. For all these reasons, PSi is a promising candidate for RF substrates [5].

In most previous works, silicon is anodized during the substrate fabrication, before device-processing (PRE-PSi). Nevertheless, the mechanical stability of PSi is often challenging, mainly for large area wafers. Indeed, the stress generated by the porous silicon layer can produce cracks or warpage of the substrate [7]. Moreover, this method does not allow flexibility in the PSi properties, such as the pore diameter. Excessive pore diameters result in surface roughness, inappropriate for processes with multiple layer depositions. Nonetheless, some weakly restrictive microfabrication processes (e.g. surface passive RF device fabrication) have been successfully achieved on mesoporous silicon layer [8], contrary to more complex processes such as standard industrial CMOS processes CMOS.

In this paper, we present an innovative technique for integrating high-quality PSi into post-process of RF circuit fabrication (POST-PSi): PSi electrochemical etching is performed after the circuits are completely processed and before the packaging steps. This approach overcomes the incompatibility issues of the PSi presence in a standard CMOS process. It also has the advantage of having a greater latitude for producing porous silicon. Indeed, the absence of high temperature annealing downstream of the anodization allows PSi to achieve a higher porosity, and hence aim for better RF performances.

Previous works propose a silicon anodization process of the sample in post-fabrication of the RF devices by the backside [9] or the frontside [10]. These complex techniques are binding for the design and fabrication process of the electrical circuits on the processed frontside substrate. Indeed, they require an access to the electrolyte or electric current (necessary for the porous silicon growth) on the frontside. Second, the whole substrate thickness is not porous. A layer of the handle substrate is maintained bulk and negatively impacts the RF performance of the substrates.

We present POST-PSi SOI substrates fabricated starting from Si wafers with nominal resistivity of heavily doped (10–20 mΩ·cm) and compare it to other common Si-based substrates. The comparisons are made for all substrates in terms of: 1) the effective electrical parameters extracted through the direct S-parameter measurements of coplanar waveguides (CPW) over a wide frequency range from 10 MHz to 10 GHz and 2) the substrate linearity performance, in terms of the harmonic distortion (HD) subjected to a 900-MHz signal by the voltage-dependent electrical characteristics of the substrate.

II. Substrate Fabrication and Description

A. Comparison Substrates

In this work, four types of Si-based substrates are compared with POST-PSi SOI substrates: standard (Std) p-type silicon (nominal 1–10 Ω·cm), HR silicon (nominal > 5 kΩ·cm), TR-enhanced HR silicon, and PRE-PSi substrates.

The TR substrates consist in an n-type HR-Si wafer with a nominal resistivity above 5 kΩ·cm and a 300-nm-thick TR poly-Si layer deposited through low-pressure chemical vapor deposition (LPCVD). A typical TR substrate structure is depicted in Fig. 1 (left).

The PRE-PSi substrate, is prepared from a 3-in strongly doped p-type silicon wafer (10–20 mΩ·cm) porosified in an electrolyte composed of 1:1 mixture of hydrofluoric acid (HF 49%) and ethanol. A current density of 75 mA/cm^2 for 40 min is applied. Finally, the PRE-PSi substrate is annealed in oxygen at 300 °C for 2 h to strengthen the microstructure, and then in nitrogen at 420 °C for 2 h to stabilize the structure. Using this process, the top 50 µm of the silicon are porosified, yielding a PRE-PSi structure such as shown in Fig. 1 (center).

On top of all four substrates, a 500-nm silicon oxide (SiO_2) layer is deposited at 300 °C by plasma-enhanced chemical vapor deposition (PECVD), followed by a 1-µm-thick layer of aluminum deposited by physical vapor deposition (PVD) for the definition of the CPW lines.

B. POST-PSi SOI Substrate Specifications

The structure of a POST-PSi SOI substrate is presented in Fig. 1 (right). The porous layer is formed from the backside to the frontside of the silicon handle substrate. The electrochemical etching stops on an etch stop layer placed between the silicon substrate and the RF circuit layers.

A hard mask on the backside substrate is used to define the location of the etching of the porous layer. The porous layer is located under the central signal to isolate it from ground lines (Fig 1).

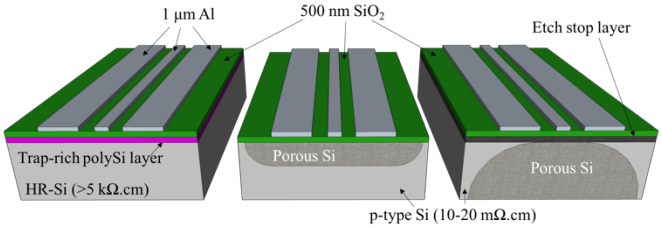

Fig. 1. Schematic of a CPW transmission line fabricated on trap-rich Si substrate (left) on a 50 µm-thick PRE-PSi layer (center) and on a 380 µm-thick POST-PSi layer (right).

C. POST-PSi SOI Substrate Fabrication

A 3-in and 380µm-thick heavily doped p-type silicon wafer (10–20 mΩ·cm) is used as starting substrate. Before processing, the silicon wafer is cleaned by O_2 plasma and immersed in 2% HF to remove the thin oxide. A HF-resistant etch-stop layer is deposited on the substrate frontside. On this layer, a 500nm-thick PECVD silicon oxide is deposited to simulate the SOI BOX. Finally, 8 mm-long CPW lines are fabricated by standard photolithography and wet etching in a 1 µm-thick aluminum layer deposited by e-beam PVD. The backside is patterned by a HF-resistant mask to define the local porosification zones.

D. Porosification

The porosification from the backside is performed in an adapted electrochemistry cell. Its particularity is making electrical contact with the silicon substrate at the edges of its backside, not involving the frontside and therefore not affecting the RF circuits. PSi is prepared by anodization in a 3:1 volume solution of HF(49%):ethanol. The growth of porous silicon is isotropic. The applied total current is adjusted to have an etching current density around 100 mA/cm^2. The anodization is performed such that the pores reach the etch-stop layer.

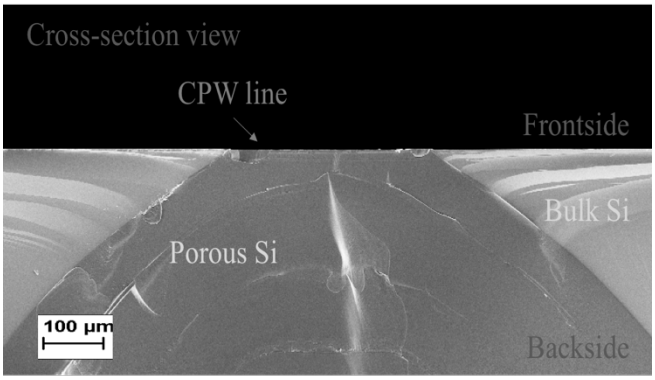

Fig. 2. Cross-sectional SEM picture of POST-PSi substrate.

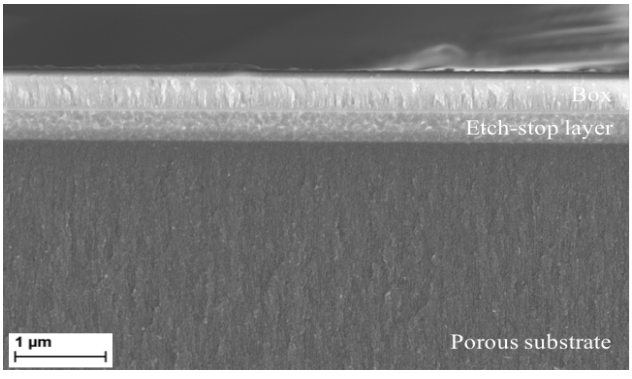

Fig. 3. Cross-sectional SEM picture of PSi layer with the etch-stop layer and the BOX on top. PSi growth reaches etch stop layer.

E. RF Characterization

The same CPW lines are used for the characterization of all substrates. The dimensions of the measured CPWs are: a central signal line (38 µm wide) surrounded by two ground lines (208 µm wide and distant of 18 µm from the signal line), with a length of 8 mm. On-wafer measurements of CPW lines were performed using an Agilent 2-port performance network analyzer (PNA)-X vector network analyzer and a pair of ground-signal-ground (GSG) |Z| probes from Cascade Microtech.

From the measured S-parameters, we extract up to 10 GHz the effective resistivity (ρ_{eff}), effective relative permittivity ($\varepsilon_{r,eff}$), RF line losses, and characteristic line impedance using the method described in [13]. The same CPWs are also measured in a large-signal setup to evaluate the signal distortion induced by the nonlinear properties of the substrates. Large-signal measurements of the CPW lines were performed on-wafer based on the setup from [14] and using an Agilent 4-port PNA-X vector network analyzer. The HD setup achieved detection of harmonic levels of a 900-MHz signal as low as −115 dBm for a maximum input power of 25 dBm.

III. Results and Discussions

A. Morphology characterization

Fig. 2. shows a cross-sectional view of a locally etched porous silicon substrate. PSi grows over the entire substrate thickness from the backside and reaches the frontside over a surface area similar to the openings made in the mask on the backside. An over-etching ensured that the porous layer is present under the whole RF device (CPW line). Due to the isotropy of the porous silicon growth, the porous layer is largely extended on the backside.

Fig. 3. is a magnification of the frontside and shows the etch stop layer. PSi reached the etch-stop layer so that there is no bulk silicon remaining under the devices, which would decrease the RF performances of the substrate.

B. Small-Signal Electrical Parameters

A comparison of effective resistivity (ρ_{eff}), effective relative permittivity ($\varepsilon_{r,eff}$), lineic attenuation coefficient (α), and characteristic line impedance of the CPW lines made on the five considered substrates is shown in Fig. 4.

Both PSi wafers present higher effective resistivities and lower line losses than the TR substrate. The POST-PSi SOI substrate achieves an effective resistivity performance value of around 7.9 kΩ·cm while the PRE-PSi substrate shows a mean value of around 5.2 kΩ·cm (representative values obtained from the average of ρ_{eff} between 1 and 10 GHz). POST-PSi has the largest increase with a resistivity approximately doubled compared to the TR substrate, that shows a mean value of around 3.8 kΩ·cm.

The line losses for the PSi substrates at 10 GHz are about 0.13 dB/mm (POST-PSi) and about 0.2 dB/mm (PRE-PSi) which, as for TR (0.3 dB/mm), are also mostly due to resistive losses in the metallic lines.

Porous silicon is a matrix composed of silicon and air. Thus, the permittivity of porous silicon is between the very low permittivity of air ($\varepsilon_r \approx 1$) and the high one of bulk silicon ($\varepsilon_r \approx 11.7$). PRE-PSi and POST-PSi have effective relative permittivities of 5.5 and 3.5, respectively, considerably lower than those of the substrates Std, HR or TR, providing higher isolation against capacitive coupling, especially at high frequencies.

C. Large-Signal Harmonic Distortion

Comparison of the measured HD levels induced in 8 mm-long CPW lines implemented on the five Si-based substrates is

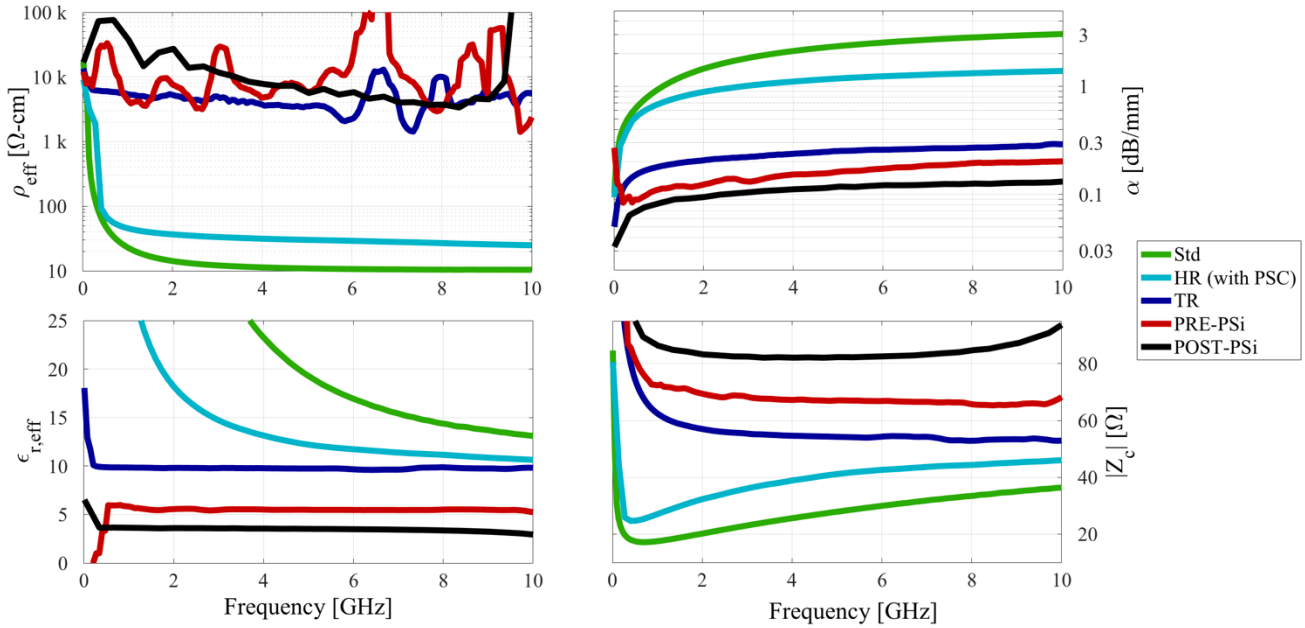

Fig. 4: Effective electrical substrate parameters extracted from wideband S-parameter measurements of RF CPW lines. Effective substrate resistivity (top left). Effective substrate relative permittivity (bottom left). CPW line losses per unit length (top right). CPW line characteristic impedance (bottom right).

shown in Fig. 5. The electrical characteristics of Std and HR substrates are strongly voltage dependent and exhibit a strong nonlinear behavior.

TR technology, by trapping PSC, shows a marked improvement of linearity substrate behavior. Reductions of more than 55 and 65 dB are obtained, respectively, for the second and third harmonics generated on a TR substrate.

PSi substrates further reduce the HD levels. The second-harmonic levels generated on PRE-PSi and POST-PSi are, respectively, 34 and 60 dB lower than on the benchmark TR solution substrate.

Due to the extremely high linearity of the POST-PSi wafer, that exhibits HD components lower than -110 dBm over the measured power range, it was necessary to measure this sample on a different set-up with lower noise floor.

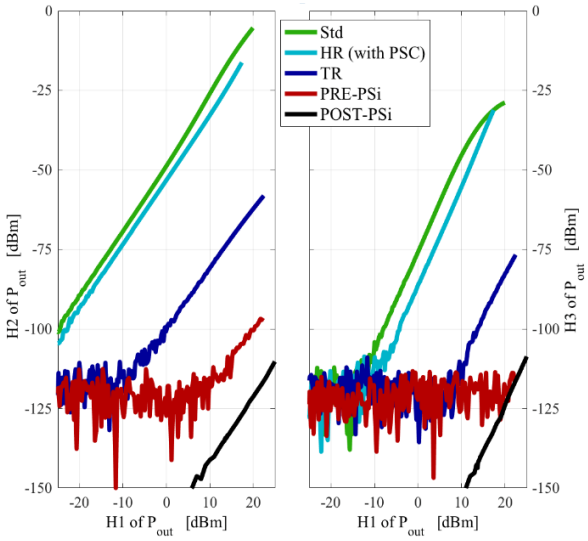

Fig. 5: Comparison of the measured HD levels induced in 8 mm-long CPW lines implemented on the various Si-based substrates under consideration. The fundamental frequency is 900 MHz, and the lines are biased to 0-V dc.

This increased linearity for PSi is explained by the tight pinning of the Fermi level throughout the entire volume of the PSi layer. In contrast to TR substrates, in which the Fermi level is pinned at the BOX interface due to traps in a thin 300-nm poly-Si layer, the PSi introduces trapping centers 50-µm deep (PRE-PSi) and whole thickness (POST-PSi) into the substrate volume, along the pore walls. The electrical characteristics of the entire thick PSi layer resist modulation by large-signal RF fields. As a result, the voltage dependence on the Fermi level, on carrier densities, and therefore on substrate conductivity, is even further reduced, conferring to the CPW transmission lines on PSi substrates remarkably high linearity.

IV. Conclusions

In this paper, the RF electrical performances of an innovative POST-PSi substrate were investigated and compared with four other silicon-based solutions, including the most widely studied PRE-PSi substrate and the benchmark TR SOI solution. In this innovative technique POST-PSi, local porosification of pockets of high-quality RF PSi-substrate is formed beneath the RF devices of interest. Only the substrate backside is involved in the process which is strongly compatible with foundry-level processes. POST-PSi also provides the highest RF electrical performances, with very strong linearity (60-dB improvement over the benchmark TR technology), low relative effective permittivity (3.5), and high effective resistivity (7.9 kΩ·cm). The combination of low permittivity and high effective resistivity of POST-PSi allows for the integration of high quality RF circuits and low crosstalk interference levels.

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References

[1] Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, *IEEE Microw. Guided Wave Lett*., vol. 9, no. 1, pp. 10–12

[2] Y. H. Wu et al., in *IEEE MTT-S Int. Microw. Symp. Dig*., Boston, MA, USA, Jun. 2000, pp. 221–224.

[3] H. S. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, and J. A. C. Stewart, *IEEE Microw. Guided Wave Lett*., vol. 9, no. 10, pp. 395–397

[4] D. Lederer and J.-P. Raskin, *IEEE Electron Device Lett*., vol. 26, no. 11, pp. 805–807.

[5] Gautier G. (2014) RF Electrical Isolation with Porous Silicon. In: Canham L. (eds) Handbook of Porous Silicon. Springer, Cham.

[6] V. Lehmann, The electrochemistry of silicon. Vch Verlagsgesellschaft Mbh, 2010, pp. 1–283.

[7] M. Capelle, J. Billoué, T. Defforge, P. Poveda, and G. Gautier, *Thin Solid Films*, vol. 585, no. C, pp. 66–71.

[8] M. Capelle, J. Billoue, P. Poveda, and G. Gautier, *IEEE Transactions on Electron Devices*, vol. 62, no. 12, pp. 4169–4173.

[9] Li C, Liao H, Wang C, Yin J, Huang R, Wang Y, *IEEE Electr. Dev. Lett.* 28:763–766, 2007.

[10] L.-Y. Ding, W.-P. Shih, Y.-C. Hu, Y.-J. Chen, and P.-Z. Chang, *Micro. Nano Lett..,* vol. 5, no. 5, p. 266, 2010.

[11] Canham L. (2014) Mechanical Properties of Porous Silicon. In: Canham L. (eds) Handbook of Porous Silicon. Springer, Cham.

[12] J. Lascaud, T. Defforge, D. Certon, D. Valente, and G. Gautier, *J. Appl Phys*., vol. 122, no. 21, p. 214903, Dec. 2017.

[13] D. Lederer and J.-P. Raskin, *Solid-State Electron*., vol. 49, no. 3, pp. 491–496, 2005.

[14] D. C. Kerr, J. M. Gering, T. McKay, M.S., C. Roda Neve, and J.-P. Raskin, in *IEEE Topical Meet. on Silicon Monolit. Integr. Circ. in RF Syst.*, SiRF '08, (Orlando, FL), pp. 151–154, 23-25 Jan 2008.