Post-process porous silicon for 5G applications

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***Abstract*—The interest of 5G in centimeter and millimeter waves relies on large blocks of available spectra and thus increased bandwidth. At these frequencies, the dielectric and conductive losses of the substrate can greatly degrade the performances of RF circuits. With high electrical resistivity and low relative permittivity, porous silicon is an ideal candidate as a high-quality RF substrate. This paper presents an innovative technique of post device fabrication integration of porous silicon (POST-PSi) with the substrate. The frontside is not involved in porous layer growth and therefore the integrity of the RF circuitry is not impacted by the POST-PSi process. A comparison of the RF performances with benchmark trap-rich (TR) silicon-on-insulator (SOI) substrate is presented. In addition to its compatibility with standard microfabrication processes and stable final structure, POST-PSi provides characteristics of low losses, high isolation and very high linearity, unmatched by any other silicon-based substrate.**

Keywords- Effective permittivity, effective resistivity, microwave losses, porous silicon (PSi), CMOS compatibility, RF substrate, silicon-on-insulator (SOI) technology.

I. INTRODUCTION

5G is the next generation of mobile networks and will achieve speeds of several Gb/s. 5G is therefore designed to support large amounts of data, but also to enable a very large number of connections and multiply the types of uses. It will be versatile, to adapt to the needs of each use: performance, energy savings, critical uses (e.g. autonomous cars), etc. For 5G, centimeter and millimeter waves are considered because they have wide ranges of available spectra (3.5-6 and 24-86 GHz) and will also bring new features such as beam forming and Multiple Input Multiple Output (MIMO) antenna arrays.

The choice of 5G technology blocks is critical to ensure the required performance. Despite the excellent performance of emerging materials, silicon-based technologies remain a strategic choice for RF applications. The co-integration of high-speed digital circuits alongside analog and RF front-end modules on the same chip, the excellent control of the silicon process and the low production cost of the substrates are some advantages of silicon technologies. However, in silicon-on-insulator (SOI) substrates, standard doped silicon handle substrate suffers from high losses and poor isolation for co-integrated circuits due to its electrical conductivity and high permittivity. A high resistivity silicon handle substrate has similar poor RF performances due to a parasitic surface conduction (PSC) effects beneath the buried oxide (BOX) layer, which degrade the effective resistivity of the substrate [1].

Over the past three decades, a series of silicon-based substrate technologies have successfully reduced this parasitic coupling and reaching higher resistivity. The introduction of a thin trap-rich (TR) layer beneath the BOX has proved to be a very effective technique while being compatible with industrial SOI CMOS thermal budgets and wafer fabrication processes [2].

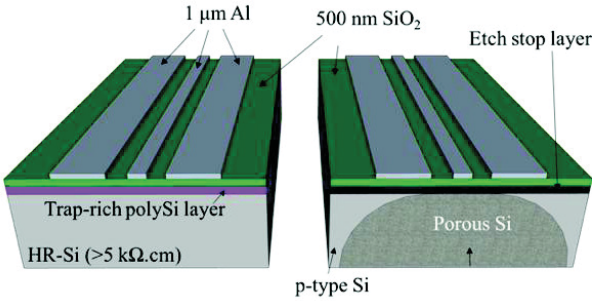

Fig. 1. Schematic of a CPW transmission line fabricated on trap-rich Si substrate (left) and on a 380 μm-thick POST-PSi layer (right).

As an alternative to TR-SOI, porous silicon (PSi) has been proposed for several decades. This material is formed by electrochemical dissolution (anodization) of bulk silicon. PSi achieves high resistivity, low permittivity, low losses, low crosstalk levels, and strong linearity. For all these reasons, PSi is a promising candidate for RF substrates [3]. In this paper, we present an innovative technique for integrating high-quality PSi into post-process of RF circuit fabrication (POST-PSi): PSi electrochemical etching is performed after the circuits are completely processed and before the packaging steps. This approach overcomes the incompatibility issues of the PSi presence in a standard CMOS process. POST-PSi SOI substrates is compared with the benchmark RF-SOI substrates in terms of their effective electrical parameters extracted through the direct S-parameter measurements of coplanar waveguides (CPW) over a wide frequency range from 10 MHz to 67 GHz, which covers most of the frequencies targeted by 5G.

II. SUBSTRATE DESCRIPTION

A. Trap-Rich Reference Substrate

The TR substrate consists in an n-type HR-Si wafer with a nominal resistivity above 5 kΩ·cm and a 300-nm-thick TR poly-Si layer deposited through low-pressure chemical vapor deposition (LPCVD). On top, a 500-nm silicon oxide (SiO_2) layer is deposited at 300°C by plasma-enhanced chemical vapor deposition (PECVD), followed by a 1-μm-thick layer of aluminum deposited

by physical vapor deposition (PVD) for the definition of the CPW lines. A typical TR substrate structure is depicted in Fig. 1 (left).

B. POST-PSi SOI Substrate

The structure of a POST-PSi SOI substrate is presented in Fig. 1 (right). A 380µm-thick doped p-type silicon wafer is used as starting substrate. An etch-stop layer is deposited on the substrate frontside. On this layer, a 500nm-thick PECVD silicon oxide is deposited to simulate the SOI BOX. Finally, 8 mm-long CPW lines are fabricated by standard photolithography and wet etching in a 1 µm-thick aluminum. The backside is patterned by a HF-resistant mask to define the local porosification zones.

The porosification is performed in an adapted electrochemical cell from the backside. Its particularity is to not involve the frontside substrate and therefore to not affect the RF circuits. PSi is prepared by anodization in a solution of HF and ethanol. The applied total current is adjusted to have an etching current density around 100 mA/cm^2. The anodization is performed such that the pores reach the etch-stop layer.

C. RF Characterization

On-wafer measurements of CPW lines were performed using an Agilent 2-port performance network analyzer (PNA)-X vector network analyzer and a pair of ground-signal-ground (GSG) Infinity probes from Cascade Microtech. The lines are 8 mm-long, the signal and ground widths are 38 and 208 µm-wide, respectively, and the spacing between the signal and ground lines are 18 µm-wide. The CPW electrical parameters are extracted using the method described in [4]. Data was removed around the frequencies for which the extraction is ill-conditioned (when $e^{-2\gamma l} \approx 1$).

III. RESULTS AND DISCUSSIONS

A comparison of effective resistivity (ρ_{eff}), effective relative permittivity ($\varepsilon_{r,eff}$), lineic attenuation coefficient (α), and effective loss tangent ($\tan\delta_{eff}$) of the CPW lines made on the two considered substrates is shown in Fig. 2. The effective loss tangent is computed as

$$\tan\delta_{eff}(f) \equiv G(f) \,/\, (\,\omega q C_0 \epsilon'_{r,eff}(f)\,) \qquad (1)$$

and the other parameters are extracted as described in [5].

At 6 GHz the POST-PSi SOI substrate achieves an effective resistivity of around 5.9 kΩ·cm while the TR substrate shows a value of around 3.0 kΩ·cm. As shown by the flatness of the loss tangent curve in Fig. 2, the substrate losses are mainly due to dielectric losses of the environment surrounding the CPW lines (substrate as well as dielectric layer) above 1-2 GHz. They are also the origin of the decay of effective resistivity with frequency.

Even though the total line losses are mainly due to resistive losses in the metal line, the almost constant difference of 0.015 dB between the losses of the POST-PSi and TR below 30 GHz is associated to a higher effective resistivity of the POST-PSi substrate.

Porous silicon is a matrix composed of silicon and air. POST-PSi with a porosity of around 65% has an effective relative permittivity of ~3.5, considerably lower than those of the TR-substrate, providing higher isolation against capacitive coupling, especially at high frequencies.

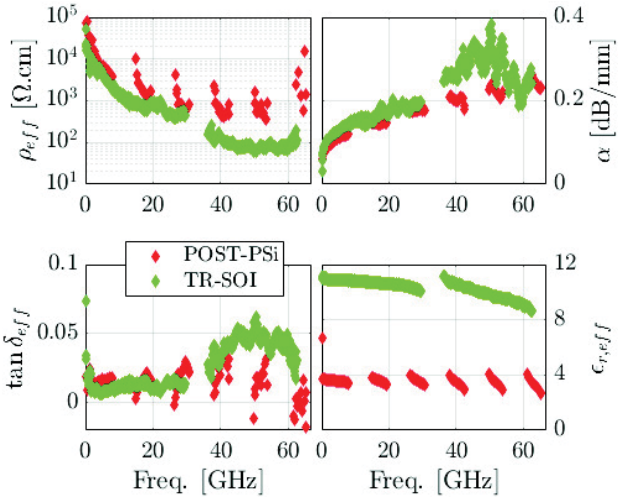

Fig. 2: Effective electrical substrate parameters extracted from wideband S-parameter measurements of RF CPW lines. (Top left) Effective substrate resistivity. (Bottom left) Effective substrate loss tangent. (Top right) CPW line losses per unit length. (Bottom right) Effective substrate relative permittivity.

IV. CONCLUSIONS

In this paper, the RF electrical performances of an innovative POST-PSi substrate were investigated and compared with the benchmark TR SOI solution. In this innovative technique POST-PSi, local porosification of pockets of high-quality RF PSi-substrate is formed beneath the RF devices of interest. Only the substrate backside is involved in the process which is strongly compatible with foundry-level processes. POST-PSi also provides the highest RF electrical performances with low relative effective permittivity (~3.5), and high effective resistivity (~ 3.6 MΩ·cm). The combination of low permittivity and high effective resistivity of POST-PSi allows for the integration of high quality RF circuits and low crosstalk interference levels.

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