Fully Depleted SOI technologies from digital to RF and beyond

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***Abstract* — Today partially depleted SOI MOSFET is the mainstream technology for RF SOI systems. Future generations of mobile communication and computing systems will require transistors with better high frequency and high speed performance at lower power consumption. Fully Depleted (FD) SOI technology is foreseen as one of the best candidates and has been intensively studied these last years. Most of the reported data concern its digital performance. In this paper, the analog/RF behavior, self-heating characteristics, non-linear behavior as well as the wideband electrical performance at cryogenic temperature of FD SOI devices are presented.**

Keywords — Silicon-on-Insulator (SOI); Fully Depleted (FD); Radio Frequency (RF); RF and analog performance; self-heating; non-linear behavior; cryogenic temperature.

I. Introduction

Today, partially depleted (PD) SOI with a channel length from 130 nm down to 45 nm is the mainstream technology for RF SOI integrated circuits (ICs). New generation of mobile communication systems such as 5G require higher cutoff frequency, better linearity and lower power consumption. Moreover the integration of high quality passive elements such inductors requires higher number and thicker metal layers. Thus, for getting higher transistor cutoff frequencies and better back-end of line (BEOL), RF SOI must move to shorter nodes. However, further reduction of device dimensions is problematic due to intrinsic physical limitations such as short channel effects, high current leakage through gate dielectrics, high series resistances, low mobility due to interface effects and high doping levels, high current density and thus self-heating and reliability issues, and so on. Fully Depleted (FD) electronic regime is a promising approach to continue the MOSFETs downscaling. Scaling the thickness of the silicon body is proposed in the case of FinFET and ultra-thin body and buried oxide (BOX), named as UTBB, technologies in order to control short channel effects (SCE) [1, 2]. In order to limit SCE, the channel thickness must be approximately 1/4 and 2/3 of the channel length, respectively, in the case of UTBB and FinFET. Technological aspects, electrostatics, scalability and variability issues in UTBB FD SOI MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [3-5].

In this paper, the analog and RF behavior of FD SOI transistor, including self-heating, non-linear characteristics, and cryogenic temperature performance are presented.

II. Technology Description

Devices studied in this work come from 28 FD SOI process by ST-Microelectronics [6]. Studied MOSFETs are n-type with gate lengths L_g from 25 to 250 nm. The gate stack consists of a high-k gate dielectric on top of a SiON interfacial layer. Equivalent gate oxide thickness is 1.2 nm. The channel is rotated by 45° from the <100> plane. Silicon film thickness is 7 nm. There is no intentional channel doping. The BOX thickness is 25 nm and the ground-plane implantation under it is well-type. More details about fabrication process can be found in [6]. Studied devices feature 16 or 40 parallel fingers of 2 or 1 μm width each, respectively, embedded in CPW (Coplanar Waveguide) pads for RF characterization.

As shown in Fig. 1, the device layout features a particular access to the back-gate, so called flip-well architecture [7], including a heavily doped n-type back plane located below the buried oxide (BOX) and a n-well which provides a natural substrate insulation between the devices.

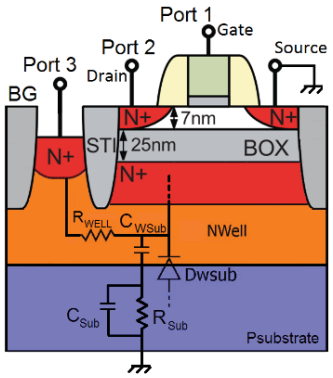

Fig. 1. Simplified cross-section of studied NMOS FD SOI transistor with back-gate scheme.

DC I-V and RF measurements were performed using a HP4145 DC analyzer and PNAX VNA 40 GHz, respectively. For the large-signal measurements, the signal at the fundamental frequency of 900 MHz generated by an Agilent E8267D is amplified up to 4 dBm and injected into the transistor gate. The output signal is recorded and measured by an Agilent E4440A spectrum analyzer and an Agilent U2000B USB Power Sensor (with a frequency bandwidth of 10 MHz - 18 GHz). The recorded output signal contains the fundamental,

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2nd and 3rd harmonics. Lake Shore cryogenic probe station was used to extend measurements temperature range from 300 K down to liquid nitrogen temperature (77 K).

III. Experiment

A. Analog behavior

In [8], the analog performance of FD SOI devices is benchmarked against other advanced CMOS technologies including bulk, PD SOI MOSFETs and FinFETs. FD SOI MOSFETs are very close and can even outperform optimized FinFETs particularly if narrow channel devices are considered. It has been demonstrated that UTBB FD SOI MOSFETs maintain their excellent performance in a wide temperature range, with very limited degradation of main parameters [9]. For instance, only 5 dB reduction of voltage gain (A_v) was observed over 200°C. This makes UTBB FD SOI MOSFETs particularly attractive for high-precision analog circuits. Furthermore, A_v was demonstrated [9] to be maximized in the moderate inversion regime (at ~V_{th}), which is beneficial for low-power applications.

B. Self-heating

Self-heating in semiconductor devices arises because of device scaling which naturally leads to higher current and power densities. Self-heating strongly affects analog device performance. It results in a higher device temperature, which leads to threshold voltage shift, mobility reduction, and consequently degradation of the output current. Bulk MOSFETs exhibit lower self-heating effect than SOI devices even if the channel temperature rise is kept under control with the new generation of SOI transistors presenting a thinner BOX [10]. However, despite of stronger self-heating than in bulk, FD SOI outperforms bulk technology over a wide frequency range [11] in terms of analog/RF performance. For the same channel length, UTBB and FinFET present similar self-heating behavior. Both devices are characterized by a quite thin and narrow silicon channel and the main thermal path from the channel is the source and drain contacts to the back-end metallic lines.

C. RF performance

Fig. 2 shows the current gain cutoff frequency of the front- and back-gate, f_T and f_{Tbg}, respectively, as a function of V_g for V_{ds} = 0.6 or 1 V and for various back-gate biases (V_{bg}). As can be seen in Fig. 2a, at V_{bg} = 0 V, the maximum f_T for 30 nm-long device is as high as ~355 GHz and similar values for f_{max} (power gain cutoff frequency) are reached (not shown here). It is worth noting that application of a positive V_{bg} interestingly shifts the maximum cut-off frequencies to a lower V_g, however, with slightly decreased peak values. The consequence of the back-gate biasing is firstly, the possibility to get the f_T and f_{max} peak values at lower V_g, as expected, (due to threshold voltage shift with V_{bg}) and secondly, flatter f_T and f_{max} versus V_g curves, i.e. wider V_g range with maximum values of f_T and f_{max}. Current gain cutoff frequency related to the back-gate transistor f_{Tbg} versus V_g is illustrated in Fig. 2b showing the double gate behavior of FD SOI transistor. Based on the measured f_{Tbg} of 70 GHz (Fig. 2b) and f_{maxbg} of 27 GHz (not shown here), the back-gate electrode could be used to design original low power and compact active mixing of RF signals.

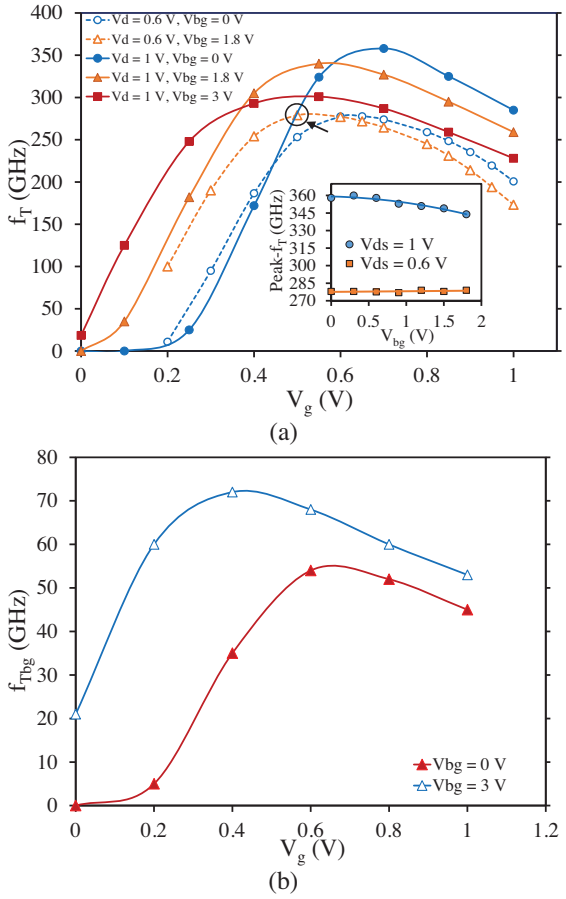

Fig. 2. Front-gate (a) f_T for V_{ds} = 0.6 and 1 V as a function of V_g for various V_{bg}, and back gate (b) f_{Tbg} versus V_g for V_{bg} = 0 and 3 V.

D. Non-linear characteristics

Fig. 3 plots distortion of 2nd and 3rd order, HD2 and HD3, in bulk and FD SOI devices. One can see that there exists a clear bias and current conditions at which FD SOI device outperforms bulk counterpart. It is worth pointing that HD2 is minimized at lower I_d and V_g-V_{th} (not shown) ranges in FD SOI than in bulk devices, thus of interest for further low-power applications.

E. Cryogenic temperature

Fig. 4 shows the current gain cutoff frequency f_T for FD SOI characterized by different channel lengths and measured at 300 and 77 K. Temperature reduction from 300 down to 77 K results in a strong f_T improvement (due to mobility and, hence, transconductance g_m increase). This relative cutoff frequency increase ($\Delta f_T = f_{T@77K} - f_{T@300K}$) becomes particularly significant in shorter devices (inset of Fig. 4). This study suggests 28 nm FD SOI as a good contender for future read-out

electronics operated at cryogenic temperatures (as e.g. around qubits or in space).

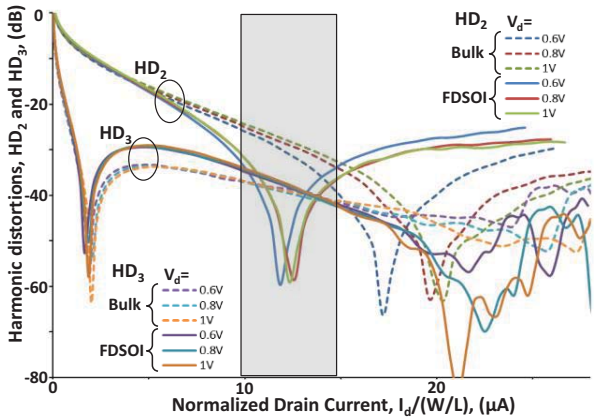

Fig. 3. Experimental harmonic distortions HD2 and HD3 as a function of normalized I_d curves for FD SOI (solid lines) and bulk (dashed lines) MOSFETs measured at various V_d. Shaded area gives example of conditions at which FD SOI device outperforms bulk counterpart.

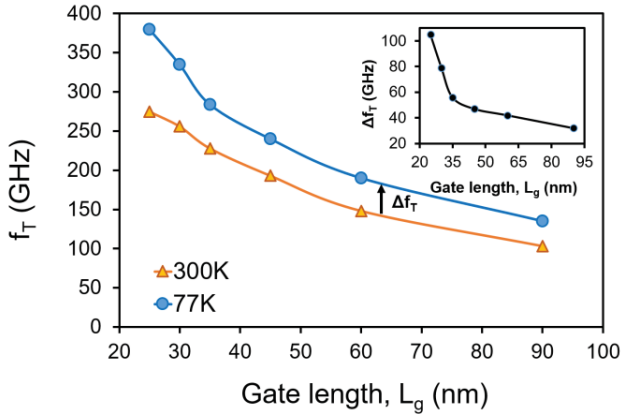

Fig. 4. f_T as a function of L_g at 77 and 300 K for FD SOI MOSFETs.

IV. Conclusion

It has been demonstrated that FD SOI devices exhibit very good analog and RF performance at room and cryogenic temperature. Effect of back-gate bias on RF FoM of front- and back-gate FD SOI MOSFET has been deeply studied based on 3-port wideband measurements. Back-gate bias application shifts and flattens f_T, f_{max} versus V_g curves thus giving more flexibility to the designers for the choice of DC points where maximum f_T and f_{max} is achievable. The impact of back-gate bias on non-linearity was also analyzed. Application of positive V_{bg} in FD SOI was shown to open a way for non-linearity reduction (providing e.g. 10-30 dB reduction in HD2, 3-5 dB in HD3, depending on bias/current conditions). Worth pointing out that minimization of non-linearity appears at lower biases (and currents) in FD SOI devices with respect to its bulk counterpart, which is beneficial for further low-power applications. FD SOI technology performances in millimeter-waves for 5G applications are under investigation.

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