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Prediction of RF performances of advanced MOS transistors from DC and low frequency measurements

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Abstract

This work presents a new method to easily and rapidly extract RF figures of merit of MOSFET transistors. Using DC and low frequency measurements, the extrinsic resistances (R_g, R_s, R_d), the intrinsic conductances (g_m, g_d), and the input capacitance C_{gg} have been extracted. The evaluation of these parameters has enabled to compute 2 RF figures of merit (FoM), namely, the current gain cutoff frequency f_T and the maximum oscillation frequency f_{max}. It has been shown that both the proposed method and the conventional RF extraction technique give quite close values.

KEYWORDS

cutoff frequency, equivalent circuit, extraction method, high frequency characterization, maximum oscillation frequency, MOSFET figures of merit, on-wafer characterization, silicon-on-insulator (SOI) technology, small-signal measurements, *S*-parameters

1 | INTRODUCTION

With significant growing from USD 157.05 Billion in 2016 to USD 661.74 Billion by 2021, the market of Internet of Things (IoT) is advertised a very promising field.[1] Various issues are challenging industrials to fulfill IoT deployment needs within many segments, such as, networking, software solutions, or even hardware. This latter is conditioned by designing radiofrequency ultra-low power sensing nodes and the microelectronics industry is once more highly solicited. To deal with this constraint, RF sensing nodes designers are pushed to go on toward deep sub-micrometer devices where the downscaling of transistors size becomes inescapable. Nonetheless, the utilization of such devices becomes critical especially when RF circuit design is accounted for. Consequently, it is required to master the behavior of these emergent transistors over broadband frequency spectrum.[2]

The most efficient method enabling the evaluation of transistors RF performance remains the estimation of the RF Figures of Merits (FoM), such as, the cutoff frequency f_T and the maximum oscillation frequency f_{max}. The deterioration of high frequency characteristics of advanced MOSFET devices is tied to the mentioned frequencies and it is issued from 2 constraints: first the impact of the series resistances (R_g, R_d, and R_s), and second the decrease of the ratios C_{gs}/C_{gd} and g_m/g_{ds} as the gate length scales down.[3] To overcome this

degradation, it is required to predict the RF performance of the considered devices at the early stage of their development enabling thus the optimization of the targeted technological node. On the other hand, the phenomena so-called short-channel effects (SCE), is another problem encountered in such deep sub-micrometer devices. They degrade both DC and high frequency characteristics, leading to poor subthreshold characteristics, growing threshold voltage dependence on the gate length, hence incrementing the leakage current, the degradation of the early voltage, power gain, and maximum oscillation frequency. Fortunately, the swap from bulk Si MOSFETs to[4] Silicon-on-Insulator (SOI) MOSFETs, has considerably minimized the SCE by reducing the total parasitic junction capacitances between the transistor and the Si substrate, while improving the gate control over the channel.

Generally, the RF measurements of the aforementioned devices are carried out at the end of the technological node development; therefore, the optimization of the technology for high frequency application is not possible. Also, in such characterization, the transistors are embedded into coplanar RF pads consuming a large testing silicon area, thus, contributing to the increase of the development cost. Moreover, the broadband frequency characterization requires sophisticated measurement equipment handled by qualified experts. All these constraints are at the origin of a motivation to develop a precocious estimation of the RF transistor performance of a technological node only based on the first electrical outputs that are obtained from transistors connected to DC pads. In such manner the technological process could be accurately optimized achieving thus high efficient devices for RF applications with low development cost.

Through an accurate equivalent electrical circuit, firstly we describe how the f_T and f_{max} can be extracted versus gate length L_g using DC and low frequency measurements. Secondly, the transconductance g_m, conductance g_{ds}, parasitic gate resistance R_g, source and drain resistances R_d and R_s are extracted using DC method. Thirdly, the total input capacitance C_{gg} is extracted at low frequency up to 5 MHz at different bias points V_{gs} in saturation and its effect on RF FoM is analyzed. Finally, the validation with RF measurements performed on the same devices is demonstrated.

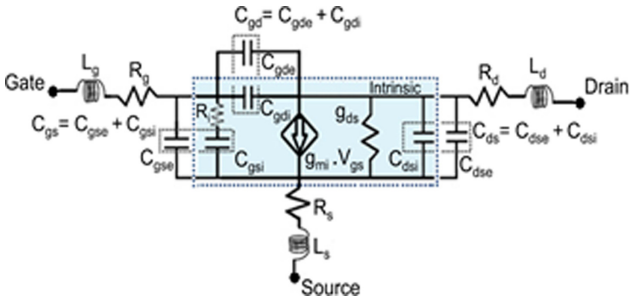

FIGURE 1 Small-signal equivalent circuit used for modeling the RF behavior of MOSFETs [Color figure can be viewed at wileyonlinelibrary.com]

2 | RF FIGURES OF MERIT

The Figure 1 shows the small-signal model of a MOSFET. The circuit can be divided in 2 parts in line with the physical meaning attributed to the elements. The extrinsic parasitic resistances and inductances (R_g, L_g), (R_s, L_s), and (R_d, L_d) of the transistor are related to the gate, source, and drain, respectively. Gate-to-source, gate-to-drain, and drain-to-source capacitances (C_{gs}, C_{gd}, and C_{ds}) are further subdivided into intrinsic and extrinsic parts, denoted by the indices "*i*" and "*e*", respectively.

In addition, the metal connections outside of (adjacent to) the active zone are modeled by the shunt admittances Y_{gp} and Y_{dp}. These admittances show a capacitive behavior, dominated by localized inter-metal capacitances, since the effect of the feeding lines is cancelled by the de-embedding method. As for the intrinsic part, enclosed by dashed rectangle (Figure 1), it depends on the bias conditions and the active region size.

Actually, MOSFET RF performance is evaluated through 2 major figures of merit, namely, f_T and f_{max}, standing for the current gain cutoff frequency and the maximum oscillation frequency, respectively. f_T is also defined as unity current gain frequency at which the short circuit current gain (H_{21}) becomes unity (0 dB); and at f_{max} the power gain reaches the unity (0 dB). Considering the MOSFET small-signal equivalent circuit shown in Figure 1, f_T and f_{max} can be expressed as in the following equations, respectively[5–7]:

$$f_T \approx \frac{g_m}{2\pi C_{gs}\left(1+\left(C_{gd}/C_{gs}\right)\right)+\left(R_s+R_d\right)\left(C_{gd}/\left(C_{gs}\left(g_m+g_{ds}\right)\right)\right)+g_{ds}} \approx \frac{g_m}{2\pi C_{gg}}, \tag{1}$$

$$f_{\max} \approx \frac{g_m}{4\pi C_{gs}\left(1+\left(C_{gd}/C_{gs}\right)\right)+\sqrt{g_{ds}\left(R_g+R_s\right)+\left(0.5C_{gd}/C_{gs}\left(R_s g_m+\left(C_{gd}/C_{gs}\right)\right)\right)}} \approx \frac{f_T}{2\sqrt{\left(R_g+R_s\right).g_{ds}+2.\pi.f_T R_g C_{gd}}}, \tag{2}$$

where C_{gg}, g_m, and g_{ds} are the total gate capacitance, gate transconductance, and output conductance, respectively. Regardless the impact of parasitic elements, f_T is approximated by $(g_m/2\pi C_{gg})$ with g_m being proportional to $N_f W_f/L_g$, while the total C_{gg} is directly related to $N_f W_f L_g$. Consequently, it is expected that f_T is independent on the transistor's width but increases with its length reduction ($f_T \sim 1/L_g^2$).

3 | TRANSISTOR DESCRIPTION

The current investigation relies on the partially depleted (PD) SOI MOSFET devices fabricated at TowerJazz foundry. These devices own a top silicon of 145 nm thick and a buried oxide (BOX) of 200 nm on top of a high-resistivity silicon substrate (8 kΩ cm) including a trap-rich layer. Those SOI substrates are manufactured by SOITEC and named enhanced integrity signal SOI substrates (eSI-SOI). The equivalent gate oxide thickness is 5 nm. The considered devices are designed under multifinger structure and embedded in CPW (Coplanar Waveguide) pads for RF characterization. The n-MOSFETs have gate length (L_g) from 240 to 320 nm, finger width (W_f) are 2 μm and number of parallel fingers (N_f) = 16. The obtained RF test structure is depicted in Figure 2. Aiming to withdraw the effect of CPW RF pads from the measured *S*-parameters of the investigated devices, the open structure shown in Figure 2 was used through de-embedding procedure.

To evaluate the area of RF and DC transistors test structures, we must consider a typical battery of transistors presenting various *W* and *L*. Indeed, carrying out characterization based on DC transistors will enable to reach a significant gain of area in the considered die. This area gain is in fact the area of a set of RF transistors with an associated open de-embedding structure for each. For a given dimension of *L* and *W*, this area is typically equal to 0.23 mm^2. Moreover, the test structures foot print gain increases when the battery of transistors contains a wide variety of dimensions.

In such manner, the development cost of a given process can be much reduced. Nonetheless, we can wonder how the

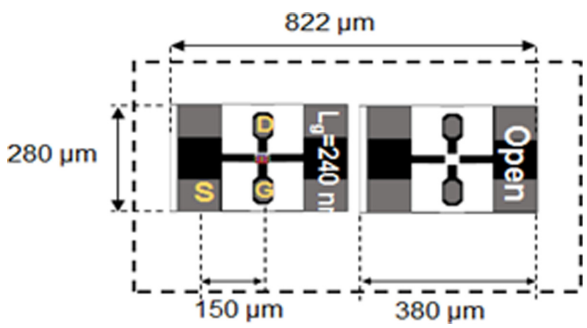

FIGURE 2 RF PD-SOI MOSFET with its associated de-embedding open structure [Color figure can be viewed at wileyonlinelibrary.com]

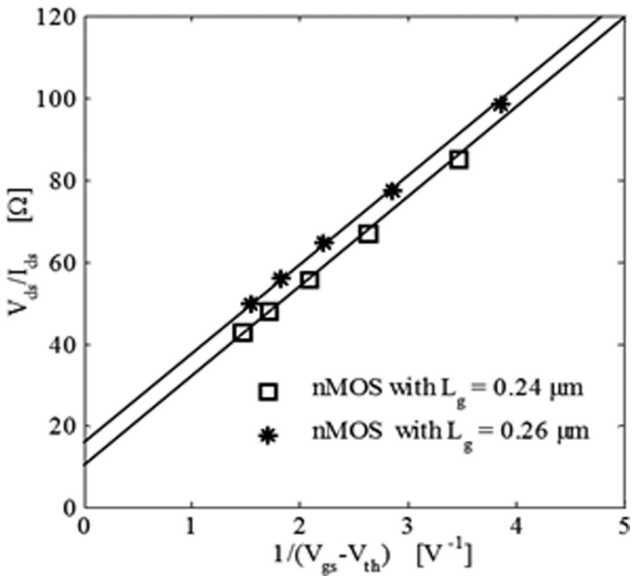

FIGURE 3 Extraction of PD-SOI MOSFET Rsd resistance using Bracale's method in DC mode

RF performance of a MOS technological node can be accurately predicted without designing specific and large RF structures and without investing to expensive RF characterization tools. In fact, the core of our work is to address this issue by proposing a new method enabling to determine RF performance only based on DC and low frequency characterization.

4 | PROPOSED EXTRACTION METHOD

The precocious prediction of RF performance is carried out through the calculation of f_T and f_{max}. However, the calculation of these parameters is conditioned by the determination of small-signal equivalent circuit elements (Figure 1). The efficiency of the proposed method lies on the fact that it enables the extraction of the aforementioned circuit elements only based on the DC and low frequency measurements. The determination of the circuit elements involved in f_T and f_{max} Equations 1 and 2 are exhibited in the following subsection.

4.1 | Series resistances

Many works have been reported on the extrinsic series resistances extraction for both DC and RF modes.[8–18] Unlike the DC methods that determine the total source-drain resistance (R_s+R_d),[8–10] the RF characterization methods allow the extraction of each series resistance value (R_g, R_d, R_s).[11–18]

Nevertheless, some DC methods found in the literature offer the possibility to determine R_s and R_d independently,[19,20] but R_g is still undetermined.

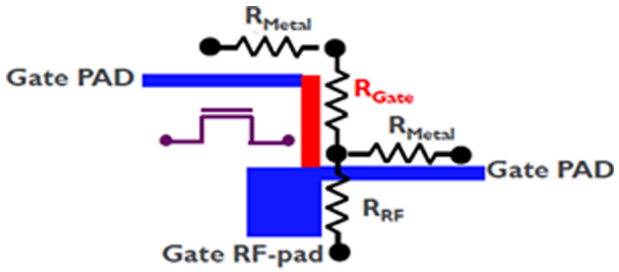

FIGURE 4 Electrical model of PD-SOI MOSFET transistor with double gate contacts [Color figure can be viewed at wileyonlinelibrary.com]

The source and drain resistances are extracted from I_{ds}–V_{ds} measurement at $V_{ds} = 20$ mV. The total resistance (R_s+R_d+1/g_{ds}) represents the I_{ds}–V_{ds} slope at various bias points of V_{gs}. At weak value of V_{ds}, with V_{gs} higher than the threshold voltage V_{th}, the channel resistance $(1/g_{ds})$ is neglected; therefore, the total resistance is reduced to (R_s+R_d). Also, by considering $R_s = R_d$, their expressions become $R_s = R_d = (R_s+R_d)/2$. Thus, by utilizing Bracale's method in DC mode,[17] the source and drain resistances can be calculated from the curve of I_{ds}–V_{ds} slopes plotted as function of $1/(V_{gs}–V_{th})$, as presented in Figure 3. Finally, the value of (R_s+R_d) is the intersection of the latter curves with I_{ds}–V_{ds} slopes axis (Figure 3).

As for the extraction of the gate resistance R_g, the transistor should have double gate DC contact connected at the beginning and the end of the gate fingers. Figure 4 illustrates the electrical model of this configuration. To simplify the extraction of the gate resistance value, a small voltage V_g is applied to the 2 gate contacts (Figure 4) in order to create a current I_g, consequently, $R_{GATE\text{-}TO\text{-}GATE}$ resistance can be deduced through Ohm's law to V_g/I_g. In addition, the metal resistances R_{Metal} are extracted by probing Gate RF-pad and Gate PAD (Figure 4) with the same method that $R_{GATE\text{-}TO\text{-}GATE}$ is computed. Thus, the gate resistance is calculated by the following expression:

$$R_g = R_{Gate} = R_{GATE\text{-}TO\text{-}GATE} - 2R_{Metal}. \quad (3)$$

Figure 5 plots the variation of R_{sd} (R_s+R_d) and R_g versus the gate length L_g. It can be noted the slight dependency of these resistances with L_g.

4.2 | Transconductances and output conductances

Thanks to pulsed IV equipment, the transistor can be correctly characterized in static mode since the problem of self-heating is avoided. The transconductance g_m and the output conductance g_{ds} were obtained from the derivative of the transfer and output characteristics, respectively. Actually, the reached values include the impact of the access resistances R_s and R_d, therefore, a correction should be made to accurately determine the intrinsic values of g_m and g_{ds}. To do so, the values of these latter are deduced using the formulae below:

$$g_m = |Y_{21}^{int} - Y_{12}^{int}|, \quad (4)$$

$$g_{ds} = Re\left(Y_{22}^{int}\right), \quad (5)$$

where Y_{21}^{int}, Y_{12}^{int}, and Y_{22}^{int} are the intrinsic admittance parameters, which have been deduced by transforming the intrinsic Z^{int} matrix, knowing that this latter is calculated by subtracting the above mentioned values of R_s and R_d from the Z-matrix characterizing the network of Figure 1.

Figure 6A shows the transconductance versus the gate voltage for different gate lengths and Figure 6B depicts the output conductance of PD-SOI MOSFET owning $W = 16 \times 2$ μm and $L_g = 0.26$ μm.

4.3 | Capacitances

Figure 7 shows the variation of total gate capacitance C_{gg} versus V_{gs}. Low frequency measurements of C_{gg} using LCR technique was performed with the B1500 semiconductor device analyzer instrument. Two important connections when measuring C_{gg} at low frequencies using LCR technique should be accounted for. The first is the high terminal (*Hi*) applied to the gate to ensure AC bias. The second is the low terminal (*Lo*) connected to the source to apply the DC bias. By performing these connections, C_{gg} including the capacitances of structure test is directly displayed on the analyzer.

It is important to note that the depicted data of C_{gg} in Figure 7 present the values after de-embedding operation. The de-embedding was performed by removing the pad parasitic capacitances obtained by open structure measurement.

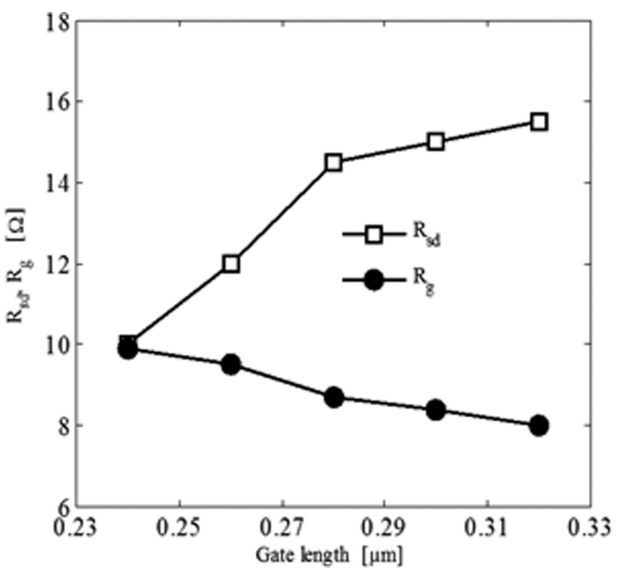

FIGURE 5 R_g, R_{sd} resistances versus gate length for PD-SOI MOSFET with $W = 16 \times 2$ μm

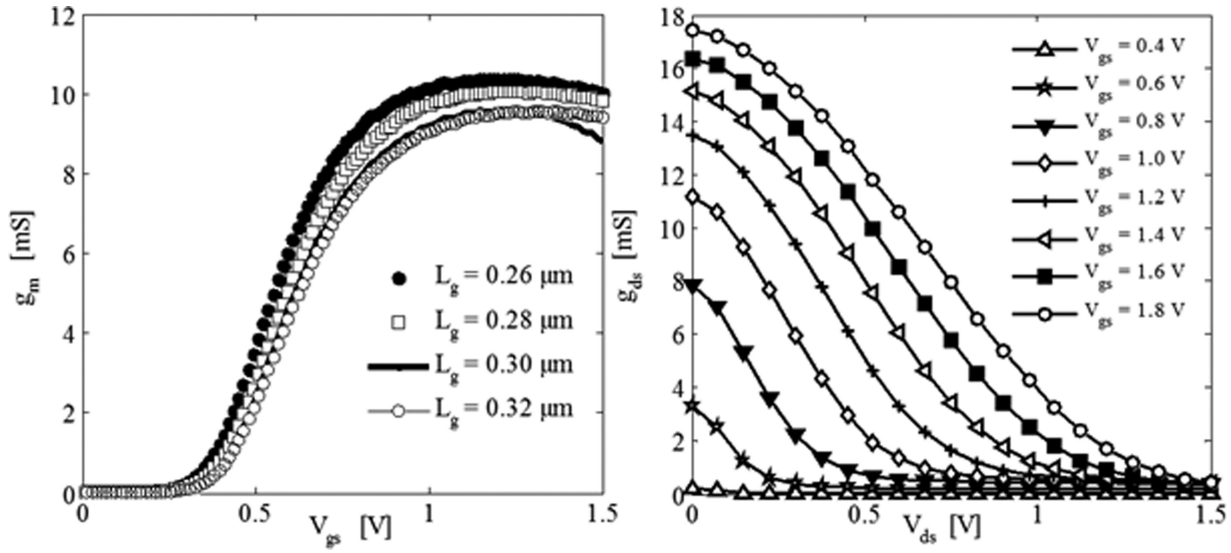

FIGURE 6 A, Transconductance (g_m) and B, output conductance (g_{ds}) of PD-SOI MOSFET A, at $V_{ds} = 1.2$ V and different gate lengths, B, with $L_g = 0.26$ µm at $V_{ds} = 1.2$ V

From the measured gate capacitance we can determine the transistor's effective channel length. It represents the physical length of the gate electrode (L_m) reduced by the overlap areas (ΔL_{eff}) which are because of the diffusion of the dopants from the source and drain regions under gate oxide; this channel length is given by the following expression[21]:

$$L_{eff} = L_m - \Delta L_{eff}, \tag{6}$$

where L_m represents mask channel length and ΔL_{eff} is the effective channel length reduction.

The value of ΔL_{eff} can be deduced based on the curves of Figure 8. Thereby, by plotting the variation of C_{gg} against L_g under the bias $V_{gs} \gg V_{th}$ and $V_{ds} = 0$ V, we can deduced the value of the extrinsic fringing capacitance $C_{fringing}$ from the intersection of the curve with the *Y*-axis, its value is around 4 fF (Figure 8, empty square). Then, by subtracting the value of $C_{fringing}$ from all points of C_{gg} measured with $V_{gs} \ll V_{th}$ and $V_{ds} = 0$ V, we obtained the curve of C_{gg} depicted in Figure 8, stars. By extrapolating this latter, the intercept with *X*-axis gives ΔL_{eff}. This is a negative value close to −0.05 µm, therefore, we have a total overlap length ΔL_{eff} of about 0.05 µm i.e. 0.025 µm on each side of the channel.

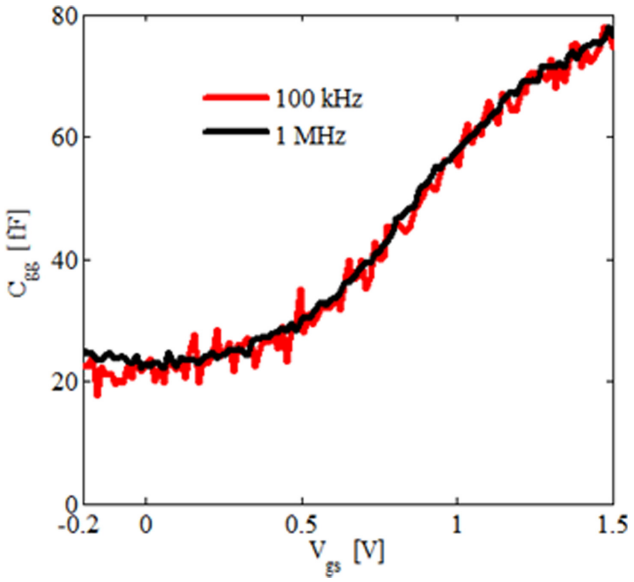

FIGURE 7 Capacitance C_{gg} measured using LCR technique after de-embedding with $W = 2 \times 16$ µm and $L_g = 0.26$ µm [Color figure can be viewed at wileyonlinelibrary.com]

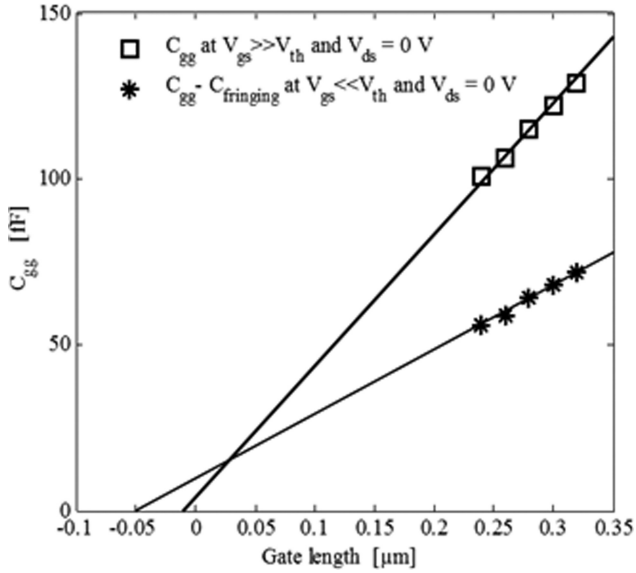

FIGURE 8 Total gate capacitance versus gate length PD-SOI MOSFET at different bias conditions for the extraction of fringing and overlap capacitances

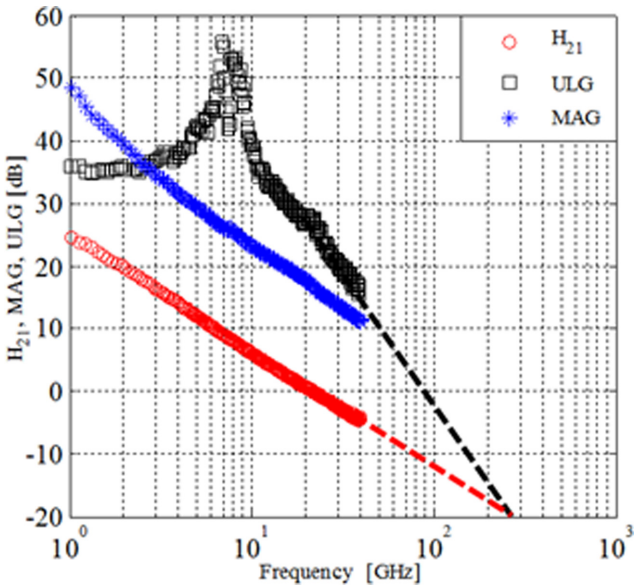

FIGURE 9 Extraction of f_T from |H21| and f_{max} from MAG and ULG after de-embedding from measured *S* parameters of PD-SOI MOSFET in saturation bias condition (V_{ds} = 1.2 V) and strong inversion (V_{gs} at maximum g_m) [Color figure can be viewed at wileyonlinelibrary.com]

5 | CUTTOFF FREQUENCY

Anritsu 37369A vector network analyzer connected to a cascade PM8 probe station was used to perform on-wafer *S*-parameter measurements up to 40 GHz under saturation (V_{ds} = 1 V) and cold (V_{ds} = 0 V) conditions, for different applied gate voltages (V_{gs}). The ground-signal-ground (GSG) pattern infinity probes were involved. By using a (LRM) calibration procedure, the *S*-parameters reference planes corresponding to the active part of the transistors can be defined. The CPW feed line pads were de-embedded thanks to a dedicated open structure implemented on the Si chips for each device. Based on the measured *S*-parameters, the current gain and the available power gain were extracted and exhibited in Figure 9. After that, by extrapolating the mentioned curves to the frequency axis the values of f_T and f_{max} were deduced.

Figure 10 presents the figures of merit (f_T, f_{max}) obtained using the proposed method based on DC and low frequency measurements, compared with those obtained from the RF method based on *S*-parameters. A very good agreement between both data is observed.

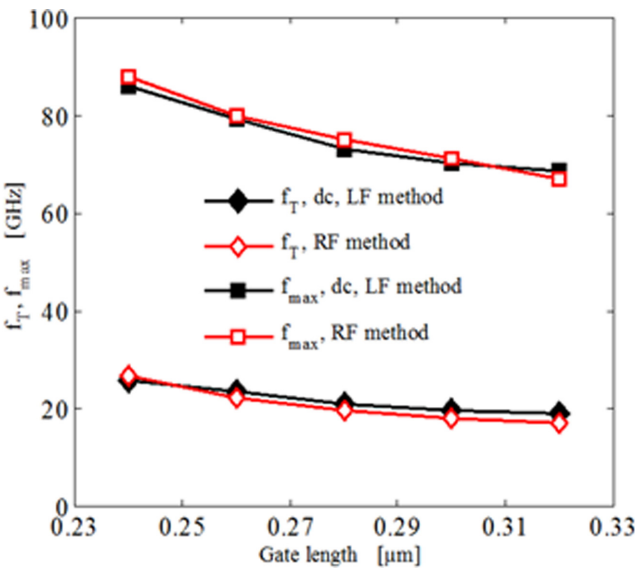

FIGURE 10 f_T and f_{max} versus gate length for $W = 16 \times 2$ µm obtained with low frequency method proposed in this work and by conventional RF method [Color figure can be viewed at wileyonlinelibrary.com]

6 | CONCLUSION

The present work deals with novel contribution on the extraction method of MOSFET RF figures of merit. An efficient extraction technique is proposed to accurately determine the RF figures of merit (f_T, f_{max}) of the MOSFET transistor only based on DC and low frequency measurements. Therefore, we do not need to rely on the design of specific RF CPW test structures that take up a large silicon area. In addition, with the proposed extraction method there is no need of sophisticated RF characterization equipment. The performance obtained from the proposed approach is well validated, this alternative solution, which can significantly reduce the development cost, is provided to foundries to precociously estimate the RF performance of new nodes at the early stage of their development. Thanks to this cheap extraction technique newly developed nodes can be optimized not only for digital but also for RF applications.

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Thermally enhanced GaN hybrid-IC power amplifier using embedded IC process in a copper sheet

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Abstract

This article introduces new packaging that improves the heat dissipation of RF power devices. Typically, power devices are mounted on a printed circuit board, in which the heat dissipation is made only through the bottom area of a device. The heat dissipation of the proposed structure is made through the bottom and side areas. As a result, proposed technology provides 30% improved heat dissipation in the RF GaN power amplifier. A copper sheet having a high thermal conductivity of around 400 W/mK is used as a core material to embed the power device. The measured results show that the drain efficiency of the fabricated X-band power amplifier (PA) improved by about 13% in the proposed package structure.

KEYWORDS

embedded IC, high-power amplifier, hybrid-IC, integrated passive devices, power packaging