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28 nm FDSOI analog and RF Figures of Merit at N_2 cryogenic temperatures

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ABSTRACT

This work presents a detailed characterization of 28 nm FDSOI CMOS process at cryogenic temperatures. Electrostatic, Analog and RF Figures of Merit (FoM) are studied. At liquid nitrogen temperatures, 30% to 200% enhancement of drain current, I_d, and maximum transconductance, g_{m_max}, values are demonstrated. Current gain cutoff frequency, f_T, increase by about 85 GHz is shown. Temperature behavior of analog and RF FoMs is discussed in terms of mobility and series resistance effect. This study suggests 28 nm FDSOI as a good contender for future read-out electronics operated at cryogenic temperatures (as e.g. around qubits or in space).

1. Introduction

Ultra-thin body with ultra-thin buried oxide (UTBB) technology used for fully-depleted silicon-on-insulator (FDSOI) transistors is widely recognized as a promising candidate to continue downscaling trends beyond 28 nm node low-power CMOS applications requested by ITRS [1]. This technology has demonstrated a fast trend toward RF-digital integration for such applications as, e.g. 5G and Internet of Things (IoT). It has already shown improved DC, analog and RF performances. It features lower variability [2], better electrostatic control and short channel effects [3–5]. Moreover, lower parasitic capacitances and resistances [6–8] in this technology provides good RF [9] and analogue [10] Figures of Merit (FoM). Multi-threshold voltage strategy capabilities and non-linearity improvement by featuring back-gate control scheme [11,12] constitute other superiorities compared to older SOI and bulk technologies. Lower self-heating effect with respect to "older generation" SOI technology is another important property of this process thanks to the use of thin BOX [13]. Nevertheless, even with thin BOX, the temperature rise in the channel due to self-heating can reach 87 K [14]. However, despite of stronger self-heating than in bulk, FDSOI outperforms bulk technology over a wide frequency range [14,15].

Our previous work [16] extended those studies and investigated the potential of this technology for future cryogenic applications, such as e.g. read-out circuitry of quantum bits ("qubits") by an integrated control system [17]. Nowadays high interest for quantum computing is motivated by a strong enhancement of computational power at deep cryogenic temperatures [18,19]. Understanding of physical behavior and potential perspectives of advanced technologies at cryogenic temperatures are of interest not only for quantum computers but also for space applications. Influence of cryogenic temperature on 28 nm bulk and FDSOI DC characteristics was previously addressed in [18,20], respectively with a main focus on EKV model.

This paper is an extended version of our previous work [16] incorporating additional experimental results and more detailed analysis. We investigate electrostatic, analog and RF parameters of FDSOI MOSFETs in a temperature range down to liquid nitrogen (77 K). Devices with gate lengths down to 25 nm are considered. Our focus is on the main MOSFET parameters and FoMs, such as threshold voltage (V_{th}), subthreshold slope (SS), drain induced barrier lowering (DIBL), transconductance (g_m), transconductance-to-drain current ratio (g_m/I_d), Early voltage (V_{EA}), intrinsic gain (A_v), and current gain cutoff frequency f_T.

2. Experimental details

Devices studied in this work originate from 28 FDSOI process by STMicroelectronics [21]. Studied n-type MOSFETs feature gate lengths L_g from 25 to 250 nm. The gate stack consists of a high-k gate dielectric on top of a SiON interfacial layer. Electrical thickness of the gate oxide is 1.2 nm. The channel is rotated by 45° from the < 1 0 0 > plane. Silicon film thickness is 7 nm. There is no intentional channel doping. The BOX thickness is 25 nm. The ground-plane under the BOX is well-type. More details about fabrication process can be found in [21]. Studied devices feature 60 parallel fingers of 2 μm width each, embedded in CPW (Coplanar Waveguide) pads in common-source configuration for RF characterization.

DC current-voltage measurements were performed with HP4145

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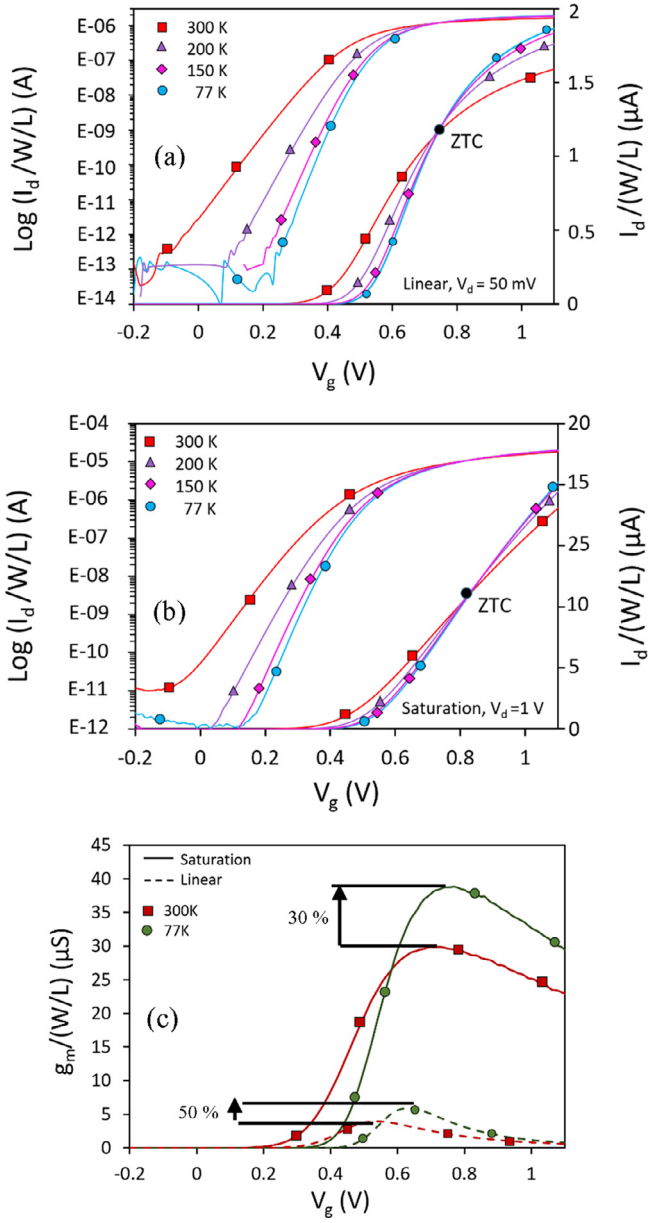

Fig. 1. (a) I_d-V_g in linear regime (V_d = 50 mV), (b) I_d-V_g in saturation regime (V_d = 1 V) and (c) g_m-V_g curves in linear and saturation regimes of 25 nm- long device at different ambient temperatures from 300 K down to 77 K. ZTC point in linear and saturation regimes is indicated in (a) and (b).

analyzer. Drain current versus gate voltage, I_d-V_g at various drain biases, and drain current versus drain voltage, I_d-V_d curves at different gate biases, were measured in order to extract electrostatic parameters and analog Figures of Merit (FoM). S-parameters measurements were performed using PNAX VNA 40 GHz. Measured S-parameters were converted to Y-parameters. Open structures were used for de-embedding. More details about characterization procedures can be found in [9]. Lake Shore cryogenic probe station was used to extend measurements temperature range from 300 K down to liquid nitrogen temperature of 77 K. The back-gate (i.e. ground-plane) is connected to the ground, V_{bg} = 0 V.

3. Results and discussion

3.1. Electrostatic parameters

Fig. 1 shows typical transfer drain current versus gate voltage, I_d-V_g, and transconductance versus gate voltage, g_m-V_g plots obtained in linear (with the drain bias, V_d, of 50 mV) and saturation (V_d = 1 V) regimes for various ambient temperatures for the 25 nm-long device. As shown in Fig. 1b, temperature reduction from 300 K to 77 K results in maximum g_m improvement by 50 and 30% in linear and saturation regimes, respectively.

Fig. 1(a) and (b) evidence the presence of the zero-temperature coefficient (ZTC) bias point in the studied devices at which drain current is constant when temperature varies from room to cryogenic temperature. This point is a result of mutual cancellation of the threshold voltage and mobility temperature dependencies at a certain gate voltage [22]. This point is used by designers to guarantee stable biasing in analog circuits such as e.g. amplifiers, over a large operating temperature range [23]. It is interesting to note that the ZTC point lies here close to the bias corresponding to maximum g_m and maximum g_m improvement with temperature lowering.

Fig. 2 shows threshold voltage (V_{th}) as a function of gate length at 300 K and 77 K (Fig. 2a) and as a function of temperature in devices with various gate lengths (Fig. 2b). Threshold voltage is extracted using g_m/I_d method [24] as the gate voltage which corresponds to the maximum of abs [$d(g_m/I_d)/dV_g$] versus gate voltage curve. This method was proven to be applicable both in linear and in saturation regimes [25], resistant against secondary effects [26], and to be efficient in a wide temperature range [27].

As shown in Fig. 2a, V_{th} is increasing by ~0.06 V with temperature, T, reduction from 300 K to 77 K. This is smaller than reported previously for 28 nm bulk technology [18]. Contrarily to bulk device, V_{th} variation with temperature in fully-depleted device is due to Fermi

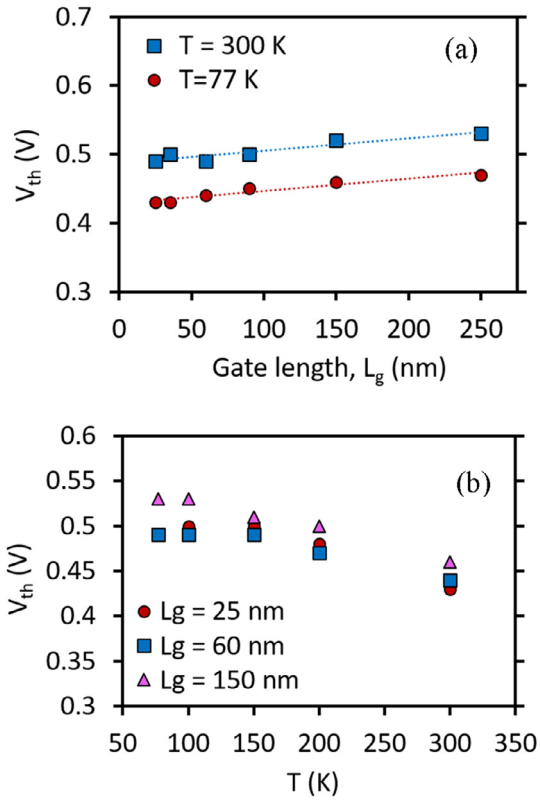

Fig. 2. Threshold voltage versus gate length (a) at 77 K and 300 K and versus temperature (b) for L_g = 25, 60 and 150 nm- long devices in linear regime V_d = 50 mV.

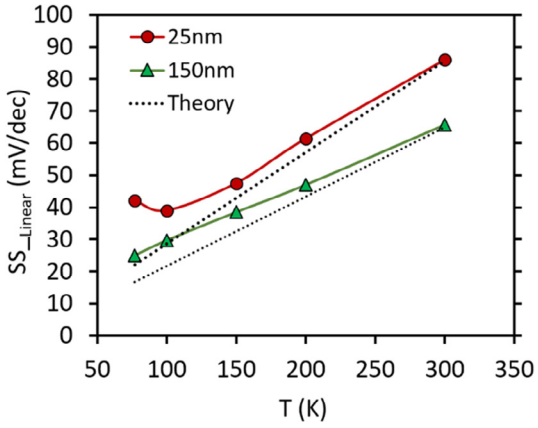

Fig. 3. Subthreshold slope (SS) in linear regime (V_d = 50 mV) versus temperature for short (L_g = 25 nm) and long (L_g = 150 nm) devices.

potential variation and is shown to be strongly attenuated in ultra-thin devices [28,29]. If one assumes the linear V_{th} variation with temperature, then $\Delta V_{th}/\Delta T$ is ~0.3 mV/K which is smaller than the numbers reported for high-temperature V_{th} variation in thin-film MOSFETs (~0.6 mV/K) [28,29]. However, from Fig. 2b, one can see that V_{th} versus T dependence deviates from linear behavior at lower temperatures tending to saturate at T below 100 K. In fact, at cryogenic temperatures quasi-Fermi potential variation with temperature slows down (tending to invariance) due to incomplete dopant ionization, resulting in a saturation of V_{th} (T) dependence.

Fig. 3 illustrates variation of subthreshold slope, SS, versus temperature evidencing SS improvement at low temperatures. This leads to improvement of the switching performances of the transistor at low temperature as illustrated by the reduction of the SS from ~87 mV/decade at 300 K to ~40 mV/decade at 77 K in 25 nm-long device. As reported in [30], this technology node can demonstrate a very low subthreshold swing of 7 mV/decade at 20 mK with a back-gate biasing of V_{bg} = 0 V. In [30] it is shown that by decreasing V_{bg} to −2.5 V, the subthreshold swing can further be reduced to SS = 2 mV/dec which is consistent with the displacement of mean channel position toward the front-gate interface which results in increasing the front-gate coupling capacitance [31].

The observed improvement is, however, not as strong as one could expect from the theoretical proportionality to T (dotted lines) at low V_d:

$$SS = n.\ k.\ T/q.\ (\ln 10) \quad (1)$$

where n, k and q are body factor, Boltzmann constant and electron charge, respectively.

Moreover, the improvement is lesser in shorter devices, as was already pointed out for the bulk counterparts in [18]. Attenuated SS improvement with temperature decrease could be related to the interface traps-related effect, as discussed in [18,20], and to the body factor-related effect which is stronger in shorter devices. Detailed discussion about SS behavior at cryogenic temperatures can be found in [18,20,30,32]. In analog/RF circuits, the SS is related to the maximum g_m/I_d figure of merit in saturation as discussed below.

Fig. 4 shows DIBL versus temperature for the devices with different gate lengths. It is extracted from the shift of V_g at a constant normalized drain current ($I_{d\_norm} = I_d/(W/L)$ of 10^{-7} A in linear and saturation regimes:

$$DIBL = \Delta V_g/(0.95\ V) \quad (2)$$

As can be seen in Fig. 4, with temperature reduction from 300 K to 77 K DIBL slightly improves (5–6 mV/V) almost independently on the gate length. To the first order, this appears consistent with the continuation of DIBL temperature dependence measured and modeled from 25 to 150 °C in [33].

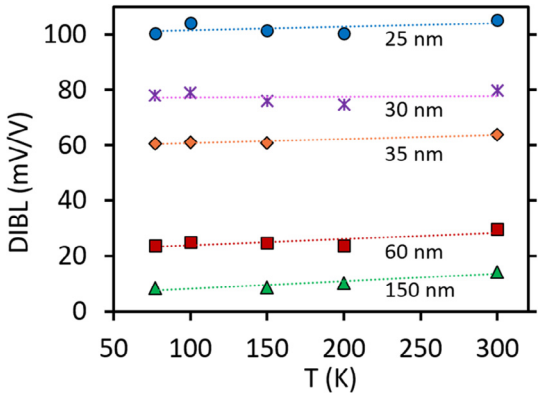

Fig. 4. DIBL as a function of temperature extracted at a constant normalized drain current $I_d/(W/L) = 10^{-7}$ A for the devices with different gate lengths (L_g = 25, 30, 35, 60 and 150 nm).

3.2. DC analog Figures of Merit

Analog performance in this work is evaluated through analysis of such device parameters as: transconductance, g_m, g_m/I_d ratio, normalized drain current $I_d/(W/L)$ taken at a constant g_m/I_d of 5 and 10 V^{-1}, Early voltage, V_{EA} and intrinsic gain, A_v. V_{EA} is extracted from I_d-V_d curve by I_d/g_d (with $g_d = dI_d/dV_d$). V_{EA} eliminates the g_d dependence on I_d which allows for fair comparison between different devices [34–36]. Then, intrinsic gain, A_v, as one of the main analog key-factors of any MOSFET can be calculated as:

$$A_v = g_m/g_d = (g_m/I_d)\ V_{EA} \quad (3)$$

The g_m/I_d versus normalized drain current $I_{d\text{-}norm} = I_d/(W/L)$ plot is a very useful representation to compare different devices at different temperatures. This is because of its independency on V_{th}, as well as, to the 1st order, on gate length L_g [34,35].

Fig. 5 shows g_m/I_d as a function of normalized I_d extracted at 300 K and 77 K for 25 nm and 90 nm-long devices. One can see the g_m/I_d maximum improvement by cooling the device down to 77 K, which is directly linked to SS decrease. Furthermore, normalized drain current taken at a fixed g_m/I_d enhances both in moderate and strong inversion regimes, usually linked to mobility increase as expected at low T.

As mentioned above, comparison of I_{d_norm} extracted at a fixed g_m/I_d allows removing the effect of V_{th} shift with temperature as previously explained in [34,35]. I_{d_norm} taken at g_m/I_d = 10 V^{-1} and 5 V^{-1} which correspond to gate biases of ~V_{th} + 0.2 and +0.4 V, respectively, for various gate lengths for 77 K and 300 K (in linear and saturation) are shown in Fig. 6. I_{d_norm} improvement, i.e. $I_{d\_norm\_77K}/I_{d\_norm\_300K}$ ratio, as a function of the gate length is shown on the same graph. One can

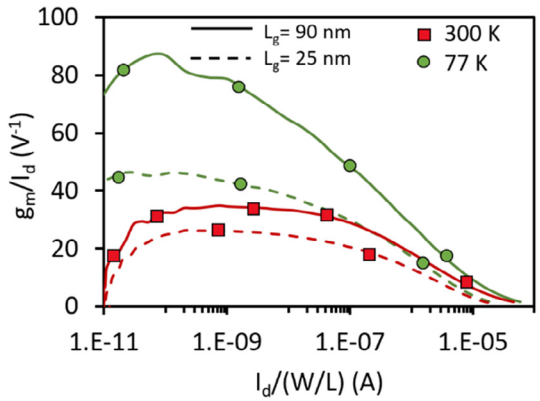

Fig. 5. g_m/I_d as a function of normalized drain current $I_d/(W/L)$ at 77 K and 300 K. L_g = 25 and 90 nm. V_d = 1 V.

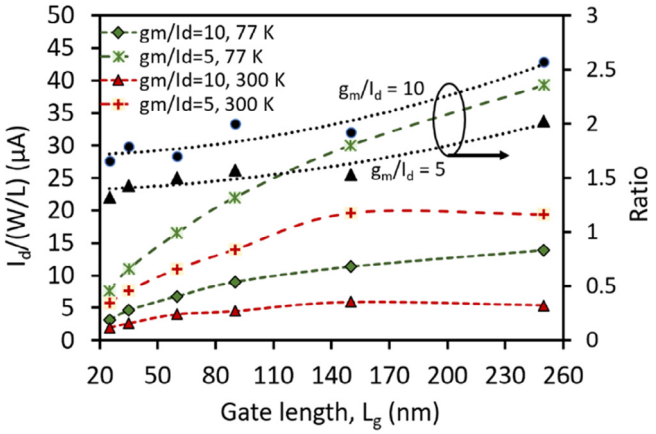

Fig. 6. Normalized I_d taken at $g_m/I_d = 10\,V^{-1}$ and $5\,V^{-1}$ as a function of gate length, L_g at 77 K and 300 K. $I_{d\_norm\_77K}/I_{d\_norm\_300K}$ ratios are shown by dotted lines.

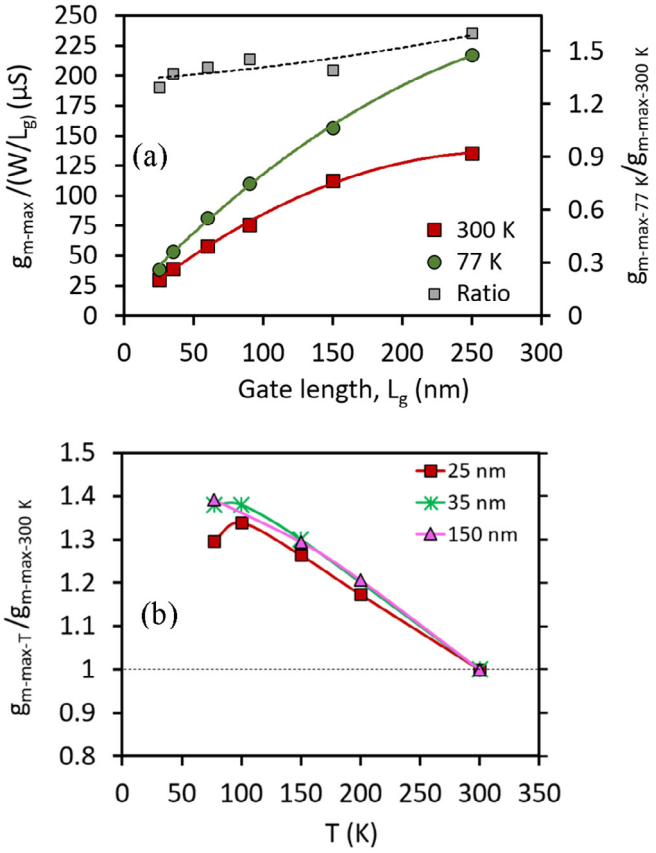

Fig. 7. (a) Normalized DC g_{m_max} in saturation regime (V_d = 1 V) as a function of gate length, L_g at 77 K and 300 K. Their ratio is shown in dotted line (square symbols); (b) maximum g_m at different temperatures normalized to maximum g_m at 300 K for 3 devices with L_g = 25, 35 and 150 nm.

notice that the improvement is smaller in shorter devices.

Fig. 7a shows maximum normalized g_m versus gate length for two temperatures (77 K and 300 K). As can be seen in this figure, the improvement of $g_{m\text{-}max}$ by temperature lowering is smaller in shorter devices (similarly to improvement of I_{d_norm} extracted at a constant g_m/I_d). Moreover, from the temperature dependence of g_{m_max} improvement, shown in Fig. 7b, one can see that in the case of shorter devices, $g_{m\text{-}max}$ improvement with temperature is not monotonic, exhibiting a maximum at 100 K.

From Figs. 6 and 7, one can see that improvement of g_{m_max} and

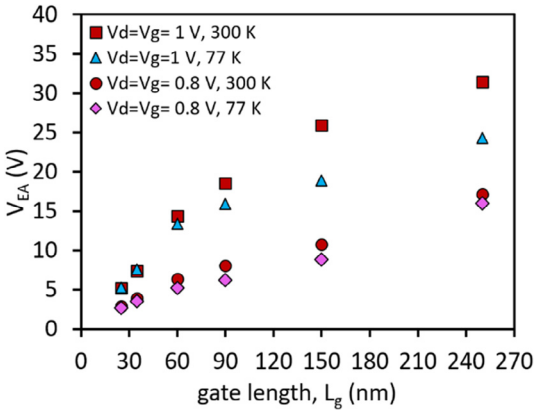

Fig. 8. Early voltage in saturation regime as a function of gate length, L_g from 25 nm up to 250 nm at 77 K and 300 K extracted at a fixed $V_g = V_d$ of 0.8 and 1 V.

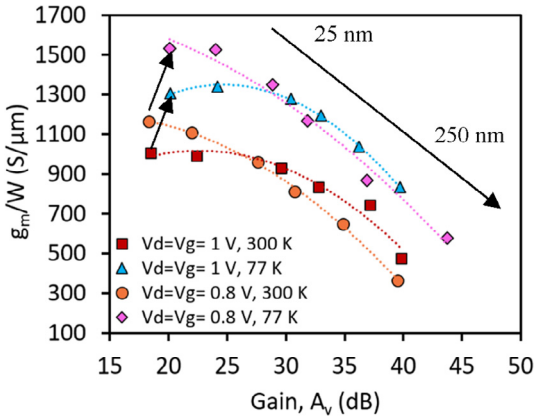

Fig. 9. Normalized transconductance (g_m/W) versus intrinsic gain (A_v) taken at a fixed $V_g = V_d$ of 1 V and 0.8 V for 77 K and 300 K for different L_g = 25, 35, 60, 90, 150 and 250 nm.

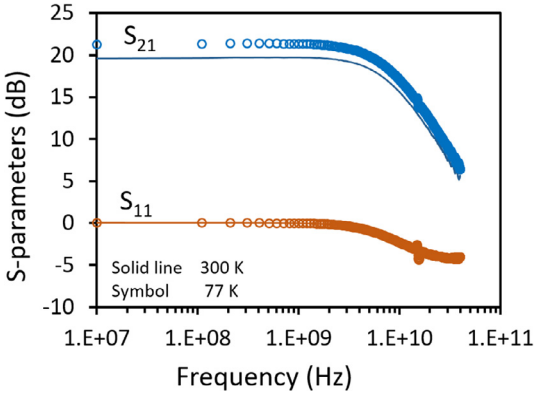

Fig. 10. Measured S-parameters (S_{21} and S_{11}) of 25 nm gate length transistor at 300 K (solid-line) and 77 K (symbols) in saturation regime (V_d = 1 V) and at V_g corresponding to maximum g_m .

I_{d_norm} at cryogenic temperatures is 30 to 200% depending on the gate length and regime of operation. These values are comparable with (and even higher than) the observations for the 28 nm bulk technology [18]. Next to that, reduction of the g_{m_max} and I_{d_norm} improvement in shorter devices is evident. There are two reasons for the reduced improvement of g_{m_max} and I_{d_norm} in short channels. Firstly, effect of series resistance, R_{sd}, is stronger. This reason is supported by stronger improvement observed for the regimes at which the impact of series resistance is

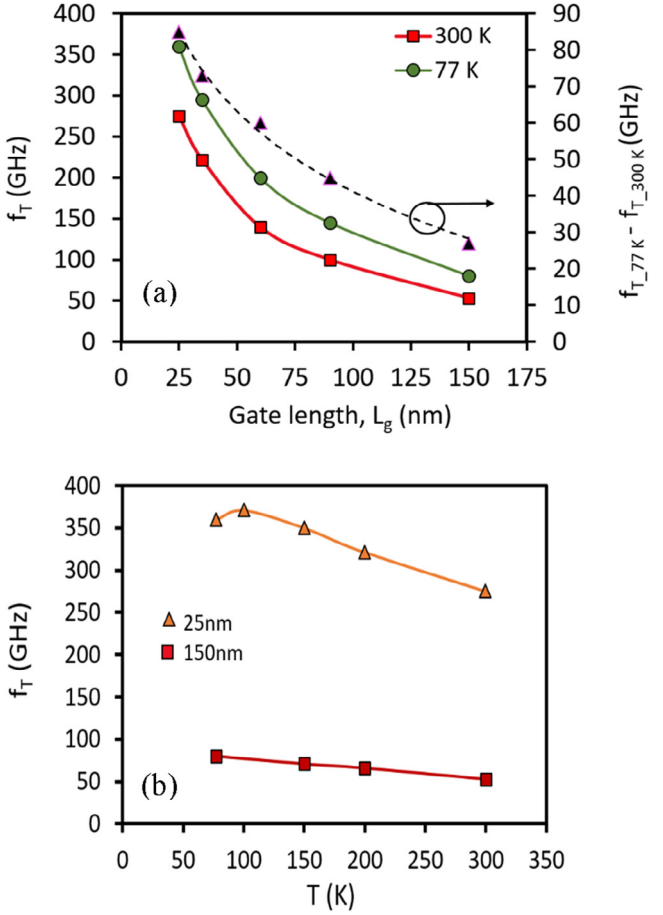

Fig. 11. f_T as a function of (a) L_g at 77 K and 300 K and (b) temperature for short (L_g = 25 nm) and long (150 nm) devices.

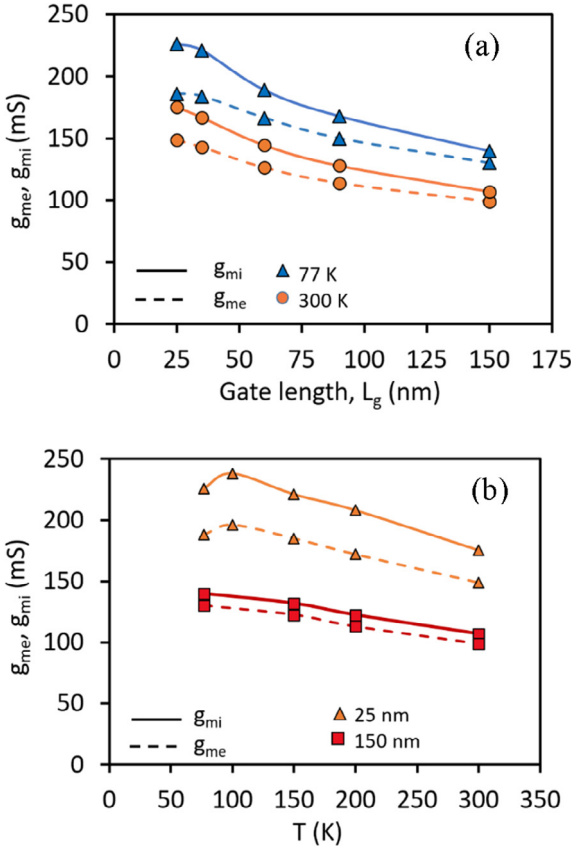

Fig. 12. RF g_{mi} and g_{me} as a function of (a) gate length, L_g for 77 K and 300 K and (b) temperature, T for L_g = 25 nm and 150 nm as a short and long device, respectively.

smaller, as e.g. (1) I_{d_norm} taken at $g_m/I_d = 10\,V^{-1}$ w.r.t that taken at $5\,V^{-1}$ and (2) g_{m_max} extracted in linear with respect to saturation regime (Fig. 1b). Secondly, mobility, μ, improvement in short channel devices is smaller than in long ones, as reported previously [37]. Indeed, short-channel mobility is strongly affected by the presence of defects in the extensions and source/drain regions. Resulting mobility temperature dependence is defined through the balance between two mechanisms: Coulomb scattering on the defects (with μ_{Coul} reduction with T lowering) and phonon scattering (with μ_{ph} increase with T lowering). This appears in the improvement rate of $g_{m\text{-}max}$, which first slows down with temperature lowering and then drops exhibiting a maximum at ~100 K (as shown in Fig. 7b).

Fig. 8 shows Early Voltage (V_{EA}) as a function of gate length for 300 K and 77 K taken at saturation $V_g = V_d = 0.8$ and 1 V. Some reduction of V_{EA} is observed at 77 K, particularly visible in longer devices at a higher $V_g = V_d$. One of the reasons of V_{EA} reduction at 77 K is lower gate voltage overdrive (GVO = V_g-V_{th}). Indeed, V_{th} increases at lower temperatures, and therefore, when extraction is done at a constant V_g (as in real applications), GVO is lower and thus V_{EA} is naturally lower.

Fig. 9 shows g_m-A_v metric widely used for comparative assessment of analog FoM of different technologies or at different temperatures (or regimes of operation). One can see that temperature lowering results in simultaneous g_m and A_v improvements.

3.3. RF FoMs

In this section, we discuss RF FoM extracted from S-parameters measured in a frequency range from 10 MHz up to 40 GHz at different temperatures. The measured reflection (S_{11}) and transmission (S_{21}) coefficients at 300 K and 77 K are shown in Fig. 10. As can be seen in this figure, temperature lowering results in S_{21} increase which is translated into higher power gain. S_{11} stays unaffected by temperature reduction down to 77 K which correspond to stable input impedance. The RF transconductance (g_m) and current gain cutoff frequency (f_T) are extracted from de-embedded S-parameters in which the parasitic effects of the connection pads are eliminated by open-pad de-embedding method [9,36].

Fig. 11a shows f_T as one of the main RF FoMs versus gate length at 77 K and 300 K. f_T is obtained from extrapolation of H_{21} parameter to 0 dB in saturation (V_d = 1 V) and at V_g that corresponds to maximum g_m [9]. This advanced technology node is known to feature very high f_T reaching several hundreds of GHz at room temperature [38]. Temperature reduction from 300 K to 77 K results in strong f_T improvement (due to μ and, hence, g_m improvement). This increase ($\Delta f_T = f_{T\_77K} - f_{T\_300K}$) becomes particularly significant in shorter devices (Fig. 11a). f_T temperature dependence for 25 nm and 150 nm devices is illustrated in Fig. 11b. In the shortest device (25 nm), f_T temperature dependence exhibits a maximum at 100 K (similarly to DC g_{m_max} improvement discussed above).

By converting S-parameters to Y-parameters, the RF value of g_m can be extracted from [9]:

$$g_m = |Y_{21} - Y_{12}| \tag{4}$$

The same trends are observed in "extrinsic", g_{me}, (i.e. including series resistance, R_{sd}), and "intrinsic", g_{mi}, (i.e. without R_{sd} effect) values extracted from RF measurements [9] which are shown in Fig. 12.

The same trends are observed in g_{me}, g_{mi} and DC g_m temperature dependences, featuring a maximum at ~100 K (see Figs. 7b and 12b). Thus, we can suggest that the main reason of such trend is related to the mobility temperature dependence μ(T) as discussed above. It can be

also seen in Fig. 12 that due to higher current in shorter devices, series resistance effect is stronger than that in longer device which results in larger difference between g_{me} and g_{mi} in the former than in the latter. The same logic can be applied when one compares low temperature case (higher current) with room temperature case (lower current). Indeed, stronger difference between g_{me} and g_{mi} is observed at 77 K w.r.t room temperature.

4. Conclusion

Potential of 28 nm FDSOI MOSFETs for future cryogenic applications has been assessed in details. Electrostatic, analog and RF Figures of Merit have been considered. Threshold voltage was shown to be more stable versus temperature than in the bulk counterpart. It was demonstrated that V_{th} versus T dependence deviates from linear behavior at lower temperatures tending to saturate at T below 100 K due to incomplete dopant ionization. SS improvement with temperature lowering was shown to be degraded especially in shorter devices due to the interface traps and body factor- related effects. Temperature reduction down to 77 K has been shown to result in improvements of g_{m_max} and I_d (by 30–200%), f_T (by ~85 GHz) as well as slightly (by a few dB) improved intrinsic gain. The presented results suggest 28 nm FDSOI technology as a promising candidate for cryogenic circuits implementation, such as e.g. control block and readout circuits companion chips (operated at 77 K) for quantum computing (qubits being operated at 20 mK).

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