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Enhanced ultraviolet photoresponse in a graphene-gated ultra-thin Si-based photodiode

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Abstract

We present an ultra-thin lateral SOI PIN photodiode with transferred monolayer graphene as the transparent gate, to provide enhanced ultraviolet (UV) performance and mechanical flexibility beyond standard Si-based devices. The device dark current shows intact characteristics after the post-CMOS thinning and graphene transfer processing steps. The device responsivity presents high potential in UV and visible wavelength detections (i.e. within the 200–900 nm range) under monochromatic light illumination. A maximum responsivity of 0.18 A W^{-1} has been experimentally achieved at 390 nm wavelength and validated by simulation, for a diode with intrinsic length L_i of 20 μm. Additionally, the ~5 μm-thick device chip with direct board assembly paves the way towards the development of hybrid flexible electronics.

Keywords: graphene, transparent gate, PIN photodiode, silicon-on-insulator, ultra thin, backside illumination, ultraviolet detection

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, the co-integration of graphene in electronics and photonics has attracted substantial attention because of its unique optical, electronic, mechanical, and chemical properties including a transmittance exceeding 95% within 200–900 nm wavelength range [1], a carrier mobility superior to 100 000 cm^2 V^{-1} s^{-1} [2], a high flexibility and robustness [3], and a high environmental stability [4, 5]. Thanks to the development of graphene manufacturing methods (particularly the chemical vapor deposition (CVD) method [6, 7]) and the recent progress in transfer techniques (e.g. wet transfer [8, 9]), graphene has demonstrated its great potential for the realization of optical sensors [1, 10].

Silicon is a widely-used semiconductor material for ultraviolet (UV) and visible (VS) photodetectors, thanks to its suitable bandgap, low-density surface states, high reliability, mature manufacturing (i.e. in CMOS technology [11, 12]) and high-speed operation. Therefore, the Si-based diode is often used as an optical sensor thanks to its unparalleled industrial advantages. However, in the UV region, Si-based photodetectors face the major hurdles of low responsivity (typically, $<$0.10 A W^{-1} for wavelength $\lambda < 400$ nm) due to a high reflection coefficient and a shallow penetration depth (e.g. 100 nm at $\lambda = 400$ nm) of UV light in silicon, as well as the significant carrier recombination close to the surface, hence limiting the performance. Thin-film lateral PIN photodiodes have been developed in silicon-on-insulator (SOI) CMOS

technology to take up these challenges [12, 13], including very high speed or frequency performance [13]. Initial simulations indicated that effective light absorption within the UV and VS ranges could be improved in the SOI-based photodiode by using a multilayer stack and an anti-reflection coating (ARC) [14]. The responsivity could thus reach a maximum of 0.18 A W^{-1} under the fully-depleted condition when operated in photoconductive mode (i.e. without amplification or photomultiplication). To the best of our knowledge, the highest experimental responsivity achieved by such a sensor in standard SOI CMOS technology is 0.10 A W^{-1} at 400 nm wavelength with an 80 nm-thick Si film [14]. On the other hand, it has been found that the optical absorption wavelength can be modulated (within the 450–900 nm range) by placing reflectors below the photodiodes [15]. To overcome previous experimental limitations, this work presents a graphene-gated ultra-thin Si-based photodiode experimentally validated and fabricated via the following major steps: (1) thinning from the backside of the full Si substrate of a processed SOI CMOS die by xenon difluoride (XeF_2), (2) wet transfer of a monolayer graphene sheet on the backside SiO_2 layer of the released die (~5 μm-thick), (3) chip assembly on a circuit board and (4) wire bonding. The graphene layer is chosen as the transparent gate, to take advantage of its unique combination of excellent conductivity and transparency in the whole UV to VS spectrum, well beyond transparent conductive oxides. The backside XeF_2 thinning and the graphene transfer onto the SOI buried oxide (or BOX) are used to present a flat surface for optimal graphene adhesion and to allow back illumination avoiding any unwanted optical reflection or absorption in the device front multilayer stack (e.g. CMOS polysilicon layer or metal interconnects). The UV responsivity achieved in this graphene-gated Si photodiode has been optimized, comparable not only with graphene/bulk Si detector but also with other reported state-of-the-art GaN and SiC-based photodetectors, e.g. 0.09 A W^{-1} at 254 nm and 0.12 A W^{-1} at 365 nm in the Si-based, 0.14 A W^{-1} at 350 nm in the GaN-based, and 0.20 A W^{-1} at 310 nm in the SiC-based photodetectors [16–19]. Moreover, the direct assembly of the ultra-thin (~5 μm-thick) device is realized on a printed circuit board (PCB) in this work for test purpose, but it could be transferred onto a flexible substrate. This work demonstrates relevant findings for the development of flexible hybrid electronic devices which is of great interest for the scientific community but still challenging to implement into practical applications [20–25].

2. Experiment

2.1. Post CMOS process

The device samples used in this work were primarily manufactured in a commercial 1 μm SOI CMOS technology, with the monolithic integration of PIN diodes, MOS transistors, micro-hotplate and control circuit, as a stable, multi-sensing system for harsh-environment industrial applications including long duration exposure to light [12], flow [26], and humidity [27]. Figure 1 depicts the processing steps to fabricate the graphene-gated ultra-thin Si-based photodetector from the CMOS PIN diode, that is, the Si substrate etching, graphene transfer and chip-on-board assembly. First, a dry Si isotropic etching with XeF_2 ($2XeF_2 + Si \rightarrow 2Xe + SiF_4$) is carried out to release the microelectromechanical system (MEMS) device [28]. The device sample (with a size of 1.8 mm × 1.8 mm) is placed upside down on the surface of a Gel-Pak/quartz support which is used as carrier for ensuring safe device holding and improving the die rigidity (see figure 1(a)). As depicted in figure 1(b), the released device sample has a final thickness of about 5 μm with a multilayer stack comprising Si_3N_4 (560 nm-thick, as a passivation layer), SiO_2 (2.5 μm-thick, to form the membrane where the photodiode is embedded), polysilicon (300 nm-thick, as implantation mask), SiO_2 (25 nm-thick, gate dielectric for the MOS transistor), Si (250 nm-thick, the active layer), and SiO_2 (1.0 μm-thick, BOX). The BOX is used as an etch-stop material (SiO_2 selectivity of >1000:1 with XeF_2 [28]) in this Si thinning step. Next, a single layer of graphene grown by CVD on Cu foil is transferred onto the BOX backside of the thinned die by the poly(methyl methacrylate) (PMMA)-assisted wet transfer technique [9, 29], as depicted in figure 1(a). Acetic acid is thereafter used to remove PMMA to keep the Gel-Pak intact. Finally, Epo-Tek, i.e. a viscous, liquid, conductive glue [30], is used to fix the sample over a 1.4 mm-diameter hole perforated in the PCB (i.e. chip-on-board assembly), followed by a low-temperature annealing (100 °C) for the curing, Gel-Pak removal and wire bonding, overall to facilitate back-illumination measurements using conventional optoelectronic set-up. The intrinsic length (L_i) of the lateral PIN diode under test is 20 μm, with 2 finger diodes interdigitated in parallel over a total active area of 52 μm × 60 μm [15]. In addition, the released ~5 μm-thick die features mechanical flexibility beyond standard Si-based devices [20, 25].

2.2. Graphene characterization

Besides transferring graphene on the CMOS thinned die, a graphene sheet of ~3.9 mm × 5.5 mm has also been transferred on a 100 nm-thick SiO_2/Si substrate for quality assessment purposes. Graphene has been characterized using scanning electron microscopy (Zeiss Gemini SEM Ultra-55), Raman spectroscopy (LabRAM HR equipment, Horiba scientific) and electrical measurements (see figure 2(a)). The latter shows that the sheet resistance is about 2.1 kΩ/sq (see current–voltage curves in figure 2(b)). This value, which is comparable with previous reports in the literature, indicates a good quality graphene [8]. Raman spectra are presented in figures 2(c) and (d), using a green laser illumination (with excitation energy of 2.41 eV, power level below 1 mW to avoid local heating). Based on the relative magnitude between the G (centered at ~1580 cm^{-1}) and 2D (centered at ~2700 cm^{-1}) bands, monolayer graphene on 100 nm-thick SiO_2/Si is clearly identified in figure 2(c) with the peak intensity (I) ratio I_{2D}/I_G over 2 [31, 32]. The I_{2D}/I_G ratio is inferior to 1 shown in figure 2(d) for graphene transferred on the BOX of the thinned SOI CMOS die, which is usually indicative of the multilayer graphene presence. However, the unusual Raman signature in figure 2(d) is attributed to an effect of the non-conventional substrate underneath [33], i.e. the front multilayer stack of the released

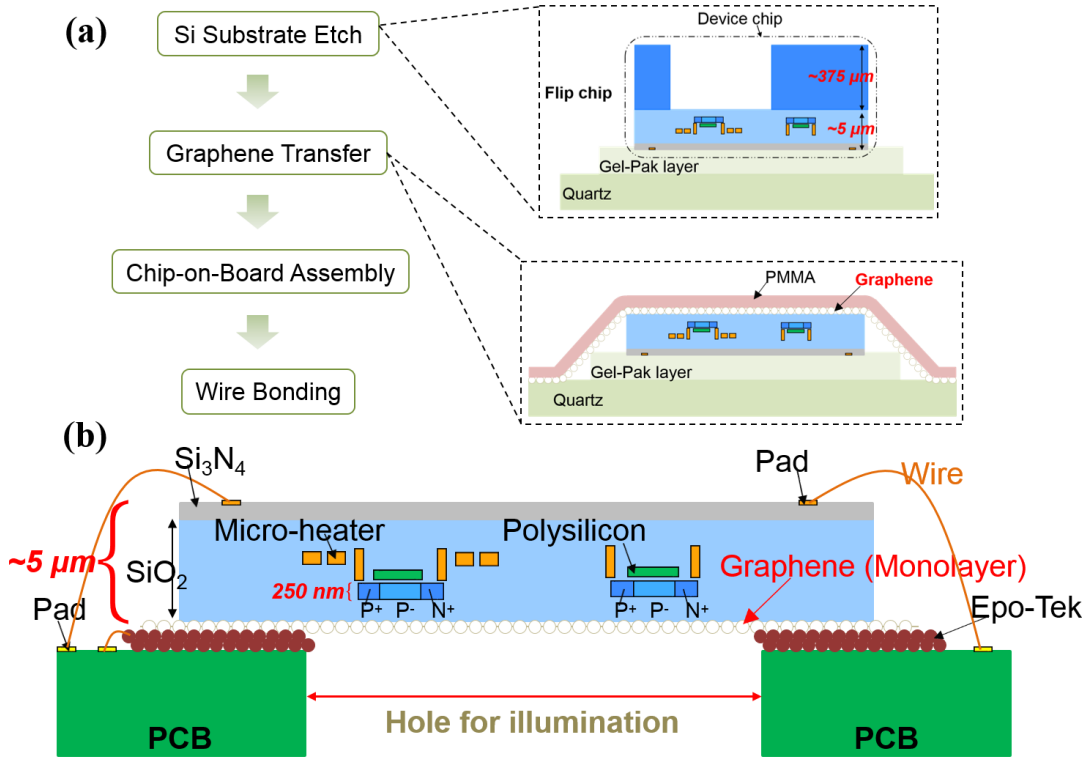

Figure 1. (a) Process sequence illustration; (b) chip-on-board schematic for the ultra-thin die with graphene back gate (not to scale).

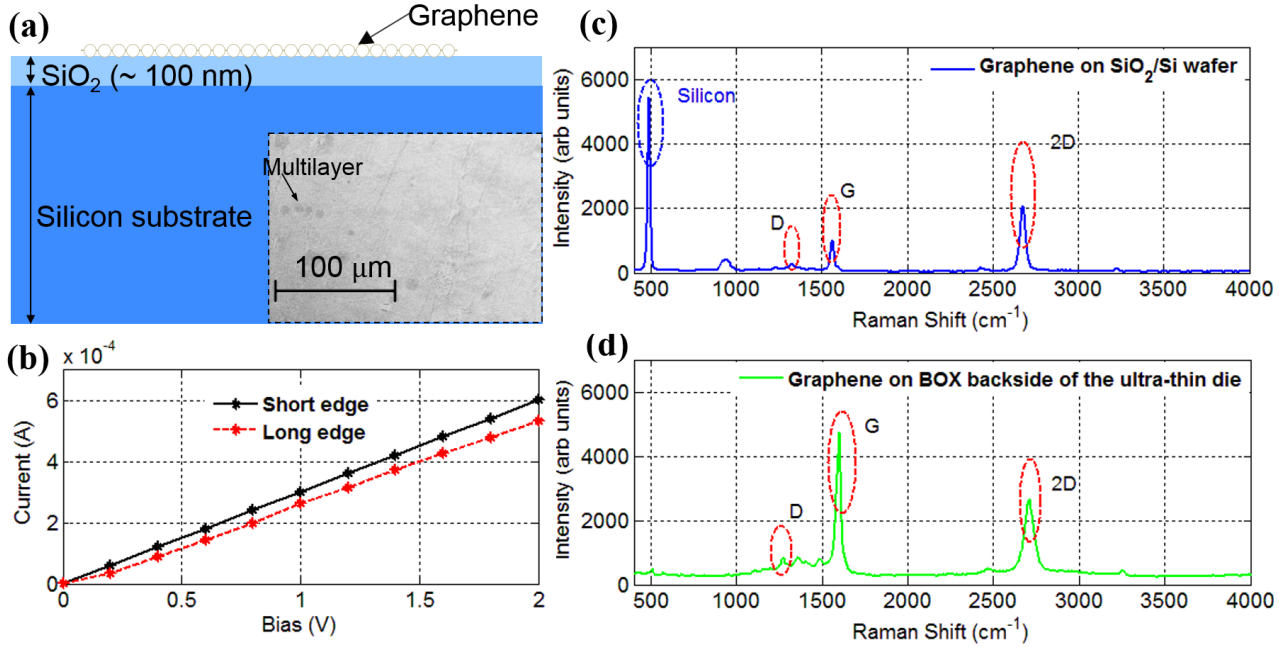

Figure 2. (a) Illustration of graphene transferred on SiO_2/Si wafer, the inset is a SEM image; (b) current–voltage curves of graphene sheet (~3.9 mm × 5.5 mm); (c), (d) Raman spectra of graphene on the SiO_2/Si wafer and on the BOX backside of the ultra-thin die, respectively.

die. We then observe the presence of small multilayer regions which represent less than 1% of the surface area [7], as shown in SEM image of inset to figure 2(a). The very small intensity of the disorder-induced D band (centered at ~1350 cm^{-1}) in figures 2(c) and (d) demonstrates that high-quality graphene has been produced during the CVD process and the wet transfer process resulted in little or no damage [9, 31].

3. Results and discussion

3.1. Electrical control of graphene gate

Electrical characteristics of the ultra-thin photodiode with graphene transparent gate electrode are first investigated, before complete PCB assembly. A blue LED (peak at 480 nm, with light power density on the order of 8×10^{-5} W cm^{-2}) is used

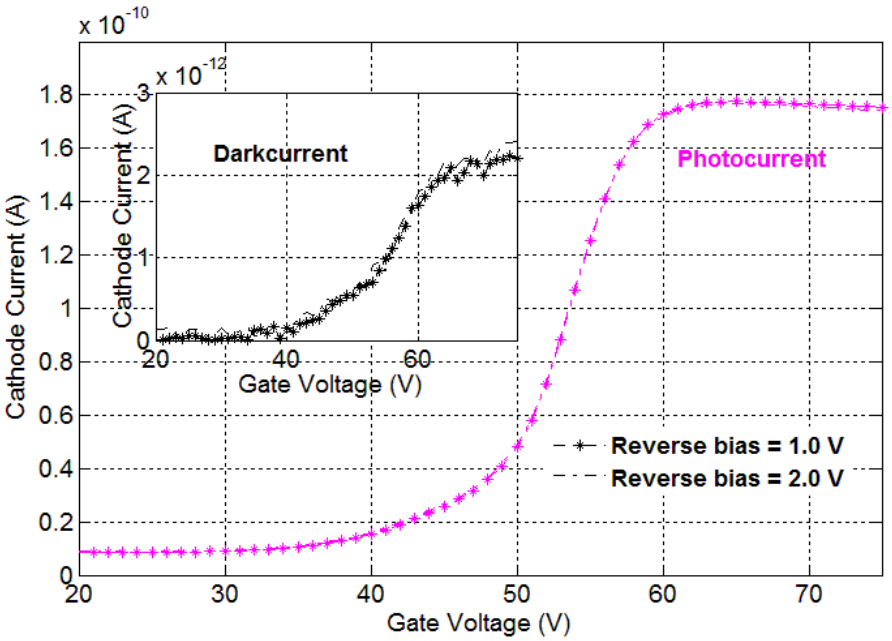

Figure 3. Device output photocurrent (main curve) and dark current (inset) versus gate voltage, in the graphene-gated ultra-thin lateral PIN diode ($L_i = 20$ μm), at reverse biases of 1.0 and 2.0 V, under topside illumination at 480 nm wavelength ($P_{in} = \sim 8 \times 10^{-5}$ W cm^{-2}).

as the light source for the top illumination, compatible with measurements on a Karl Suss PA200 probe station. Metal surface of PA200 chuck is taken as a bottom metal mirror to compare with the aluminum bottom reflector used in [15], where one 1.0 μm-thick Al backside layer was deposited as the back gate and bottom reflector.

Figure 3 presents the dark and illuminated device current–voltage curves under reverse biases of 1.0 and 2.0 V, respectively, where the back-gate bias is varied from 20 to 75 V to modulate the depletion condition in the diode intrinsic region. The device output photocurrents reach their maximum and plateau for a gate bias >60 V, where the intrinsic region is under fully-depleted condition as explained in [34].

Device responsivity R can be extracted by using [15]:

$$R = \frac{I_{tot} - I_{dark}}{P_{in}}, \tag{1}$$

where I_{tot} and I_{dark} are, respectively, the device output currents under illumination and dark condition, and P_{in} is the incident optical power on the device total surface area.

The extracted responsivity (0.07 A W^{-1} at 480 nm) is consistent with the value which was discussed in [15], validating the excellent transparency and electrical gate-control characteristics of the graphene transparent gate. The inset presents the device dark current versus gate voltage. The dark current keeps at the level of 10^{-13}–10^{-12} A with the intrinsic region changing from accumulation to full depletion. These low current levels are consistent with the dark current obtained in the diode after standard MEMS membrane reactive ion etch and annealing [34], similar to values obtained without any CMOS post-processing, indicating that our post-CMOS thinning and transfer processing steps preserve the excellent SOI diode performance. The difference of transfer characteristics in the dark and illuminated conditions of the gated lateral PIN photodiode is mainly due to the appended electrical field across the depleted region, which is induced by the photo-generated carriers. With further improvement of the Si film quality, e.g. improving carriers' lifetime and reducing surface recombination velocity, the difference can be decreased. Additionally, graphene may improve the device long-term reliability and durability, besides offering an excellent transparency and electrostatic gate control. Indeed, its unique mechanical properties [35], chemical inertness [4], and thermal stability [5] makes it an ideal protective layer. Given the cost-effectiveness and the scalability of the graphene synthesis and transfer procedures, graphene represents a promising material to co-integrate with CMOS technologies [36].

3.2. Optical simulation in atlas/SILVACO

To obtain a primary understanding of the device optical response under backside illumination, two-dimensional (2D) numerical simulations based on device physics and optics are conducted in Atlas/SILVACO [37]. Incident light is illuminated perpendicularly from the BOX side, instead of the front-side illumination which was discussed in our previous work [12], to avoid unwanted absorption in the CMOS polysilicon layer. Absorption in the thin Si layer is calculated with the transfer matrix [38] implemented into Atlas/SILVACO to describe the light penetration and propagation in the device multilayer stack.

Corresponding to the device schematic view shown in figure 1(b), the width of the simulated 2D device is considered to be 60 μm, the length of the P^- region (i.e. intrinsic length L_i) is 20 μm, the length of the P^+ and N^+ regions is 3.0 μm, the active Si film thickness is 250 nm, and the BOX thickness is 1.0 μm. The doping levels of the P^+, P^-, and N^+ regions are, respectively, 1×10^{20}, 5×10^{16}, and 1×10^{20} cm^{-3}.

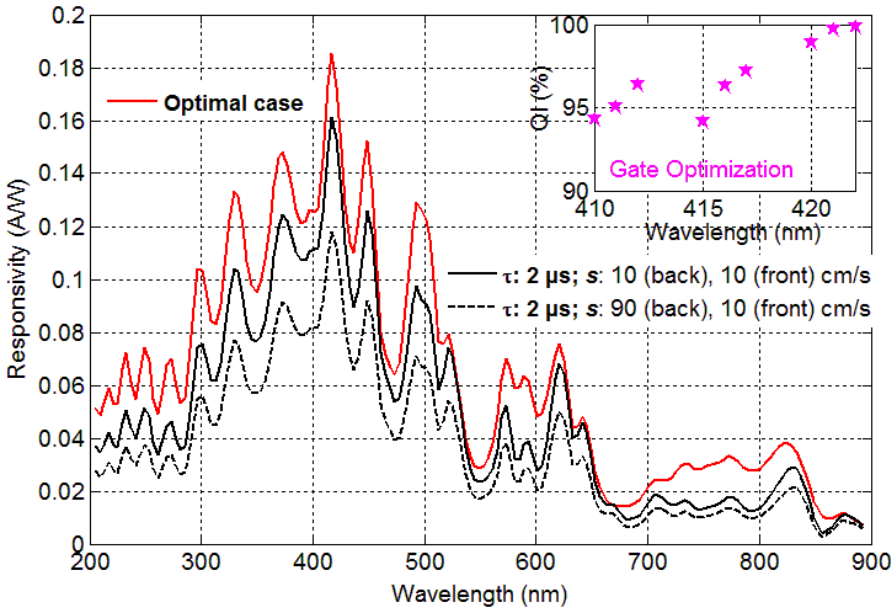

Figure 4. Simulated responsivity in the ultra-thin SOI lateral PIN diode ($L_i = 20$ μm), with average ($\Delta\lambda$ of 10 nm) in the UV and VS wavelength ranges, considering different electrical conditions in the intrinsic region. The inset illustrates the QI achieved under fully-depleted condition around the 410–422 nm wavelength range.

Volume carrier lifetime is 2.0 μs, with surface recombination velocity of 10 or 90 cm s^{-1} at front or back oxide interface [15]. Contacts of the anode and cathode electrodes are Ohmic.

Setting the optical indices of all the materials, numerical simulations of the lateral PIN photodiode with $L_i = 20$ μm are performed. Under backside perpendicular light incidence, the device responsivity is calculated for each single wavelength within the 200–900 nm range where the back-gate bias is 0 V, based on the relation between current and light power as given in equation (1). Detailed results of responsivity averaged (with a bandwidth $\Delta\lambda = 10$ nm) for each 4 nm wavelength increment are presented in figure 4 for the UV and VS wavelength ranges.

The optimal case of responsivity (red curve in figure 4) is calculated based on the available photocurrent generated in the intrinsic region (i.e. without recombination losses) divided by the device incident light power. The highest responsivity of ~0.18 A W^{-1} is obtained at ~410 nm, with several responsivity peaks of 0.1, 0.12, 0.075 and 0.04 A W^{-1} observed at ~300, 500, 610 and 820 nm of wavelengths, respectively. These peaks are consistent with the peaks of optical absorption (defined as the ratio between the photocurrent available in the device and the photocurrent of the source) obtained in the UV and VS wavelength ranges. While considering the carriers' volume recombination in the intrinsic region, a global decrease of the responsivity (the solid black curve) is observed with considered carrier lifetime (τ) of 2 μs and surface recombination velocity (s) of 10 cm s^{-1}, representative of defects related to the SOI diode without any post CMOS processing [34]. A second further decrease while increasing the back surface recombination to 90 cm s^{-1} (the dashed black curve, representative of defects related to the SOI PIN diode after deep reactive-ion etching to form the membrane without annealing [12]), indicating the dominant effect of the back surface on device output response in which side, light is incident. However, by implementing the innovative transparent gate, the internal quantum efficiency (QI = output photocurrent/available photocurrent) exceeds 95% in the PIN photodiode under fully-depleted condition, which is depicted in the inset to figure 4 for the wavelength range of 410–422 nm. Similar results have been obtained and discussed on different structures in [39–41], with a transparent gate optimization to approach the optimal responsivity.

3.3. Characterization of responsivity

Full characterization (i.e. within the UV and VS wavelength ranges) of the device responsivity are finally performed after the chip-on-board assembly using a semiconductor parameter analyzer (Agilent 4156C) to get the electrical output. For the light supply, we use a Muller LXH 100 light source and a monochromator to select a single wavelength λ in the UV and VS wavelength range (within the 200–900 nm range), with bandwidth $\Delta\lambda$ ~ 10 nm and power densities in the range of 10^{-6}–10^{-4} W cm^{-2}, in which linearity of the device optical response with light intensity has been demonstrated in [15]. The graphene-gated Si-based photodiode in this work shows superior performance in terms of optical linearity in the UV/blue wavelength range, comparing to a germanium-based photodetector [42]. Backside illumination is implemented from the BOX side as shown in figure 1(b). Fabrication and measurements have been reproduced, the corresponding average responsivities extracted for the graphene-gated ultra-thin lateral PIN photodiodes ($L_i = 20$ μm) are presented in figure 5 (at a reverse bias of 2.0 V), with the error bars depicting standard deviations.

In the VS range, peak responsivities are obtained at ~490, 590 and 760 nm with ~0.11, 0.08 and 0.04 A W^{-1} fairly close

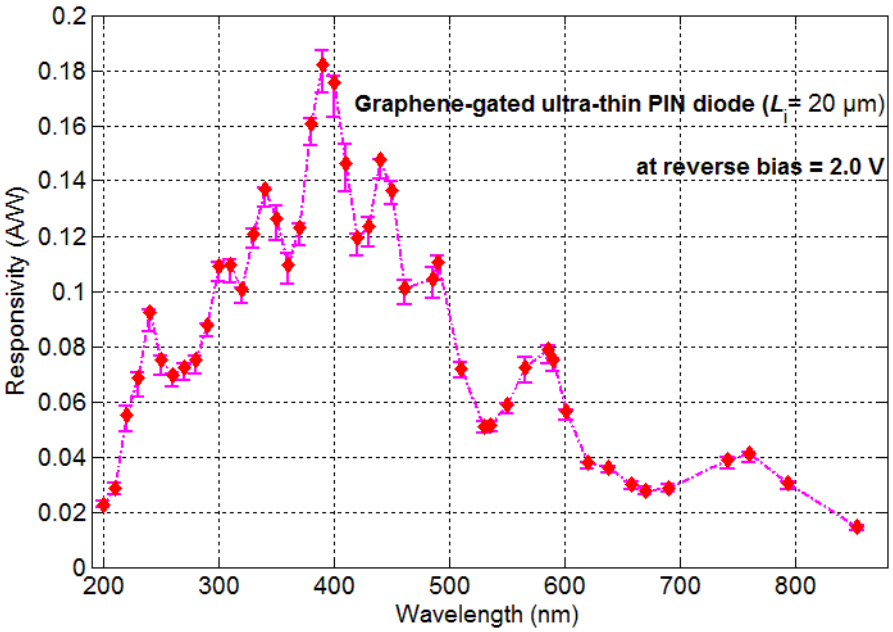

Figure 5. Experimental responsivities within the ultraviolet (UV) and visible (VS) wavelength range, measured in the ultra-thin lateral PIN diodes ($L_i = 20$ μm) with graphene transfer, under backside illumination (average values depicted by a diamond symbol and standard deviations by an error bar).

to simulations. Large improvement of responsivity is therefore obtained for wavelengths below 600 nm in these ultra-thin SOI lateral PIN photodiodes under the backside illumination, when compared with that of the same SOI lateral PIN diodes presented in previous works [12, 15], e.g. responsivity of 0.06 A W^{-1} at 590 nm with a gold bottom reflector and 0.04 A W^{-1} with Si substrate reflector, where large optical absorption observed in the CMOS polysilicon layer under the topside illumination greatly reduced the device optical response.

In the UV range, the highest responsivity is obtained at 390 nm, with 0.18 A W^{-1}. Other peak responsivities are achieved with ~0.15, 0.17, 0.14, 0.11, 0.07 and 0.09 A W^{-1}, respectively, at ~440, 400, 340, 300, 260 and 240 nm wavelengths. These are comparable with or even better than the most representative results in [14], i.e. responsivities achieved 0.18 and 0.10 A W^{-1}, respectively, at 400 and 480 nm wavelengths, by using an ARC coating layer for the optical optimization of absorption in the SOI lateral PIN photodiode. Moreover, the ultra-thin graphene-gated lateral PIN diode achieves a higher responsivity within the 300–400 nm wavelength range compared with the recent advanced graphene-enhanced ultraviolet bulk silicon Schottky photodetector without Al_2O_3 antireflection layer [16], where 0.15, 0.12, 0.07 A W^{-1} of the photoresponsivities were achieved at wavelength $\lambda = 400$, 365 and 254 nm respectively. It is worth noting that in our research, the silicon active layer is 250 nm thick and the light penetration depth is ~100 nm at λ of ~400 nm [14], which can explain the highest responsivity is obtained at 390 nm in the experiments as a compromise between the light absorption and the carriers' surface and volume recombination. Furthermore, the measured responsivities with the corresponding wavelengths are consistent with the values of the optimal responsivities obtained in simulation, where all the photo-generated carriers are collected in the intrinsic region of the diode. This confirms the excellent device quality (i.e. minimal defect formation during the fabrication process) as well as the effect of graphene gate transparency and photoresponse optimization under backside illumination. The remaining quantitative deviations including slight shifts in the peaks and valleys between the simulation and the experimental observation in figures 4 and 5 may result from the inaccurate material thicknesses specifically implemented into this simulation, considering that the thickness tolerance in the used SOI technology is around 5%–10% [12].

4. Conclusion

In this work, we present an ultra-thin SOI-based photodiode with complete Si substrate thinning by XeF_2, wet graphene transfer on BOX as a transparent control gate and chip-on-board assembly for back illumination and responsivity optimization. Electrical characteristics in dark and illumination conditions demonstrate that the process steps preserve the CMOS device quality and enable the gate bias control. A maximum responsivity of 0.18 A W^{-1} at 390 nm is experimentally obtained and supported by simulations, validating the unique combination of graphene gate conductivity and excellent transparency. With the high overall responsivity achieved in the 200–900 nm range in close agreement with theory, the device shows its high potential in the UV and VS light detection. Moreover, the ~5 μm final thickness of the chip enables its use in future flexible applications.

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