

28 FDSOI RF Figures of Merits and Parasitic Elements at Cryogenic Temperature

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Abstract—This work presents, for the first time to our best knowledge, RF characterization of 28 nm FDSOI CMOS process at cryogenic temperatures including extraction of parasitic elements of small-signal equivalent circuit and two main RF Figures of Merit (FoM), i.e. current cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). Increases of f_T and f_{max} by about 85 GHz and 30 GHz, respectively, are demonstrated at cryogenic temperatures. The observed behavior of RF FoMs versus temperature is analyzed in terms of small-signal equivalent circuit elements. This study suggests 28 nm FDSOI as a good candidate for future cryogenic applications.

Keywords— FDSOI, UTBB MOSFETs, RF Figures of Merit (FoM), Cryogenic temperature, parasitic elements

I. INTRODUCTION

Motivation for the in-depth studies of advanced technologies at cryogenic temperatures is two-fold: (i) space applications and (ii) read-out circuitry of quantum bits (“qubits”) by an integrated control system [1]. High demand for quantum computing is motivated by a strong enhancement of computational power at deep cryogenic temperatures which provides larger qubit numbers [2]. 28 FDSOI technology has already demonstrated improved DC, analog and RF performances at room temperature (RT) [3][4]. Some previous works [2][5][6], analyzed the behavior of advanced MOSFETs at cryogenic temperatures. However, those works are mostly limited to static parameters (as short-channel effects, threshold voltage, subthreshold swing, etc.). Influence of cryogenic temperature on 28 nm bulk and FDSOI technologies with a main focus on analog parameters and EKV model has been discussed in [2], [5]. Our previous work [7], investigated the ability of 28 FDSOI technology for cryogenic applications from DC to RF covering electrostatic, analog and RF figures of merit (FoM). We demonstrated strong improvement of transconductance (g_m) to drain current (I_d) ratio g_m/I_d , g_m , I_d , and cut-off frequency (f_T) at 77 K. However, in terms of RF performance that study was limited to f_T only. To our best knowledge there are no extended studies of RF behavior of 28 FDSOI MOSFETs at cryogenic temperatures. Our present work fills this gap and extends our previous work to detailed cryogenic RF analysis of 28 FDSOI process including equivalent circuit extraction. First, RF FoMs of nMOSFETs from 28 FDSOI with different gate lengths in a temperature (T) range of 77-300 K are extracted. Then, our main focus is on the reconstruction of small-signal equivalent circuit of UTBB MOSFET based on intrinsic and parasitic elements by which RF FoMs are determined.

II. DEVICE AND MEASUREMENT DETAILS

Devices studied in this work come from ST-M 28 FDSOI process [8], with gate lengths (L_g) from 25 to 150 nm. The Si film, BOX and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. Studied nMOSFETs feature 60 fingers

of 2 μm width, embedded in CPW pads for RF characterization. DC I-V and RF S-parameters are measured down to liquid nitrogen temperature (77 K). S-parameters are measured in a frequency range from 10 MHz up to 40 GHz under saturation ($V_{ds} = 1$ V) and “cold” ($V_{ds} = 0$ V) conditions for different applied gate voltages (V_{gs}). The back gate was kept grounded. The CPW feed line pads are de-embedded by dedicated open structure for each device measured at every temperature.

III. RESULTS AND DISCUSSION

A. RF FoMs

The variation of two main RF FoMs, current cutoff frequency (f_T) and maximum oscillation frequency (f_{max}), versus (a) L_g and (b) T are shown in Figs. 1 and 2, respectively. f_T and f_{max} are obtained from extrapolation of H_{21} parameter and unilateral gain (ULG) to 0 dB, respectively, in saturation and at V_{gs} that corresponds to maximum g_m . This advanced technology node is known to feature high f_T and f_{max} reaching several hundreds of GHz at room temperature [3][9]. As shown in Fig. 1 and 2, L_g (150 to 25 nm) and T (300 to 77 K) reduction results in strong f_T and f_{max} improvements, by about 85 and 30 GHz, respectively.

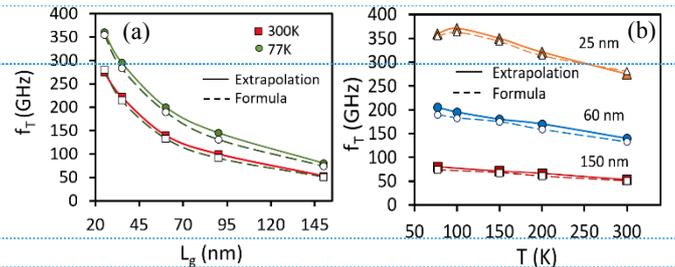


Fig. 1. f_T (a) vs. L_g for 77 and 300 K (b) vs. T by extrapolation (solid lines) and small-signal equivalent circuit extraction (dashed lines) at max g_m .

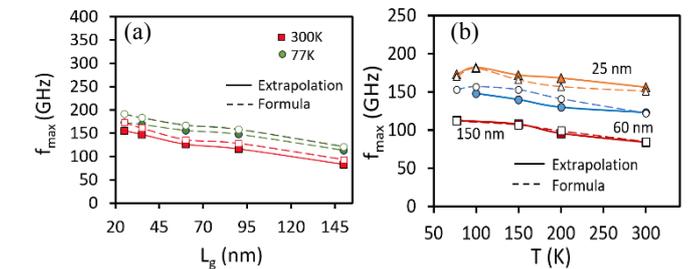


Fig. 2. f_{max} (a) vs. L_g for 77 and 300 K (b) vs. T by extrapolation (solid lines) and small-signal equivalent circuit extraction (dashed lines) at max g_m .

However, one can see in Fig. 2 that f_T and f_{max} curves in the shortest device feature a maximum at ~ 100 K and thus their improvement at 77 K is attenuated. This will be discussed in the next section in terms of mobility (μ) and thus g_m behavior in such devices.

B. Extraction of small-signal equivalent circuit elements

Based on the MOSFET small-signal equivalent circuit shown in Fig. 3 (including intrinsic and parasitic elements), f_T and f_{max} are approximately expressed by Eq. 1 and 2 [10]:

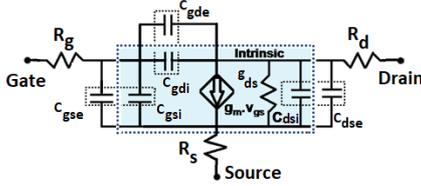


Fig. 3. RF model of UTBB MOSFET small-signal equivalent circuit.

$$f_T \approx \frac{g_{me}}{2\pi(C_{gs}+C_{gd})} \quad (1), \quad f_{max} \approx \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + (R_s + R_g)g_{ds}}} \quad (2)$$

Small-signal equivalent circuit elements were extracted from S-parameters measurements using the procedure explained in [3]. Figs. 4, 5 and 6 show variations of g_m , gate capacitance ($C_{gg}=C_{gd}+C_{gs}$) and both series and gate resistances (R_{sd} and R_g), respectively, as a function of L_g at 300 and 77 K (figures (a)) and as a function of T (figures (b)). Based on Eqs.1 and 2, improvement of f_T and f_{max} with decreasing of L_g and T observed in Fig. 1 and 2 is directly correlated with increase of g_m (due to L_g reduction and μ improvement at low T) and decrease of C_{gg} which is mainly by L_g reduction as shown in Fig. 4 and 5.

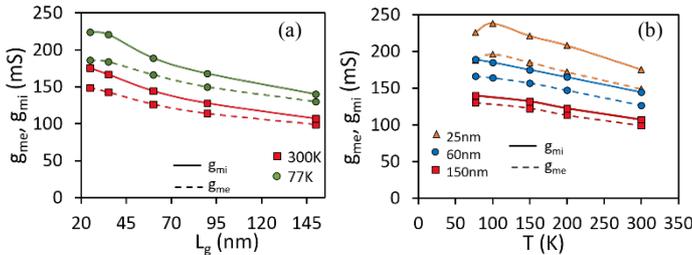


Fig. 4. g_m, g_{me} (a) vs. L_g for 77 and 300K (b) vs. T for $L_g = 25, 60$ and 150 nm.

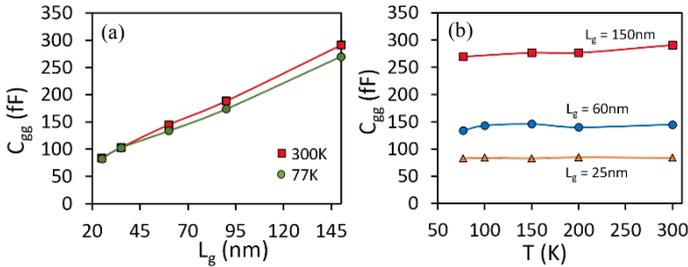


Fig. 5. C_{gg} vs. (a) L_g for 77 and 300K (b) vs. T for $L_g = 25, 60$ and 150 nm.

Indeed, from Figs. 1, 2 and 4, one can see that T lowering results in simultaneous g_m , f_T and f_{max} improvements. However, the improvement becomes smaller in the shortest device. As shown in Fig. 4b, for 25 nm device, improvement rate of RF “extrinsic”, g_{me} , (i.e. including R_{sd}), and “intrinsic”, g_{mi} , (i.e. without R_{sd} effect) drops at 77 K exhibiting a maximum at ~ 100 K similarly to RF FoMs shown in Figs. 1 and 2. This is due to complex mobility behavior as previously discussed [6][7]. In fact, μ in short-channel devices is strongly degraded by the presence of defects in the extensions and source/drain regions. Resulting μ temperature dependence is defined through the balance between two mechanisms: Coulomb scattering on the defects (with μ_c reduction with T lowering) and phonon scattering (with μ_{ph} increase with T lowering). Next to that, R_{sd} can be seen to decrease slightly at 77 K (Fig. 6) which could be explained by dominant behavior of metallic interconnection lines. However,

the observed reduction lies close to the limit of extraction precision. As a result of very slight (if any) R_{sd} decrease with T, Fig. 4b shows almost constant difference between g_{me} and g_{mi} for each device from 300 down to 77 K. However, the effect of R_{sd} in shorter devices and at lower T, i.e. the cases featuring higher g_{mi} level, is more pronounced, as can be seen from stronger difference between g_{mi} and g_{me} . Next to that, from Fig. 5 one can see that C_{gg} does not change much with T lowering. Therefore, observed f_T and f_{max} T-dependencies are mostly due to g_m (and in turn μ and R_{sd}) T-dependence.

Similarly to our previous RT observations [3], f_{max} is lower than f_T , except for long-channel devices. This is due to the gate resistance (R_g) which increases dramatically in shorter devices (Fig. 6a). T lowering down to 77 K has almost no effect on this trend. This is because of gate stacked materials behavior which remains unchanged by T lowering down to 77 K as shown in Fig. 6b. To support the above analysis in terms of equivalent circuit elements, f_T and f_{max} were re-calculated based on Eqs.1 and 2 using extracted parasitic and intrinsic elements and shown in Figs. 1 and 2. One can see that “re-calculated” f_T and f_{max} are in good agreement with the values obtained by extrapolation of H_{21} and ULG, confirming the above discussion.

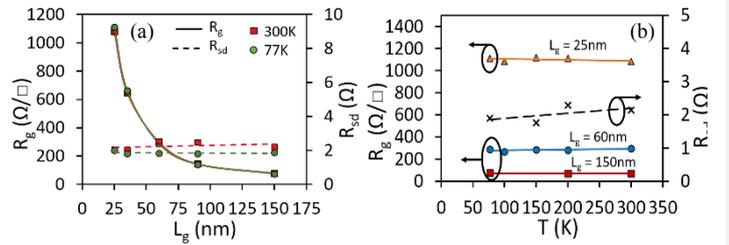


Fig. 6. R_g, R_{sd} (a) vs. L_g at 77 and 300 K (b) vs. T for $L_g = 25, 60$ and 150 nm.

IV. CONCLUSION

In this work, the potential of 28 FDSOI MOSFETs for future cryogenic RF applications has been assessed by analysis of RF FoMs and complete small-signal equivalent circuit elements. Temperature reduction down to 77 K has been shown to result in improvement of f_T (~ 85 GHz) and f_{max} (~ 30 GHz). Temperature evolution of RF FoMs was explained in terms of mobility and parasitic elements behavior. This was supported by the fact that f_T and f_{max} reconstructed based on the MOSFET small-signal equivalent circuit model agree well with those extracted by extrapolation of H_{21} and ULG in a temperature range down to 77 K. The work will further be extended to the temperature range down to 4.2 K.

ACKNOWLEDGMENT

The work was partially funded by Eniac “Places2Be” and Ecsel “Waytofast” projects.

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