A Novel Very Low Voltage Topology to implement MCML XOR Gates

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Abstract—A new very low-voltage topology to implement MOS current mode logic (MCML) XOR gates is proposed in this paper. Instead of stacking several level of transistors to implement a two inputs XOR gate, a p-type differential pair is used to steer the current in n-type differential pairs through current mirrors. The proposed topology allows to reduce the minimum supply voltage of MCML XOR gates while guaranteeing a fully current mode behavior as in the conventional XOR gate. The proposed topology has been compared against the conventional and triple tail MCML XOR gates. Simulation results referring to a 40nm CMOS technology for V_{DD}=1V confirm that the XOR gate presented in this work exhibits a lower propagation delay than the previously published low voltage MCML XOR gate. Furthermore both theoretical analysis and simulation results in a 40nm process show that the proposed topology is able to work with a V_{DD} as low as 0.65V whereas state of the art topologies are not usable below 0.8V.

Keywords—MCML; low voltage; nanometer CMOS; current mode; XOR Gate.

I. INTRODUCTION

High-speed digital communications and chip-to-chip interconnections are becoming more and more popular in the nanometer CMOS era. These applications require high performance logics suitable to be implemented with CMOS processes and able to guarantee high operating frequencies and low power consumption. Optical communications as well as, very high sampling frequency ADCs demand the use of logic styles able to operate at tens of Gb/s: these speeds cannot currently be achieved using the conventional CMOS logic style [1-3].

Mixed-signal integrated circuits have nowadays become pervasive due to the continuously increasing demand of systems on chip integrating digital and analog functions with more and more stringent specification requirements. The conventional CMOS logic style exhibits a large switching noise that lowers the performance of the analog building blocks and therefore it cannot be used on the same substrate with very high-resolution analog circuits [4-5]. MOS current mode logic (MCML) in contrast to the standard CMOS logic provides higher speed, better power efficiency at high frequencies, lower switching noise and lower sensitivity to process variations [6].

The exclusive-OR (XOR) gate is a key component to build high speed digital circuits such as comparators, adders, multipliers, test pattern generators etc. [7-10].

The most challenging drawback in the use of nanometer CMOS processes is the very low supply voltage available, (which is usually less than 1V). This constraint on the supply voltage does not allow stacking several levels of transistors in a MCML gate, so that the traditional MCML XOR gate is not usable in practice anymore as will be pointed out in the next sections of this paper.

Low voltage CML topologies based on the triple tail cell concept have been introduced in [8] and analyzed in [9] referring to bipolar technologies. Recently, a new low-voltage MCML XOR gate topology has been proposed in [10]. It exploits the triple-tail cell concept, provides differential signaling and does not need any additional circuitry when compared against previous low voltage topologies. A MCML triple tail XOR gate topology exploiting multi-threshold CMOS processes has been introduced in [11]. Exploiting transistors with different threshold voltages, level shifters are not required, and supply voltage can be reduced [11].

In this work we present a novel low voltage MCML XOR gate topology in which the high performance of p-type MOS transistors in nanometer technologies is exploited to develop very low voltage logic gates by using a "folded" approach instead of the conventional "stacking" approach. A similar approach has been adopted in [12] for the implementation of low voltage D-Latches. In *Section II* we review the conventional MCML XOR gate and the triple tail XOR gate and compute the minimum supply voltage of the two circuits from a theoretical perspective. In Section III we introduce the proposed MCML XOR gate topology showing its advantages in terms of minimum supply voltage. Simulation results and comparisons are shown in Section IV. Conclusions are finally reported in section V.

II. Review of MCML XOR Gate Topologies

A. Conventional MCML XOR Gate

The circuit schematic of the conventional MCML XOR gate is depicted in Fig. 1. The transistor M_1 implements the bias current source of I_{SS} value. MOS devices M_2 to M_7 implement the conditional pulldown network, whereas the active load is implemented through p-type transistors M_8 and M_9. The upper level and lower level differential couples are driven by differential inputs A and B respectively. When input B is low, M_2 is off, the tail current I_{SS} flows through M_3 and is steered either to M_6 or M_7 according to the differential input A. The tail current I_{SS} is steered to the load transistors M_8 and M_9 to provide the differential output voltage [6].

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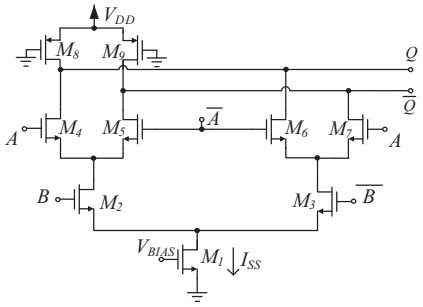

Fig. 1 Conventional MCML XOR Gate

The output differential voltage swing V_{SWING} of the conventional MCML XOR gate can be written as:

$$V_{SWING} = 2 \cdot I_{SS} \cdot R_P \quad (1)$$

where R_P is the equivalent linear resistance of the p-type devices M_8 and M_9 computed as in [5], [10] and [13].

In order for this circuit to properly operate, all the NMOS transistors have to work in saturation and this condition set a limitation on the minimum supply voltage V_{DD}.

Denoting as V_{CMA} and V_{CMB} the common mode voltage of differential input A and B respectively, the following conditions have to be fulfilled in order to guarantee saturation operation for all NMOS devices in the XOR gate circuit in Fig. 1:

$$V_{DS1} = V_{CMB} - V_{GS2,3} > V_{DS1,sat} \quad (2)$$

$$V_{DS2,3} = V_{CMA} - V_{GS4-7} - \left(V_{CMB} - V_{GS2,3}\right) > V_{DS2,3,sat} \quad (3)$$

$$V_{DS4-7} = V_{DD} - \frac{V_{SWING}}{2} - (V_{CMA} - V_{GS4-7}) > V_{DS4-7,sat} \quad (4)$$

where V_{DS}, V_{GS}, and $V_{DS,sat}$ are the drain source, gate source and saturation drain source voltage of the different transistors in Fig. 1 respectively. From equations (2) and (3) it is evident that, setting $V_{CMA} = V_{CMB}$ results in $V_{DS2,3} = 0$, if $M_{2,3}$ and $M_{4\text{-}7}$ are equally sized. In the past, MCML designers used source followers to lower the common mode voltage level V_{CMB} with respect to V_{CMA} thus allowing M_2 and M_3 to work in saturation [5], [6], [8], [11]. However, source follower stages are not power efficient and consume large silicon area footprint. Furthermore by using a source follower (implemented trough a common drain transistor M_{10}) the implemented voltage shift is equal to V_{GS10}.

By using these assumptions the minimum supply voltage can be computed from (1) as follows:

$$V_{DS1} = V_{CMB} - V_{GS2,3} = V_{CMA} - V_{GS10} - V_{GS2,3} \quad (5)$$

Assuming that the differential signal A is the output of a conventional MCML inverter (differential pair) we can write:

$$V_{CMA} = V_{DD} - \frac{V_{SWING}}{4} \quad (6)$$

Finally, substituting (6) in (5) and using (2), we can express the minimum supply voltage for the conventional MCML XOR gate as follows:

$$V_{DD,min,conv} = \frac{V_{SWING}}{4} + V_{GS10} + V_{GS2,3} + V_{DS1,sat} \quad (7)$$

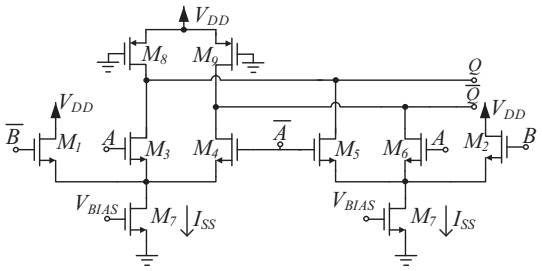

Fig. 2 Triple Tail MCML XOR Gate

From (7), it is evident that the conventional MCML XOR gate is not suited to be used for V_{DD} in the range of 1V assuming typical device parameters for nanometer CMOS technologies.

B. Triple Tail MCML XOR gate

The low-voltage triple tail XOR gate introduced in [10] is reported in Fig. 2. It is made up of two triple-tail cells (M_3, M_4, M_1) and (M_5, M_6, M_2) with two tail current sources of I_{SS} value. The MOS devices M_1 and M_2 are connected between the supply node and the common source node of differential pairs M_3–M_4 and M_5–M_6 respectively. When the differential input B is high, M_2 is on and the differential pair M_5–M_6.is off. In the same condition, M_1 is off and the differential pair M_3–M_4 is on: the output voltage is generated according to the differential input A.

The minimum supply voltage, $V_{DD,min,TT}$ for the triple tail XOR gate is computed by following the same approach followed for the conventional XOR gate as:

$$V_{DD,min,TT} = \frac{V_{SWING}}{4} + V_{GS3,4} + V_{DS7,sat} \quad (8)$$

where V_{DS}, V_{GS}, and $V_{DS,sat}$ are the drain source, gate source and saturation drain source voltage of the different transistors in Fig. 2 respectively.

It has to be pointed out that, the performances of the triple tail XOR gate strongly rely on the sizing of MOS devices M_1 and M_2 with respect to the other devices. Furthermore, the common-mode voltage and the voltage swing of inputs A and B have to be carefully chosen to provide proper operation. In particular, MOS devices M_1 and M_2 have to be sized much larger than the other transistors in order to keep the output swing high and guarantee a good noise margin [10].

According to [10] the output differential voltage swing for the triple tail XOR gate can be expressed as follows:

$$V_{SWING,TT} = 2R_P I_{SS} \frac{M}{1+M}. \quad (9)$$

where M is the ratio between the aspect ratios of $M_{1,2}$ and $M_{3\text{-}6}$.

In order to keep the output swing high and guarantee a good noise margin, values of M in the range of 8-10 have to be chosen when adopting short channel MOS technologies. When M is set to be greater than 8 the input capacitance of M_1 and M_2 is very large and the gates (or buffers) driving M_1 and M_2 are heavily loaded: this results in a strong limitation of the speed performance of the triple tail XOR gate topology.

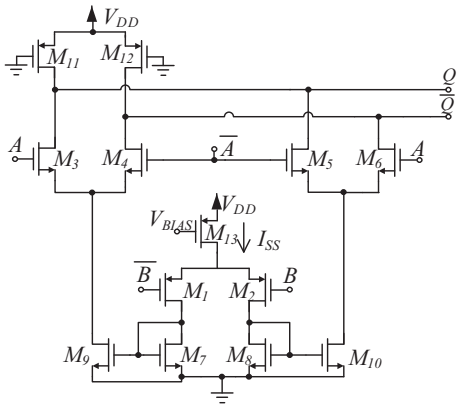

Fig. 3 Proposed Folded MCML XOR Gate

III. Proposed MCML XOR gate topology

In this paragraph we introduce a novel, low voltage, MCML XOR gate. The proposed XOR gate exploits the idea of folding one level of the conventional XOR gate. The proposed topology is shown in Figure 3. When input B is low the P-channel differential couple M_1-M_2 steers the current I_{SS} to the current mirror M_8-M_{10}, whereas, when input B is high I_{SS} is steered towards M_7-M_9. The differential pair made up of devices M_3-M_4 is active when B is high, and the XOR gate generates the output according to the differential input A. When B is low only the differential couple M_5-M_6 is active and the XOR gate generates the output according to not A.

A. Minimum supply voltage

Denoting as V_{CMA} and V_{CMB} the common mode voltage of differential input *A* and *B* respectively, the following conditions have to be fulfilled in order to guarantee proper operation of the proposed XOR gate (i. e. all transistors from M_1 to M_{10} working in saturation):

$$V_{DS9,10} = V_{CMA} - V_{GS3-6} > V_{DS9,10,sat} \quad (10)$$

$$V_{DS3,4} = V_{DD} - \frac{V_{SWING}}{2} - (V_{CMA} - V_{GS3-6}) > V_{DS3,4,sat} \quad (11)$$

$$|V_{DS13}| = V_{DD} - (V_{CMB} - |V_{GS1,2}|) > |V_{DS13,sat}| \quad (12)$$

Assuming that the differential signal A is the output of a conventional MCML inverter we can write $V_{CMA} = V_{DD} - \frac{V_{SWING}}{4}$ as in (6). The differential input B in Figure 3 can be generated from a p-type MCML inverter (made up of a PMOS differential pair with NMOS load). In this cases V_{CMB} can be easily set to the optimum value which allows to minimize the supply voltage V_{DD}:

$$V_{CMB} = \frac{V_{SWING}}{4} \quad (13)$$

By using the expressions in (6) and (13) for V_{CMA} and V_{CMB} respectively in (10) and (12) the minimum supply voltage of the proposed folded XOR gate can be written as:

$$V_{DD,min,folded} = \frac{V_{SWING}}{4} + V_{GS3-6} + V_{DS9,10,sat} \quad (14).$$

B. Threshold lowering for very low voltage XOR gates

Equation (14) can be rewritten in terms of the threshold voltages V_{TH} and overdrive voltages $V_{OV} = V_{GS} - V_{TH}$ as follows:

$$V_{DD,min,folded} = \frac{V_{SWING}}{4} + V_{TH} + 2V_{OV} \quad (15)$$

Referring to a 40nm CMOS technology V_{TH} is typically in the range of 0.4V, whereas V_{OV} and $\frac{V_{SWING}}{4}$ can be both set in the range of 0.1V, resulting in about 0.7V of minimum V_{DD}.

To further reduce the minimum supply voltage a threshold lowering technique based on moderate forward body bias can be exploited by using the following body connections for the circuit in Fig. 3: Body of M_1 and M_2 connected to ground; Body of M_7, M_8, M_9 and M_{10} connected to the common source of M_1 and M_2; Body of M_3, M_4, M_5 and M_6 connected to *VDD*.

With this arrangement the V_{TH} can be reduced to about 0.3V and a minimum supply voltage in the range of 0.6V becomes feasible. It has to be noted that in this configuration all transistors are forward body biased by the same bulk source voltage $V_{SB} = \frac{V_{SWING}}{4} + V_{TH} + V_{OV}$ which is about equal to 0.5V in a 40nm CMOS technology.

IV. Design and comparisons

The triple tail XOR gate and the proposed XOR gate have been compared by means of transistor level simulations referring to a commercial 40nm CMOS technology within Cadence Virtuoso environment.

A supply voltage V_{DD} = 1V, an output swing V_{SWING} = 800mV and a reference bias current I_{SS} = 25μA have been assumed for the comparisons. All the comparisons have been carried out referring to the same power consumption for both circuits.

Bias settings and devices sizing for the reference tail current I_{SS} are shown in Table I. Values in Table I have then been scaled with the current according to [6] for I_{SS} ranging from 25 to 100μA.

It has to be noted that, for values of V_{SWING} lower than 800mV the triple tail XOR gate is not able to properly operate (M_1 and M_2 in Fig. 2 are not able to properly steer I_{SS} even for M=8), whereas the proposed folded XOR gate is able to work with V_{SWING} set to 400mV. The possibility to operate at lower V_{SWING} allows the proposed XOR gate to operate at a lower minimum supply voltage than the triple tail XOR gate.

The two XOR gate topologies have been simulated referring to two testbenches (TB1 and TB2) and two fan-out settings (FO1 and FO4). MCML inverter/buffer cells have been used as driving and load cells in all the simulations. In TB1 ideal voltage sources feed the differential A and B inputs of the gate under test, whereas in TB2 an MCML inverter/buffer cell, biased and sized at I_{SS}, drives each one of the A and B inputs.

Simulation results for V_{DD}=1V and for the reference I_{SS} are summarized in Table I, and show that the proposed topology outperforms the triple tail one under testbench 2 conditions.

The propagation delay of the two compared XOR gates is reported in Figures 4 and 5.

Table I: Bias settings and devices sizing for the compared XOR gate.

	Triple Tail XOR Gate	*Proposed Folded XOR Gate*
V_{DD}	*1V*	*1V*
L	*40nm*	*40nm*
Reference I_{SS}	*25 μA*	*25 μA*
R_P	*16 KΩ*	*16 KΩ*
$W_{1,2}$	*5.76 μm*	*0.72 μm*
$W_{3,4,5,6}$	*0.72 μm*	*0.36 μm*
$W_{7,8,9,10}$	-	*0.36 μm*

Table II: comparisons in terms of propagation delay at I_{SS}=25μA

	Triple Tail			*Folded*		
	CML Buf (ps)	*XOR (ps)*	*TOT (ps)*	*CML Buf (ps)*	*XOR (ps)*	*TOT (ps)*
TB1-FO1	-	27.2	**27.2**	-	32.7	**32.7**
TB1-FO4	-	49.2	**49.2**	-	39.9	**39.9**
TB2-FO1	58.8	27.2	**86.0**	14.1	32.7	**46.8**
TB2-FO4	61.3	49.2	**110.5**	14.1	39.9	**54.0**

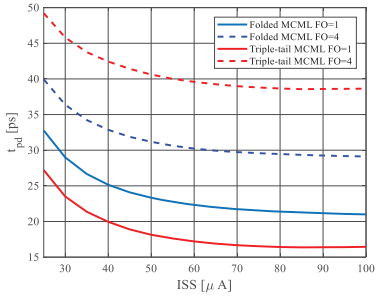

Fig. 4 Propagation delay comparisons for testbench1, in FO1 and FO4 conditions and V_{DD}=1V.

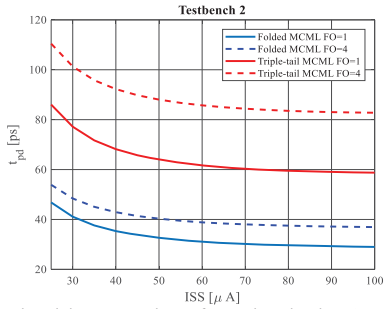

Fig. 5 Propagation delay comparisons for testbench2, in FO1 and FO4 conditions and V_{DD}=1V.

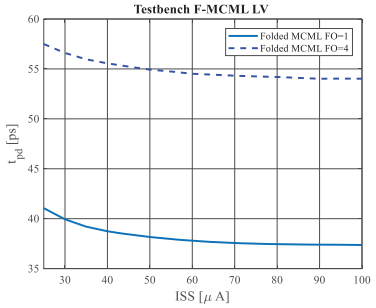

Fig. 6 Propagation delay as a function of I_{SS} for the proposed Folded XOR gate for V_{DD}=0.65V, testbench1, FO1 and FO4.

Finally, the proposed topology has been tested with V_{DD} set at its minimum value of 0.65V and the propagation delay as a function of I_{SS} is shown in Figure 6.

V. Conclusion

In this paper we have introduced a novel low voltage topology to implement MCML XOR gates. The proposed XOR gate and the low voltage triple tail XOR gate have been compared referring to a 40nm CMOS process. Simulation results for V_{DD} = 1V have demonstrated that the proposed topology allows a speed improvement of about 50% with respect to the triple tail one in the most common testbench conditions. Due to the capability to work with lower V_{SWING}, and exploiting a threshold lowering technique, the proposed circuit has been able to work at the lowest minimum supply voltage. Simulation results have shown the capability to operate at V_{DD}=0.65V whereas the triple tail XOR gate is not able to properly work for V_{DD} lower than about 0.8V.

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